Computer Architecture Practice
20 May 2020
Instruction Set Architecture for 16-bit Processor

1) Instruction Format and Size: F D E

This design considers the Instruction size as 16-bits.
The processor has 16 registers ranging from 0000 to 1111 (ie., R0, R1, ...R15.)
CF = Carry Flag
Rdst = Destination register
Rsrc1 = Source Register 1
Rsrc2 = Source Register 2
{} = Concatination
[] = Address Value of Oprand

2) Register based Instructions:

Opcode	Rdst	Rsrc2	Rsrc1
		4 bits	4 bits

3)

Opcode : 0000 to 1111

4) Load Instruction:

Opcode	Rdst	Address
4 bits	4 bits	8 bits

5)

Opcode : 1111

6) Store Instruction:

Opcode	Rdst	Address
4 bits	4 bits	8 bits

7)

Opcode : 1110

8) Opcode (Operation Code) Encoding:

*******Assumed each stage of addition and subtraction as one pipelining stage due to equal delay for the logical operation.