AT91RM3400 Development Kit

User Guide

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Section 1

Overview

1.1 Scope

The AT91RM3400 Development Board enables real-time code development and evaluation. It supports the AT91RM3400 ARM7TDMI®-based 32-bit RISC microcontroller.

This guide focuses on the AT91RM3400 Development Board as an evaluation and demonstration platform:

- Section 1 is this overview.
- Section 2 gives information on setting up the installation.
- Section 3 contains a description of the development board.
- Section 4 details the configuration straps.
- Section 5 shows board schematics.

1.2 Deliverables

The development kit is delivered with:

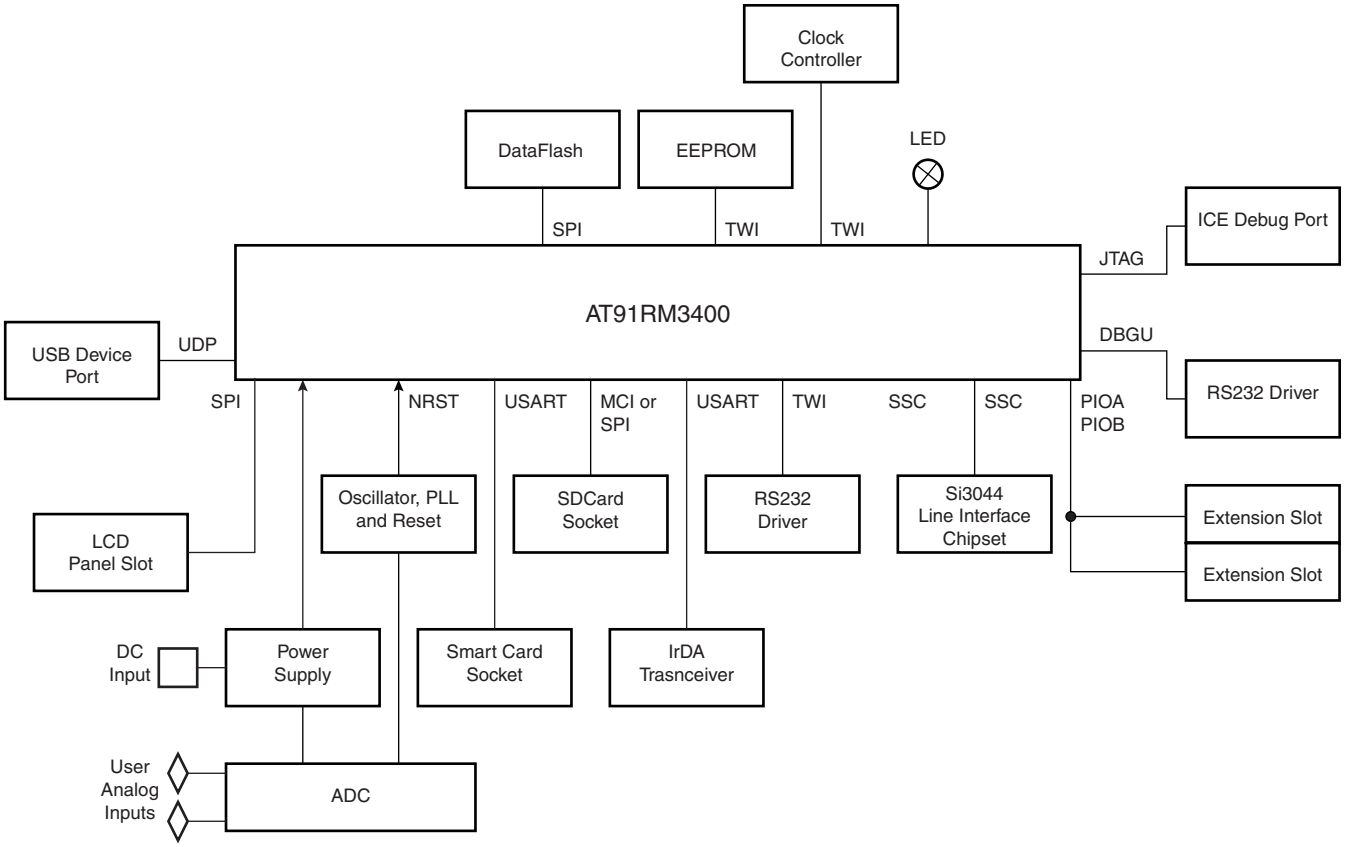
- One AC adapter 100 - 240V ~ 1.0A, 50 - 60 Hz
- One modem RS232 cable
- One A/B-type USB cable
- Two power supply cables, one US format, one French format
- One CD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 The AT91RM3400 Development Board

The board consists of an AT91RM3400 together with the following:

- 128K bytes of EEPROM with two-wire interface access
- 8M bytes of serial DataFlash®
- Three communication ports (USB host and device, serial and IrDA)
- JTAG/ICE and debug interface
- Expansion connector

Figure 1-1. AT91RM3400 Development Board Block Diagram



Section 2

Setting Up the AT91RM3400 Development Board

2.1 Electrostatic Warning

The AT91RM3400 development board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to connect the AT91RM3400 development board, the following elements are required:

- The AT91RM3400 development board itself
- Power supply cable capable of supplying 7V to 12V at 1A (not supplied)

2.3 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.

The board has a voltage regulator providing +3.3V. The regulator allows the input voltage range to be from 7V to 12V.

2.4 Getting Started with the AT91RM3400

The AT91RM3400 Development Kit is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains.

Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91RM3400.

Section 3

Board Description

3.1 AT91RM3400 Processor

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - Runs at up to 55 MHz providing 0.9 MIPS/MHz
  - Based on ARMV4T Architecture
  - In-circuit Emulator including Debug Communication Channel
- Additional Embedded Memories
  - 96K Bytes of SRAM and 256K Bytes of ROM
- System Peripherals:
  - Enhanced Clock Generator and Power Management Controller
  - Two On-chip Oscillators with Two PLLs
  - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
  - System Timer Including Periodic Interrupt, Watchdog and Second Counter
  - Real-time Clock with Alarm Interrupt
  - Debug Unit, Two-wire UART and Support for Debug Communication Channel
  - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
  - Seven External Interrupt Sources and One Fast Interrupt Source
  - Two 32-bit PIO Controllers with Up to 63 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
  - 19-channel Peripheral Data Controller (DMA)
- USB 2.0 Full Speed (12 M-bits per second) Device Port
- Multimedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)

- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

3.2 Memory

- 128-Kbyte EEPROM with 2-wire interface
- 8-Mbyte serial DataFlash

3.3 Memory Card

- SD Card/MMC
  - Supports MultiMedia and SD Card
  - Analog switches provide support for DataFlash Card
- Smart Card Interface

3.4 Clock Circuitry and Analog Functions

- 32.768 kHz standard crystal for the AT91RM3400
- 18.432 MHz standard crystal for the AT91RM3400
- Temperature sensor
- Analog-to-digital converter

3.5 Reset Circuitry

- Reset Controller

3.6 Power Supply Circuitry

- 3.3V DC/DC converter
- 1.8V DC/DC converter

3.7 Remote Communication

- IrDA Transceiver
- Host Interface via RS-232 DB9 male socket
- Line interface
- Debug Port via RS-232 DB9 connector
- Device USB socket

3.8 User Interface

- One LED and sixteen user buttons managed via general PIO lines

3.9 Expansion Slots

- Four expansion slots give access to all the microcontroller's signals

3.10 Debug Interface

- 20-pin JTAG interface connector
- Serial Debug Unit

Section 4

Configuration Straps

4.1 Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM3400 development board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
S1	Closed	The thermistor input of MAX17J7 (MN2) is tied to GND.
S2	Closed	The guard ring is connected to GND.
S4	Closed	The **PA20**/DCD1/TIA2 PIO line is connected to the LED (DS4)
S5	Closed	The **PB9**/NPCS2/RD1 PIO line is connected to the buzzer (LS1)
S6	Closed	Chip select AFF_CS is connected to the LCD panel.
S7	Closed	The **PB27**/DTXD/IRQ3 PIO line is connected to the READY/BUSY of the Serial DataFlash (MN9).
S8	Open	The Write Protect signal is not active for the DataFlash (MN9).
S9	Closed	The PA8/**TWCK**/PCK3 PIO line is connected to the EEPROM clock (MN10).
S10	Closed	The PA7/**TWD**/PCK2 PIO line is connected to the EEPROM I/O line (MN10).
S11	Open	The PA3/**NPCS0**/PCK1 is not connected to the serial DataFlash chip select (MN9).
S12	Closed	The ADC_CS PIO line is connected to the Analog-to Digital Converter chip select.
S13	Closed	The TD2/**IRQ2**/PB6 PIO line is connected to the Analog-to-Digital Converter End of Conversion signal.
S14	Closed	Analog-to-Digital Converter V_{REF} PIO line is connected to GND.
S15	Closed	The PA4/**NPCS1** PIO line is connected to the LCD panel.
S16	Closed	The PA30/**DXRD** PIO line is connected to the DBGU receive signal
S17	Closed	The PA14/**RXD1 PIO line is con**nected to the USART1 read signal.
S18	Closed	The PA17/**CTS1**/TIOB0 PIO line is connected to the USB CNX signal.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
S19	Closed	The **PA21**/RI1/TIOB2 PIO line is connected to the receive buffer output of the DBGU transceiver (MN26).
S20	Closed	The PB25/**IRQ1**/TD1 PIO line is connected to the ready signal of the smart card reader (MN15).
S21	Closed	The PA22/**RXD2**/DRXD PIO line is connected to IrDA receive signal (MN16).
S22	Closed	The **PA9**/TXD0 PIO line is connected to the data signal of the smart card reader (M15).
S23	Closed	The **PB0**/TF0/TIOB3 PIO line is connected to the ring detector of the Si3044 (MN18)
S24	Closed	The **PB4**/RK0/PCK0 PIO line is connected to the off-hook detector of the Si3044 device (MN18).
S25	Closed	The PB1/TK0/**TCLK3** PIO line is connected to the receive clock of the Si3044 device (MN18).
S26	Closed	PB3/**RD0**/RTS3 PIO line is connected to the serial data out of the Si3044 device (MN18).
S27	Closed	The PB5/**RF0**/TIOA3 PIO line is connected to the frame synchro of the Si3044 device (MN18)
S28	Closed	CELL input of MAX1757 is tied to GND (MN2).
S29	Closed	PA18/DTR1/TIOA1 PIO line is connected to the reset line of the Si3044 device (MN18)
J3	Open	Extend Battery Temperature Sensor S1 must be open if installed.
J4	Closed	VDDCORE user entry measures 1.8V
J6	1-2	JTAGSEL is tied to GND
J13	Closed	User entry measures 5V full range.
J22	Open	Hardware compatibility with AT24C128/256/512
J23	Closed	PA3/**NPCS0**/PCK1 is connected to the serial DataFlash chips elect (MN9).

Note: Shaded cells indicate configuration straps/jumpers with open connections.

Note: Signal names in bold indicate that the function is shared between several signals.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- AT91RM3400 Board Layout - Top View
- AT91RM3400 Board Layout - Bottom View
- Power Supply
- AT91RM3400
- LCD and Keyboard
- Serial Devices
- Serial Interfaces
- I2S Analog Front End
- DAA
- Diagram

Figure 5-1. AT91RM3400 Development Kit Top VIew

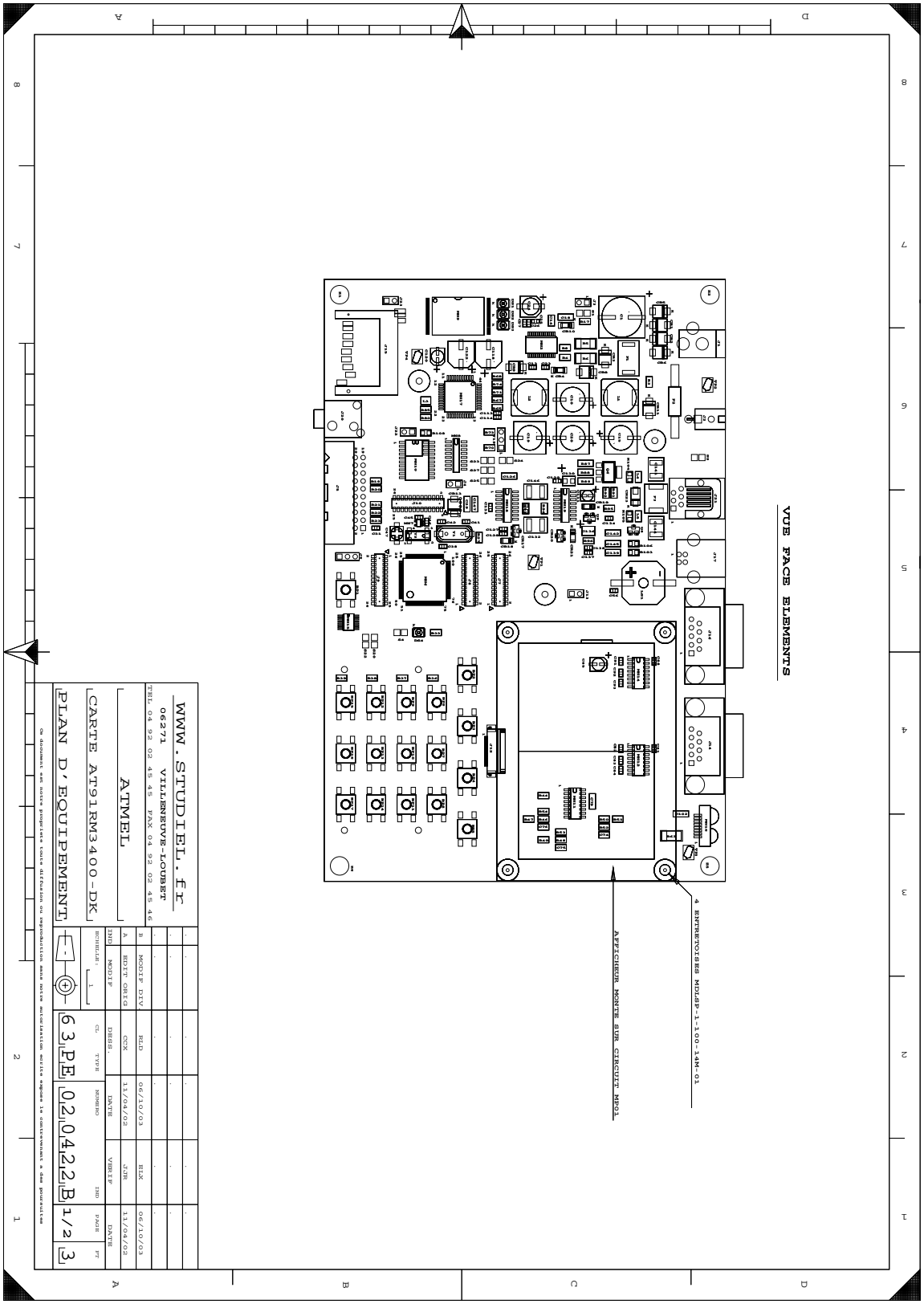


Figure 5-2. AT91RM3400 Development Kit Bottom VIew

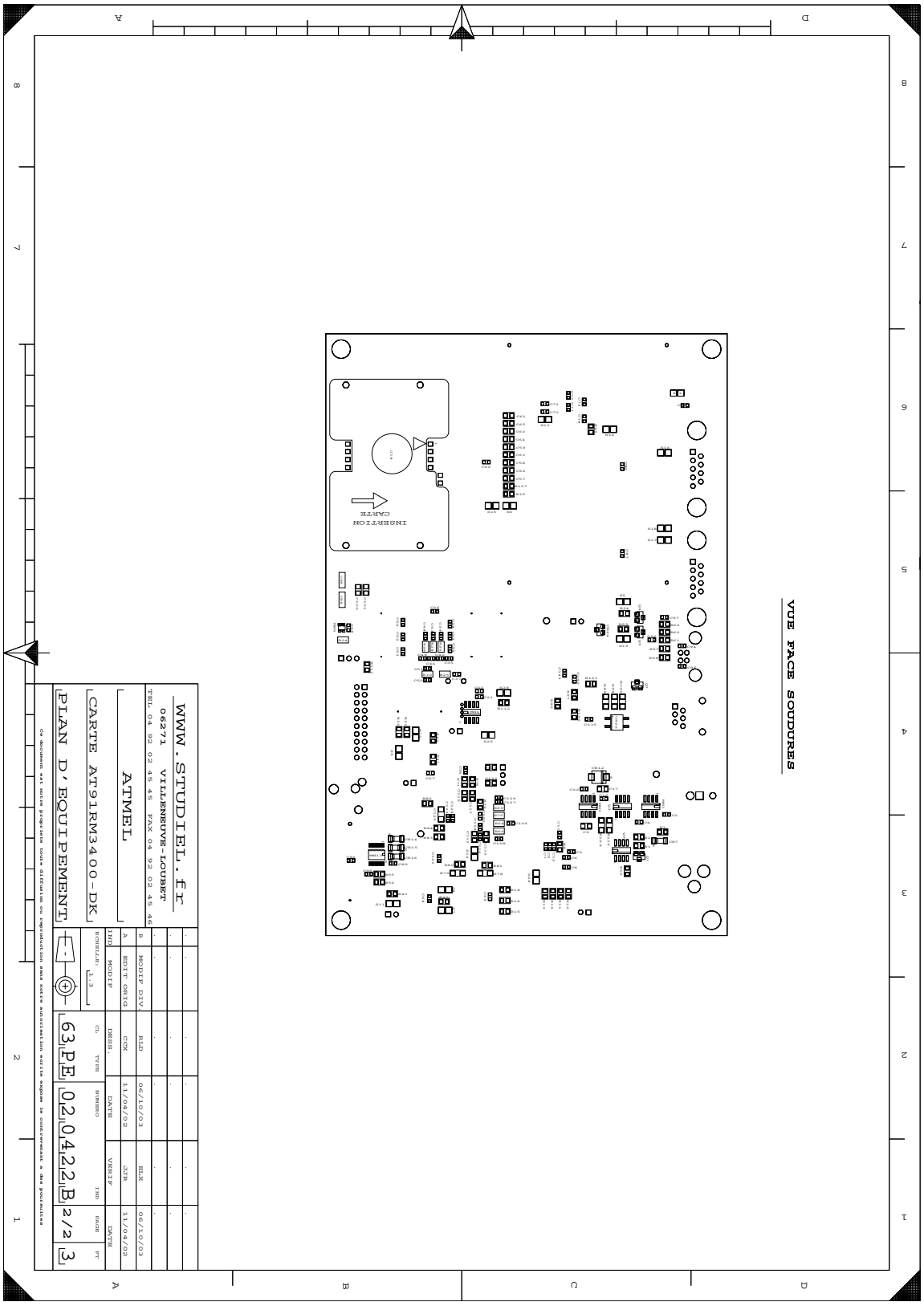


Figure 5-3. Power Supply

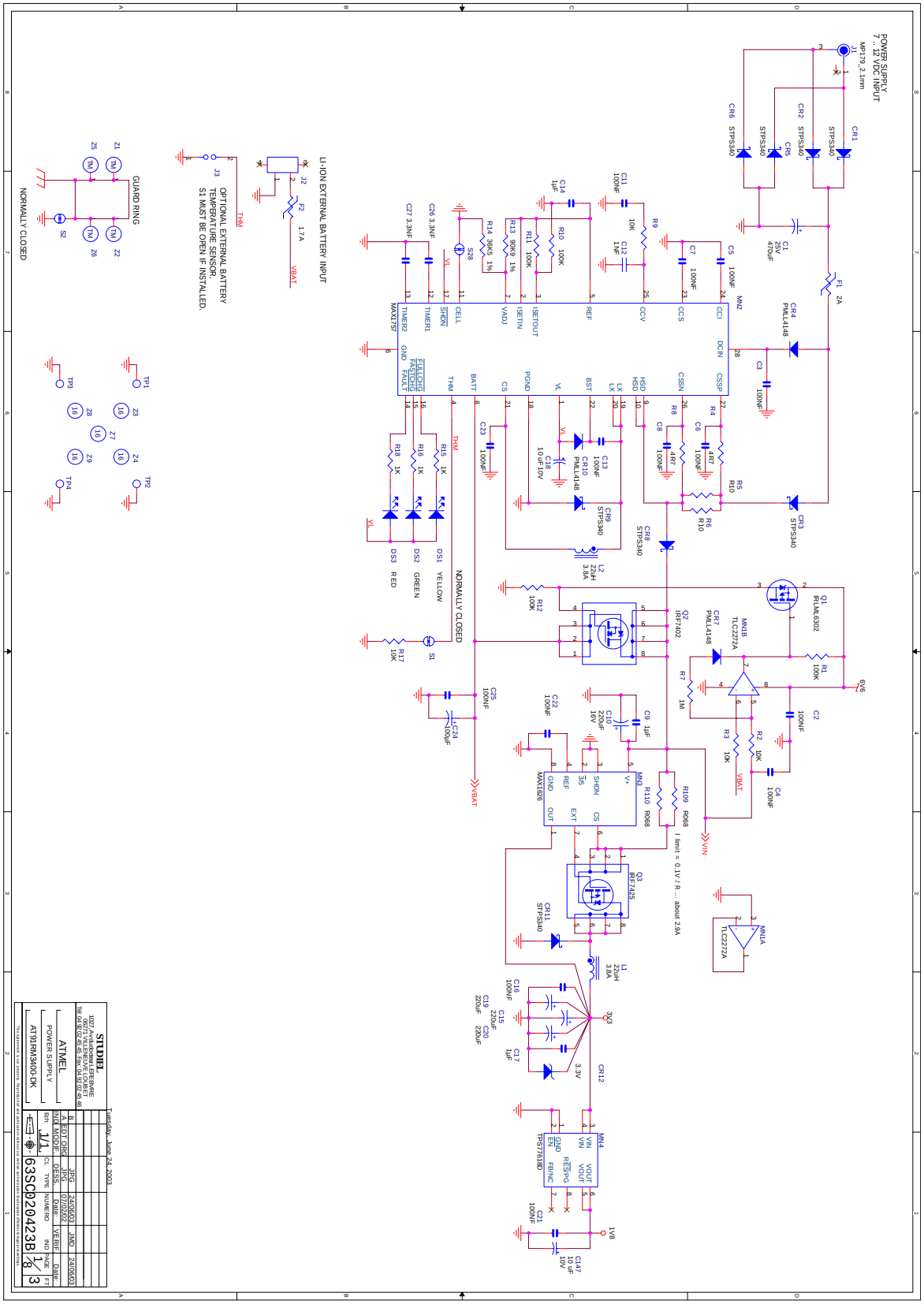


Figure 5-4. AT91RM3400 Chip

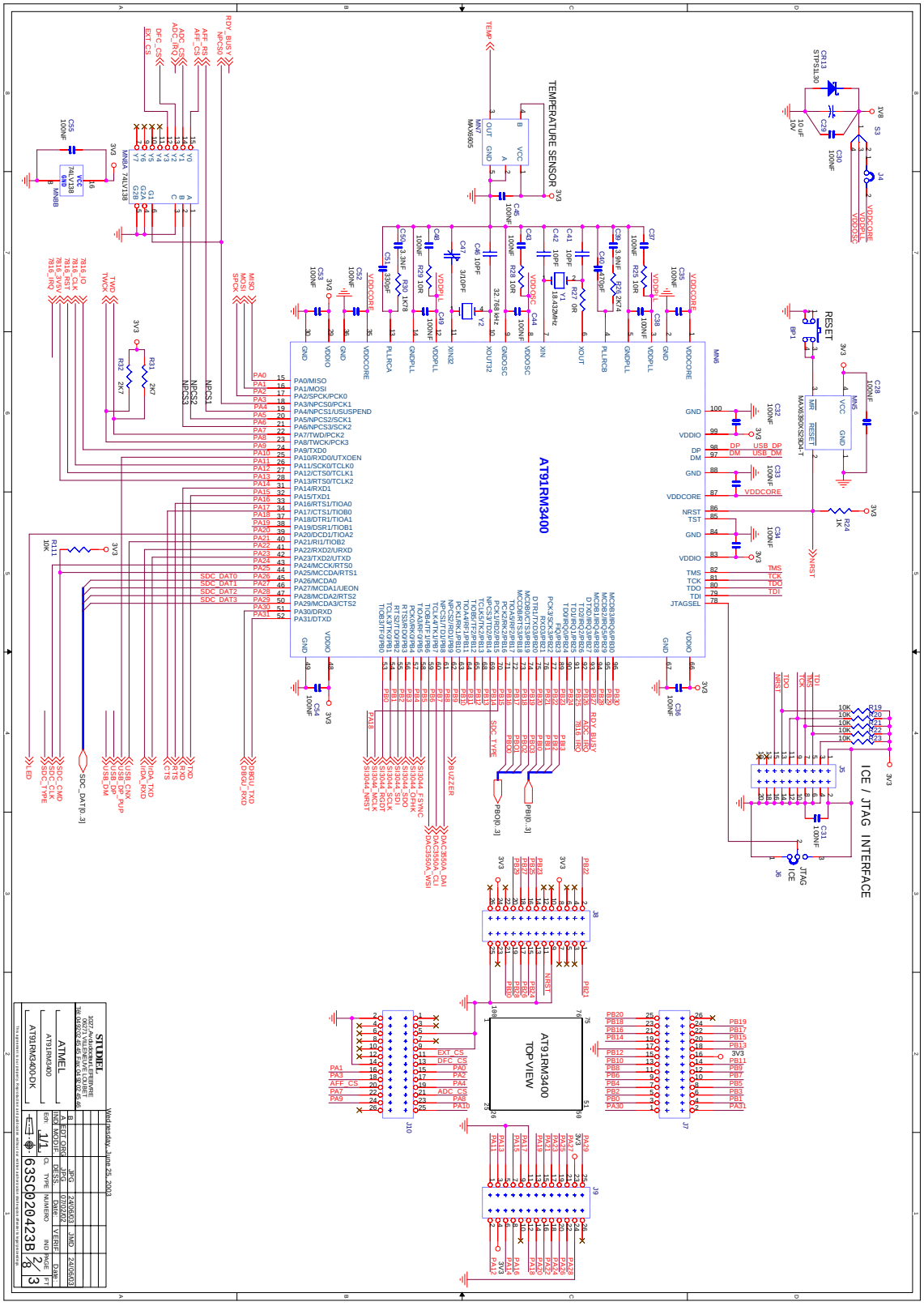


Figure 5-5. LCD and Keyboard

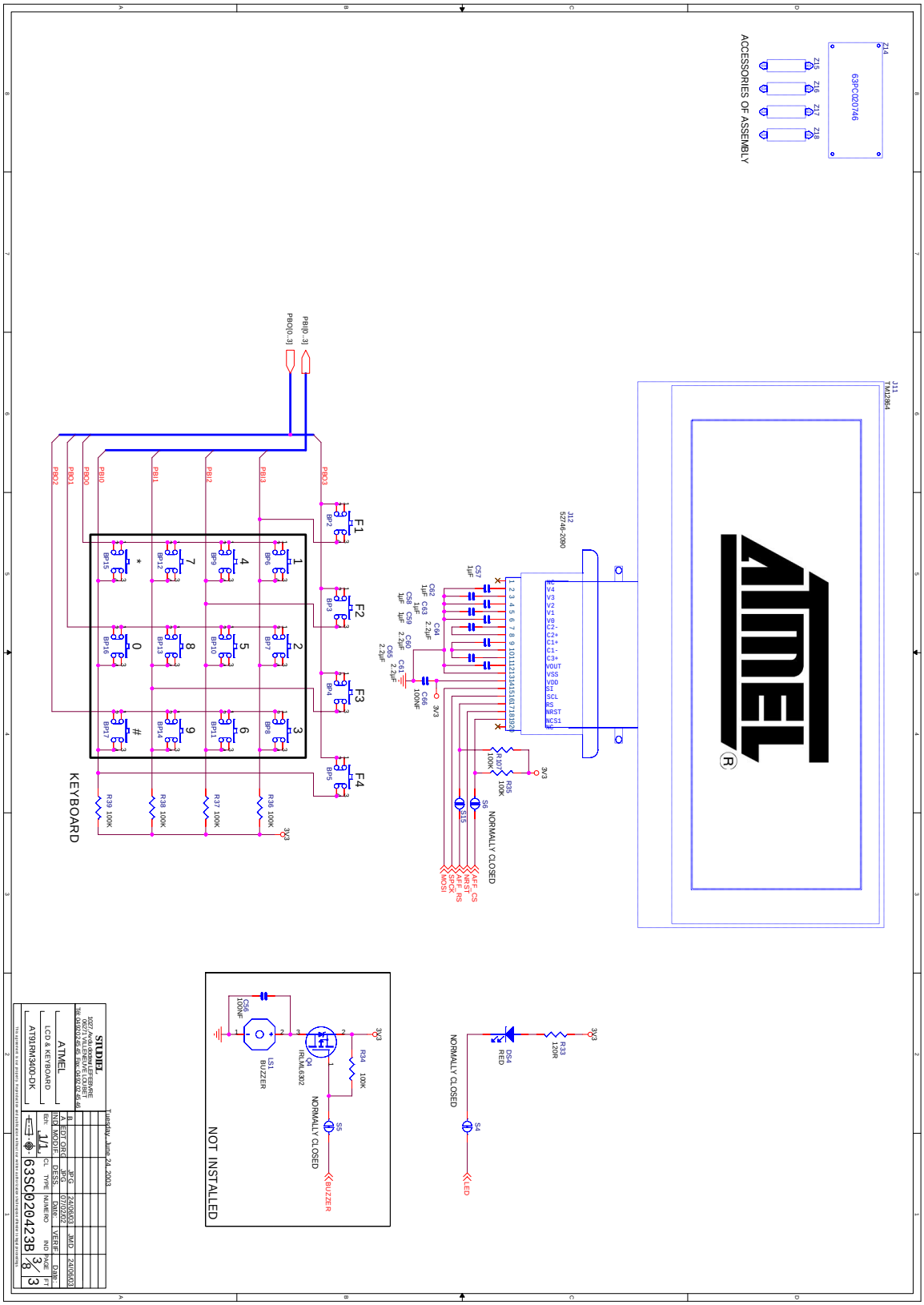


Figure 5-6. Serial Devices

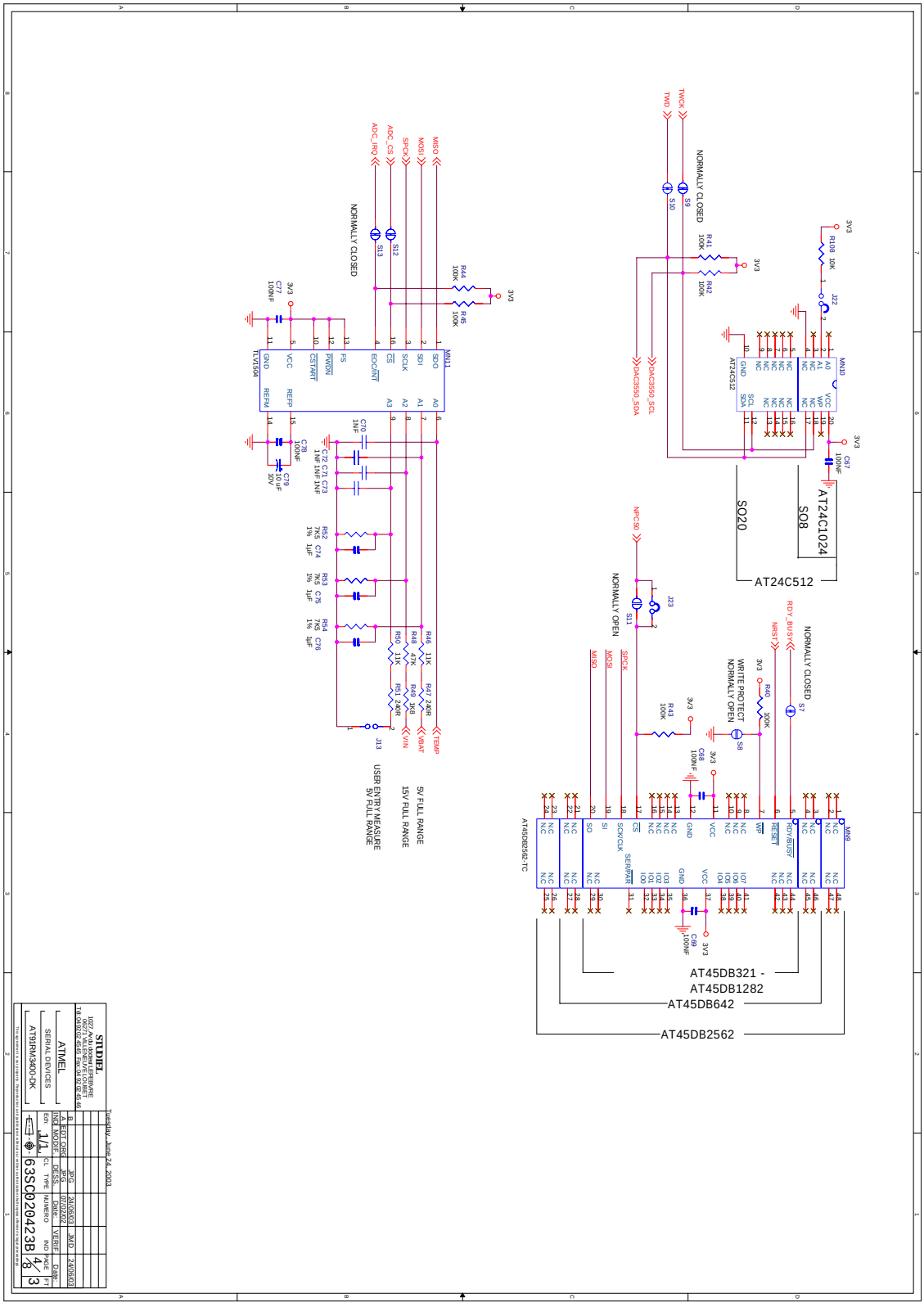


Figure 5-7. Serial Interfaces

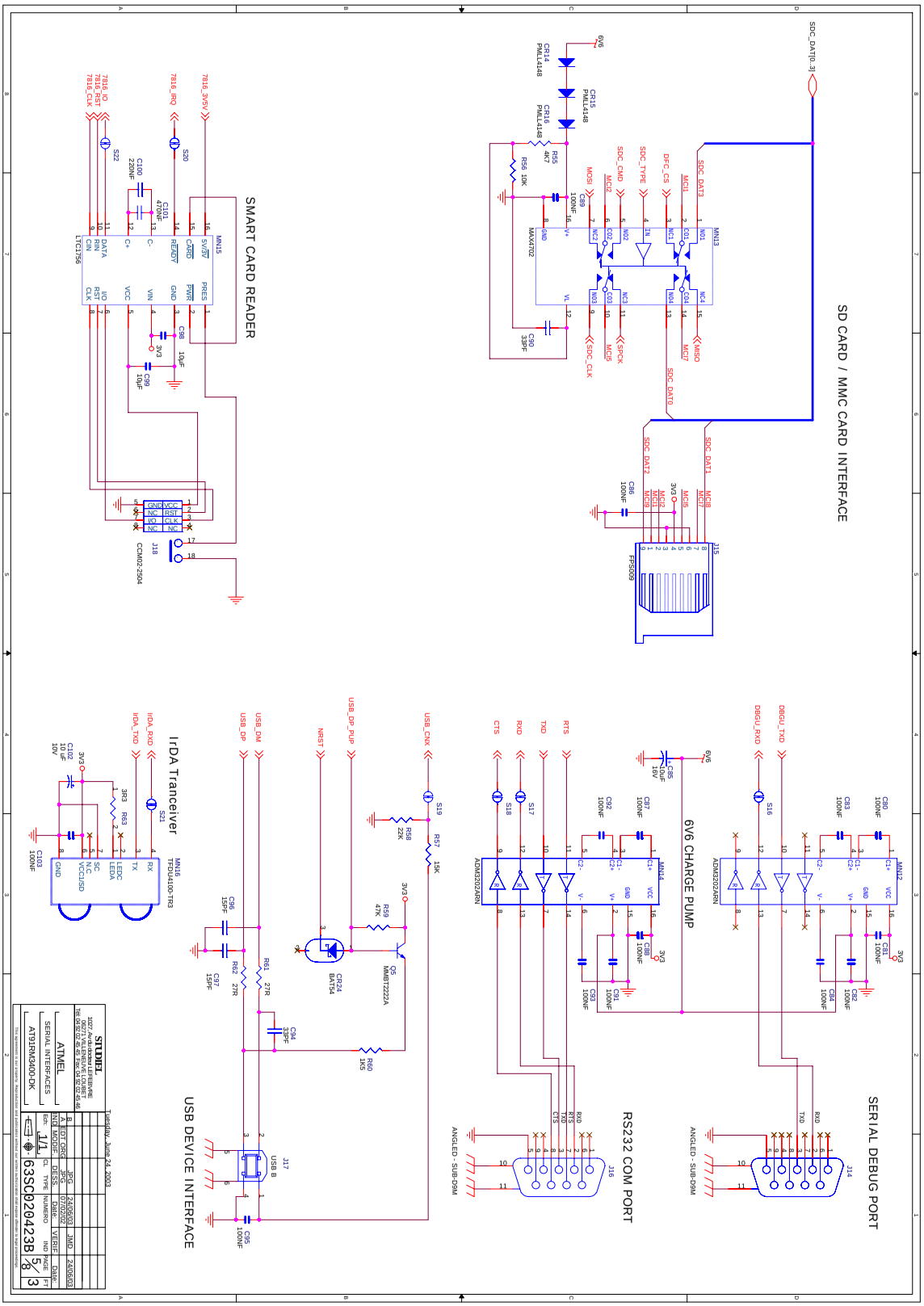


Figure 5-8. I2S Analog Front End

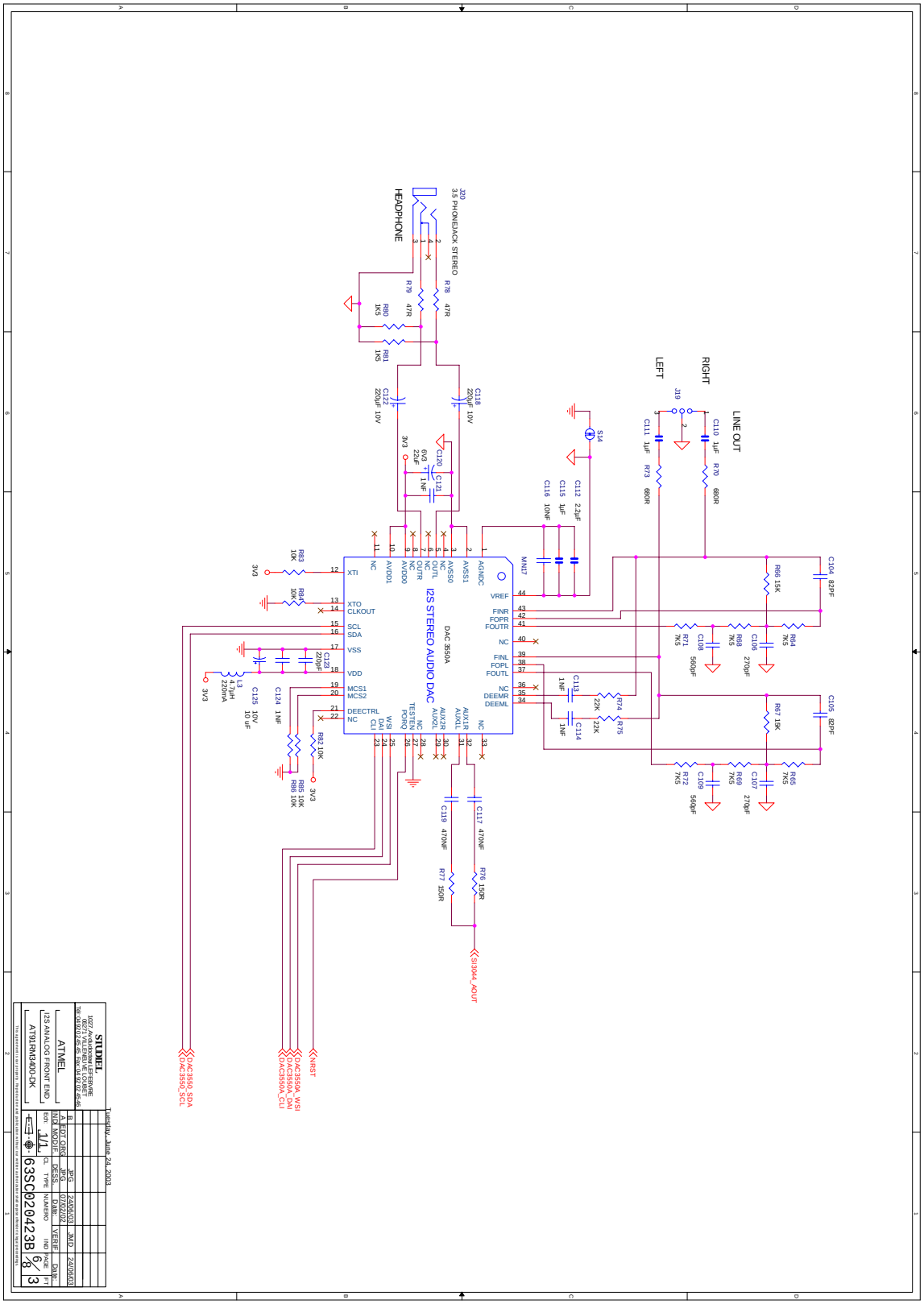


Figure 5-9. DAA

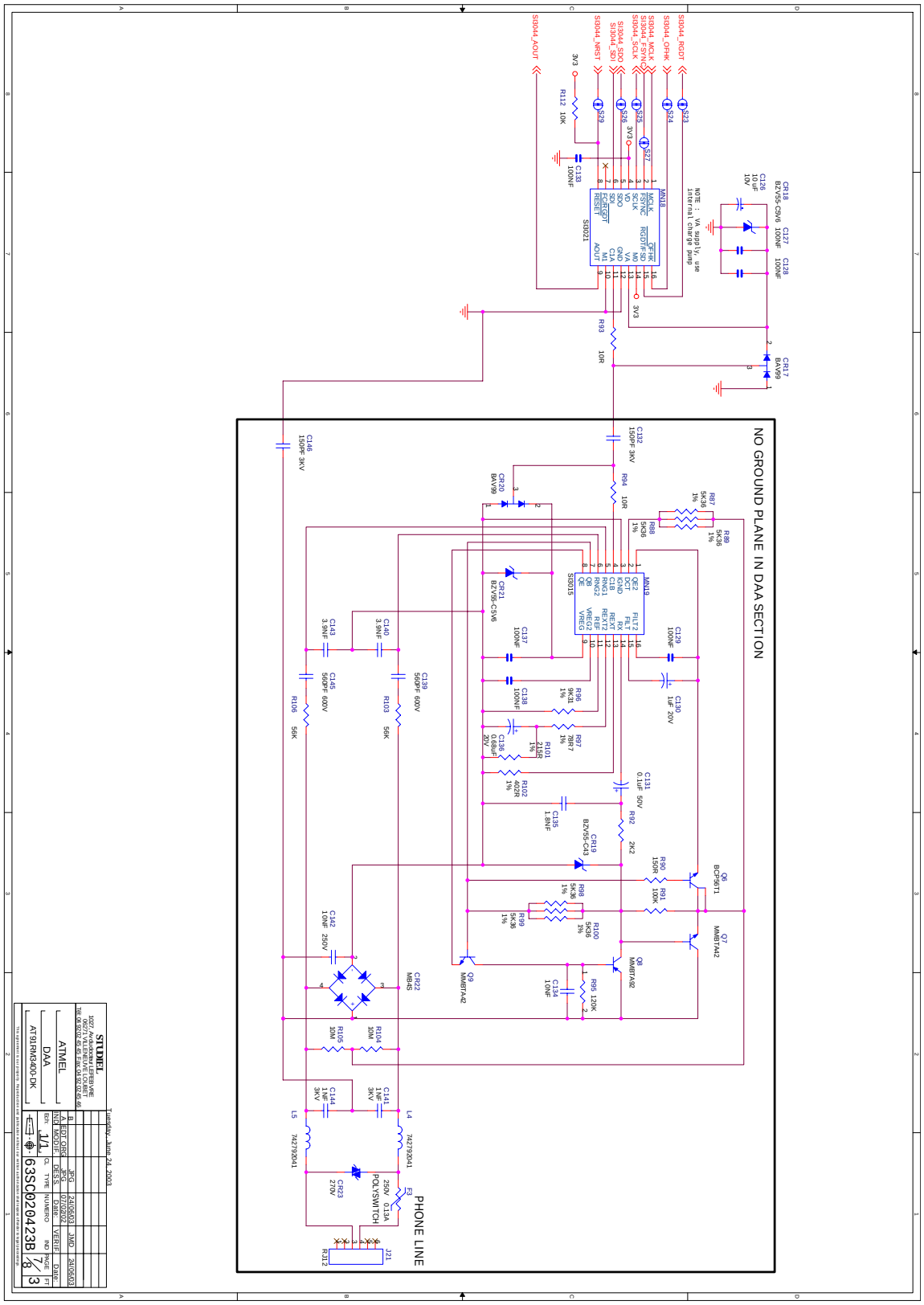
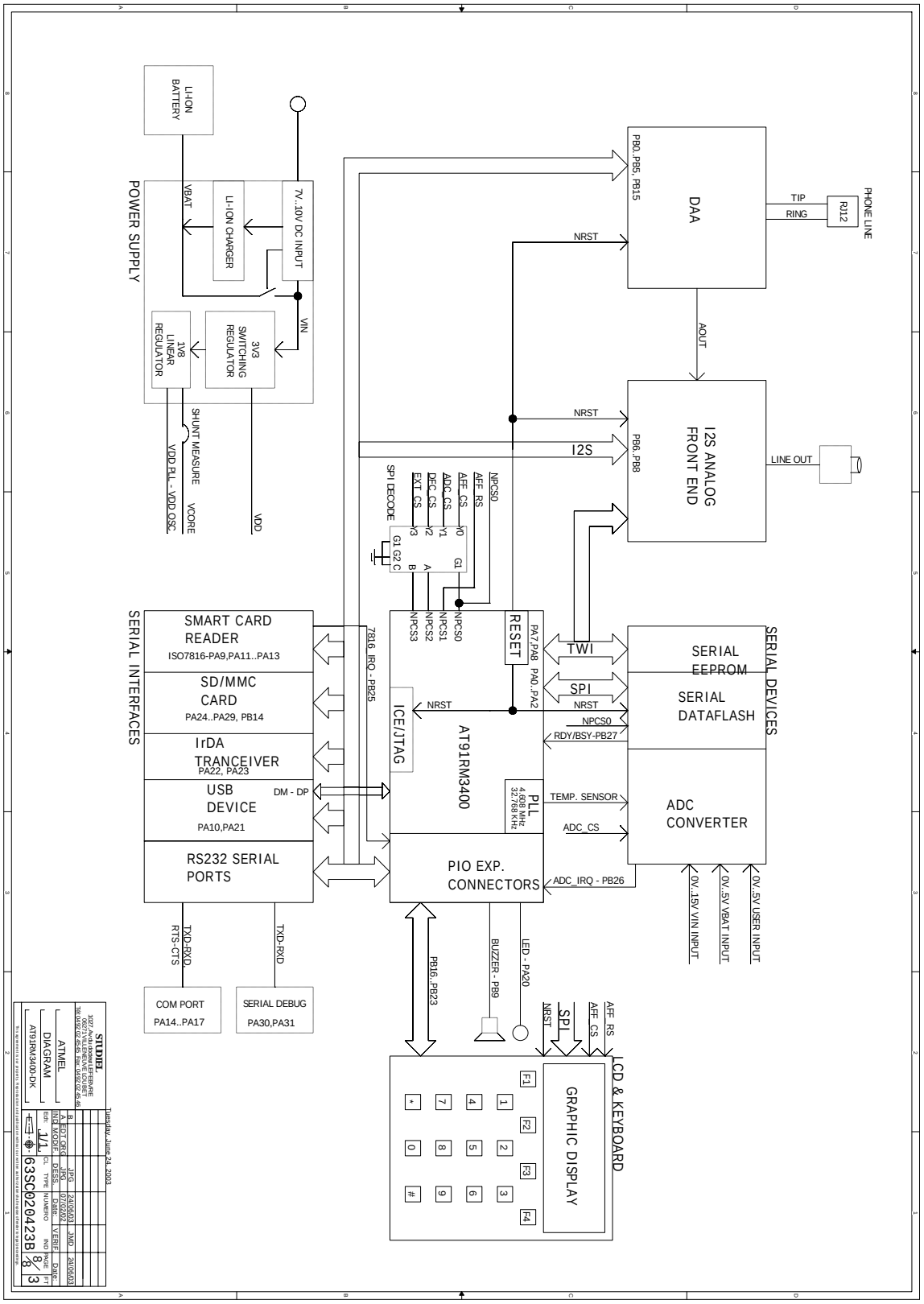


Figure 5-10. Diagram



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