Experiment 7

Bipolar Junction Transistors as Switches and Amplifiers

EECS 170A - Lab Bench #1

November 27, 2017

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1 Procedure

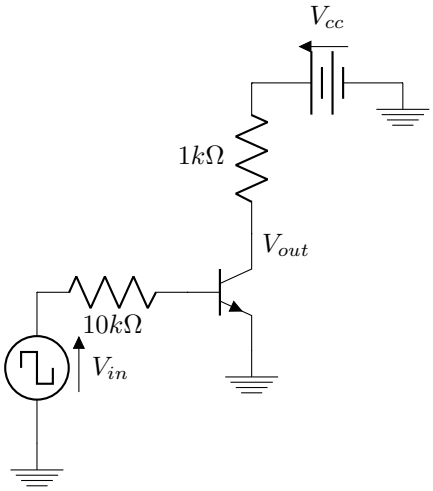
The objective of this lab is to understand the use of the bipolar-junction transistor (BJT) in circuits, in particular the common-emitter amplifier, also known as the inverter. First, the circuit is tested with a pulse input. The inverting behavior as well as the transients are observed, and the time delay, rise time, and fall time are measured. This experiment demonstrates the switching capabilities of the BJT. Next, the BJT is used as an amplifier for sinusoidal input signals. An input signal at 10kHz is applied, and the input voltage is increased until the output voltage starts to clamp. The gain is then measured. After this, the upper cutoff frequency as well as the gain at this frequency are determined. Lastly, a square wave input at the cutoff frequency is tested and its output observed.

2 Results and Analysis

2.1 Inverting Characteristics of the BJT

The inverter circuit is constructed using a BJT. The input and output signals of the BJT inverter circuit are analyzed to determine its unique properties. The output signal is taken from the collector of the BJT in the circuit, which can be visualized below:

Figure 1: BJT Inverter Circuit



By supplying the inverter with a 10kHz square input signal with fixed minimum and maximum values at 0V and 5V respectively with a 50% duty cycle and a V_{cc} value of 5V, the following input and output signals are observed on the oscilloscope:

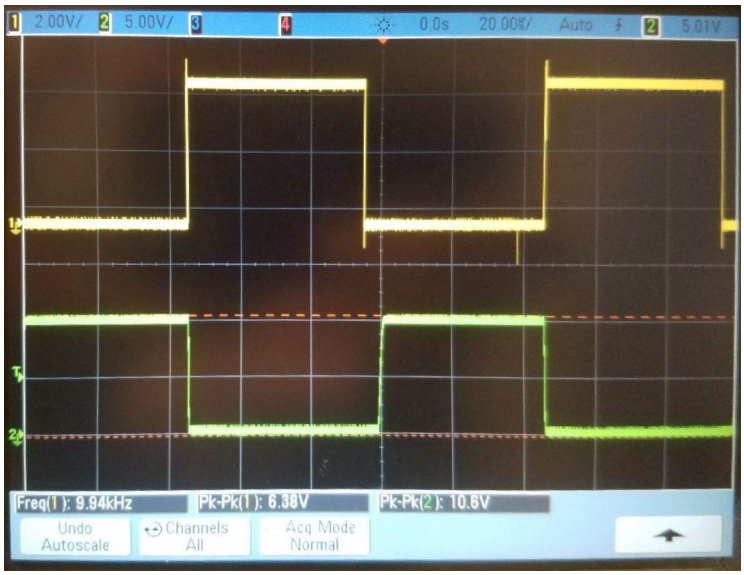


Figure 2: Input and Output Signals of BJT Inverter

This image reflects the input and output of the same circuit in Figure 1. However, the V_{cc} value in this particular image is set to 10V instead of 5V. Because an image for $V_{cc} = 5$V was not taken, this image is used instead because the shape of the waveforms would be identical but with different amplitudes for the output signal.

When the square source is at its maximum, a large voltage is supplied to the base of the BJT. This translates to a forward-bias applied across the base-emitter junction and base-collector junction. At this point the BJT is operating in the saturation region. In the saturation region, the transistor effectively acts as a short circuit thus causing the output voltage at the emitter to be zero.

When the square source is at its minimum, essentially no voltage is supplied to the base of the BJT. As a result, the base-emitter junction and the base-collector junction are reverse biased and the BJT is operating in the cutoff region. In the cutoff region, the transistor effectively acts as an open circuit, so the output voltage at the emitter is equivalent to the value of V_{cc}.

By zooming in to the output signal, the rise and fall time of the signal can be measured.

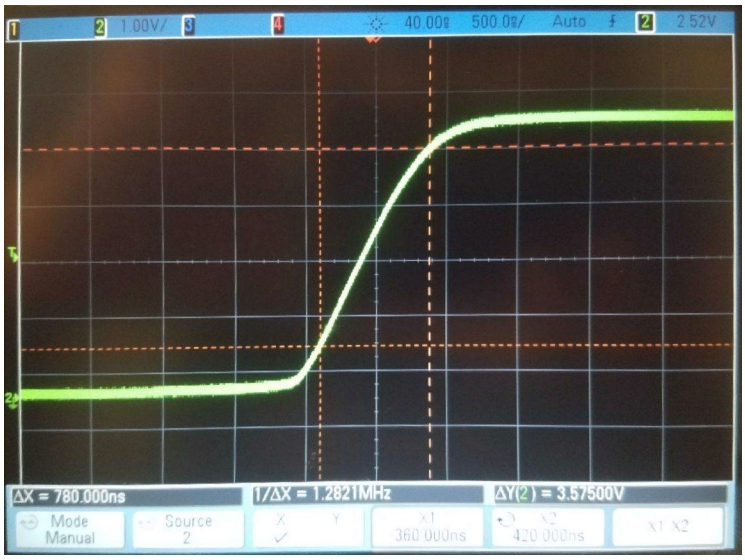


Figure 3: Rise Time of Output Signal

The rise time is found by measuring the difference in time of when the signal reaches 10% of its relative maximum and when the signal reaches 90% of its relative maximum at the rising edge. Using this method, the rise time of the output signal, t_r is measured to be 780ns.

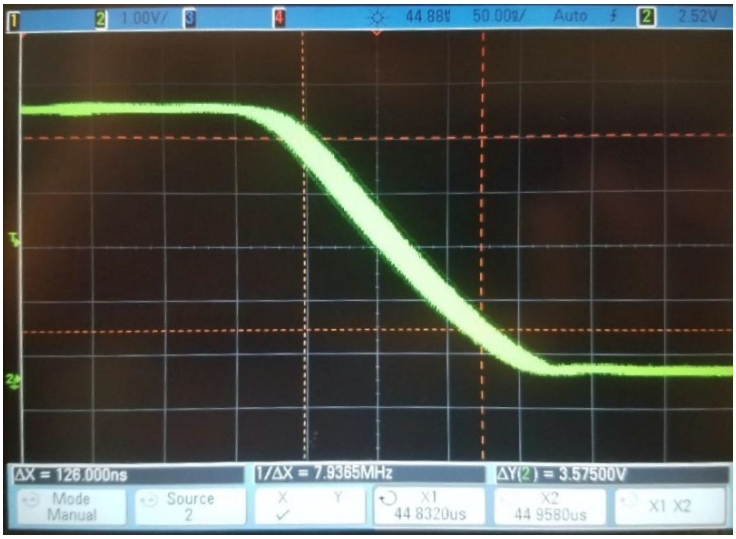


Figure 4: Fall Time of Output Signal

The fall time is found by measuring the difference between the time in which the signal reaches 90% of its relative maximum and the time in which the signal reaches 10% of its relative maximum at the falling edge. Using this method, the fall time of the output signal, t_f is measured to be 126ns.

The delay times between the input and output signals for the saturation to cutoff transition and the cutoff to saturation transition of the BJT can be found by finding the difference between the time in which the input and output signals reach 50% of their respective relative maxima. The measurement taken for the delay time for the saturation to cutoff transition of the BJT is shown in the following figure:

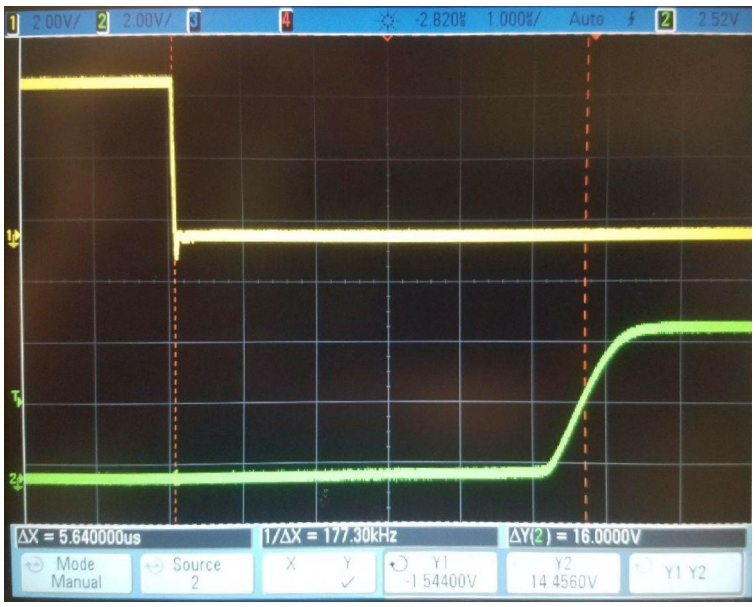


Figure 5: Delay Time for Saturation to Cutoff Transition

The delay time, t_d, for the saturation to cutoff transition of the BJT is measured to be 5.64µs. t_d for the cutoff to saturation transition of the BJT is very close to the value found for t_f, and is approximately 130ns. The t_d value for the saturation to cutoff transition is the more significant one by a large margin.

While the delay times are large for the BJT inverter circuit, they are still reasonable at 10kHz. This is because at 10kHz, the period of the wave is 0.1ms. The maxima and minima of a square wave at that frequency would then have a duration of 50µs which is significantly larger than the delay times, meaning their effects are relatively minimal. However, for high frequency applications, the BJT inverter circuit will fail. If the input signal has a frequency of 3GHz, then the period of the wave would be 0.333ns. The delay times of the BJT inverter are orders of magnitudes larger than the period of the wave. Inversion of the input signal would not be observed because the slow switching time of

the BJT.

Table 1: Inverter Times

	Time [us]
Delay time (rising edge)	5.64
Delay time (falling edge)	0.130
Rise time	0.780
Fall time	0.126

2.2 Amplifying Characteristics of the BJT

2.2.1 Gain and Frequency Response of Common-Emitter Amplifier

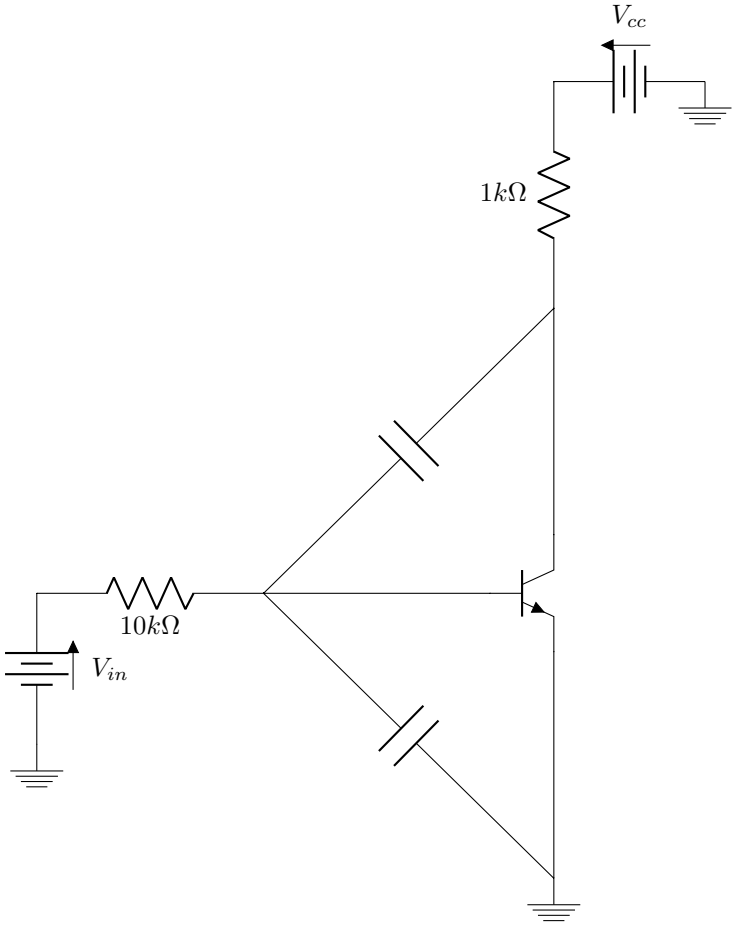
This portion of the experiment demonstrates the amplification behavior of the inverter, also known as a common-emitter amplifier. Its properties are characterized by analyzing its gain and frequency response.
The amplifier's input signal has a 200mVpp amplitude and an 800mVpp offset. When the amplitude is increased to 400mVpp, distortions occur in which the waveform becomes clipped. This is because the output waveform is amplified, but its peak and trough voltages are limited by the supply and ground voltages, respectively.

Figure 6: Common-Emitter Amplifier 10kHz Distortions

The amplifier does not have a perfect frequency response due to the structure of the BJT used. The BJT has two pn-junctions, one between the collector and the base and one between the base and the emitter. Due to a variety of effects,

the junctions each have an associated capacitance. At DC, current can easily flow through the BJT. Thus, these capacitances are not accurately modeled using a series capacitance since that would simply charge. A better model uses parallel capacitances, like in figure (7) below:

Figure 7: High Frequency BJT Model



At low frequencies, the parasitic capacitances acts as broken circuits. Thus, the circuit reduces to an ideal common-emitter amplifier. However, at higher frequencies, signals can short through the parasitic capacitances. Specifically, a short path exists between ground and the collector, making $V_{out} = 0$V. Thus, as frequency increases, the output voltage for a given input voltage, and therefore the gain, should drop. This is because gain is defined as $\frac{V_{out}}{V_{in}}$ [1].

At 10kHz, the input voltage is the starting value of 200mVpp, and the output voltage is 1.63Vpp. Thus, the gain is 8.15. Since parasitic capacitances should drop the gain at higher frequencies, a cutoff frequency can be defined. The

cutoff frequency f_c is the frequency at which the output voltage is $\frac{1}{\sqrt{2}}$ of the peak output voltage for a given input voltage [2]. So, in this case, f_c is the frequency at which the output voltage is $\frac{1.63}{\sqrt{2}}$ Vpp $\approx$ 1.15 Vpp. This can be measured by simply increasing the frequency until an output voltage amplitude of 1.15 Vpp occurs. Using this method, the cutoff frequency $f_c \approx$ 150kHz is obtained. At this point, the gain is approximately 5.75.

Table 2: Common-Emitter Amplifier Frequency Response

Frequency [kHz]	Gain [unitless]
10	8.15
150	5.75

2.2.2 Square Wave Response of Common-Emitter Amplifier

The frequency of the square wave response is set to the cutoff frequency $f_c =$ 150kHz. In order to understand the square wave response of a common-emitter amplifier, the 20% duty cycle case is considered first.

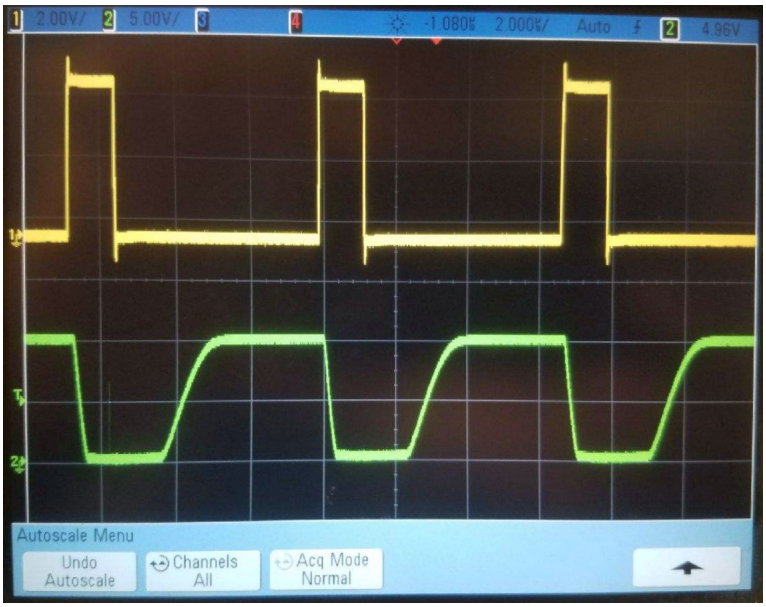


Figure 8: Common-Emitter Amplifier Square Wave Response 20% Duty Cycle

When the square wave pulse is high, the output drops nearly to ground due to the inverting characteristics of the amplifier. When the input drops to ground, the output gradually becomes high for the same reason. There is a brief delay between the falling edge of the input waveform and the rising "edge" of

the output waveform. This is because the capacitors in figure (7) need to charge first before the low-pass filter's DC characteristics take over. The charging and discharging of the capacitors represents the formation and destruction of the depletion regions in the BJT.
The reason the output waveform appears to saturate is because the duty cycle is low enough that the input signal remains low for long enough that a steady state can be established. It saturates at 10V, the supply voltage, because the output voltage cannot exceed supply. The amplifier operates on the principle of using the weaker signal to enable or disable a transistor switch that controls a larger voltage. This larger voltage is the supply voltage, which is why the output cannot exceed supply.
When the duty cycle is increased to 50%, the same physical principles still apply.

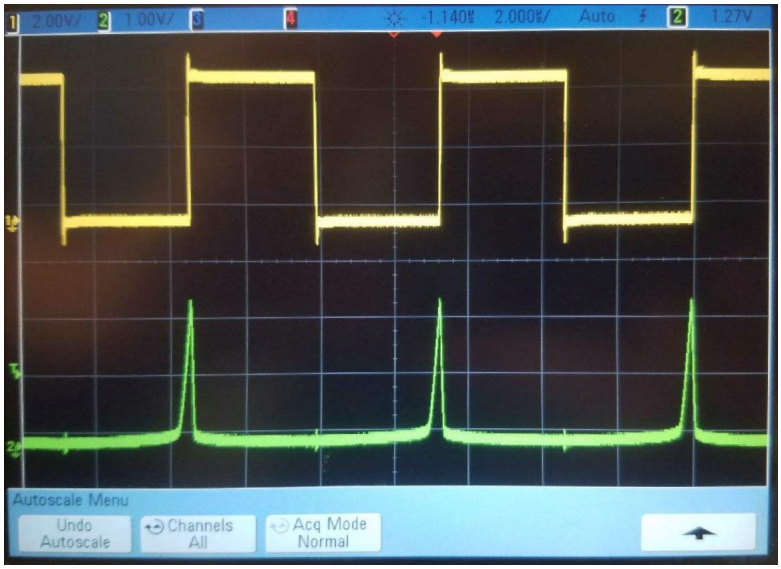


Figure 9: Common-Emitter Amplifier Square Wave Response 50% Duty Cycle

The output waveform waits for a time delay and then begins to develop. However, because the duty cycle is longer, the input signal remains low for a shorter period of time. Thus, the output voltage does not have a sufficient amount of time to fully develop and is cut short when the rising edge of the input occurs.

3 Discussion

3.1 Inverting Characteristics of the BJT

The BJT inverter circuit yields an expected output given a periodic square input signal. As expected, the 10kHz input signal is essentially inverted by the inverter with slight delay and ramping due to the recombination of excess carriers during the BJT's transition from saturation operation to cutoff operation and vise versa. The large delay times or slow switching behavior characteristic of the BJT makes the BJT inverter circuit unusable in high frequency RF applications.

3.2 Amplifying Characteristics of the BJT

The low-pass filtering characteristics of a common-emmiter amplifier are demonstrated. As expected, the gain drops as the operating frequency is increased. Thus, a cutoff frequency f_c may be considered. The cutoff frequency is determined to be 150kHz. When applying the square wave input, the output waveforms differ depending on the duty cycle. At a 20% duty cycle, the output waveform slowly saturates to a maximum voltage until the input waveform experiences a rising edge. At this point, the output reverts back to ground. This process repeats itself at the input's falling edge. At a 50% duty cycle, the input is low for too short of a time period to experience this voltage saturation. Thus, the output waveform is merely a small, short pulse at the rising edge of the input.

4 References

1. http://www.ittc.ku.edu/~jstiles/412/handouts/5.8\%20BJT\%20Internal\%20Capacitances\%20and\%20high\%20frequency\%20model/section\%205_8\%20BJT\%20Internal\%20Capacitances\%20lecture.pdf
2. http://alignment.hep.brandeis.edu/Lab/Filter/Filter.html