CMPE 160 Laboratory Exercise 5

Combinational Logic Circuit Design Using Karnaugh Map Simplification

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Abstract

In this laboratory exercise, an arbitrary function was implemented using a simplified Karnaugh map. A product of sums and a sums of product expression was generated. Both circuits were designed in Quartus II and then simulated in Modelsim. A forces file was initially used to control input pins, however, the test bench provided on MyCourses proved to be a more effient way to test the circuit. The cost of each circuit was evaluated. The cheap circuit was implemented a breadboard. The function was a four-input, one-output function described using min-term notation.

Design Methodology

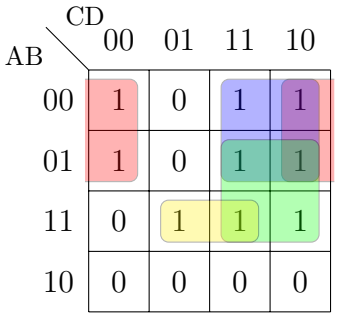
A function provided in equation 1 is a min-term representation of F.

$$F = \sum_{ABCD}(0, 2, 3, 4, 6, 7, 13, 14, 15) \tag{1}$$

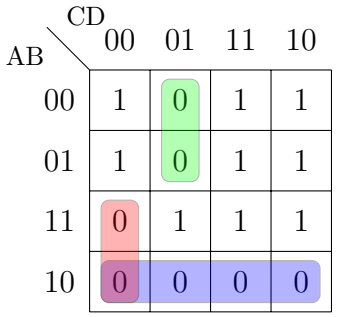
Every number above shows in the input combinations that would result in a 1 in binary. The 4-bit input is represented by A, B, C, and D in that order.

Karnaugh Maps

Two Karnaugh Maps were created to implement the function using max-term and min-terms. The sum-of-products (min-terms) and product-of-sums (max-terms) expressions were found below.



(a) Min-terms K-Map



(b) Max-terms K-Map

Figure 1: K-Maps for both POS and SOP functions

The groups in Figure 1 were written as a sum-of-products (SOP) and a product-of-sums (POS). Figure 1a shows 4 groupings and therefore 4 terms were generated. Figure 1b however, shows 3 groupings.

Reduced Expressions

An expression can be extracted from each expression. This results in a boolean expression in POS or SOP form.

$$F_{SOP} = \bar{A}\bar{D} + ABD + \bar{A}C + BC \tag{2}$$

$$F_{POS} = (\bar{A} + B)(\bar{A} + C + D)(A + C + \bar{D}) \tag{3}$$

The POS and SOP expressions above can be implemented using a circuit with AOI logic.

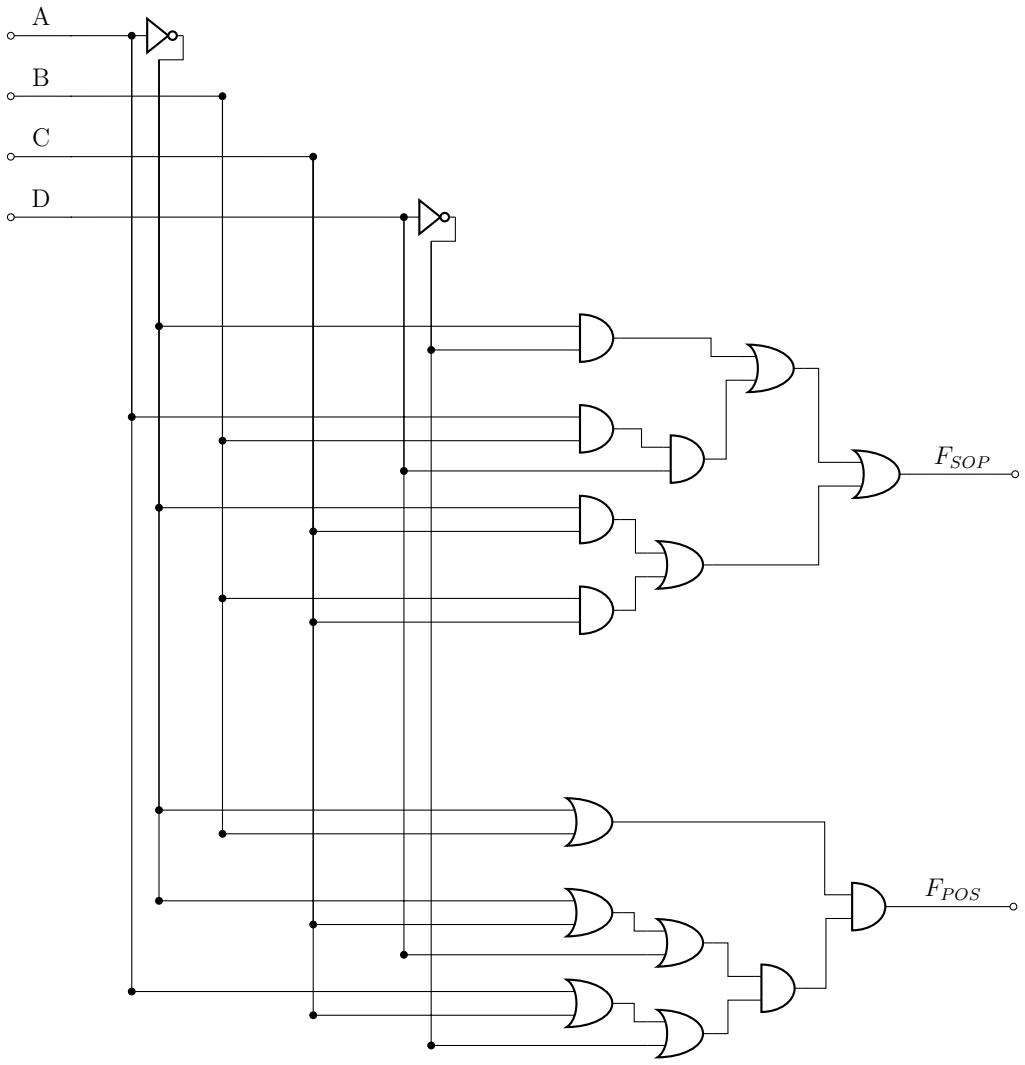


Figure 2: Circuit diagram for F_{SOP} and F_{POS}

Figure 2 is a circuit diagram for both the POS and SOP implementations of F. It displays the pin numbers to the chips in the format `CHIP_PIN`. Both input and output pins are shown on either side of every node.

Results and Analysis

THe hardware was contructed and tested using 3 chips. An AND, OR, and INVERT chip was needed to implement the circuit shown in Figure 2. The DC power supply was configured to produce a 5 V source and a maximum of 0.1 A. The first three switch were configured as inputs and four of the LED were wired as outputs. All of the input combinations of the input switches matched the output combinations on the LEDs as in Table **??**.

Conclusion

This exercise implemented a 3-input, 4-output function, F, first using boolean algebra and then translated to a circuit. The circuit was tested in ModelSim to verify the correct combination of gates were used. Finally the circuit was implemented on a breadboard and was tested using the input switches and the LEDs as output. The purpose of this exercise was to design a circuit completely from the definition to the hardware implementation.

Questions

1. A total of 6 two-input gates were used in this circuit design. This was made possible by using DeMorgan's Law to further simplify X and therefore use one of the gate outputs of W. A total of four 2-input AND gates and two 2-input OR gates were used.

2. A total of 3 ICs were used. Every 2-input, 1 output IC holds four gates. Because the OR and AND gate counts did not exceed 4, one chip could be used for each. In the case of the inverter, a 1-input, 1-output gate, a total of 6 inverter gates are inside the chip. Only one inverter was needed in order to implement the circuit. Therefore, 1x 74LS08 2-input AND gate, 1x 74LS32 2-input OR gate, and 1x 74LS04 1-input inverter chips were used.