CMPE 160 Laboratory Exercise 11

Modeling of Combinational Circuits Using Concurrent and Sequential Statements

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Abstract

In this laboratory exercise a 4:1 multiplexor circuit was implemented in VHDL. Dataflow, behavioral, and structural implementations were performed. The 74LS153 chip was simulated in ModelSim with varying input sequences to varify integrity of functionallity. The exercise was successful in simulating the chip as the outputs of the mux had expected values and predicted propagation delays.

Design Methodology

The circuit in question is meant to emulate the 74LS153 chip which includes two 4:1 multiplexors with active low enable on each. The select lines are the same for both multiplexors however each have a separate set of input lines.

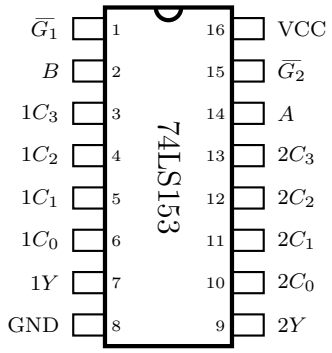

Figure 1: 74LS153 chip

Figure 1 shows the pin configuration on the 74LS153. In the figure, A and B are the select lines, $\overline{G_1}$ and $\overline{G_2}$ are the enable pins and are labeled as such to indicate their active low behavior. The two four bit numbers $1C$ and $2C$ are the input pins for each multiplexor. Finally the outputs are labeled $1Y$ and $2Y$.

The VHDL program made to emulate the chip was implemented in three different ways: Dataflow, Behavioral, and Structural. Dataflow did not take into account the time constraints of the gates inside but rather only the functionality of it. Therefore changes in input would result in immediate change in output. Behavioral was implemented similarly to the dataflow, however, the worst case scenario propagation delay of 22 ns was taken into account.

Finally the structural was implemented using an entity for every gate and their own delays.

Table 1: Gate and their delays in the 74LS153

Gate	Delay (ns)	Input
OR	7	4
AND	7	4
NOT	4	1

Each gate was written separately and given their own delay. This final structural implementation provided a more realistic emulation of the propagation delay experienced on the actual chip.

Results and Analysis

A test bench is required to test the VHDL circuit. To do this an input sequence must be chosen. The first input sequence started with a 4-bit number and performed a circular left-shift every 50 ns. The select lines which created a 2-bit number (BA) was incremented every 100 ns. The input consisted of two of these 4-bit numbers that would each shift left twice on every interval. To maximize the number of changes in input, these two 4-bit numbers swaped the input they were going to on every 100 ns cycle.

Table 2: Test set 1

G	B	A	C3	C2	C1	C0
0	0	0	1	1	1	0
0	0	0	0	0	0	1
0	0	1	1	1	0	1
0	0	1	0	0	1	0
0	1	0	1	0	1	1
0	1	0	0	1	0	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0

Table 2 shows the inputs and the select line combinations. The double row splits indicate a passing of 100 ns. The first row of each grouping shows the first 4-bit number being left shifted. The row each mux input will see changes on every select line change.

The second test set was meant to test every select combination of two different four bit numbers.

Table 3: Test set 2

G	B	A	C3	C2	C1	C0
0	0	0	1	0	1	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	1	0
0	0	0	0	1	0	1
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	0	1	0	1

Each of the constant 4-bit numbers were placed into one of the input vectors. The BA counter was then incremented every 100 ns. The third and final test set is simply the same as Test set 2, however, the strobes (G) were set to HIGH which disables the multiplexors. The circuit was tested in Modelsim using the test bench with the described processes. A screenshot of the wave capture was taken.

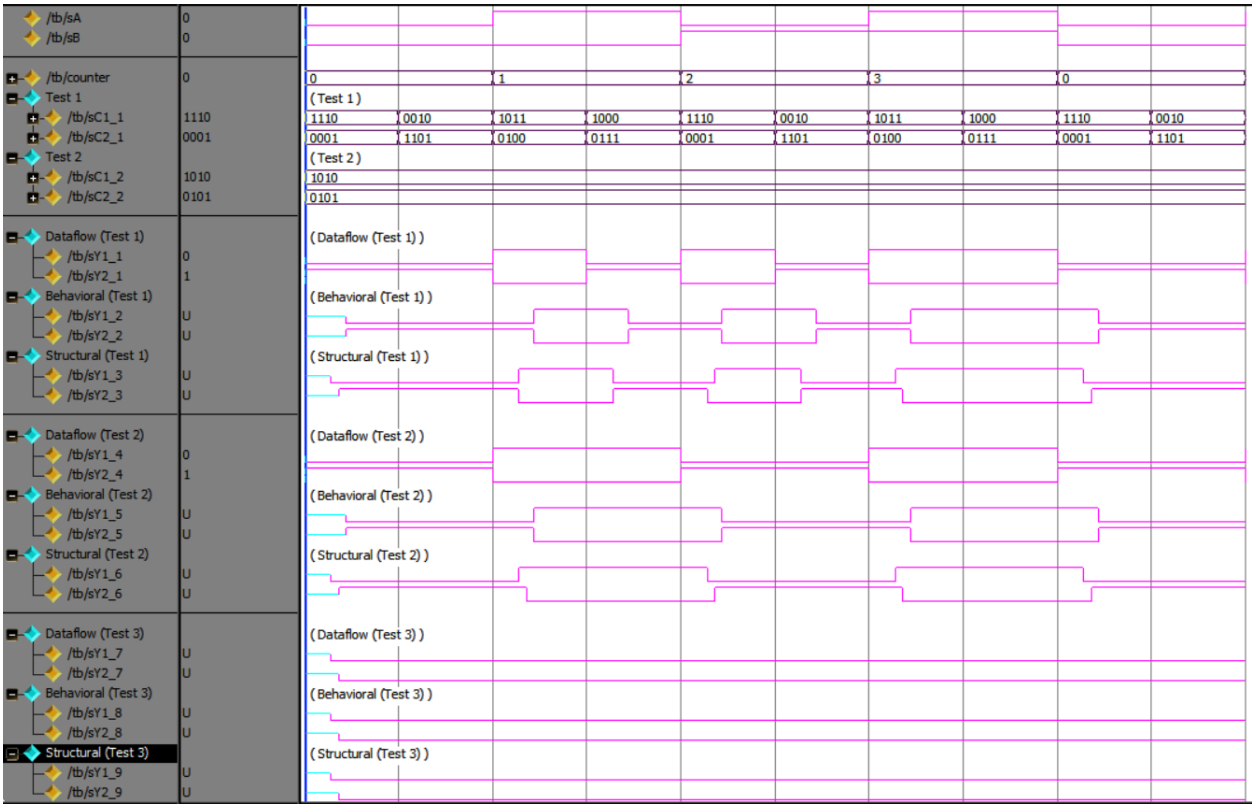

Figure 2: Wave captures I/O of all three tests.

The wave output yielded expected results. Inputs for test set 1, `C1_1` and `C1_2`, left shifted

every 50 ns as well as swapped places. The BA counter used for all Three test sets was incremented every 100 ns. Test set two has a constant set of inputs into each mux. Test set three has a HIGH input into both of its strobes and therefore yields a LOW signal during the entire test.

Conclusion

In this laboratory exercise, the functionality of a 74LS153 chip was emulated in three ways in VHDL. A dataflow implementation with no propagation delay, a behavioral with worst case delay, and a structural with individual delays for each gate were created. Three test sets with varying inputs were created to succinctly test the circuit. A wave capture was recorded to verify the integrity of the circuit. The exercise was successful as the desired outputs were attained from the original circuit and the test bench verified this integrity.

Questions

A circuit with inputs, a b c d, internal signals, u v w x y, and output z was defined.

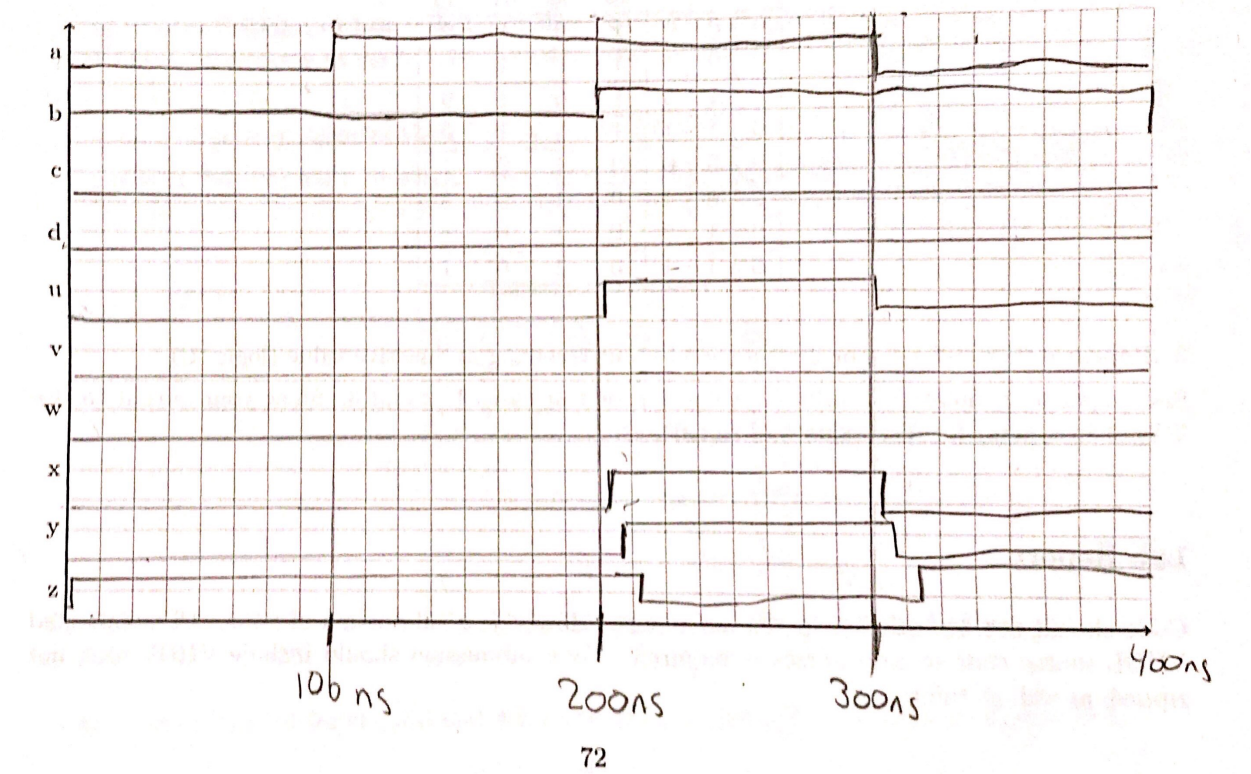

Figure 3: Wave capture of the defined circuit.

Figure 3 shows a wave capture generated over a 400 ns period.

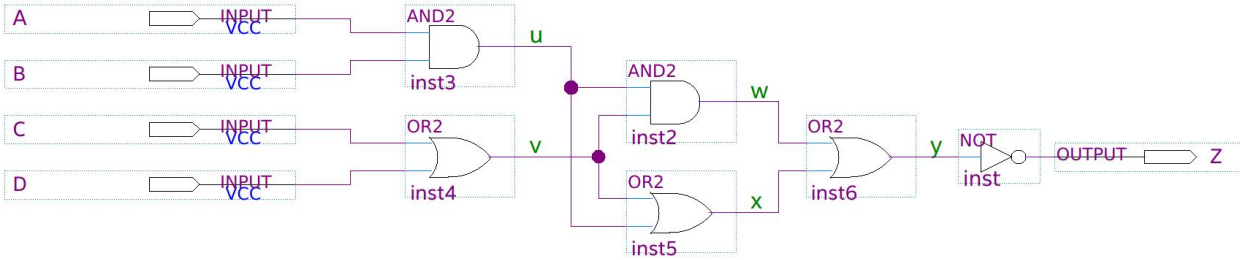

Figure 4: Wave capture of the defined circuit.

The circuit was drawn in Quartus and the internal and external signals were labeled in Figure 4.