# Homework 10

Andrei Tumbar

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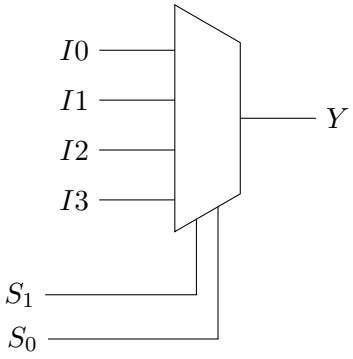
## 1 Write VHDL code (dataflow) to describe the circuit in two ways.

```
-- VHDL code for Question 1

library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Q1 is
port (
  A, C, D, E, F: in STD_LOGIC;
  L : out STD_LOGIC
);
end Q1;

architecture V1 of Q1 is
        signal B, G, H, I, J, K: STD_LOGIC;
begin
  B <= NOT A;
  H <= B AND C AND D;

  G <= NOT F;
  I <= E OR G;
  J <= NOT I;

  K <= H XOR J;
  L <= NOT K;
end V1;

architecture V2 of Q1 is
begin
  L <= NOT (((NOT A) AND C AND D) XOR (NOT(E AND (NOT F))));
end V2;

-- end of VHDL code
```

## 2 Design a multiplexor circuit to describe the VHDL code.




## 3 Design a 3:8 decoder circuit to describe the VHDL code.