CMPE 160 Laboratory Exercise 4

Combinational Logic Circuit Design Using Boolean Algebra Simplification

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Performed: February 6th
Submitted: February 13th

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Abstract

In this laboratory exercise, a circuit was implemented for a 3-input, 4-output function. The second (N_1) and third (N_2) inputs were representing a 2-bit binary number (N), the first input (C) was used as a control switch. When the control switch has a logical 0, the 4-bit out represented N^2. When C is a logical 1, the output represents $5N$. The min-terms were acquired from the 4-bit output (W, X, Y, Z). The boolean expressions were then simplified. A circuit diagram was drawn to implement the function in Quartus II. Outputs were simulated in ModelSim using every possible input. The circuit was then built on a breadboard using ICs.

Design Methodology

Truth Table

A truth table was generated to denote the outputs from a set of inputs for the function.

Table 1: Truth Table for mathematical operations N^2 and $5N$

	C	N_1	N_0	W	X	Y	Z	
0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	N^2
2	0	1	0	0	1	0	0	
3	0	1	1	1	0	0	1	
4	1	0	0	0	0	0	0	
5	1	0	1	0	1	0	1	$5N$
6	1	1	0	1	0	1	0	
7	1	1	1	1	1	1	1	

Table 1 shows the inputs and outputs of the function. When C is a 0, the 4-bit output $WXYZ$, represents N^2. When C is 1, the output is $5N$. Each output column can be treated as their own function:

$$W = \sum m(3, 6, 7) \tag{1}$$

$$X = \sum m(2, 5, 7) \tag{2}$$

$$Y = \sum m(6, 7) \tag{3}$$

$$Z = \sum m(1, 3, 5, 7) \tag{4}$$

The min-terms above can be expanded to their boolean expressions in terms of C, N_1, and N_0 and then simplified.

$$W = \bar{C}N_1N_0 + CN_1\overline{N_0} + CN_1N_0$$

$= \bar{C}N_1N_0 + CN_1(\overline{N_0} + N_0)$	Distributive property
$= \bar{C}N_1N_0 + CN_1$	Identity Law
$= N_1(\bar{C}N_0 + C)$	Distributive property
$= N_1(N_0 + C)$	Consensus Theorem

Each term from the min-term in equation 1 was expressed by a sum of products. It was then simplified using the rules of boolean algrebra. The same technique was applied for X, Y, and Z

$$X = \bar{C}N_1\overline{N_0} + C\overline{N_1}N_0 + CN_1N_0$$

$= \bar{C}N_1\overline{N_0} + CN_0(\overline{N_1} + N_1)$	Distributive property
$= \bar{C}N_1\overline{N_0} + CN_0$	Identity Law
$= (\bar{C}\overline{N_0})N_1 + CN_0$	Associative Property
$= (\overline{C + N_0})N_1 + CN_0$	De-Morgan's Law

The last step was done in order to reuse the output from the $N_0 + C)$ OR gate in the W expression. This way a 3-input NAND would not need to be used.

$$Y = CN_1\overline{N_0} + CN_1N_0$$

$= CN_1(\overline{N_0} + N_0)$	Distributive property
$= CN_1$	Identity Law

$$Z = \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + C\overline{N_1}N_0 + CN_1N_0$$

$= \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + CN_0(\overline{N_1} + N_1)$	Distributive property
$= \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + CN_0$	Identity Law
$= \bar{C}N_0(\overline{N_1} + N_1) + CN_0$	Distributive property
$= \bar{C}N_0 + CN_0$	Identity Law
$= N_0(\bar{C} + C)$	Distributive property
$= N_0$	Identity Law

The simplification for Z initially looks like a mistake because of its simplicity. However, the coresponding rows where Z was a 1 were identical to the N_0 column. In the case of Y, no gates could be reused from the first two functions.

A schematic diagram was drawn to implement these functions in one circuit. The circuit has three input pins and four output pins.

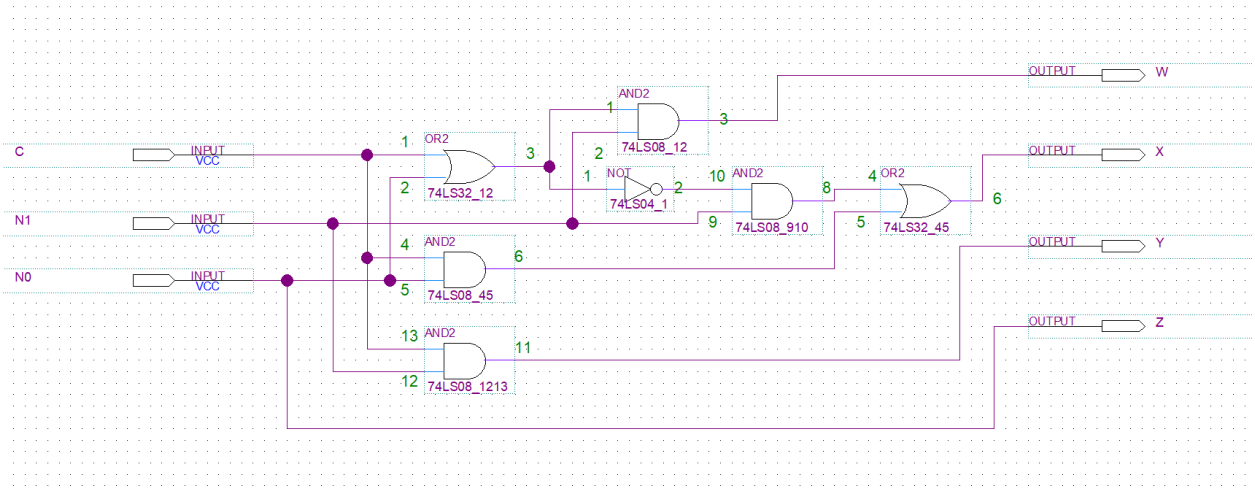

Figure 1: Circuit diagram for function with 3-inputs and 4-outputs.

Figure 1 was drawn in Quartus II using the circuit diagram function. Outputs Y and Z are easy to follow being one or zero gates. The first two outputs reused the OR gate labeled 74LS32_12. Each gate was labeled according to its IC name followed by the input pins used. The green labels are the pin numbers for both output and input on the ICs.
The above circuit was run through a simulation in ModelSim to show the resultant outputs from all of the input combinations.

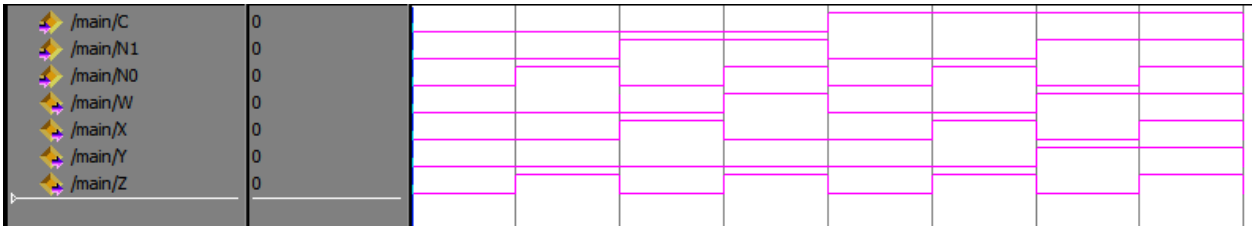

Figure 2: Simulation of the circuit using ModelSim.

Figure 2's first three rows show the inputs. The final four show the output pins. The input and output combinations match those in Table 1. This means that the circuit was set up correctly.

Results and Analysis

THe hardware was contructed and tested using 3 chips. An AND, OR, and INVERT chip was needed to implement the circuit shown in Figure 1. The DC power supply was configured to produce a 5 V source and a maximum of 0.1 A. The first three switch were configured as inputs and four of the LED were wired as outputs. All of the input combinations of the input switches matched the output combinations on the LEDs as in Table 1.

Conclusion

This exercise implemented a 3-input, 4-output function, F, first using boolean algebra and then translated to a circuit. The circuit was tested in ModelSim to verify the correct combination of gates were used. Finally the circuit was implemented on a breadboard and was tested using the input switches and the LEDs as output. The purpose of this exercise was to design a circuit completely from the definition to the hardware implementation.

Questions

1. A total of 6 two-input gates were used in this circuit design. This was made possible by using DeMorgan's Law to further simplify X and therefore use one of the gate outputs of W. A total of four 2-input AND gates and two 2-input OR gates were used.

2. A total of 3 ICs were used. Every 2-input, 1 output IC holds four gates. Because the OR and AND gate counts did not exceed 4, one chip could be used for each. In the case of the inverter, a 1-input, 1-output gate, a total of 6 inverter gates are inside the chip. Only one inverter was needed in order to implement the circuit. Therefore, 1x 74LS08 2-input AND gate, 1x 74LS32 2-input OR gate, and 1x 74LS04 1-input inverter chips were used.