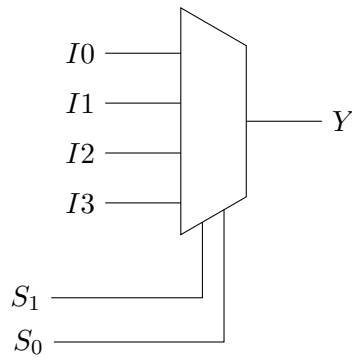# Homework 10
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1 Write VHDL code (dataflow) to describe the circuit in two ways.

2 Design a multiplexor circuit to describe the VHDL code.

$I0$

$I1$

$I2$

$I3$ — Y

S_1

S_0

3 Design a 3:8 decoder circuit to describe the VHDL code.

Decoder 3:8

	000 — Y_0
A	001 — Y_1
	010 — Y_2
	011 — Y_3
B	100 — Y_4
	101 — Y_5
C	110 — Y_6
	111 — Y_7