# CMPE 160 Laboratory Exercise 7

## Sequential Circuit Elements

Andrei Tumbar
Performed: February 27th
Submitted: March 26th

Lab Section: 4
Instructor: Mr. Byers
TA: Sam Myers
Kobe Balin
Georgi Thomas

Lecture Section: 1
Professor: Mr. Cliver



Your Signature: _____

# Abstract

In this laboratory exercise a D flip-flop was created using two D-latches. This circuit configuration allows the resultant output value to only change on a clock edge. By implementing two D-latches with active-low enable, they were connected together to create the D flip-flop. Modelsim was used to simulate the design created in Quartus. Finally, the circuit was implemented on a breadboard and the clock signal was created using a 1 $Hz$ wave generator.

# Design Methodology

A D-latch is a circuit that can store boolean values and load new values. For this functionality, three actions must be implemented. `SET`, `RESET`, and `HOLD` are needed. `SET` and `RESET` are used to load the value 1 or 0 into the latch. `HOLD` will keep the previous value constant.

Table 1: Function table for low enable D-latch

| En | D | Q | Qn |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | X | $Q_0$ | $\overline{Q_0}$ |

Table 1 shows the latch with a two input function. Because this D-latch is active-low enable, when the enable signal is low, Q takes on the value of D. When the enable is high, Q keeps the old value. This latch is asynchronous meaning that the Q value will change immediatly if the enable is low.

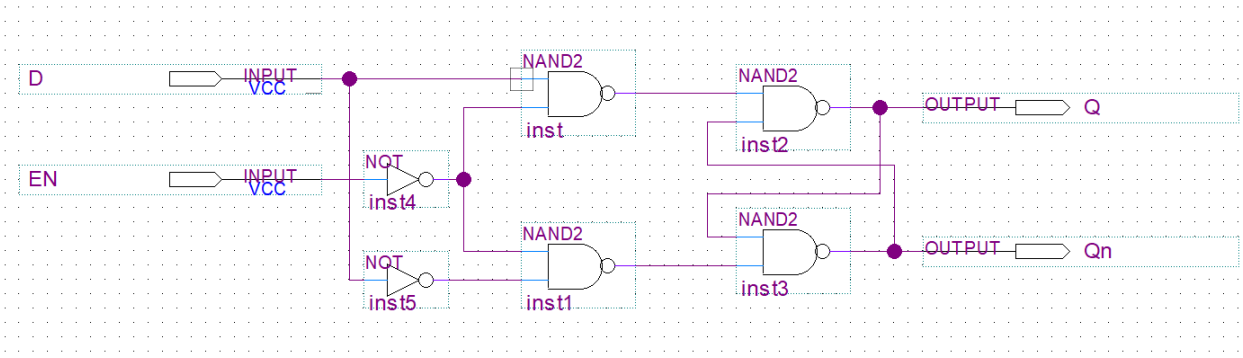


Figure 1: D-latch circuit schematic

Figure 1 is a circuit schematic of the two-input D-latch described in Table 1. There is an inverter placed after the enable input to cause the latch to be active low.
To create a clock sensitive and synchronous D flip-flop, two D-latches must be used. By using two latches and inverting the enable signal used on the second one, the time delay between the two enables will cause the resultant value to only change on a clock edge.

Table 2: Rising edge-triggered D flip-flop

| clk | D | Q | Qn |
|---|---|---|---|
| ↑ | 0 | 0 | 1 |
| ↑ | 1 | 1 | 0 |
| otherwise | X | $Q_0$ | $\overline{Q_0}$ |

Table 2 is very similar to Table 1 in that the resultant values of Q and Qn are the same. However, Q only changes on a rising edge of the enable/clock signal.

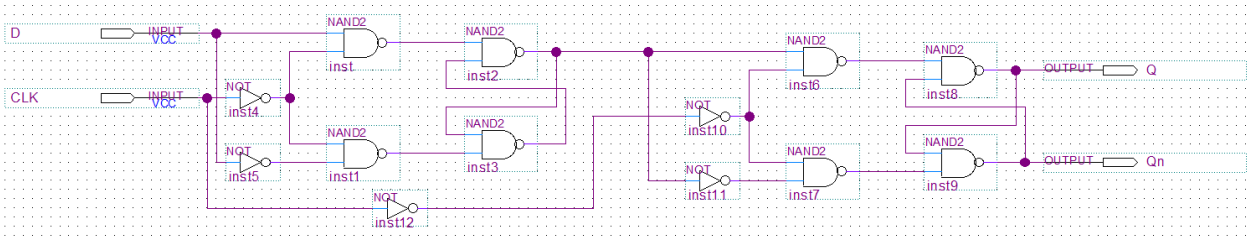


Figure 2: D flip-flop circuit schematic

Figure 2 shows the circuit configuration of the D flip-flop using two D-latches. The output of the first latch is sent to the input of the second latch. The `CLK` signal is inverted and sent to the enable of the second D-latch. The time delay on the inverter of the `CLK` will cause the output, Q, to change only when the clock value is rising.

# Results and Analysis

After the D-latch and flip-flop were designed in Quartus, a simulation in Modelsim was performed.

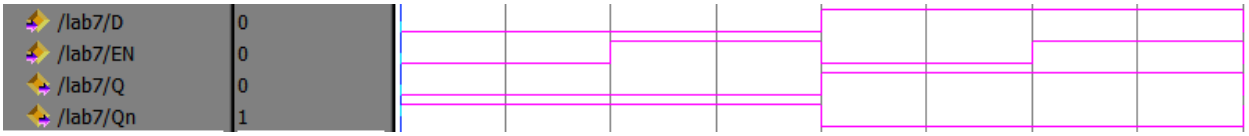


Figure 3: D-latch simulation

Figure 3 shows the results of the a modelsim simulation run with the D-latch circuit. When the `EN` signal was low, `Q` took the value of `D`. When the `EN` is high, `D` is ignored and `Q` is held to the current value. This is exactly how the D-latch was described in the previous section.

The D flip-flop was also simulated in this exercise. The enable signal however was changed to a clock signal.

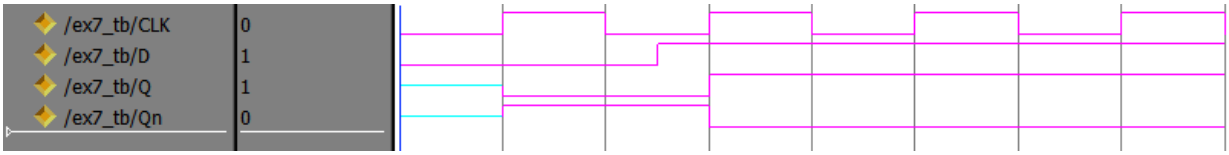


Figure 4: D flip-flop simulation

The change on the D signal in Figure 4 was placed offset to the `CLK` changes as to show a typical occurance in this circuit. Also, if the input signal, `D` were to change too closely to the clock edge, the circuit would enter a metastasis in which either 0 or 1 could result. The results of this simulation were as expected. The value of `Q` is unknown before the first clock edge therefore depicted with a line inbetween the logical 1 and 0 values. On every rising clock edge `Q` takes on the value of `D`.

After the simulations were completed, two D-latches were implemented and tested on a breadboard. After the integrity of the D-latches were verified, the two latches were combined to create a D-flipflop.

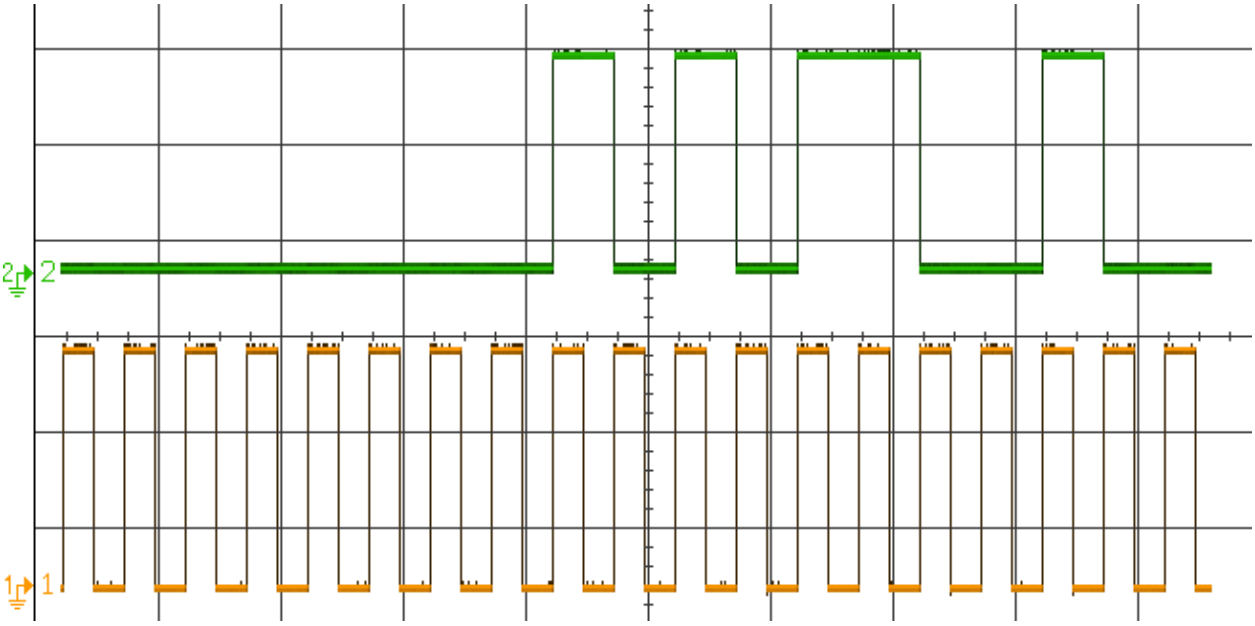


Figure 5: D flip-flop oscilloscope capture.

Figure 5 shows the results of the oscilloscope capture of from the D flip-flop implementation on the breadboard. Probe 1 was placed on the clock signal which shows a $1\,Hz$ square wave generated by the square wave function on the oscilloscope. Probe 2 was placed on the output signal. The input signal was arbitrarily controlled to test the integrity of the circuit. The results here correctly depict the functionality of the D flip-flop because value changes on the output only occur on the rising edge of the clock signal.

# Conclusion

In this laboratory exercise, a D-latch and D flip-flop were designed and simulated and later built on a breadboard. The use of a clock was made clear in designing the D flip-flop as the time delay on the inverter between the two D-latches allows for the output value to update only on a rising clock edge. The resulting simulations and breadboard experiment were successful in that they produced the desired output described.

# Questions

1. Design a falling edge-triggered D flip-flop using D latches with active-low enable.

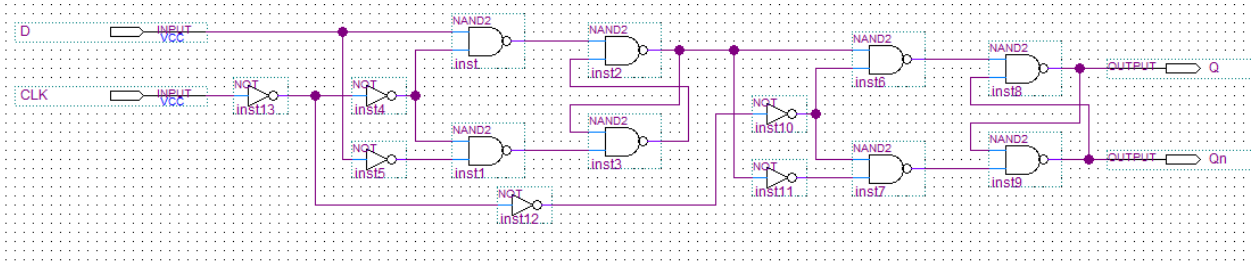


Figure 6: Falling edge triggered D flip-flop with active low enabled D latches

The only different between the falling edge-triggered D flip-flop and the rising edge is the inverter directly after the `CLK` signal. This will flip the clock and make all of the original rising edges be falling edges.

2. The 74LS175 is a quad D flip-flop IC with an asynchronous master reset pin. The maximum time needed for the MR (master reset) is $30\,ns$. The maximum time to output change after the rising clock edge is $25\,ns$. The minimum setup time before the rising clock edge is $20\,ns$. Finally the minimum hold time after the rising clock edge is $5\,ns$.