CMPE 160 Laboratory Exercise 4

Combinational Logic Circuit Design Using Boolean Algebra Simplification

Andrei Tumbar
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Lab Section: 4
Instructor: Mr. Byers
TA: Sam Myers
Kobe Balin
Georgi Thomas

Lecture Section: 2
Professor: Mr. Cliver

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Abstract

This laboratory exercise, a circuit was implemented for a 3-input, 4-output function. The second (N_1) and third (N_2) inputs were representing a 2-bit binary number (N), the first input (C) was used as a control switch. When the control switch has a logical 0, the 4-bit out represented N^2. When C is a logical 1, the output represents $5N$. The min-terms were acquired from the 4-bit output (W, X, Y, Z). The boolean expressions were then simplified. A circuit diagram was drawn to implement the function in Quartus II. Outputs were simulated in ModelSim using every possible input. The circuit was then built on a breadboard using ICs.

Design Methodology

Truth Table

A truth table was generated to denote the outputs from a set of inputs for the function.

Table 1: Truth Table for mathematical operations N^2 and $5N$

	C	N_1	N_0	W	X	Y	Z	
0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	N^2
2	0	1	0	0	1	0	0	
3	0	1	1	1	0	0	1	
4	1	0	0	0	0	0	0	
5	1	0	1	0	1	0	1	$5N$
6	1	1	0	1	0	1	0	
7	1	1	1	1	1	1	1	

Table 1 shows the inputs and outputs of the function. When C is a 0, the 4-bit output $WXYZ$, represents N^2. When C is 1, the output is $5N$. Each output column can be treated as their own function:

$$W = \sum m(3, 6, 7) \tag{1}$$

$$X = \sum m(2, 5, 7) \tag{2}$$

$$Y = \sum m(6, 7) \tag{3}$$

$$Z = \sum m(1, 3, 5, 7) \tag{4}$$

The min-terms above can be expanded to their boolean expressions in terms of C, N_1, and N_0 and then simplified.

$$W = \bar{C}N_1N_0 + CN_1\overline{N_0} + CN_1N_0$$

$= \bar{C}N_1N_0 + CN_1(\overline{N_0} + N_0)$	Distributive property
$= \bar{C}N_1N_0 + CN_1$	Identity Law
$= N_1(\bar{C}N_0 + C)$	Distributive property
$= N_1(N_0 + C)$	Consensus Theorem

Each term from the min-term in equation 1 was expressed by a sum of products. It was then simplified using the rules of boolean algrebra. The same technique was applied for X, Y, and Z

$$X = \bar{C}N_1\overline{N_0} + C\overline{N_1}N_0 + CN_1N_0$$

$= \bar{C}N_1\overline{N_0} + CN_0(\overline{N_1} + N_1)$	Distributive property
$= \bar{C}N_1\overline{N_0} + CN_0$	Identity Law
$= (\bar{C}\overline{N_0})N_1 + CN_0$	Associative Property
$= (\overline{C + N_0})N_1 + CN_0$	De-Morgan's Law

The last step was done in order to reuse the output from the $N_0 + C)$ OR gate in the W expression. This way a 3-input NAND would not need to be used.

$$Y = CN_1\overline{N_0} + CN_1N_0$$

$= CN_1(\overline{N_0} + N_0)$	Distributive property
$= CN_1$	Identity Law

$$Z = \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + C\overline{N_1}N_0 + CN_1N_0$$

$= \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + CN_0(\overline{N_1} + N_1)$	Distributive property
$= \bar{C}\overline{N_1}N_0 + \bar{C}N_1N_0 + CN_0$	Identity Law
$= \bar{C}N_0(\overline{N_1} + N_1) + CN_0$	Distributive property
$= \bar{C}N_0 + CN_0$	Identity Law
$= N_0(\bar{C} + C)$	Distributive property
$= N_0$	Identity Law

The simplification for Z initially looks like a mistake because of its simplicity. However, the coresponding rows where Z was a 1 were identical to the N_0 column. In the case of Y, no gates could be reused from the first two functions.

A schematic diagram was drawn to implement these functions in one circuit. The circuit has three input pins and four output pins.

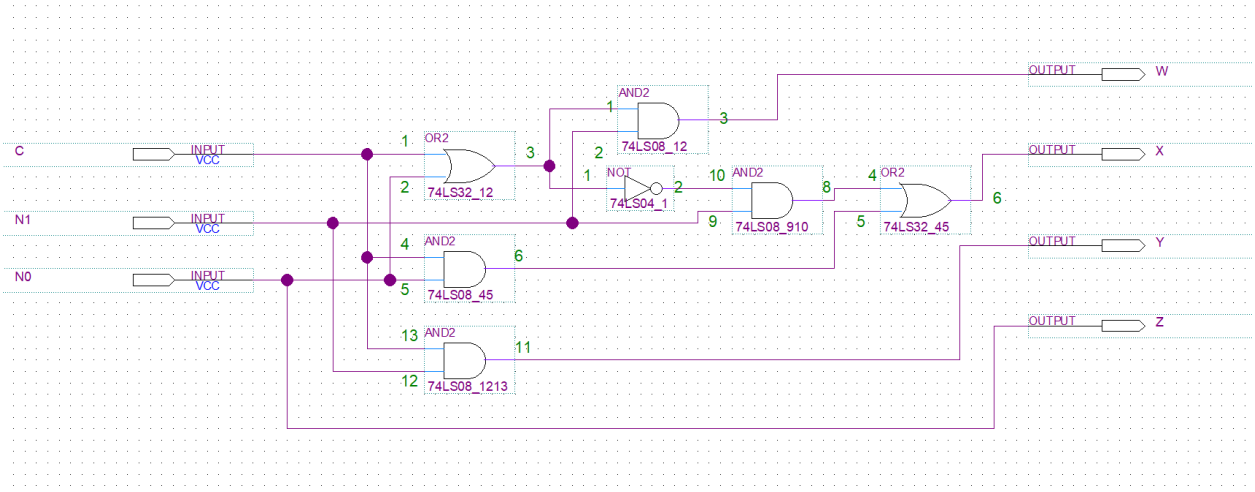

Figure 1: Circuit diagram for function with 3-inputs and 4-outputs.

Figure 1 was drawn in Quartus II using the circuit diagram function. Outputs Y and Z are easy to follow being one or zero gates. The first two outputs reused the OR gate labeled 74LS32_12. Each gate was labeled according to its IC name followed by the input pins used. The green labels are the pin numbers for both output and input on the ICs.
The above circuit was run through a simulation in ModelSim to show the resultant outputs from all of the input combinations.

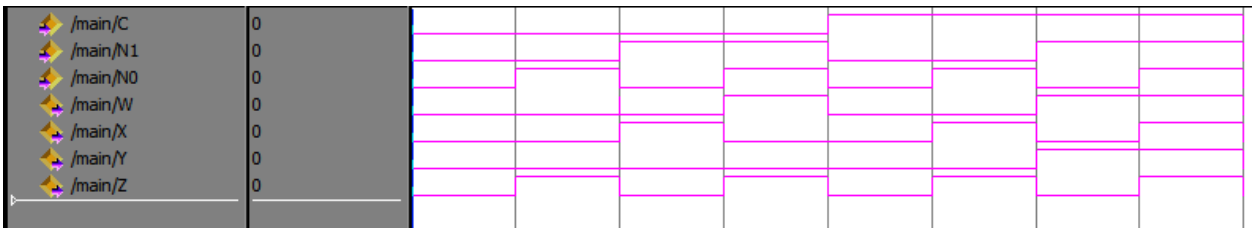

Figure 2: Simulation of the circuit using ModelSim.

Figure 2's first three rows show the inputs. The final four show the output pins.

Part Two

In part two, delay and oscillation period associated with inverters were investigated. Five inverters were wired in a series with a space for a probe to record the voltage on each node. The order that the inverters were connected proved unimportant as long as the final connection looped back to the first inverter.
Figure 3 shows the circuit diagram for the inverter oscillator. The CH1 probe was placed on the node before the first inverter. This probe acted as the reference measurement which subsequent measurements would be based off of. The CH2 probe was placed after each of

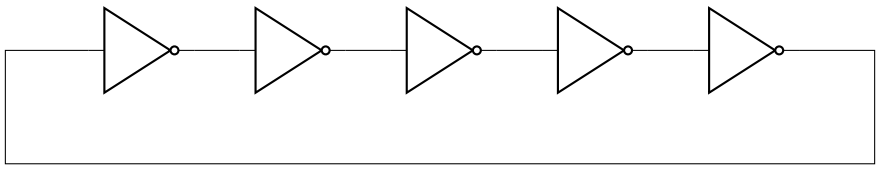

Figure 3: Circuit diagram for the inverter oscillator

the inverters and a delay measurement was taken. Both probes were grounded prior to any measurement. Each measurement needed to take in account the logical value of each probe. Because the the first probe was set in front of a rising inverter, the possible measurements were: rising to falling or rising to rising. Four measurements where taken after each inverter to find the total gate propagation.

Results and Analysis

Part One

NAND gate

The first gate that was tested was the NAND 74LS00N IC. By connecting the multimeter to the output node measurements were taken. Table 2 shows the results of the mesurements taken for the NAND gate.

Table 2: Measurements of a two input NAND gate circuit

Switch 1 Position	Switch 2 Position	$V_{in,1}$ (V)	$V_{in,2}$ (V)	V_{out} (V)	LED (on/off)
Closed	Closed	0	0	4.1	ON
Closed	Open	0	5	4.1	ON
Open	Closed	5	0	4.1	ON
Open	Open	5	5	0.27	OFF
				Logical function of gate:	NAND
				Lab kit part number for gate:	74LS00N

Table 2 shows the input and output voltages measured in the NAND gate. The inputs are either $0\,V$ or $5\,V$ depending on the position of the switch. When the switch is closed, the input is connected to ground therefore setting the potential of the input to $0\,V$. Conversely, when the switch is open, the potential of the input node is near $5\,V$. It is near $5\,V$ because there is still a resistor in series before. Table 1's output voltages conform to the electrical characteristics described on the IC's datasheet. The high output voltage is described to have a minimum value of $2.7\,V$, at $4.1\,V$ this easily meets the requirement. For the low output voltage, the datasheet describes a maximum value of $0.5\,V$ with a typical value of $0.35\,V$.

The measured voltage was $0.27\,V$ which is close to that described on the sheet. In regards to the output of the circuit, because it was a NAND gate, the only time the LED should be OFF is when both inputs are logical 1. The expected result was observed.

OR gate

The next gate that was tested was the two input OR gate. The 74LS32N chip was used to take measurements. Table 3 shows the measurements taken in this section of the exercise.

Table 3: Measurements of a two input OR gate circuit

Switch 1 Position	Switch 2 Position	$V_{in,1}$ (V)	$V_{in,2}$ (V)	V_{out} (V)	LED (on/off)
Closed	Closed	0	0	0.09	OFF
Closed	Open	0	5	4.07	ON
Open	Closed	5	0	4.07	ON
Open	Open	5	5	4.07	ON
				Logical function of gate:	OR
				Lab kit part number for gate:	74LS32N

The input circuit and resultant measurements in Table 3 for this circuit are the same because nothing was changed from there. The outputs, however, are different because this gate conforms to a different range of values. The typical and minimum output voltages on the 74LS32 gate are $3.4\,V$ and $2.7\,V$ respectively. The measured voltage was $4.07\,V$ on all logical 1 outputs. This value is well within the limits. The logical 0 output voltage was measured to be $0.09\,V$. With a listed maximum voltage of $0.4\,V$, this measurement is also well within the limits. The LED is only OFF when both inputs are OFF. This is consistent with the logical function of the OR gate.

XOR gate

The XOR (74LS86) gate is meant to output a logical 1 when the two inputs are inequivalent. Table 4 shows the measurements taken for this IC.
Again, inputs in Table 4 are equivalent to the other two sets of measurements. The measured low outputs were under the maximum logical 0 voltage of $0.5\,V$. The measured high outputs of $4.1\,V$ were well above the minimum voltage for logical 1 of $2.7\,V$. The LEDs were expected to be ON when the input signals have opposite logical states. This same expected output was observed in Table 4.

Part Two

Four different screen captures from the oscilliscope were taken on each of the nodes to show the delay propagation. Images taken from oscilliscope were inverted to make better use of colors and contrast.

Table 4: Measurements of a two input XOR gate circuit

Switch 1 Position	Switch 2 Position	$V_{in,1}$ (V)	$V_{in,2}$ (V)	V_{out} (V)	LED (on/off)
Closed	Closed	0	0	0.151	OFF
Closed	Open	0	5	4.1	ON
Open	Closed	5	0	4.1	ON
Open	Open	5	5	0.163	OFF
				Logical function of gate:	XOR
				Lab kit part number for gate:	74LS86AN

Screen captures from the oscilliscope show the voltages relative to ground on each of the nodes inbetween the gates over time. They oscillate with a period of about $55\,ns$ because the circuit consists of an odd number of inverters.
Four measurements were taken in Table 5 corresponding to the total delay propagation from the reference point to that gate.

Table 5: Effect of propagation delay

74LS04 (pin to pin)	Number of Gates of Delay	Propagation Delay (ns)
2 to 4 (rising to falling)	1	3.4
2 to 6 (rising to rising)	2	11.7
2 to 12 (rising to falling)	3	14.7
2 to 10 (rising to rising)	4	19.4
	Period:	55.6

The delay propagation shown in Table 5 shows that rising to falling vs rising to rising inversions have different values associated. If the direction of inversion is ignored, the average delay for each gate is $4.55\,ns$. When taking account of the direction of inversion, the average rising to falling delay was $3.25\,ns$ whereas the rising to rising was $5.8\,ns$. The period measured was $55.8\,ns$. The square wave oscillated on the figures 3-6 because there was an odd number of inverters in the circuit. After the signal ran through all of the inverters the original low signal inverted itself. Therefore the first oscillator would have a different input signal. If an even number of inverters were used, the probes would display no change in potential over time.
The measured period refers to the period of oscillation in the reference probe. The total time it would take to switch the logical value on the reference node would be $19.4 +$ *one inverter delay*. This is because the delay for four gates was $19.4\,ns$, however, there are five inverter gates. If the average gate delay of an inverter ($5\,ns$) was added to the total

delay measured, the half period delay would be around $23.2\,ns$. The full period would be calculated to around $46.4\,ns$. However, the measured period was $55.8\,ns$ meaning that the final inverter had a delay of $8.4\,ns$. This number is still within the range on the datasheet of the chip.

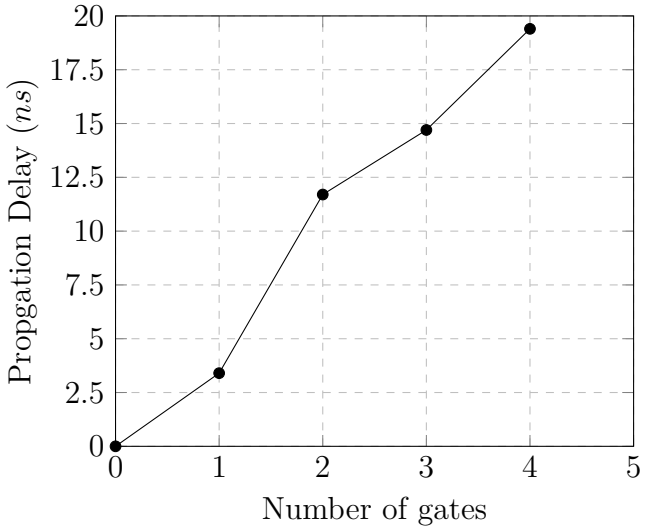

Figure 4: Graphed delay propagation vs number of gates used

Figure 4 shows the delay propagation from each inverter. The odd x-values indicate a rising to falling measurement while the even numbers read a rising to rising measurement. It can clearly be seen that the rising to falling delays are shorted than the rising to rising. This can be seen in the slopes between the ploted points. The slope from even to odd numbers is far lower than that of odd to even numbers.

Conclusion

This laboratory exercise investigated the logical and electrical properies of gates by testing a variety of different two-input logical gate chips. In the second part, the delay propagation and period of oscillation associated with a chain of inverter gates was investigated. A $55.8\,ns$ period of oscillation was observed for a 5-inverter chain. The purpose of this lab was to clarify how chips and their datasheets are used within circuit design.

Questions

1. What are these voltage values for the 74LS27

   (a) Minimum input voltage for logic 1
   2 V

(b) Maximum input voltage for logic 0
0.7 V

(c) Minimum output voltage for logic 1
2.7 V

2. Define propagation delay, and discuss how it impacts the output a gate. Why is it a consideration in digital designs?

   Propagation delay is the total time it takes for a circuit to provide an output signal given a set of input signals. Delays are propagated through the use of multiple gates because each gate has a delay associated with it. It is important to consider this delay in digital designs because an output value should not be read until the maximum delay from any path in the circuit has elapsed.

3. Design an XOR gate using 74LS08 (2-input AND), a 74LS04 (6-inverter) and a 74LS32(2-input OR).

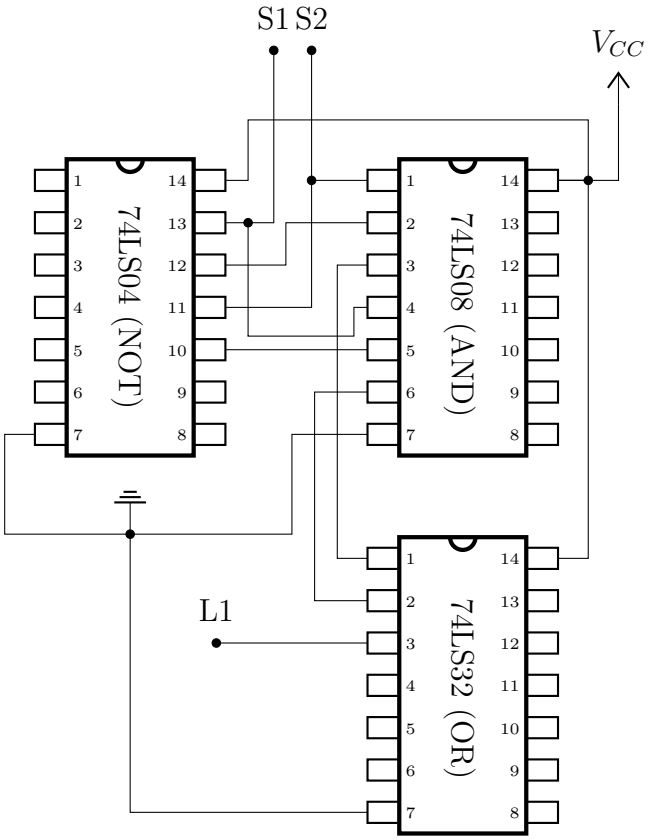

Figure 5: Circuit for 2-input XOR