# EEEE 380 Exercise 6

# Dynamic Logic

Andrei Tumbar

Instructor: Dr. Moon
TA: Karen Chen

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: _____

## Abstract

In this exercise, the behaviour of dynamic logic circuits was investated. Unlike in static logic where voltage on any given node will have a direct path to ground or the supply voltage, dynamic circuits will charge capacitors which will share charge across nodes even when disconnected from the supply voltage. These circuits are subject to degredation overtime in the form of leakage current and parasitic capacitance. This lab specifically looked at the domino circuit which implements the function $F = AB$.

## Basic Domino Logic Gate

The domino logic gate in question will have two inputs `A` and `B` as well as a `CLK` signal. A pulse sweep was used to control these inputs to show the response of the dynamic circuitry with all combinations of inputs.

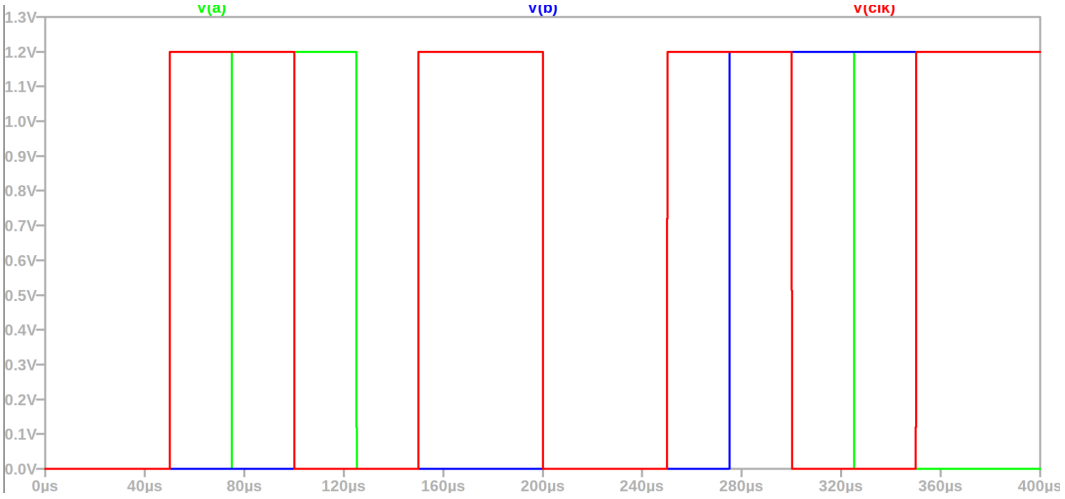


Figure 1: Domino logic inputs

We can see in Figure 1 the only time this circuit should output a high logic signal is when all three signals are high. This only occurs between 270 µs and 300 µs. The basic domino logic gate will not model the capacitance at the NMOS drains for the `A` and `B` nodes. This will not properly model the charge sharing that will be seen in the real circuit.

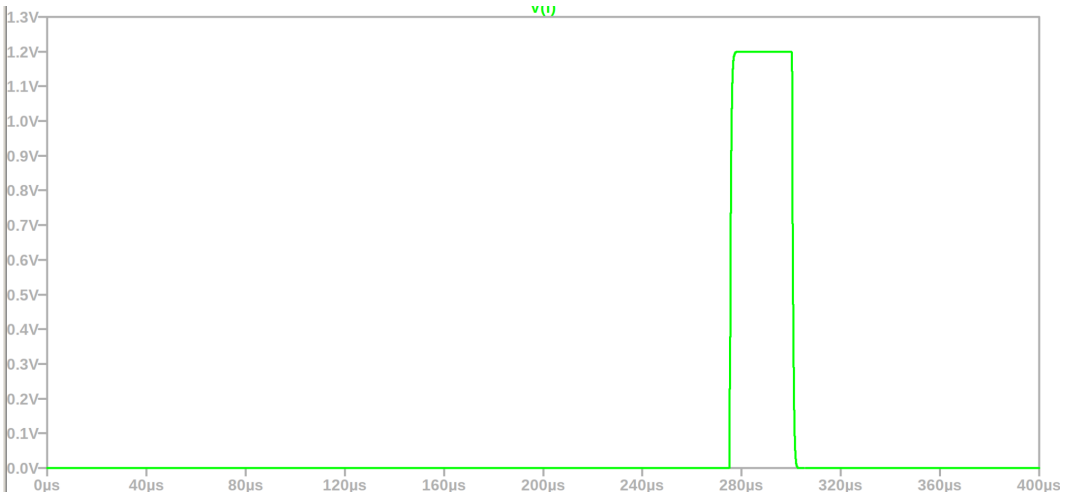


Figure 2: Basic domino logic circuit simulated results

Looking at the results of simulating the basic dynamic logic circuit in Figure 2, we can see the circuit will undergo the expected bevahiour.

## Domino Logic with Charge Sharing

When the capacitance of the NMOS drains is modeled in LT-Spice, we can see that the output logic will not keep the same behaviour.

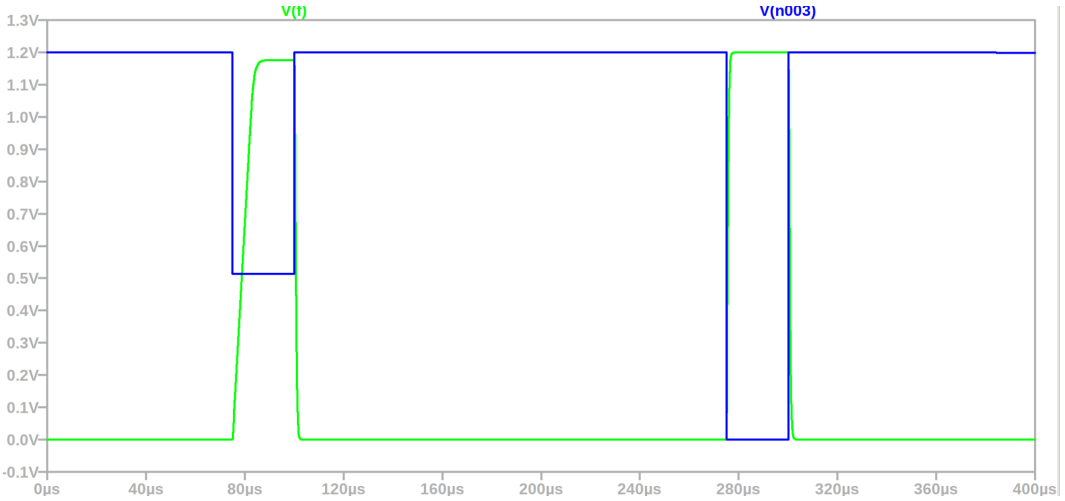


Figure 3: Simulated basic domino logic with charge sharing

We can see in Figure 3 that the voltage at the inverter input will drop when only the `CLK` and `A` nodes are high. This is because the charge stored on the capacitor connected to the inverter input node will split its charge between itself and the capictor on the drain of the `A` NMOS device. The voltage supply is disconnected from this node as the `CLK` signal is high which keeps the pull-up network off.

When the inverter input undergoes charge sharing, its voltage drops to 0.515 V. This matches the calculated value of 0.514 V found during the prelab. When the inverter input node drops below the threshold voltage the output node is sent to high. This is why the output glitch occurs.

## Domino Logic with Keeper PMOS

To solve the issue above, an extra device is added to connect the inverter input to a voltage source when it would otherwise be spliting its capacitance across other nodes. To do this the output of the circuit is connected to a PMOS in the pull-up network. This will connect the inverter input to the voltage supply when output of the circuit is low. In this case the inverter input is high meaning its charge could be split across another node.

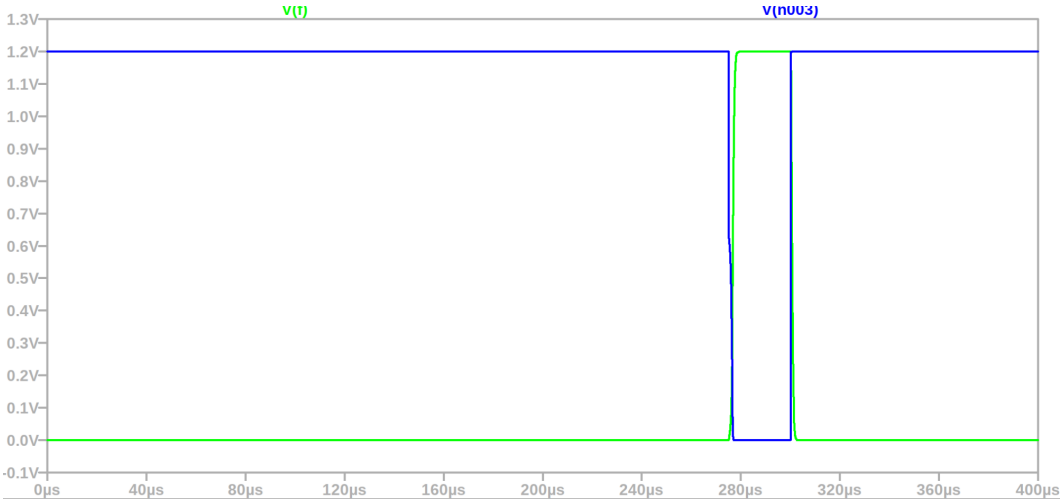


Figure 4: Simulated enhanced domino logic with PMOS keeper

Comparing the simulated results of Figure 4 to those in Figure 3, we can see that the charge sharing glitch is eliminated. The logic output returns to the expected output which is identical to that in the basic domino logic circuit shown in Figure 2. The worst case voltage on the inverter input will never drop below supply voltage of 1.2 V with the PMOS keeper device. Without the keeper, this voltage will drop to 0.515 V.

## Conclusion

This laboratory exercise looked at the bevaviour properties of the dynamic logic circuitry. The logical response of the basic domino circuit implementing the $F = AB$ function showed expected results. When parasitic capacitance was modeled in the input node drains, we saw a glitch when the PMOS network was off and the voltage on the input of the inverter was split across another node in the pull-down network. To solve this glitch, a keeper PMOS was connected in parallel to the pull-up network which connected the inverter input to a voltage supply when the output of the circuit was low.