# EEEE 380 Exercise 3

# CMOS Inverter Design and Dynamic Behavior

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By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

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## Abstract

In this exercise, the behaviour of CMOS inverter under load was investigated. A SPICE simulation was used to find the various properties of the inverter as well as the behaviour of the VTC when different parameters are varied. Finally, a inverter ring oscillator with capacitive loads was used to show the periodic behaviour of the ring oscillator and the effect of varying loads on this period.

## CMOS Inverter (Static)

A simple CMOS inverter was drawn in LTspice to show the inverter response due to varying the input voltage.

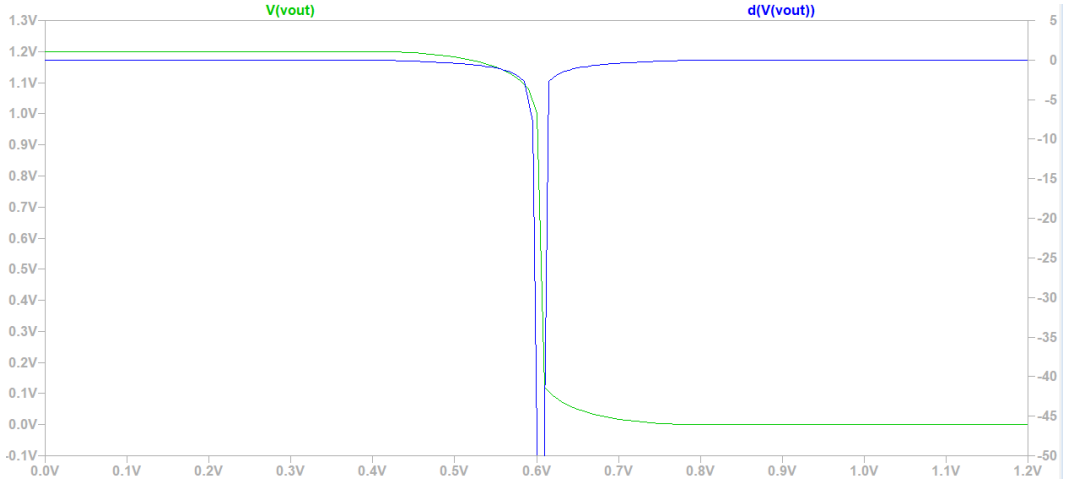


Figure 1: RTC Curve for NMOS/PMOS width of 8 µm

To show how the strength of the pull-up network was affected by an increase in the relative widths between the NMOS and the PMOS, the PMOS transistor was given a width of 16 µm.

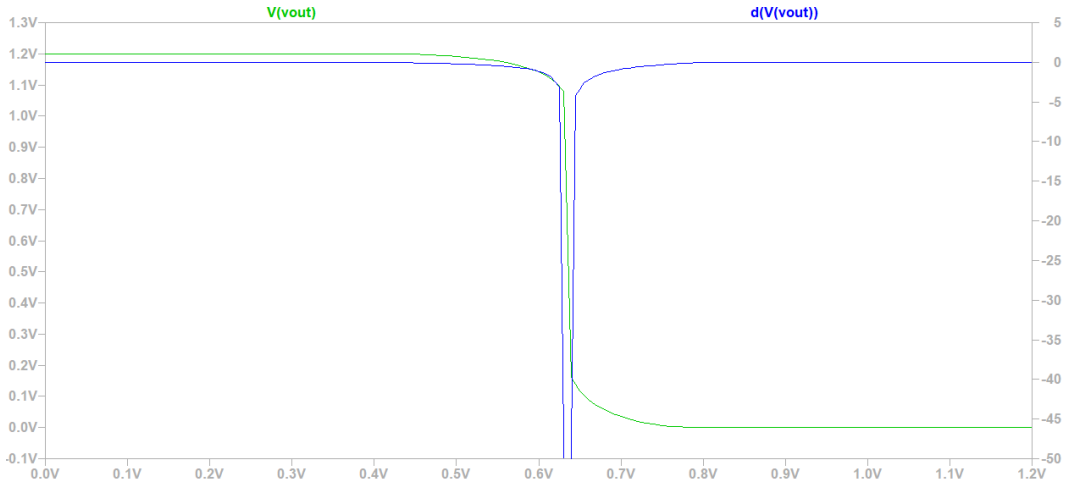


Figure 2: RTC Curve for PMOS width of 16 µm

Table 1: Simulated parameters of CMOS inverters

| $W_p$ (µm) | $V_{OH}$ | $V_{OL}$ | $V_{IH}$ | $V_{IL}$ | $V_{th}$ | NMH | NML |
|---|---|---|---|---|---|---|---|
| 8 | 1.2 | 0 | 0.652 | 0.555 | 0.606 | 0.555 | 0.548 |
| 16 | 1.2 | 0 | 0.691 | 0.597 | 0.636 | 0.597 | 0.509 |

Table 1 shows the various parameters derived from the simulation of both CMOS inverters. The noise margins were also calculated to show the tolerance this device would have inside a larger network.

The results show that when the relative strength of the pull-up network (PMOS) was increased (relative to NMOS), the noise margins on the high end increased while they decreased on the low end. This makes sense as signal output will remain higher for longer if the PMOS strength is increased. Relatively close noise margins were achieved when the $K_r$ ratio was kept at 1 in the $W_p = 8\,\mu m$ case.

Looking back at the prelab calculations, both the $V_{th}$ derived when the $W_p$ value is doubled ($0.634V$) and the $V_{th}$ value at NML = NMH ($0.6V$) agree with the simulated values: $0.636V$ and $0.606V$ respectively.

## CMOS Inveter (Dynamic)

The dynamic behaviour of a CMOS can be interpreted as its VTC curve when the output node is under capacitive load. The rise and fall times are defined as the time it takes $V_{out}$ to rise and fall from $V_{10\%}$ to $V_{90\%}$.

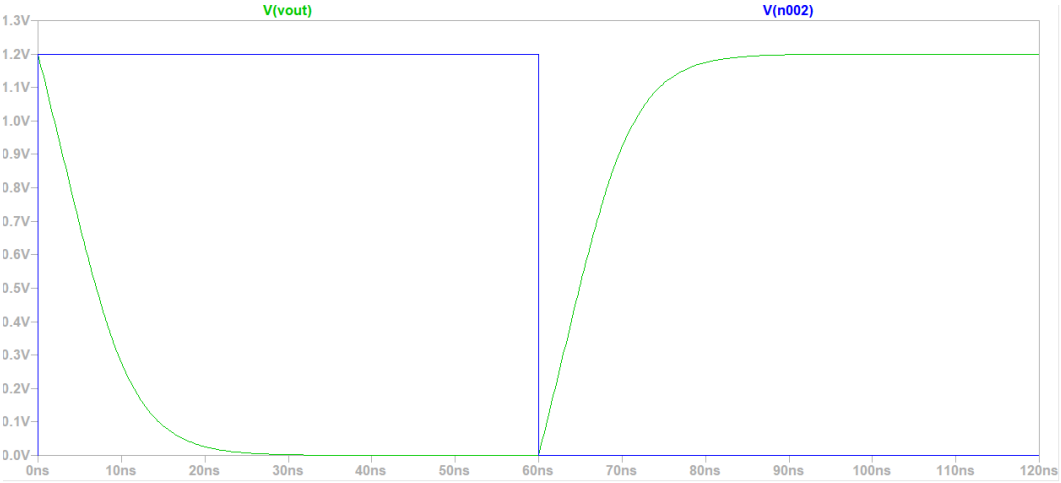


Figure 3: Dynamic behaviour of CMOS with $W_p = 8\,\mu\text{m}$

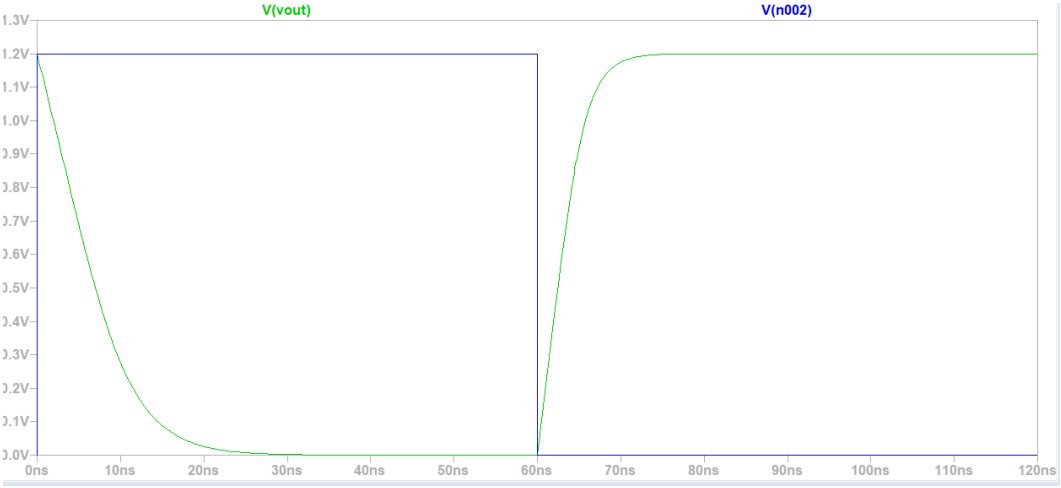


Figure 4: Dynamic behaviour of CMOS with $W_p = 16\,\mu\text{m}$

Figures 3 and 4 show the inputs and output of the CMOS inverter when under a capative load of 25 pF. It can be seen that when the PMOS strength is increased, the rise time of the inverter will decrease because the PUN strength is able to charge the load faster.

Table 2: Rise and Fall times of CMOS inveter under load

| $W_p$ (µm | $t_{fall}$ | $t_{rise}$ |
|---|---|---|
| 8 | 12.45 ns | 12.55 ns |
| 16 | 12.35 ns | 6.17 ns |

Table 2 shows what was previously described. Then the strength of the PMOS was increased, only the rise time was affected by halving it to about 6 ns.

## Ring Oscillator

Ring oscillation is a special circuit that will exhibit an oscillating behaviour. It works by placing a circular chain of an odd number of inverters in series such that the signal on nodes between inverters will oscillate. The oscillation period is based on the load on the circuit which can be simulated with a capacitor between each inverter.

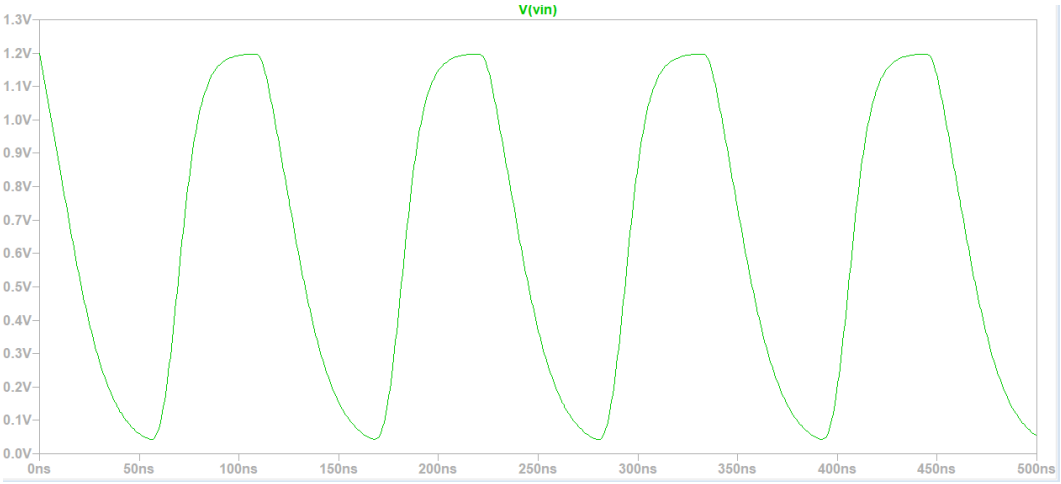


Figure 5: Ring oscillation with only parasitic load

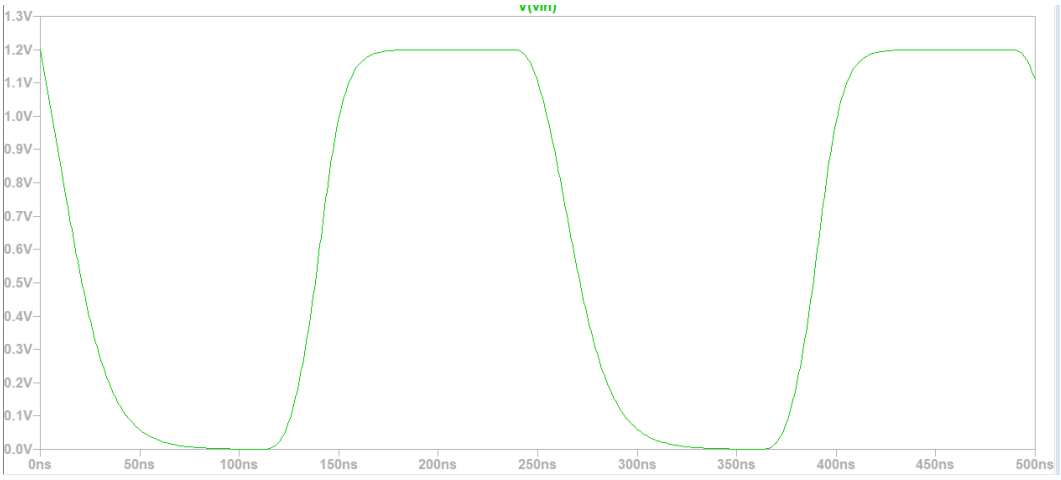


Figure 6: Ring oscillation with parasitic load and circuit load of 50 pF

Figures 5 and 6 show the oscillation periods with and without a 50 pF load on each inverter node. The oscillation period will increase with the load which is expected because it will take longer to charge up a larger capacitor in the loaded case.

Another change that can be made to the ring oscillator is to change $V_{DD}$.

Table 3: Oscillation period when varying $V_{DD}$

| $V_{DD}$ | Period (ns) | Rise/Fall time per inverter |
|---|---|---|
| 1 | 166.95 ns | 16.695 |
| 1.2 | 109.61 ns | 10.961 |
| 2 | 43 ns | 4.3 |

Table 3 shows the effect that varying $V_{DD}$ has on the period of oscillation on the overall ring oscillator. The rise/fall time per inverter is found with the assumption that the rise and fall times are about even and that each inverter is identical. The period can then be divided by $2N$ where $N$ is the number of inverters in the ring. Looking at the results, it makes sense that the period should decrease when increasing $V_{DD}$ because the capacitor is driven with more current from the inverters when the supply voltage is higher.

Equation 1, derived from the prelab, shows the relationship between the load, no load, external capacitance to the load capacitance.

$$C_{Leff} = \frac{t_{noload} \cdot C_{ext}}{t_{load} - t_{noload}} \tag{1}$$

$$C_{Leff} = \frac{109.61\,\text{ns} \cdot 50\,\text{pF}}{240.30\,\text{ns} - 109.61\,\text{ns}} = 41.90\,\text{pF} \tag{2}$$

The experimental value found in Equation 2 is close the to predicated value in the prelab.

## Conclusion

This exercise looked at the static and dynamic behaviour of CMOS inverters. It plotted VTC curves for varying relative powers of the PUN and PDN. The rise and fall times were then experimented with by adding a capative load to the output of the inverter. PUN strength was increased to show the effect this has on the rise time of the inverter. Finally, a ring oscillator was evaluated by running the oscillation with and without a load. The ring oscillator was also changed by varying its supply voltage to show how higher supplies would charge the loads faster. The goals of the this exercise were reached as the circuits were successfully simulated and the prelab calculations were supported by the simulation results.