EEEE 380 Exercise 4

CMOS Combinational Logic

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By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

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Abstract

In this exercise, the behaviour of a three input NAND gate was investigated. A voltage sweep of the three inputs were swept to show the inverter behaviour that can be seen from the NAND gate. All of the inputs of the NAND3 gate were tested to show the proper operation of the NAND gate.

NAND3 Input Sweep

The pull-down network of the NAND3 gate will experience body effect. The three NMOS transistors are placed in series meaning two of the devices will experience body effect. The circuit was simulated with and without body effect at $V_{50\%}$ by setting γ to 0 and 0.2.

Table 1: $V_{50\%}$ with and without body effect.

	V_{out}	X	Y	I
No body	1.70995	0.359252	0.155978	0.0036125
Body	1.85866	0.33856	0.146403	0.00341177

Looking at the results, it makes sense that the voltage drop over the NMOS transistors experiencing body effect is larger than without body effect. This is why the voltage at the X and Y nodes is lower as the top NMOS transistor was the largest voltage drop.

A voltage input sweep of the NAND3 gate was performed to show the effective inverter behaviour of the gate.

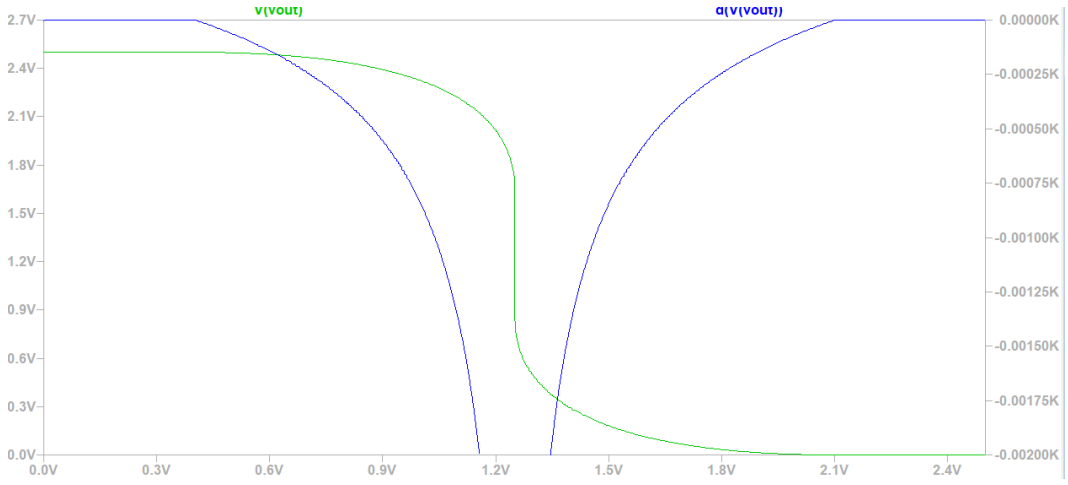

Figure 1: RTC NAND3 input sweep

Figure 1 shows the expected VTC curve that would be seen from an inverter as all of the inputs are hooked together. Because the NAND gate was designed to have equal noise margins

($NMH = NML$), the VTC is semetrical when looking on either side of the V_{th}. This also shows that the power of the pull-up network is equal to the power of the pull-down network.

NAND Functionality

To test the NAND gate, a set of all the input combinations were simulated in PSPICE. The NAND3 gate should output high in all cases expect when all the inputs are high.

Figure 2: NAND3 gate output for all input combinations

The output of the NAND3 gate is as expected. The first input combination is when $A = 1$, $B = 1$, $C = 1$ and the output is low which is expected. All other input combinations are high which is also expected.

Conclusion

This laboratory exercise looked at the logical properties of the NAND3 gate. The response of the NAND3 gate with and without body effect was investigated. Next, an input sweep for all three inputs was performed to show that the noise margins and PUN/PDN strengths were calculated correctly. Finally, the logical behaviour of the gate was tested by running all of the input combinations. The expected behaviour of the NAND3 gate was observed in all of the different tests performed.