ECE352 - Timing measurements for bonus competition

For the bonus competition at the end of the project we will measure the "wall-clock time" that the test programs need to execute, which is

number_of_execution_cycles * minimum_clock_period

For the execution cycles, we are of course using the counter that you implemented in step 2. For the minimum clock period in ns, we are using the results that the *TimeQuest Timing Analyzer* in Quartus II gives you:

1. To "level the playing field", you should all set the fitter effort to high:
   - Go to Assignments->Settings->Fitter Settings
   - Set "Fitter Effort" to "Standard Fit"
   - In our experience, messing with the options under "More Settings..." doesn't lead to better, but possible to worse, results

2. Re-compile your design

3. Open the "Compilation Report" with Ctrl-R

4. Go to *TimeQuest Timing Analyzer->Slow Model->Setup Summary* and note down "Slack" for the signal KEY[1], which is your clock signal.

5. The slack shows you how much slower the circuit is than the default delay, which is 1ns. Therefore, your minimum clock period in ns is the Slow Model slack + 1ns.

P.S.: Alternatively, you can also see the slack value in the info message window as "Worst-case setup slack" right after the "Info: Analyzing Slow Model" message (don't confuse it with the one after the "Info: Analyzing Fast Model" message, which will look much better).

P.S. 2: Why the slow model? It is the worst-case performance for the worst chip produced and sold, at the lowest allowed supply voltage and the highest allowed operating temperature.