

# Rapport lab 2-3

TSEA44

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## 1 Labb 2

### 1.1 Introduktion

Introduction

### 1.2 Tillståndsgraf och arkitektur

Design, where you explain with text and diagrams how your design works

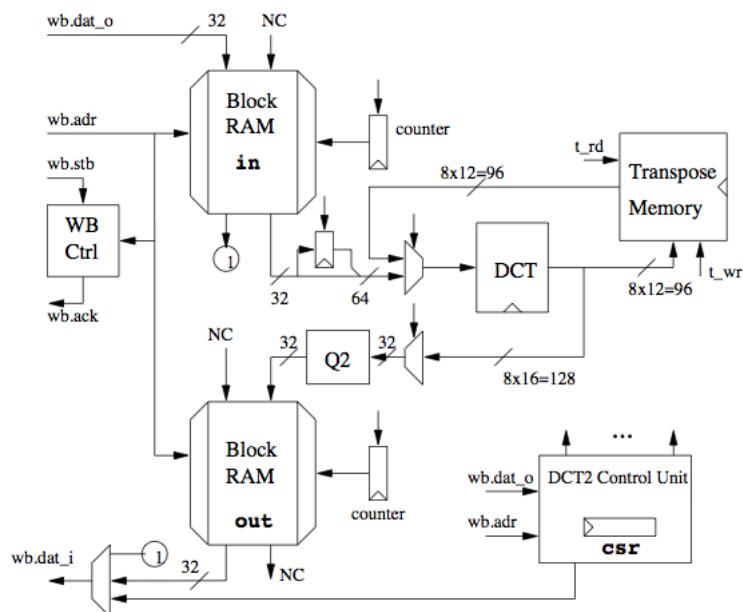
### 1.3 Resultat

Results, that you have measured

### 1.4 Sammanfattning

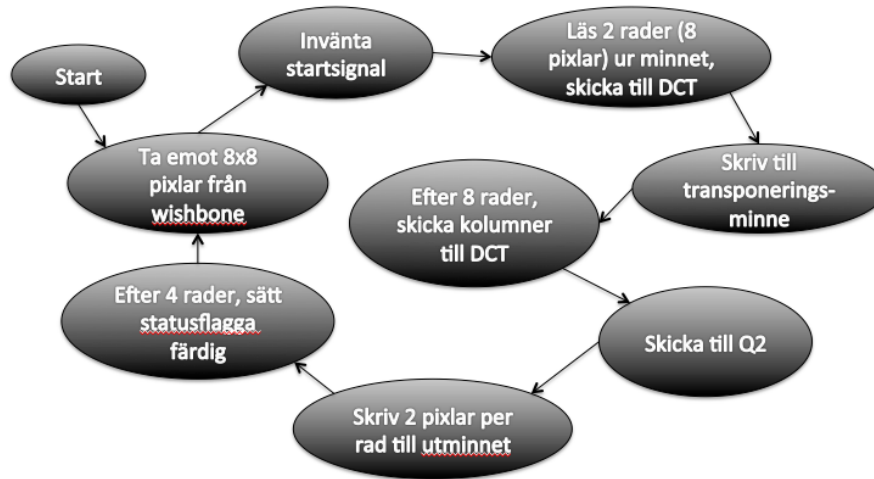
Conclusions

Vi följde labbanvisningen och hade ett blockminne med indatan där vi i labb 2 tog data och adress till inminnet direkt från wishbone bussen. Vi tar emot data så fort vi blir adresserade och inväntar en startsignal, när den kommer startar vi en räknare och sätter igång diverse statusflaggor. Räknaren är för att hålla koll på hur många pixlar vi har läst in till DCT 'n. Figur 1 visar vad som händer



Figur 1: Arkitektur för vår design

hej



Figur 2: Tillståndsgraf för vår design

## 1.5 Filer

## 2 Labb 3

### 2.1 Introduktion

Introduction

### 2.2 Design

Design, where you explain with text and diagrams how your design works

### 2.3 Resultat

Results, that you have measured

### 2.4 Sammanfattning

## 3 What to Include in the Lab Report 2

The lab report should contain all source code that you have written. (The source code should of course be commented.) We would also like you to include a block diagram of your hardware. If you have written any FSM you should include a state diagram graph of the FSM. We would also like you to discuss the following questions in detail somewhere in your lab report.

- How does your 2D DCT hardware work?
- How did you verify that your 2D DCT hardware works correctly?

- What is the performance with and without the 2D DCT hardware? This should include measurements of both the 2D DCT kernel and the entire application.
- A timestamp diagram.
- How much of the FPGA is used by the 2D DCT hardware?
- How much is the 2D DCT hardware used while encoding an image in jpegtest?
- Is the size of the 2D DCT hardware justified by the performance improvements?
- What would be required in order to implement more functionality like zigzag addressing in the 2D DCT hardware module? Would it be difficult to modify jpegfiles to take advantage of such optimizations? And of course, the normal parts of a lab report such as a table of contents, an introduction, a conclusion, etc. The source code that you have written should be included in appendices and referred to from the main document.

## 4 What to Include in the Lab Report 3

The lab report should contain all source code that you have written. (The source code should of course be commented.) We would also like you to include a block diagram of your hardware. If you have written any FSM you should include a state diagram graph of the FSM. We would also like you to discuss the following questions in detail somewhere in your lab report1:

- How does your hardware work?
- How did you verify that your hardware worked?
- How did you modify the software?
- A timing diagram.
- What is the utilization of your accelerator?
- What is the performance of jpegtest with DMA enabled?
- How long does it take (on average) to read a macroblock into the DCT accelerator via DMA?
- How much is the wishbone bus used by the DMA unit and how much is the bus used by the CPU? And of course, the normal parts of a lab report such as a table of contents, an introduction, a conclusion, etc. The source code that you have written should be included in appendices and referred to from the main document.

stakeholders	change1	change2	change3
stakeholder1	+ / -	+ / -	+ / -
stakeholder2	+ / -	+ / -	+ / -
stakeholder3	+ / -	+ / -	+ / -

Tabell 1: Shows how the different stakeholders are affected by each change.

change1	description	description
change2	description	description
change3	description	description

Tabell 2: Describes the changes and why they effect the stakeholders.

## Appendices

**A** kod.sv

**B** kod.sv

**C** kod.sv