CPU Pipeline

Instruction Fetch Module

+4
Jump
0
ALUOut
1
clk
D Q PC
En
IF_Stall

IC_RDATA
clk
D Q IR
En
IF_Stall

IC_ERROR
PC
!IF_Stall
IC_RDATA
ICDOK

RRESP
RADDR
RAVALID
RDATA
RDATAV

Instruction Cache Memory

Instruction Decode Module

op
func
Instruction Operand Selector

IR → Instruction Decoder → rs, rt, rd, op, func, ct'

R1
R2
PC
ct'
4 In 2 Out Mux

Register set
D Q A
D Q B
R1 → D Q A'
R2 → D Q B'
op ## func → D Q InstructionTo Execute
clk
En
ID_Stall

Execution Module

InstructionToExecute
Value is 0 when result is not yet computed

A → ALU → ALUNotReady
B
FPU

Register set
B → D Q ALUOut
D Q SMDR
A' → InstructionTo Execute → D Q InstructionExecuted
B' → ALU' → D Q cond
clk
En
EXE_Stall

Contains the few operations to calculate the result of a branch

Write Back Module (GPBR)

Indicates if the @ registers reffers to the GPR or FPR
WriteBackOpcode   DecodeOpcode

Means that the new instruction to execute is not ready inside the GPBR

rs   rt

rd
opcode
clk
Instruction Pending FIFO
En   R
WB_Stall   R_FIFO_WB

SrcNotReady
WriteBackOpcode
rd'

rs → @s → R1
rt → @t → T
rd → @d → D
x32 GPR(32b)
x32 FPR(32b)
GPBR
NewValue → D
rd' → W@
clk
En
WB_Stall & WBI

0
T
1
D
R2
opcode == Load or opcode == Store

Memory Module

InstructionExecuted → Is Load → Load

ALUOut → 0
RDATA → 1
clk
D Q NewValue
En
MEM_Stall

MEM_Stall & Store → WAVALID, WDATAV

MEM_Stall & Load → RAVALID

cond → Is Jump → Jump
InstructionExecuted → Is Store → Store

ALUOut → D Q RADDR
clk
En
MEM_Stall & Load

ALUOut → D Q WADDR
SMDR → D Q WDATA
clk
En
MEM_Stall & Store

Hazard Control System

Reset
Jump
SrcNotReady
ICDOK
ALUNotReady
Write
WRESPV
Read
RDATAV

Hazard Control System

IF_Stall
ID_Stall
EXE_Stall
MEM_Stall
WB_Stall
R_FIFO_WB

System Bus