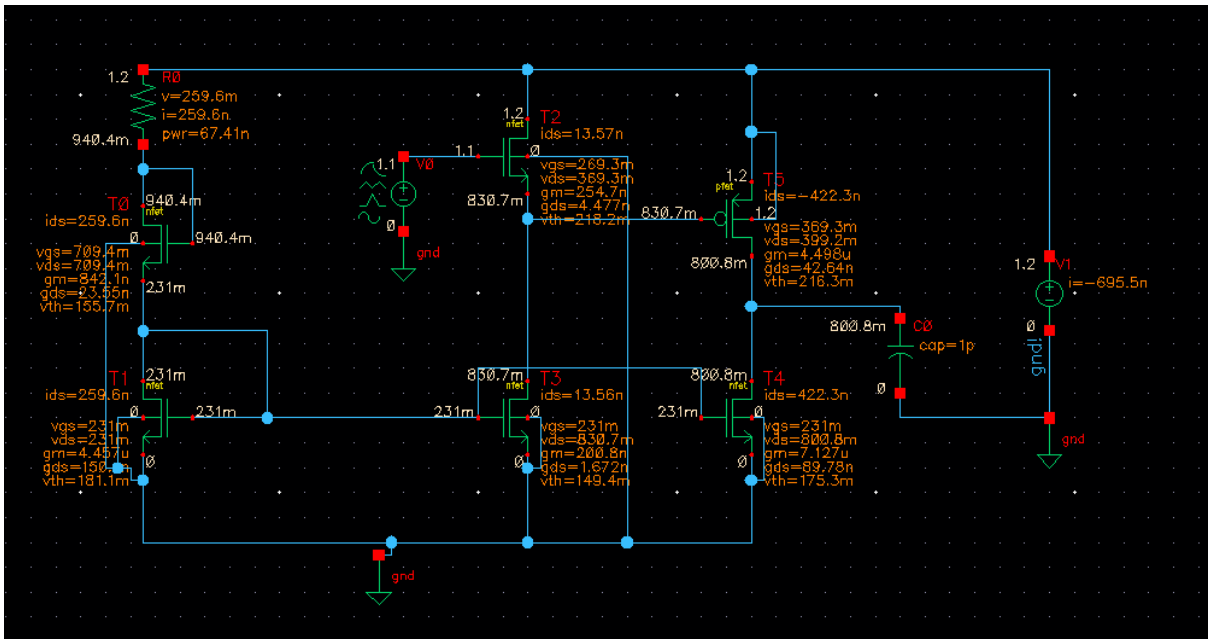
Exercise 1 – Integrated Analog Circuits

Overview of this work:

	$W[\mu m]$	$L\ [\mu m]$	$V_{GS}\ [mV]$	$V_{DS}[mV]$	$g_m[n\Omega^{-1}]$	$g_{ds}[n\Omega^{-1}]$	$V_{ov}[mV]$	$Resistance\ [\Omega]$	$Voltage$
M1	0.4	45	269	369	254.7	4.477	53	N/A	N/A
M2	0.5	118	231	830.7	200.8	1.672	81.6	N/A	N/A
M3	3.8	8.3	369.3	399.2	4.498	42.64	153	N/A	N/A
M4	1.9	11	231	800.8	7.127	89.78	55.7	N/A	N/A
M5	1	7	231	231	4.457	150	49.9	N/A	N/A
M6	0.2	65	709.4	709.4	842	23	685	N/A	N/A
R1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	$1\ M$	N/A
VDC	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1.1

$Parameter$	$DC\ Gain$	$3-dB\ BW$	$Power$
$Achieved$	$29.75\ dB$	$20.12\ kHz$	$834\ nW$



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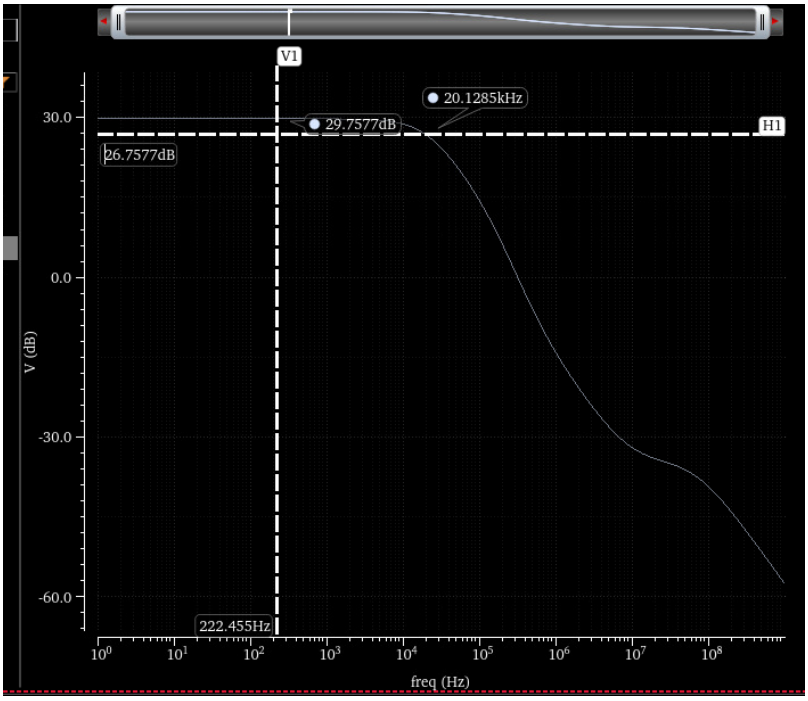
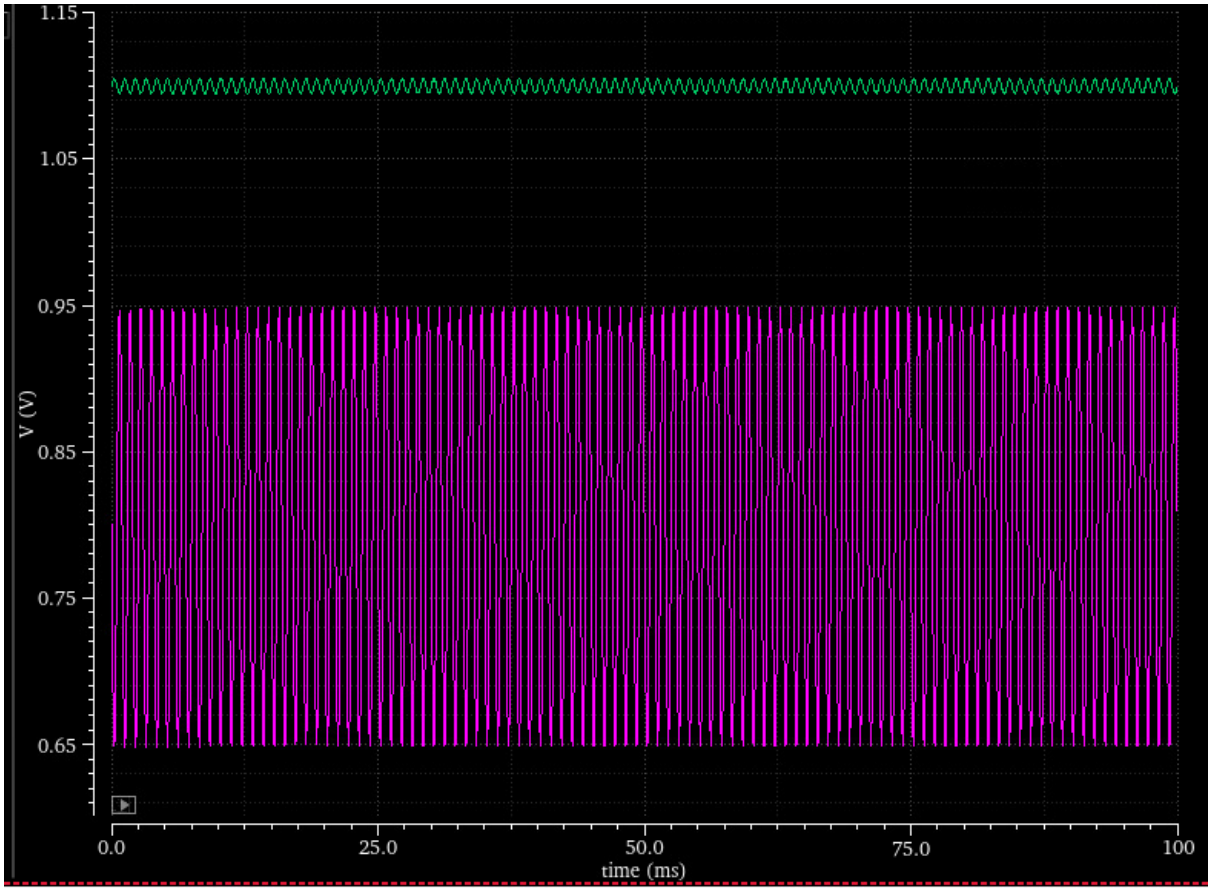


Sin IN sin Out



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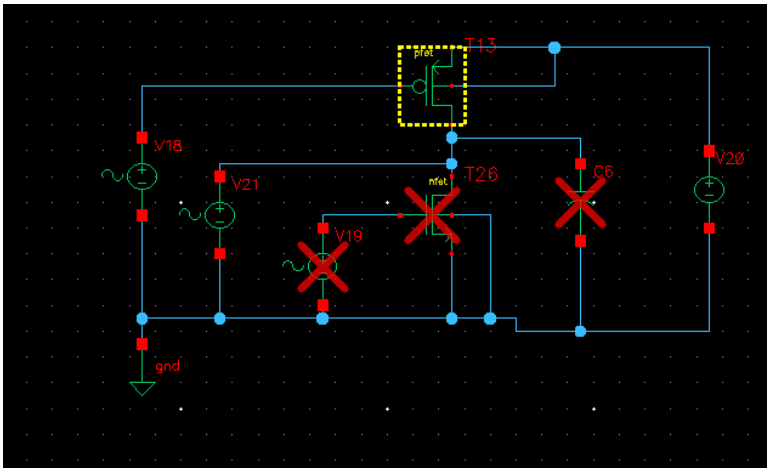
In order to set the gain of the output stage M3 M4 we need to account for the total output resistance seen at the drain of the transistors, i.e. $r_{o3}||r_{o4}$. This transistor depends on the operating point of the circuit and therefore we suggest a iterative "trial and error" approach:

1- Trivially set the output voltage to some point $V_{DC,out}$.
   a- Disconnect M4 and find a gain point on the $A_V\ vs\ OP$ line. This gain should be higher than the target gain to account for reduction in the output resistance.
   b- Connect M4 and find an OP such that the output voltage reads $V_{DC,out}$.
   c- Check the overall gain.
      - If the gain is higher than target, return to point a with lower A_v.
      - If the gain is lower than target, return to point a with higher A_v.
      - If the gain is different than target, and the gain is close than another already checked gain, return to point 1 with another $V_{DC,out}$.

This procedure is bruteforce. It differs from the recitation in that we need to account for the transistors output resistances to get a precise gain. However, we will use the logic from the recitation and will try to solve for $V_{DC,out} = \frac{V_{DD}}{2}$.

The problem we are trying to solve is multidimensional in the ammount of OP's that can be found. To make the problem even simpler, we set a high $L_p = 8\mu m$. The reasoning for this is that it makes the transistor small, and therefore, for low V_{ov} we would have both high gain and low power. We expect that the low GBW needed will be also met, and will correct accordingly. The baseline transistor width is taken to $W_p = 4\mu m$. This will be tunned to change the GBW accordingly. Its taken realtively high, to be able to tune it down or up.

To find the $A_v\ vs\ OP$ curve, we need to iterate the PMOS alone with various $V_{Gp} = [0.1: 0.01: 0.9]$. For each we calculate the gain and plot the results.



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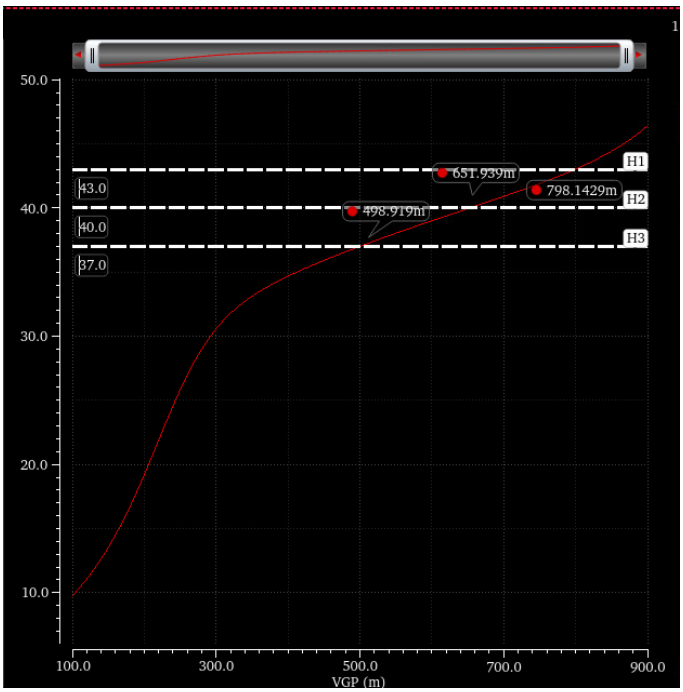
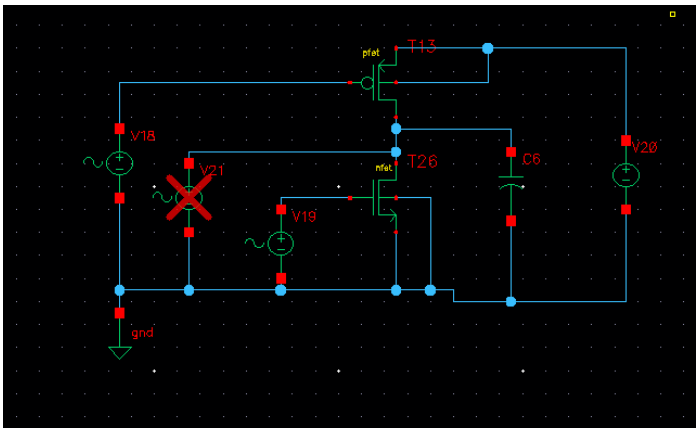


We'll start from the 40 dB ($V_{GP} = 650mV$). Choosing this means that we are hoping that after setting the DC point of the NMOS the output resistance reads $r_N||r_P = \frac{r_P}{10}$.

To check this we use $V_{GP} = 650\ mV$ and find the gate voltage needed in the NMOS to drive the drain towards 0.6V.

The simulated circuit follows:



The initial values for the NMOS were taken as $L_N = 7\mu$ and $W_N = 2\mu$. This values are randomlly chosen (there is no expectation that a size difference of ~ 2 will give a difference of ~ 10 in output resistance, however it was our experience (not documented here), that aiming for a ~ 2 output resistance ratio did not sped up the process.

The V_{GN} reads 351mV. At this voltage the AC gain reads 24 dB, meaning that the nmos resistance was smaller than expected.

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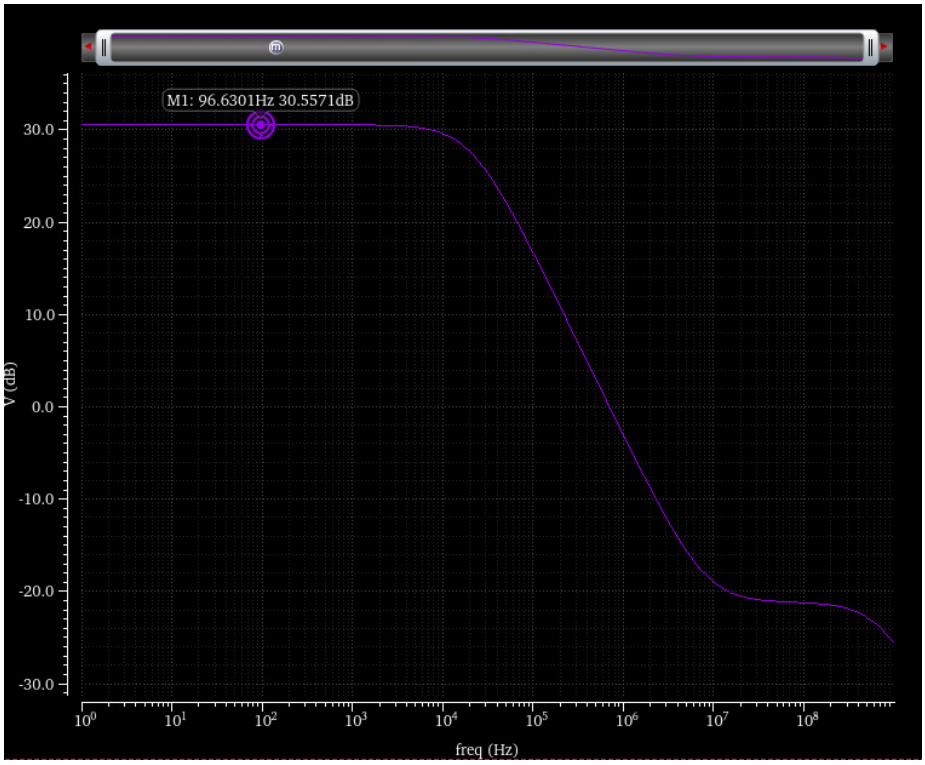
We can try again with 43dB, which means $V_{GP} = 800mV$. In this case, the nmos voltage needed to achieve $0.6V$ at the drain reads 241 mV. And now the ac gain reads 28 dB.

We next use 45 dB which is set at 866mV in the PMOS, the NMOS at this point needs to be at 200mV. The AC gain at this point is 31.76 dB.
We repeat one last time with $V_{GP} = 0.83V$. The target NMOS gate votlage is 223mV. The AC gain in this case reads 29.73 dB.

Although 29.73 dB is close to target, the problem here is that 223mV gate voltage leads to a VGS in the NMOS that's smaller than 50mV but instead reads 42mV. This means that the transistor is still in the "transistion zone" between subthreshold and strong inversion. We increased the gate votlage to $V_g = 231mV$ and compensated with a longer length of $L_n = 11.5\mu$.

At last, we increased the gain slightly by increasing the $L_P = 9\mu m$. The result is given in the next figure:



This looks great! The small deviation from target gain can be seen as a tollerance to accommodate for the previous stage loss.

<u>Second Stage:</u>

We start from the biasing point of M1. We hypothesize that if g_m is high enough, the overall gain will be 1. Therefore, the transistor sizing is set so that when its source is at 0.83V (M3 DC votlage), the transistor is saturate and conducts a small current.

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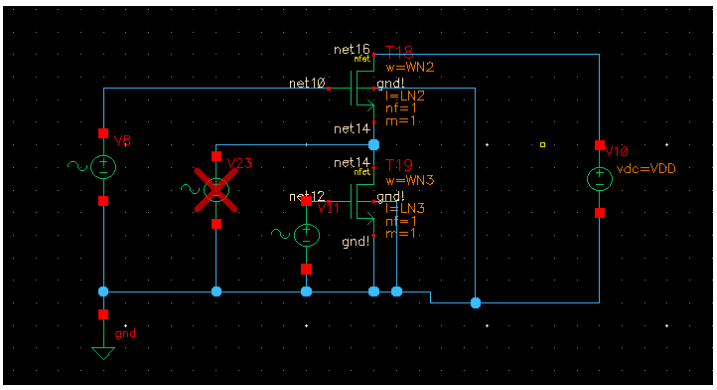
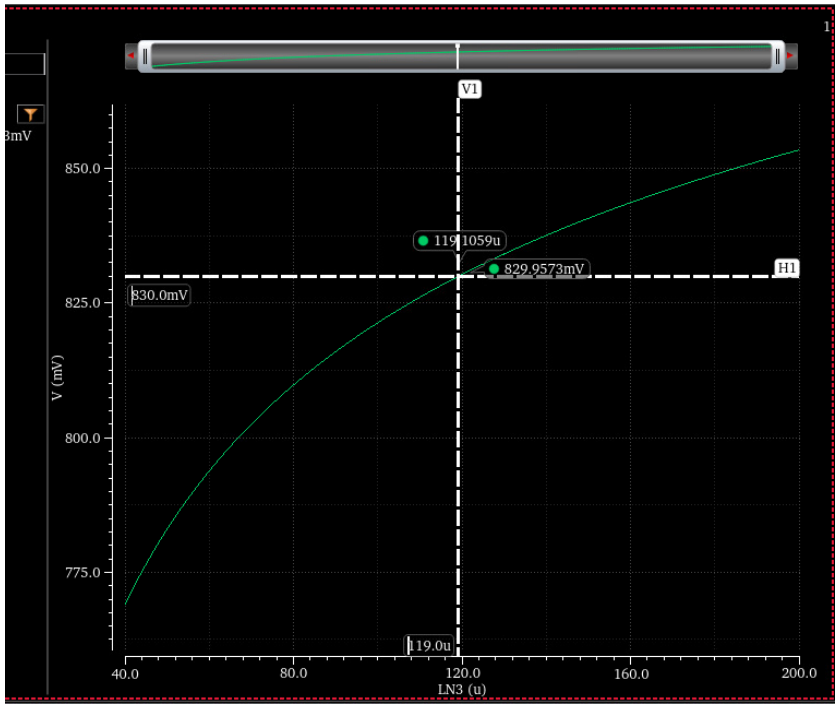
There is a clear tradeoff between the transistor size and the current passing through the transistor, as for low current we will aim for high L (there is a lower limit on the ammount of W). For example, an extremelly low current solution was found with $W_{N1} = 0.5\mu m$ and $L_{N1} = 55\mu m$. This is clearly a **huge** transitor, but there was no instruction to save on sillicon.

Then, M2 is set so that the voltage on its drain is 0.83V. Simulation resuts gave $W_{M2} = 0.5\mu m$ and $L_{M2} = 119\ \mu m$.
The circuit for the simulation and the simulation results are presented next:





The exact value for 830mV is $L = 119.1\mu m$ and therefore we chose $119\mu m$.

The AC response of the stage is shown next:

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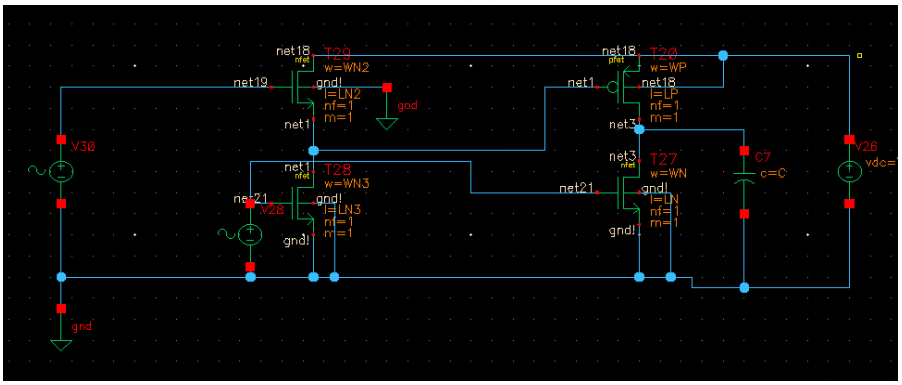
The response is a little on the lower end of the tollerance achieved for the previous stage, but this will be fine tunned next.

Connection of the two stages (no biasing stage yet)

The two stages are simulated as follows:



The AC response of the circuit is shown next:

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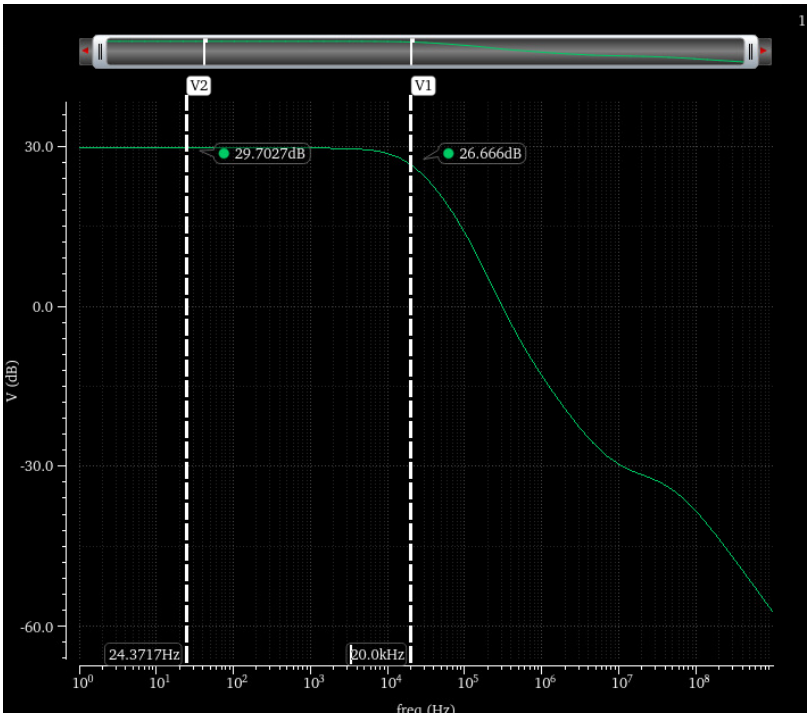
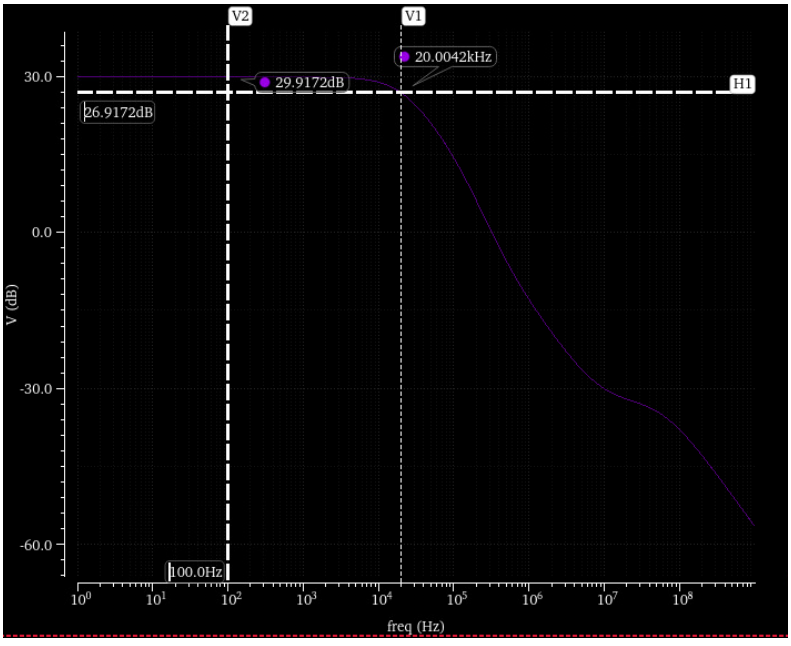


It can be shown a close response as expected. There is some fine tunning needed to softly rise the gain.
After some trian and error, we changed the following parameters:
$L_{M3} = 8.5\mu m, L_{M2} = 118\mu m, L_{M1} = 50\mu$.



It can be clearly seen that the gain is within 0.1dB of 30 dB and that the 3dB point is within 100 Hz of 20kHz.

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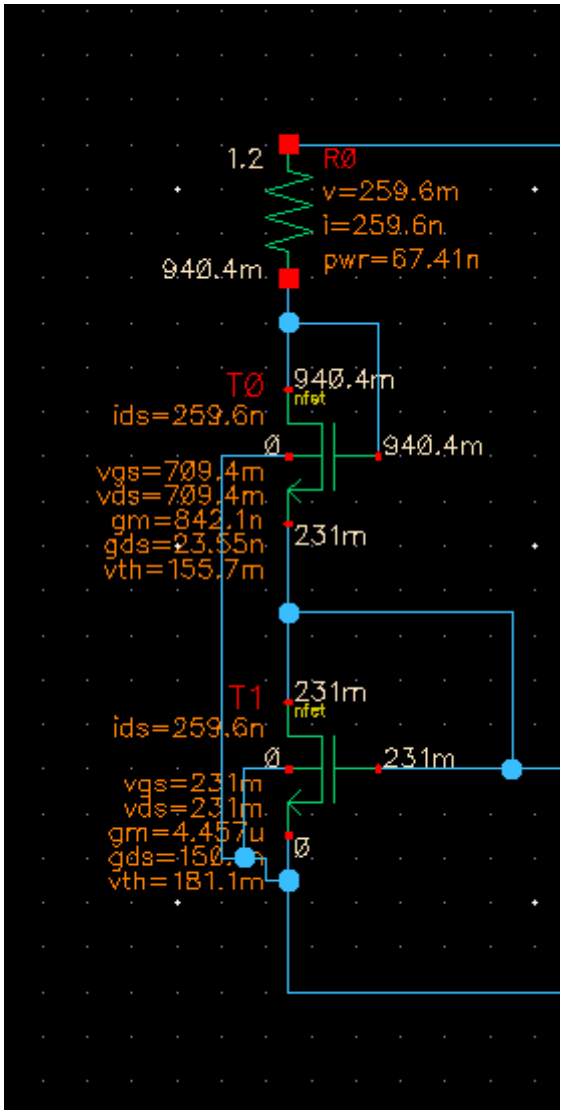
Biasing Branch:

The biasing branch was found by some trial and error, until we got $V_G = 231mV$.



The values founded were (using exercise notation):

$$W_{M5} = 1\mu m$$

$$L_{M5} = 7\mu m$$

$$W_{M6} = 200nm$$

$$L_{M6} = 65\mu m$$

$$R = 1\ M\Omega$$

After simulating the whole system we got a small error in the overall gain. Moreover, we observed that M1's overdrive voltage was reduced.
To adress these changes we manually tunned the circuit to give:

$$L_{M1} = 45\ \mu m$$

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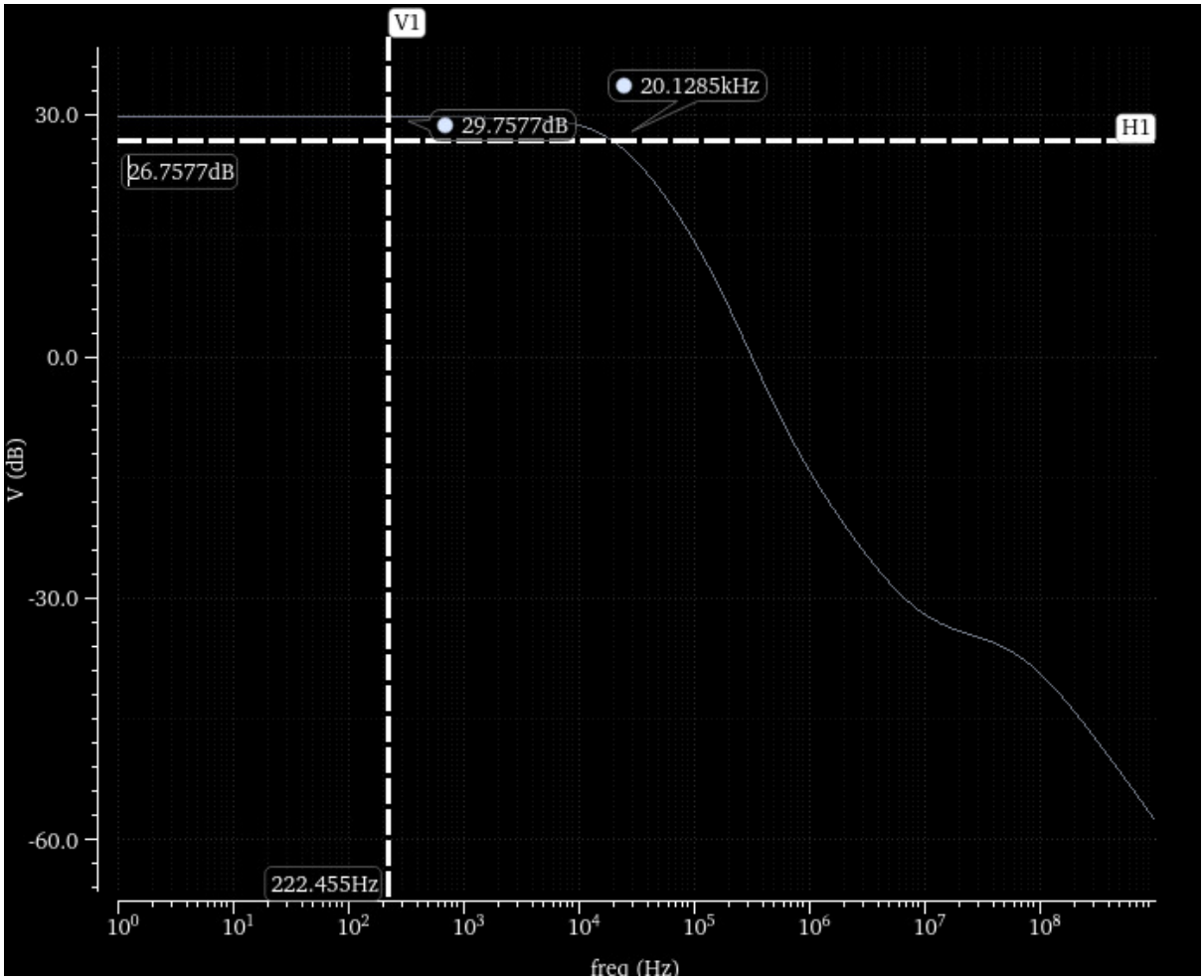
$$W_{M3} = 3.8\ \mu m$$

$$W_{M4} = 1.9\ \mu m$$

$$L_N = 11\ \mu m$$

The final AC response is given bellow



The total DC points and power consumption are shown bellow:

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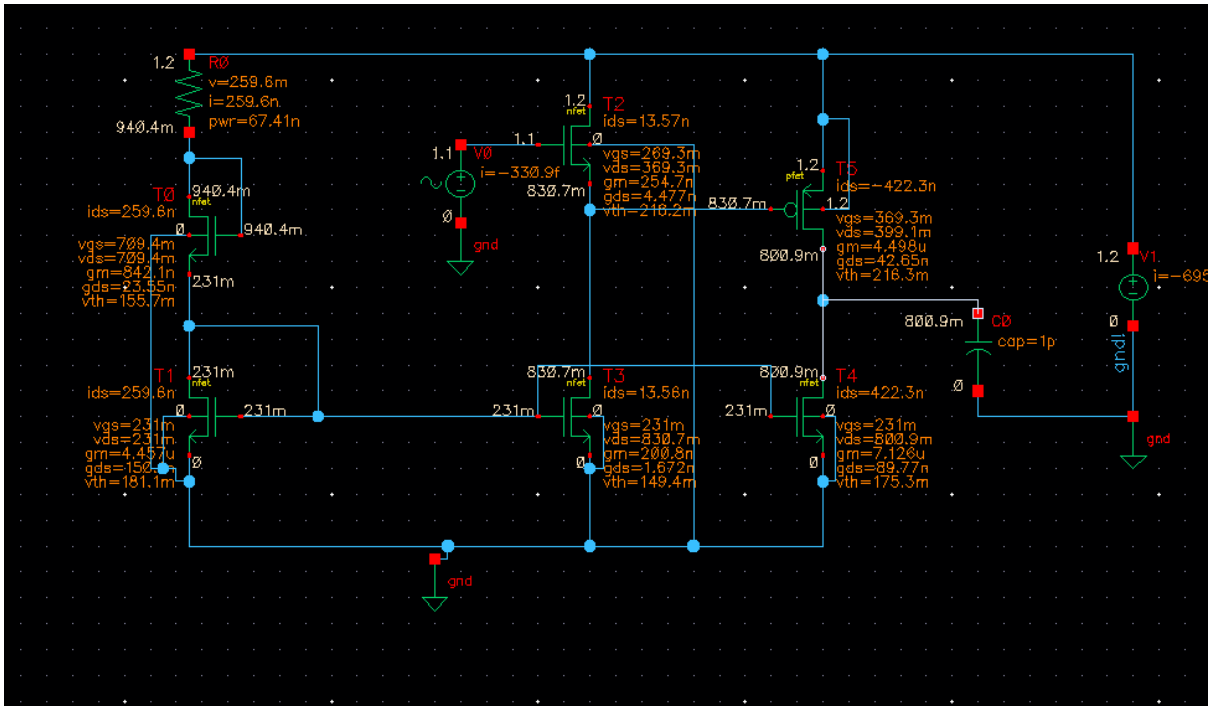

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