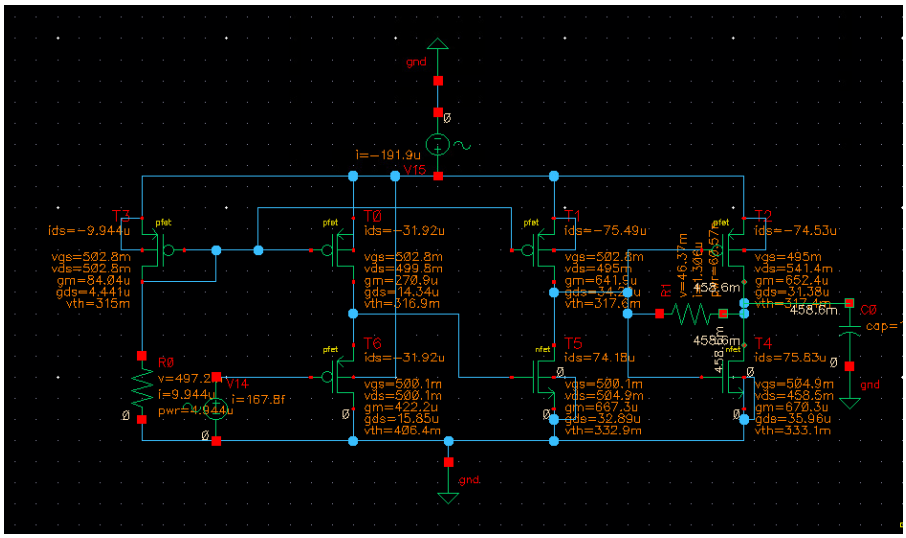
EX2 – Wide band linear driver

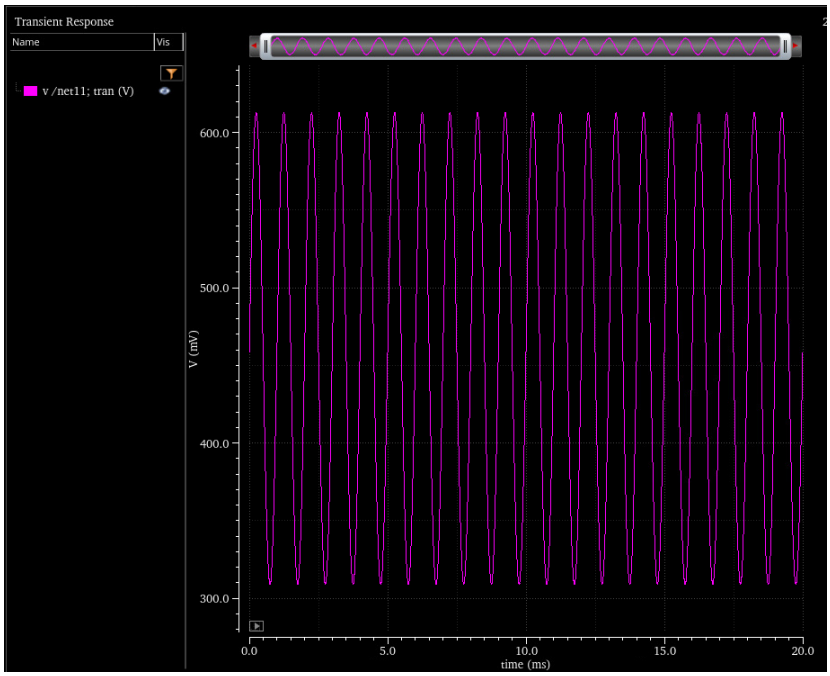
Benjamin Rein – 211864194

Martin Raskin – 342388832

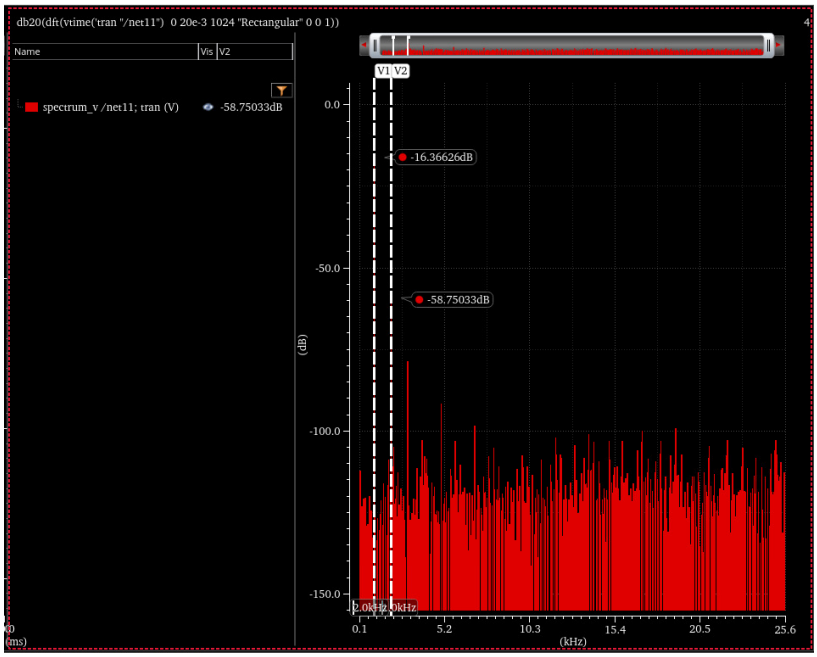
The final circuit with its DC operating points is:




The transient wave:




The spectra:




We have omitted the DC.

Summarizing OP table:

| | Total Width (um) | Length (um) | $V_{gs}$ (V) | $V_{ds}$ (V) | $V_{gs} - V_{TH}$ (mV) | $g_m$ ($\mu\Omega^{-1}$) | $g_{ds}$ ($\mu\Omega^{-1}$) | Resistance ($\Omega$) |
|---|---|---|---|---|---|---|---|---|
| M1 | 2.2 | 0.2 | 0.5 | 0.54 | 178 | 670 | 36 | |
| M2 | 9.2 | 0.2 | 0.495 | 0.458 | 171 | 652 | 31 | |
| M3 | 2.2 | 0.2 | 0.5 | 0.495 | 185 | 664 | 33 | |
| M4 | 8.9 | 0.2 | 0.5 | 0.504 | 368 | 642 | 34 | |
| M5 | 10.5 | 0.2 | 0.5 | 0.499 | 186 | 422 | 16 | |
| M6 | 3.9 | 0.2 | 0.5 | 0.5 | 94 | 271 | 14 | |
| M7 | 1.3 | 0.2 | 0.5 | 0.5 | 187 | 84 | 4.4 | |
| R1 | | | | | | | | 50e3 |
| RF | | | | | | | | 35.5e3 |

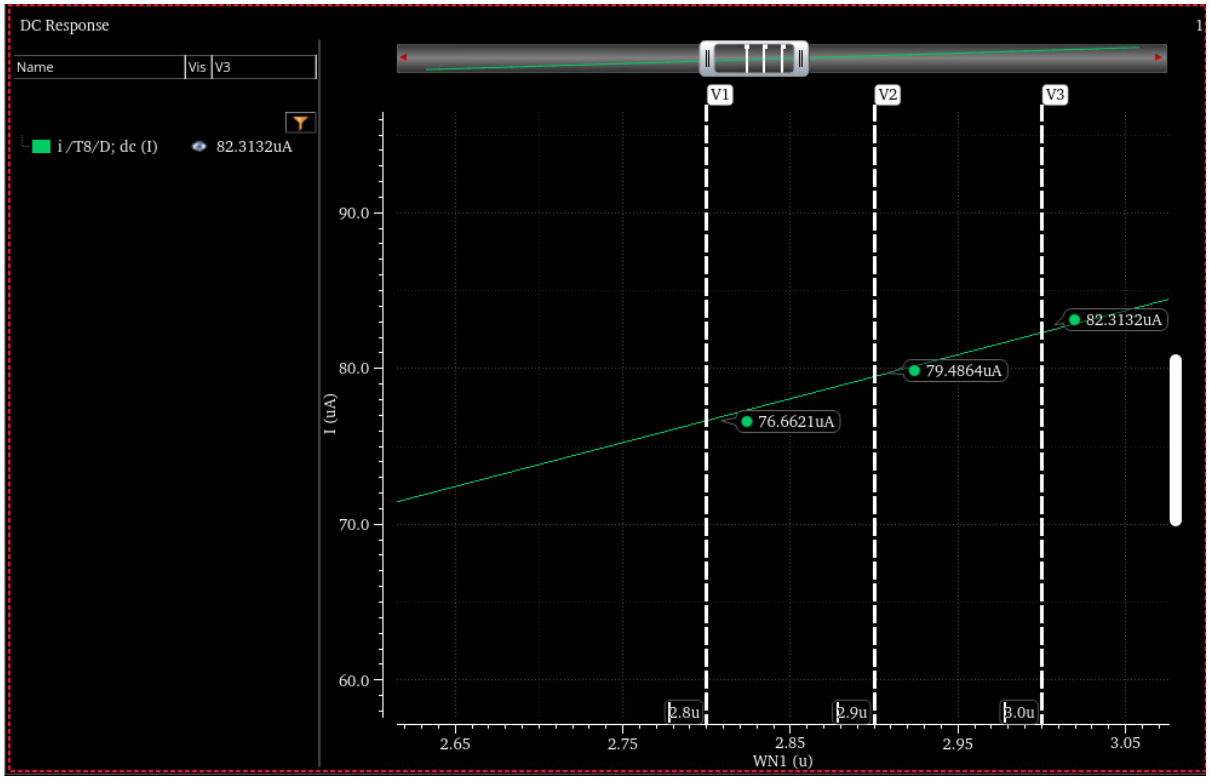
Desing specification table:

| | DC Gain | 3-db BW | Power consumption |
|---|---|---|---|
| Value | $23.6dB$ | $887\ MHz$ | $192\ \mu W$ |

We will assume that $R_F$ is big enough to not change much the output resistance of the transistors.
We will aim for a low $r_{on}$ on both M1 and M2, this means high current. However, high current means big W and therefore an increase in capacitance.

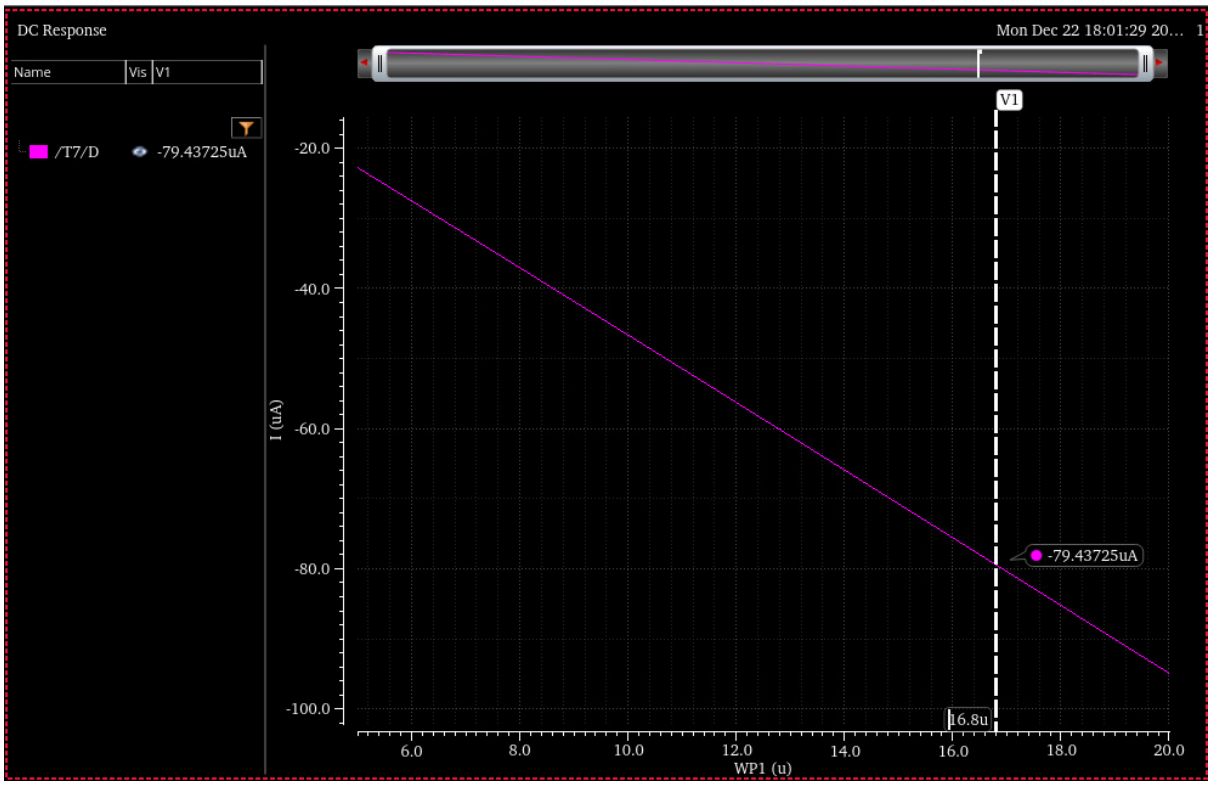
We could aim for example for 80muA the stage. Assuming that the parasitic capacitance of the transistor is small enough, we can assume that changing the transistor size, and therefore the current will increase the GBW.

We will start from $LN1 = LP1 = 500\ nm$



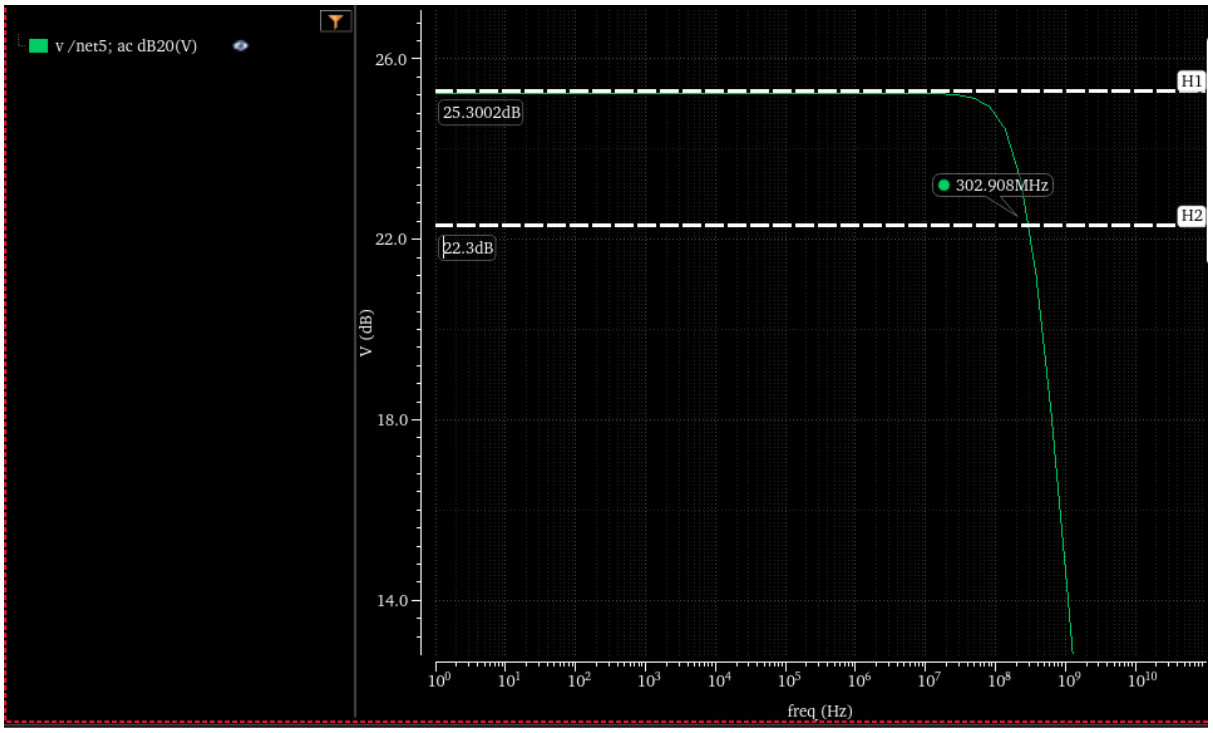

We choose $WN1 = 2.9\mu m$.

We repeat for the PMOS:



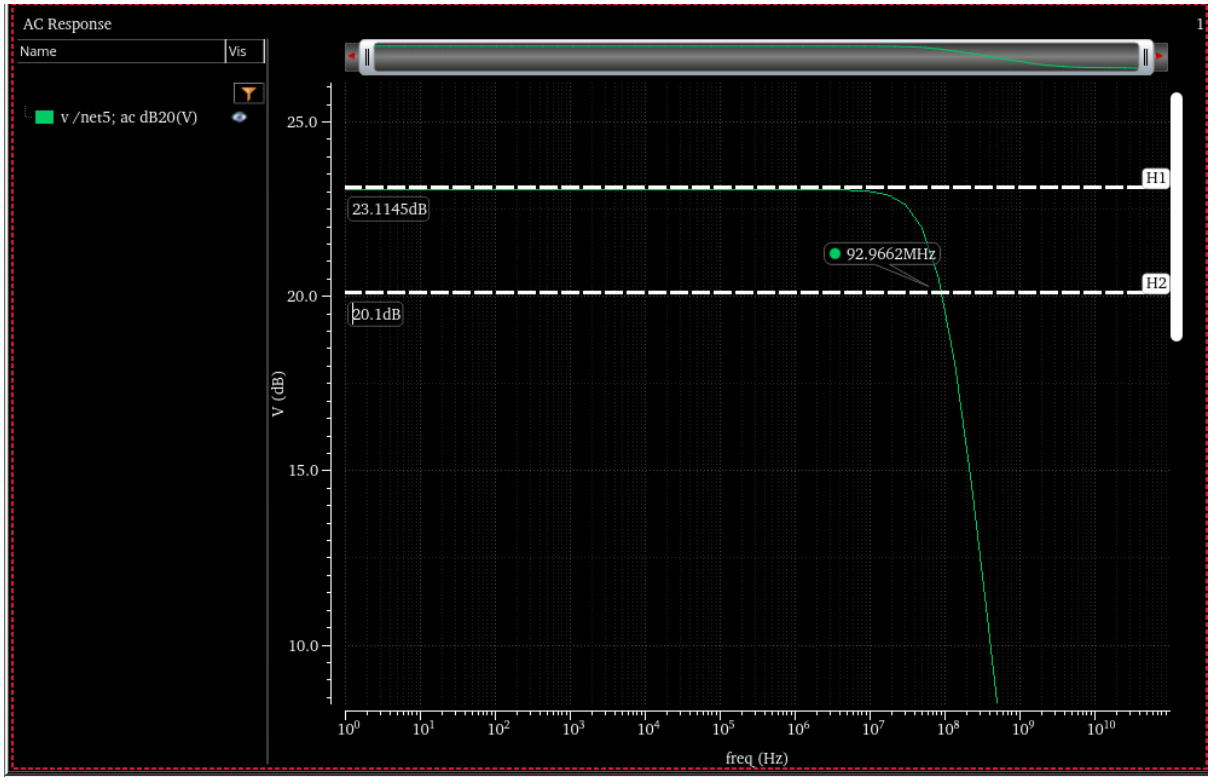

We choose 16.8 $\mu m$ as a starting point.

We show next the AC response:



The main problem with this block is the high transistors used. The DC point reads $C_{GG} \cong 50fF$ for each transistor which means that that the parasitic capacitance at the gate of M1-M2 will be the dominant capacitor. To make things simpler, we will lower the current consumption of the block.
We can aim for example at a gain of 10 dB on the output stage. We start by dividing the transistor by an equal factor (and some fine tunning).

For a reduction of 10 in the widths:



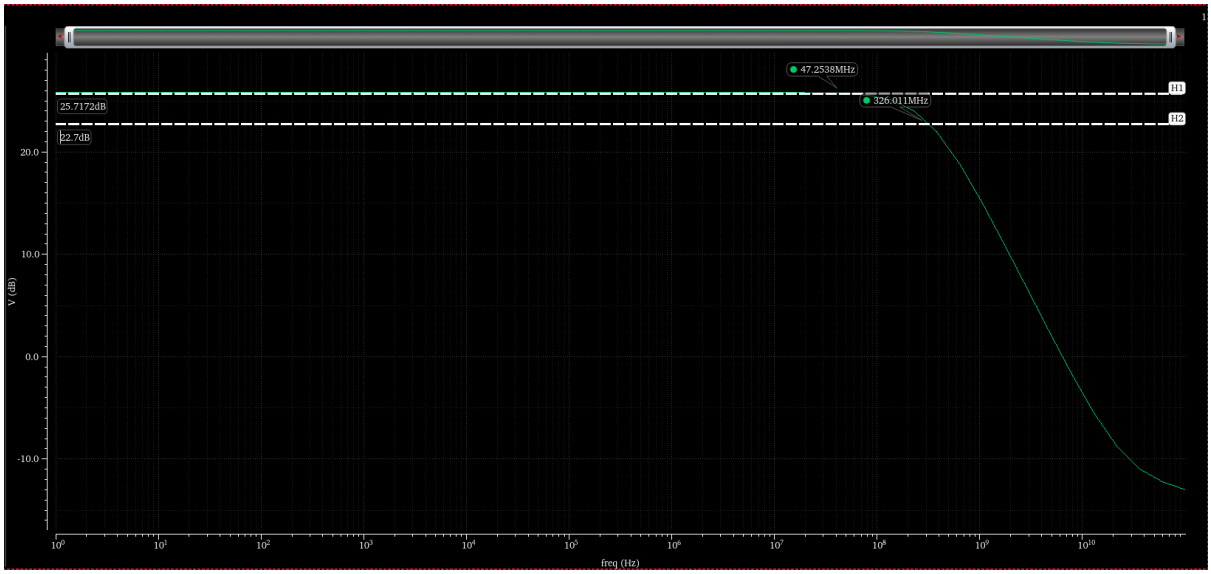

A BW of 1GHz will mean 20 dB less gain, therefore we need more gain.

We will try for a reduction of 2.5 (instead of 10) with some fine tunning to reach VDC = 0.5V:

$$LN1 = LP1 = 200nm$$

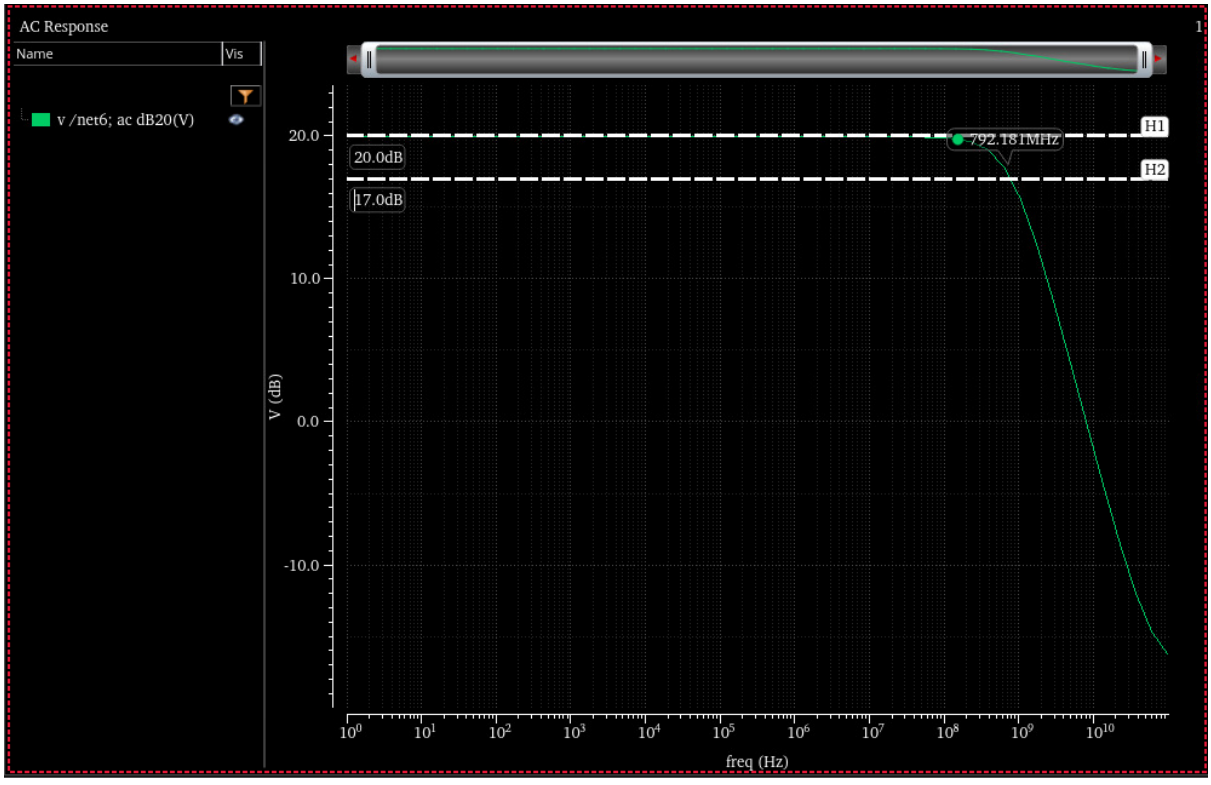
$$WN1 = 1.1um$$

$$WP1 = 4.6u$$




We need to increase the BW by a factor of ~3. This can be done by increasing the current, which will have a non linear effect because of added parasitic capacitance. We leave this like this for now and proceed to connect the second stage with the same parameters.

The AC response for the common source reads as follows:



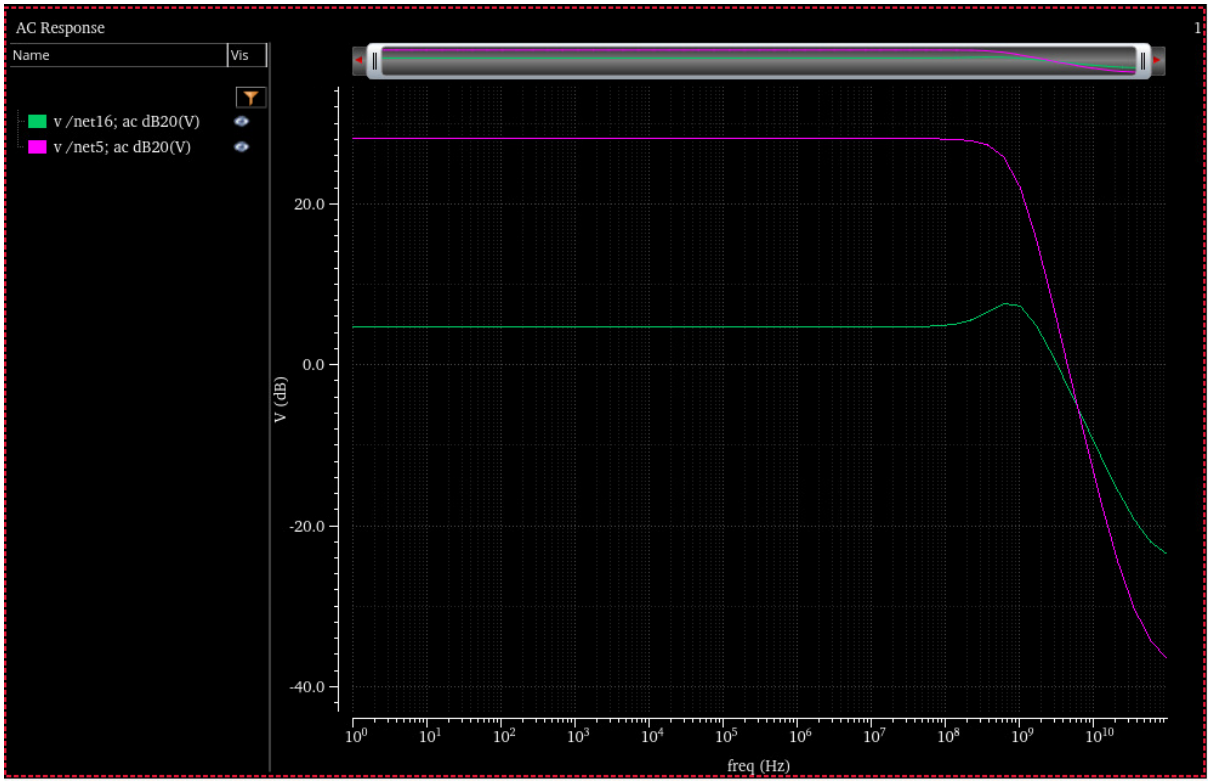

We can see that the BW is closer to 1GHz and the gain is 20dB.

Now we connect the two stages together with the resistor. The resistor is connected in feedback and will have the (desirable) effect of loading the common source and

therefore increasing the BW at expense of the gain. However, the capacitance of the output stage also loads the common source so the resistor may not be to big.

It will load less the output stage and we will correct the BW of the circuit by more current on the output stage.

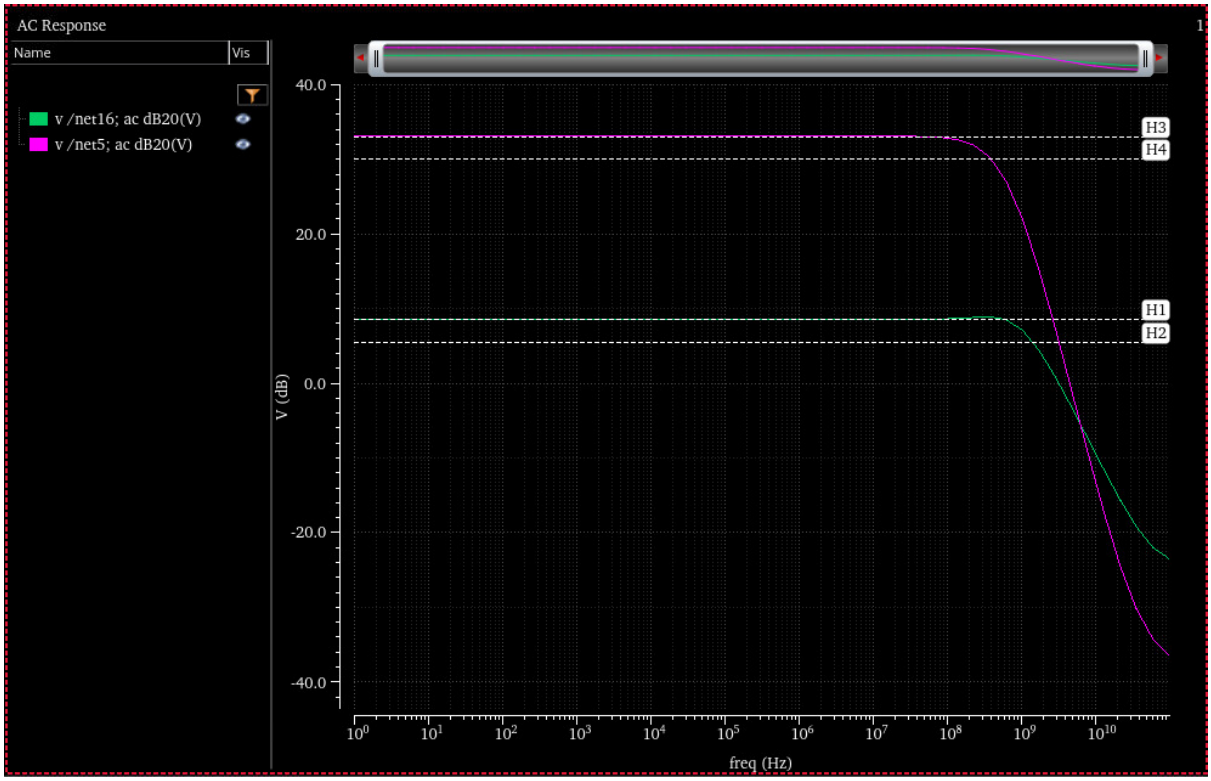
First we show the connection with no changes and a resistor value of $100k\Omega$:




We see as expected that the first stage plummets because of the low miller resistor $(\sim 10k\Omega)$ and we do see the zero that is present because of the $C_{gs}$ capacitance.

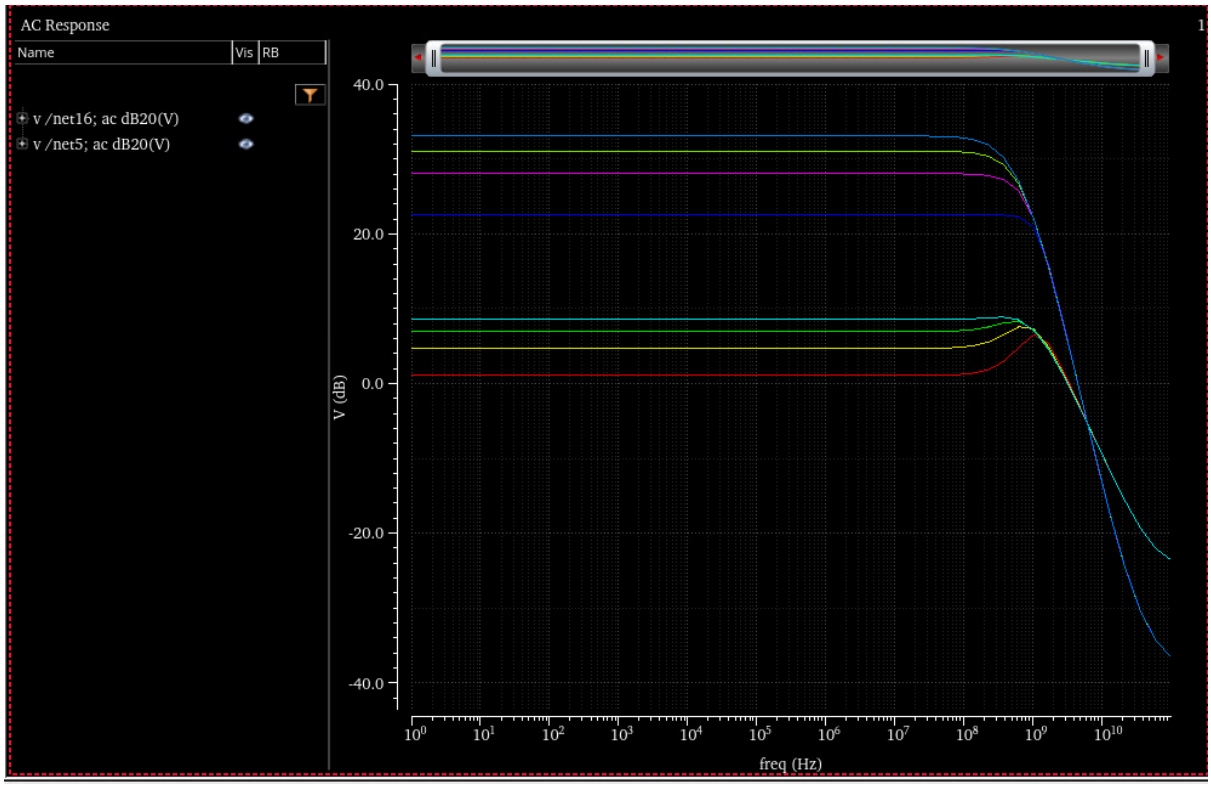
We will increase the resistor a bit to push the zero further away and gain more gain on the first stage.

The next figure shows the result of $R_F = 200\ k\Omega$.




Indeed the zero is pushed (phase margin improved). We can see that the output stage has the lowest BW.

To fix it we vary the resistor again, and try to load the output in such a way that its gain drops but the pole shifts. This will also hurt the common source.

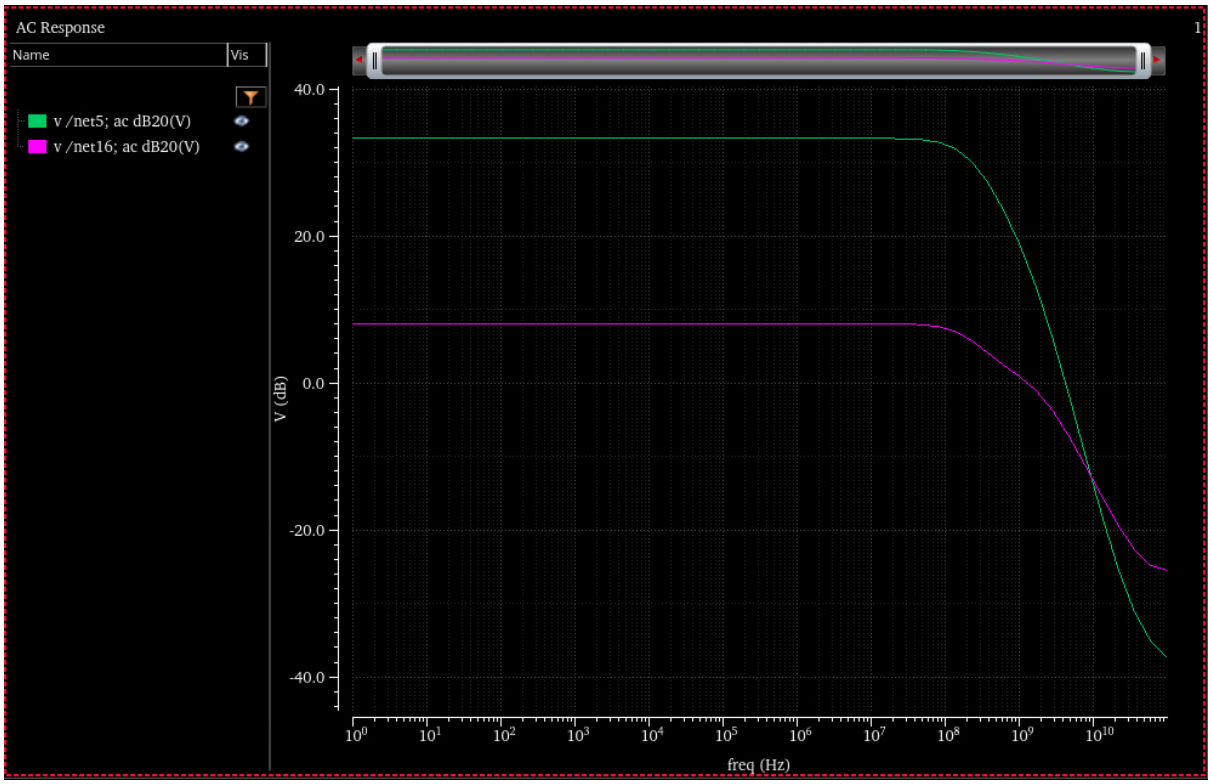


What we observe here is that the common source is close to 0dB and that the zero it provides is to close. This can be solved by increasing the current of the common source to make the resistance lower and push the zero (and the pole) further again. This will also increase the gain as the common source will become less loaded!

Using $WN2 = 2.2\mu$ $WP2 = 8.9\mu$ $R_F = 50k\Omega$ gives (the 8.9 was tweaked to give 0.5VDC):

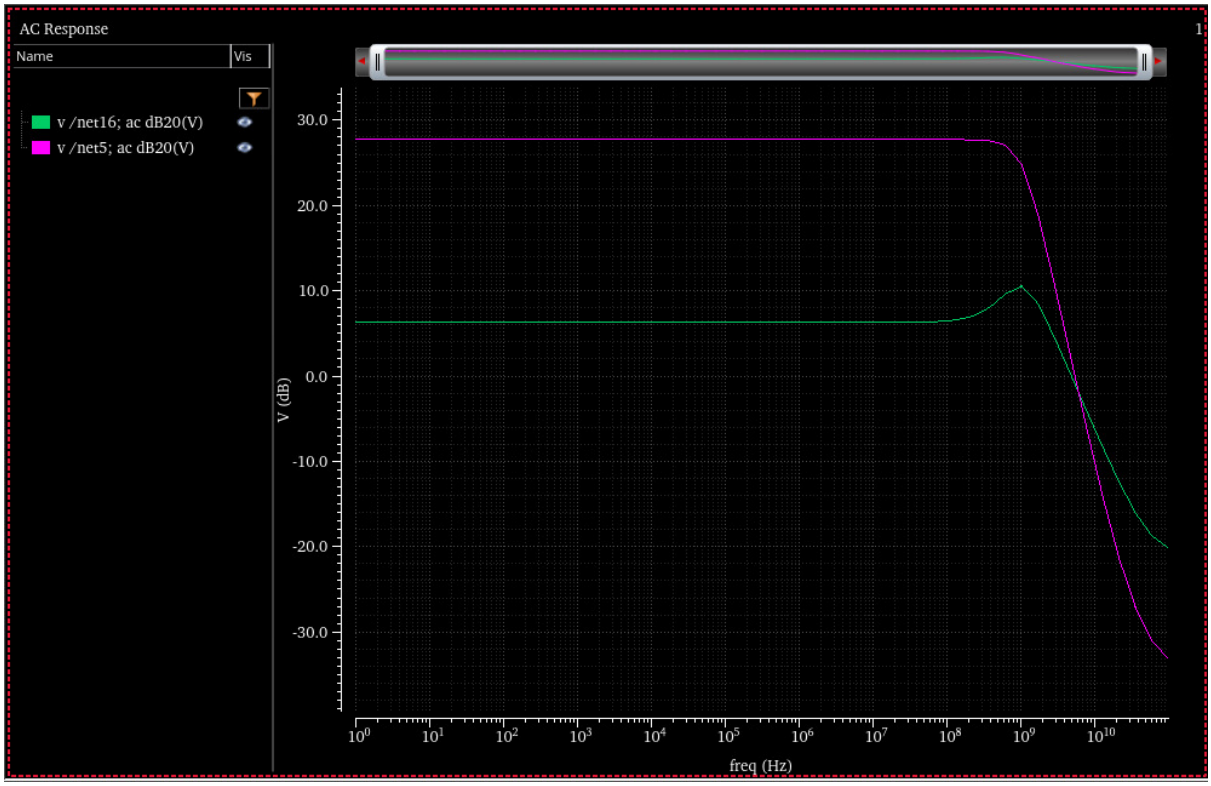
To fix this we can increase the current on the output stage. Doing so will increase the capacitances, which will have a bad effect on the pole of the common source. However, if needed we will be able to use a lower resistor (because of the bigger capacitors).

We show the results for a factor 2: $WN1 = 2.2\mu$ $WP1 = 9.2\mu$

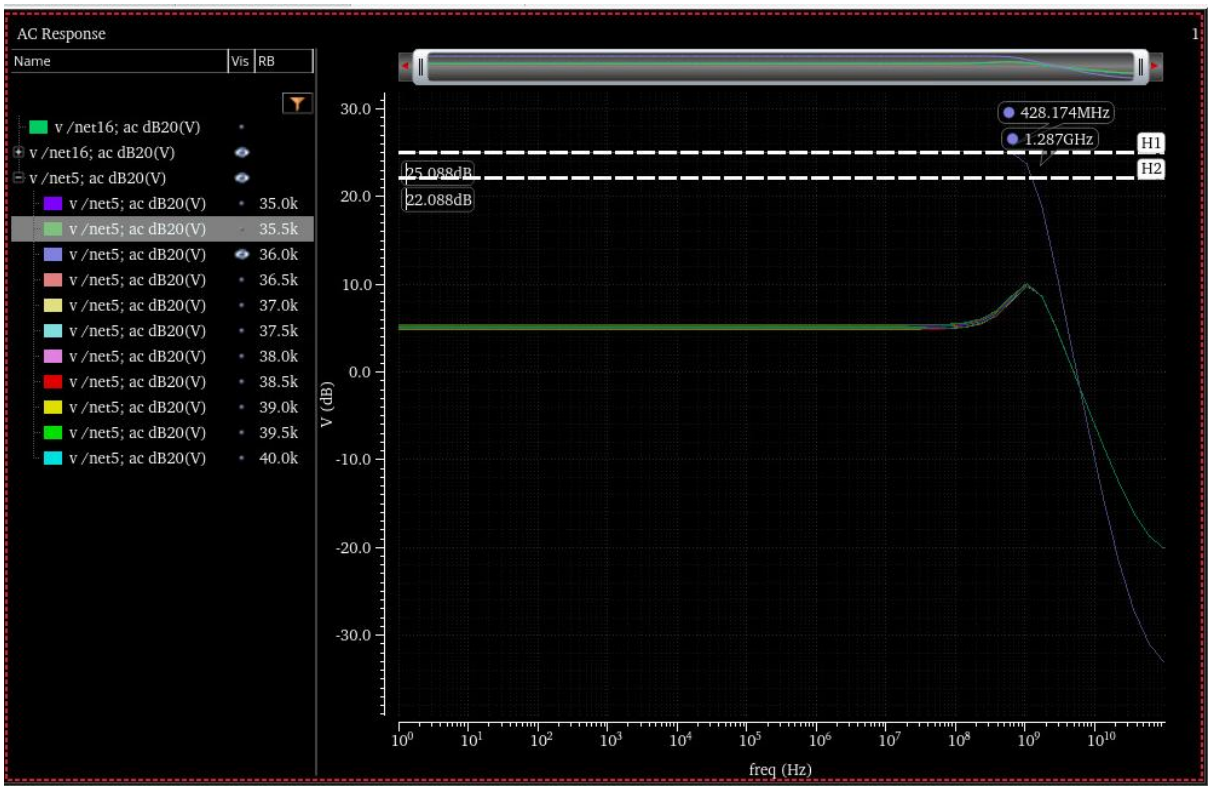



We see that the common source is very BW constrained. To fix this we will try to use more current on the common source stage so it's overall resistance is lowered.

Using $WN2 = 2.2\mu$ $WP2 = 8.9\mu$ gives (the 8.9 was tweaked to give 0.5VDC):




Increasing the current of the common source will result in higher gain and we are not interested in this. So we prefer to iterate over the resistor values:



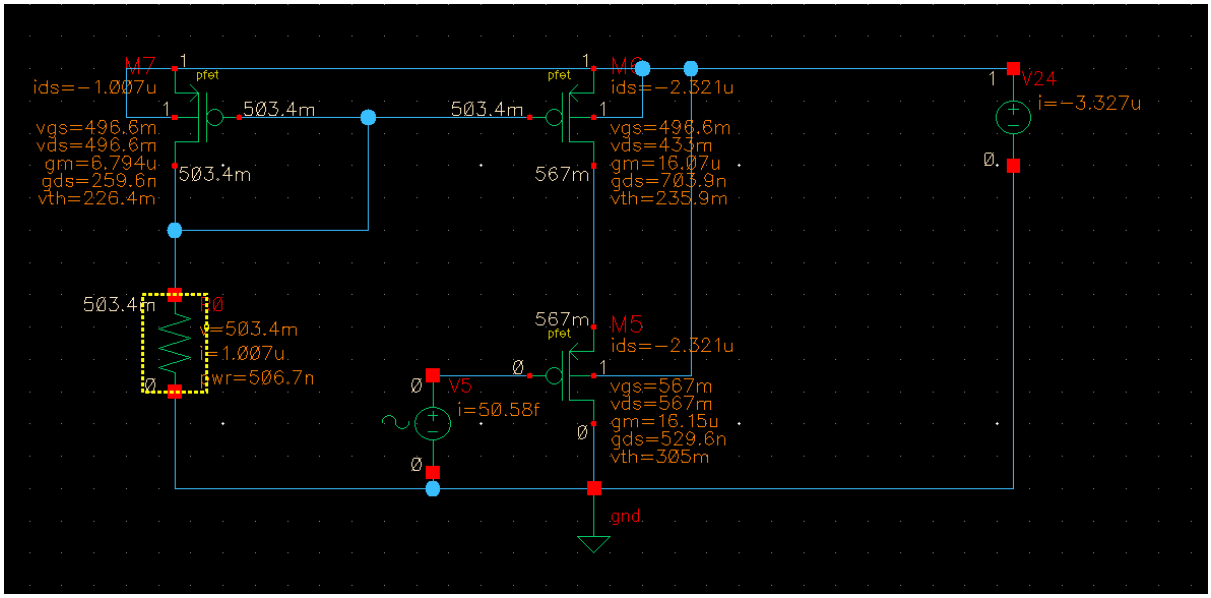

So our solution should be $35.5k\Omega$.

We would like to get 0.5V at the source of M5 which drives the NMOS (M3) of the next stage and 0.5V at the gate of M6 which drives the PMOS of the next stage (M4).
we will treat those voltages as out design constraints.
It is important to understand that M5 serves as an input buffer (does not adding gain).

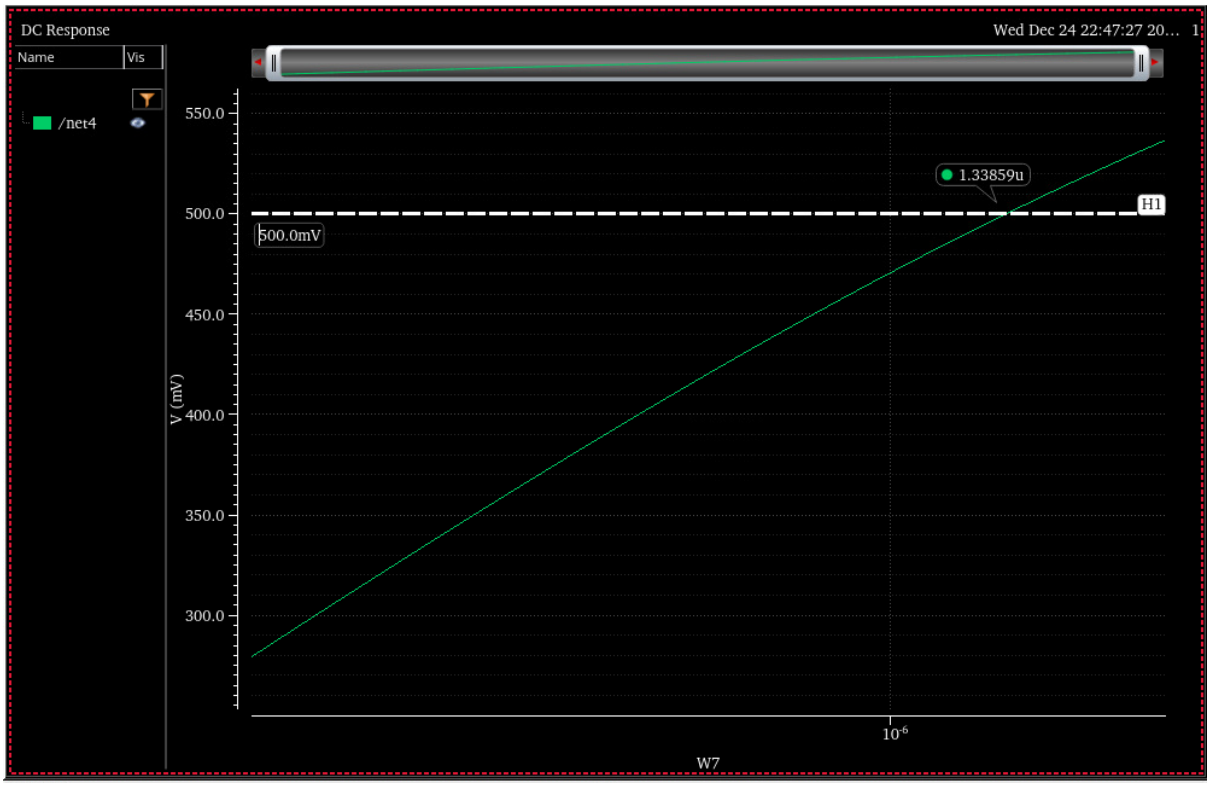
Our additional design constraint is the current that flows through the resistor and M7.
Notice that the constellation of M7-M6 serves as a current mirror that controls the current that flows through M5.
We will aim to get the highest current in M5 that stands within the design power constrain in order to get small parasitic capacitor that won't be the dominant one.
We will aim to get $10\mu A$.

According to our constraints, the resistor is $R_1 = \frac{V_{g7}}{I_{R1}} = \frac{0.5}{10\mu} = 50k\Omega$

We will fix $L_7 = 0.2\ \mu m$ and sweep on the size of M7 - $W_7, L_7$ in the range of: $0.2\mu - 2\mu\ [m]$ in the following constellation:



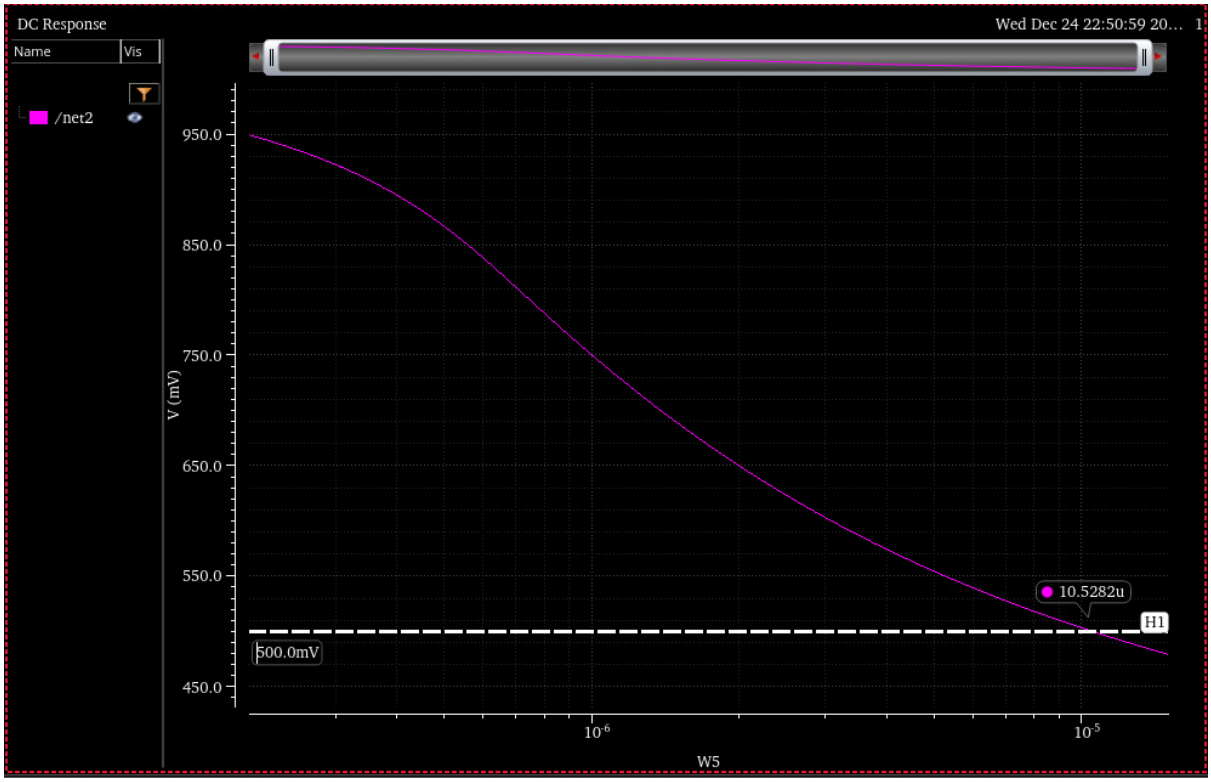
We plot the voltage on M7's gate voltage:




We see that $1\mu$ current is generated at $L_7 = 0.2\mu\ [m], W_7 = 1.3\mu\ [m]$.

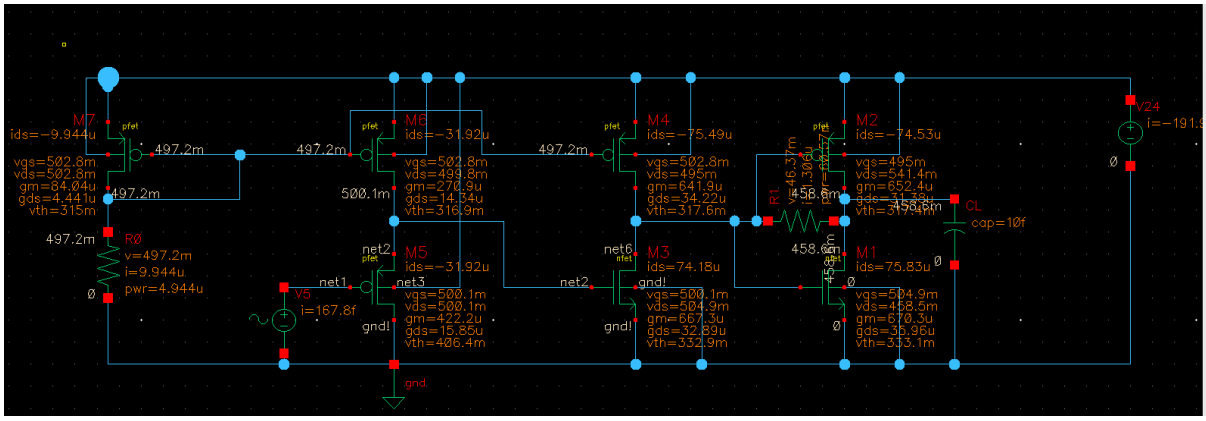
Now, let us design the M5, M6 branch.
Well choose M6 3 times bigger than M7 to get $3I_{ds7} \approx I_{ds6}$ as current mirror suggests and to withstand the current consumption. So $W_6 = 3.9u, L_6 = 0.2u$
Our constrain is $V_{s5} = 0.5V$, so according to the current equation of M5 we need to find the $\left(\frac{W}{L}\right)_5$ ratio that will satisfy the $V_{s5}$ constrain.

We will fix $L_5 = 0.2\mu$ and sweep over $W_5$ in the range$3\mu - 15\mu$ and plot $V_{ds5}$:

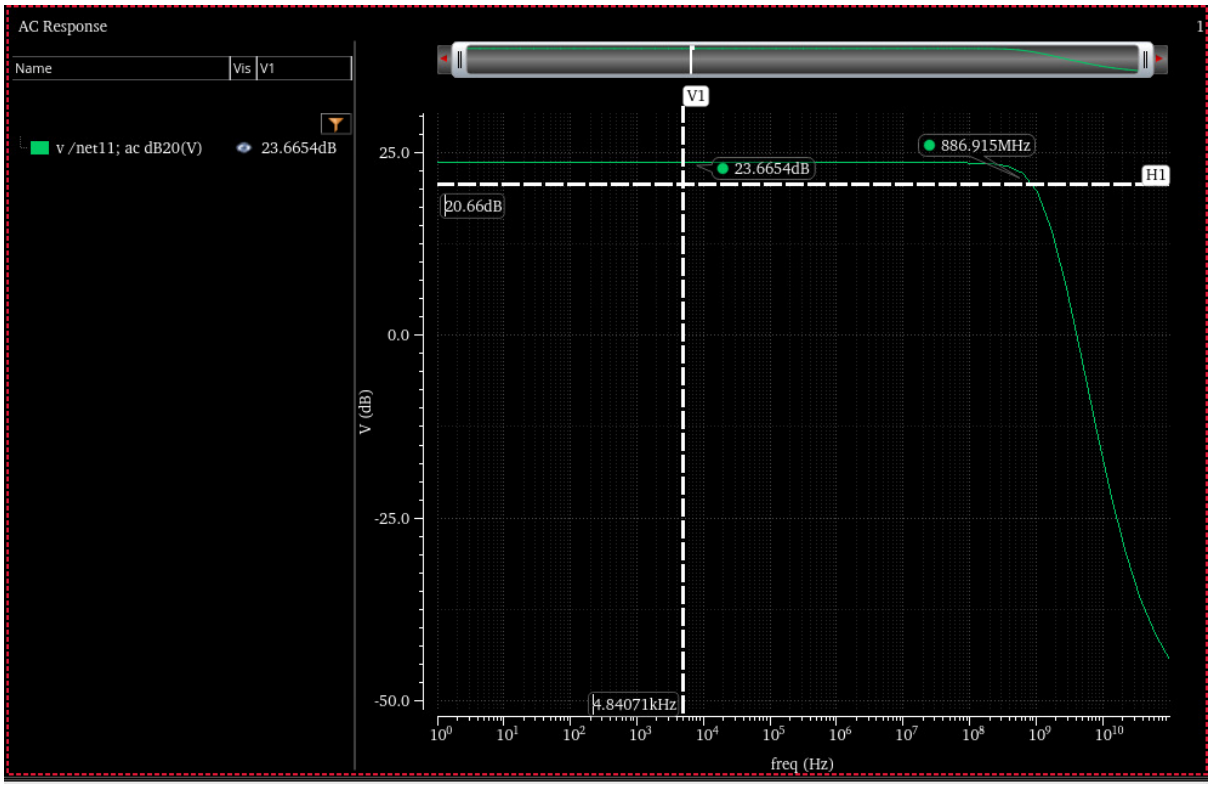



We will choose $W_5 = 10.5\mu\ [m]$

The final designed circuit is:



The AC simulation is:




Overall we were close, achieving 23.66 dB and ~890MHz.
Total power consumption $192\mu W$.