A VHDL based educational computer.

Richard James Howe : 082060589
howe.r.j.89@gmail.com

Aston University
Birmingham

Task

- Design a working computing system.
  - CPU Core.
  - RAM.
  - I/O Interface.
  - UART.
- Create Assembler.
- Make Bootloader.
- Make test programs.

Basic Concepts

Github

The code for this project (Makefiles, VHDL, C, Forth, etc.) are hosted on Github and can be found here:
`https://github.com/howerj/fyp`

References

[1] James Bowman, Willow Garage: *J1: A small Forth CPU for FPGAs*, EuroForth 2010, `http://www.excamera.com/files/j1.pdf` (2010)

[2] Javier Valcarce: *VHDL Macro: VGA80x40*, VHDL Monochrome VGA display adapter ,`http://www.javiervalcarce.eu/wiki/VHDL_Macro:_VGA80x40` (2009)

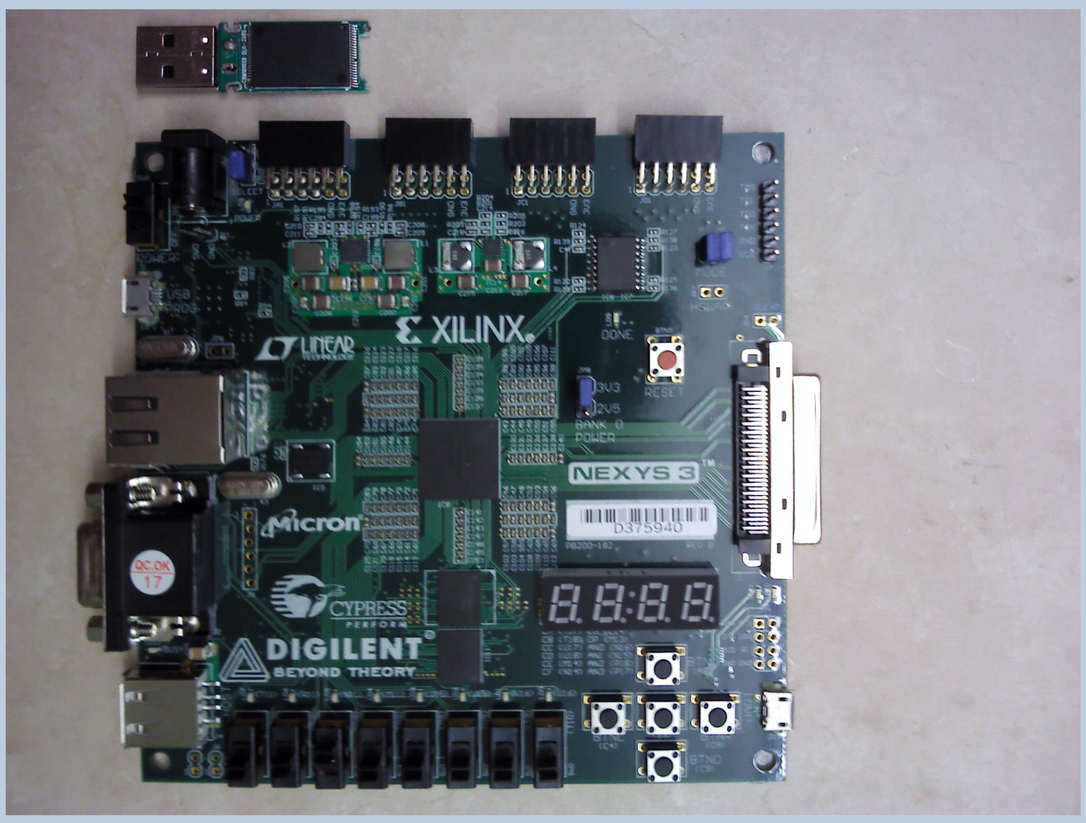
[3] Peter Bennett: *RS232 UART (VHDL)*, A UART core, `http://bytebash.com/2011/10/rs232-uart-vhdl/` (2012)

[4] Opencores: *Open source HDL cores and code*, `http://opencores.org/projects` (2013)

[5] *Nexys^{TM}3: A FPGA Spartan-6 development board*, `http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,897\&Prod=NEXYS3`, (2013)

VHDL

0.1 The Project



Using a Nexys 3 Development board, as shown above, I have created a portable computing system in VHDL intended for students like myself. The project is extensible and module, and as I have said it is also portable using no resources specific to Xilinx which would allow the system to be moved to smaller, cheaper devices.
The CPU core is based around a processor originally written in Verilog called the J1[1]. This has been rewritten in VHDL and modified due to it being less constrained in the projects scope like the original was. The processor is stack based which allows for a system which uses less space and can execute many FORTH instructions natively.

0.2 Resource Utilization

The entire system takes up very little room on the device (6slx16csg324-3) on a Nexys 3 Development board. This would allow for further expansion of the system and even multiple processor cores running simultaneously. Alternatively it could mean porting to a cheaper system while not reducing any functionality.

- Slice Registers : 295 out of 18224 (1%).
- Slice LUTs: 789 out of 9112 (8%).
- BRAMs
  - 4096x8 bit dual-port RAM, 2 (VGA Memory).
  - 8192x16 bit dual-port RAM, 1 (CPU Core).

In addition to these, also not listed is adders, comparators, subtracters, etcetera that have also been used by the design.

Firmware

The firmware is a simple bootloader, instead of compiling the program in as you would once the development is over, I have made a simple program that resides on the device that allows you to load an arbitrary program onto the core.