Parallel Patterns using Heterogeneous Computing

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ABSTRACT
Joint research project between University of St Andrews and University of Dundee for an enhancement of a Research Information Factory using heterogeneous computing and parallel knowledge-extraction patterns.

Categories and Subject Descriptors
H.4 [**Information Systems Applications**]: Miscellaneous

General Terms
Theory, Framework, Application, Research, Hardware

Keywords
knowledge-extraction, patterns, information factory, RIF, RIFF, RIFC, heterogeneous computing, parallel patterns, cassandra, spark, opencl, fastflow, cuda, 3D torus network

1. INTRODUCTION
The demand for processing data into knowledge is exponentially increasing as new raw data sources appear and the volume of data they generate increases daily. The conversion of data into actionable knowledge is important for the future of modern society. Every aspect of our lives ranging from health care to shopping are now impacted by our ability to process more data per person per day. The increase of volume, variety, velocity and veracity is a major challenge to data scientists. [8]

- The volume can not process on a single storage system and now spread over multiple systems.
- The variety causes complexity in processing to consolidate more data on same real world object.
- The speed or velocity of data creation is demanding more processing every second of the day.
- The veracity of the data requires that extra quality checks on data to improve the knowledge.

The trend over the last years is to build bigger and bigger data centers with massive energy requirements. This trend can not be sustained worldwide. Energy costs money and consumes natural resources that is becoming more undesirable.

"Research goal is to develop effective processing patterns with less overall energy cost."

2. BACKGROUND
The research into heterogeneous computing using parallel patterns.

2.1 Heterogeneous Computing
Heterogeneous computing systems [8] uses more than one type of processors. Systems gain performance enhancements by the ability to utilise dissimilar processors to execute common processing requirements. Using central processing unit (CPU), graphical processing unit (GPU) and field programmable gate array ($FPGA$) processor that enable effective processing at low energy requirements. The central processing unit (CPU) is designed with few cores optimised for sequential serial processing patterns that requires large amounts of control changes. The graphical processing unit (GPU) is designed as a massively parallel architecture of thousands of smaller, efficient cores handling multiple tasks simultaneously. The custom Application-Specific Integrated Circuit ($ASIC$) solution is capable of performing fixed spesific tasks like network connectivity, mapping information. Field Programmable Gate Array ($FPGA$) is a set of programmable logic blocks and programmable interconnects allow the same FPGA [13] to be used in many different applications. Heterogeneous uses them together as one processing unit.

2.2 Parallel Patterns
Patterns are the fundimental programming building blocks of data processing requirements. Heterogeneous computing changes the design and implimentation of common parallel patterns (task parallelism, pipelines, recursive splitting and geometric decomposition of data processing). We require new knowledge-extraction patterns using common strategies

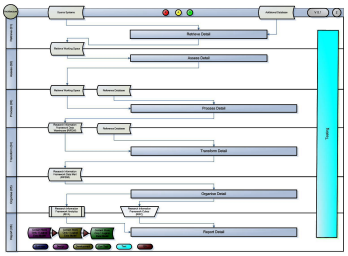

Figure 1: Research Information Factory Framework

(actors, shared queue, fork/join, loop parallelism and master/worker) with libraries (CUDA [11], OpenCL [9, 5, 13, 14], FastFlow [2] and ZeroMQ [6]).

2.3 Efficiency and Energy-awareness

The increasing drive for processing power demand increase energy levels to perform tasks. Our research targets efficiency in terms of processing time, programming effort, energy-awareness for each design pattern. Research calculates efficiency of processing [15] in Floating-point Operations Per Second per Watt (*FLOP/S/W*).

2.4 Research Information Factory

The Research Information Factory (*RIF*) is a processing appliance consisting of a framework and a cluster that supports the conversion of raw research data into knowledge using parallel patterns.

2.4.1 RIF Framework

The Research Information Factory Framework (*RIFF*) is a data processing framework designed during the period 2006 to 2011 and officially published as part of a MSc in Business Intelligence project (2012) and adapted during a Pg Cert in Data Science (2013) [1] to support unstructured and structured data patterns. The framework is a set of guidelines to process data into knowledge. Framework uses a five layer process: Research Layer (specific research requirements), Utility Layer (common processing utilities), Audit, Balance and Control Layer (schedule jobs, collect audits, control patterns) Operational Management Layer (active processing controls) Functional Layer supports the core processing pattern of **R**etrieve-**A**ssess-**P**rocess-**T**ransform-**O**rganise-**R**eport (*R-A-P-T-O-R*).

2.4.2 RIF Cluster

The Research Information Factory Cluster (*RIFC*) is a 3D torus connected cluster appliance using commondity computer equipment to process the RIFF parallel patterns. This new custom parallel cluster appliance design [1](Synaptic Assimilator) supports the RIFF. The cluster supports a Cassandra database [3] and a Spark Processing Engine [12] to handle the scalability and high availability data processing to match the parallel patterns requirements for data sources of a size larger than what a single system can handle.

3. PROPOSED SOLUTION

The research will develop new parallel patterns for knowledge extraction, new mechanisms for storing and extracting data while using minimum amounts of energy. The research over next year covers three stages:

3.1 Heterogeneous systems.

The research will study the fundamental behavior of a selection of heterogeneous computing components as implimented in a nVidia Jetson TK1 development kit. [12]

3.2 Parallel patterns for data processing

The system is evaluated on a basis of a fixed size data set processed via a specific parallel pattern changing parameters like combinations of CPU, GPU with different clock speeds, memory allocations and measuring time to complete task, energy requirements and effort in amount of code required for each parallel pattern and heterogeneous computing combination.

3.3 Research Information Factory Cluster

The Research Information Factory Cluster (*RIFC*) is a 3D torus connected cluster appliance using commondity computer equipment, a Cassandra database [3, 4] and a Spark Engine [4, 7] to handle the scalability and high availability data processing from systems like nVidia Jetson TK1 [12] and Tilera TILE-Mx100 processor [10].

4. CONCLUSION

The research goal is to process with less energy. Heterogeneous systems with parallel patterns is currently the optimum option to achieve the goal.

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