```
 1  module uart(input wire [7:0] data_in, //input data
 2              input wire wr_en,
 3              input wire clear,
 4              input wire clk_50m,
 5              output wire Tx,
 6              output wire Tx_busy,
 7              input wire Rx,
 8              output wire ready,
 9              input wire ready_clr,
10              output wire [7:0] data_out,
11              output [7:0] LEDR,
12              output wire Tx2//output data
13              );
14  assign LEDR = data_in;
15  assign Tx2 = Tx;
16  wire Txclk_en, Rxclk_en;
17  baudrate uart_baud(  .clk_50m(clk_50m),
18                       .Rxclk_en(Rxclk_en),
19                       .Txclk_en(Txclk_en)
20                      );
21  transmitter uart_Tx( .data_in(data_in),
22                       .wr_en(wr_en),
23                       .clk_50m(clk_50m),
24                       .clken(Txclk_en), //We assign Tx clock to enable clock
25                       .Tx(Tx),
26                       .Tx_busy(Tx_busy)
27                      );
28  receiver uart_Rx( .Rx(Rx),
29                    .ready(ready),
30                    .ready_clr(ready_clr),
31                    .clk_50m(clk_50m),
32                    .clken(Rxclk_en), //We assign Tx clock to enable clock
33                    .data(data_out)
34                   );
35
36  endmodule
37
```