

EE115B-Digital Circuits

HW2

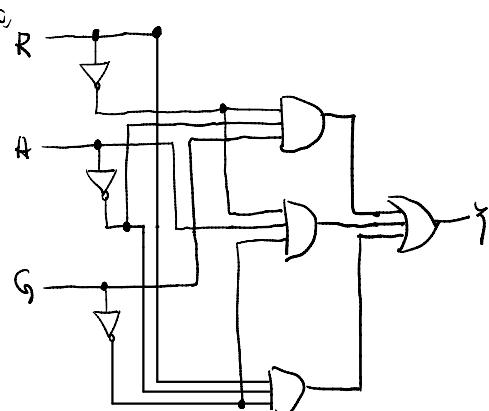
Due on May. 15, 2024

1	1	0
1	0	1
0	1	1
0	1	0

1. Design a circuit to detect the malfunction of traffic lights. Use R, A, G to denote red, yellow, and green lights. Use Y=1 to represent the traffic light works well.
- Draw the truth table. (5 marks)
 - Write the logic expressions. (5 marks)
 - Draw the circuit. (5 marks)

a)	R	A	G	Y
	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	0
	1	0	0	1
	1	0	1	0
	1	1	0	0
	1	1	1	0

$$\text{b), } Y = \bar{R}\bar{A}G + \bar{R}A\bar{G} + R\bar{A}\bar{G}$$



2. Draw the following function using only 2-input-NAND and 2-input-NOR and Inverter
- $Y = (AB+CD)'$ (5 marks)
 - $Y = (AB+CD)EF$ (5 marks)

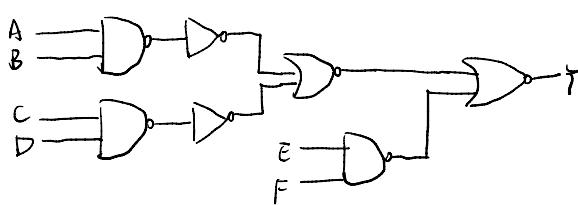
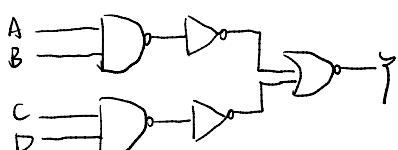
$$\text{a), } Y = \overline{\overline{AB} + \overline{CD}}$$

$$= \overline{\overline{AB}} + \overline{\overline{CD}}$$

$$\text{b), } Y = (\overline{AB} + \overline{CD})\overline{EF}$$

$$= \overline{\overline{(\overline{AB} + \overline{CD})}EF}$$

$$= \overline{\overline{AB} + \overline{CD} + \overline{EF}}$$

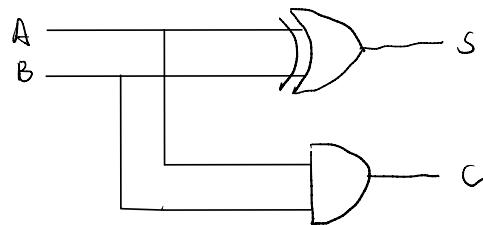


3. Adder

- Draw the truth table of half-adder and write the function of C and S (5 marks)
- Using logic gate to draw the half-adder with the function you designed in a) (5 marks)

(a)

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$$S = \bar{A}B + A\bar{B} = A \oplus B$$

$$C = AB$$

- Design a 3-bits (inputs are A_2-A_0 , B_2-B_0 , C_{in}) look ahead carry adder.

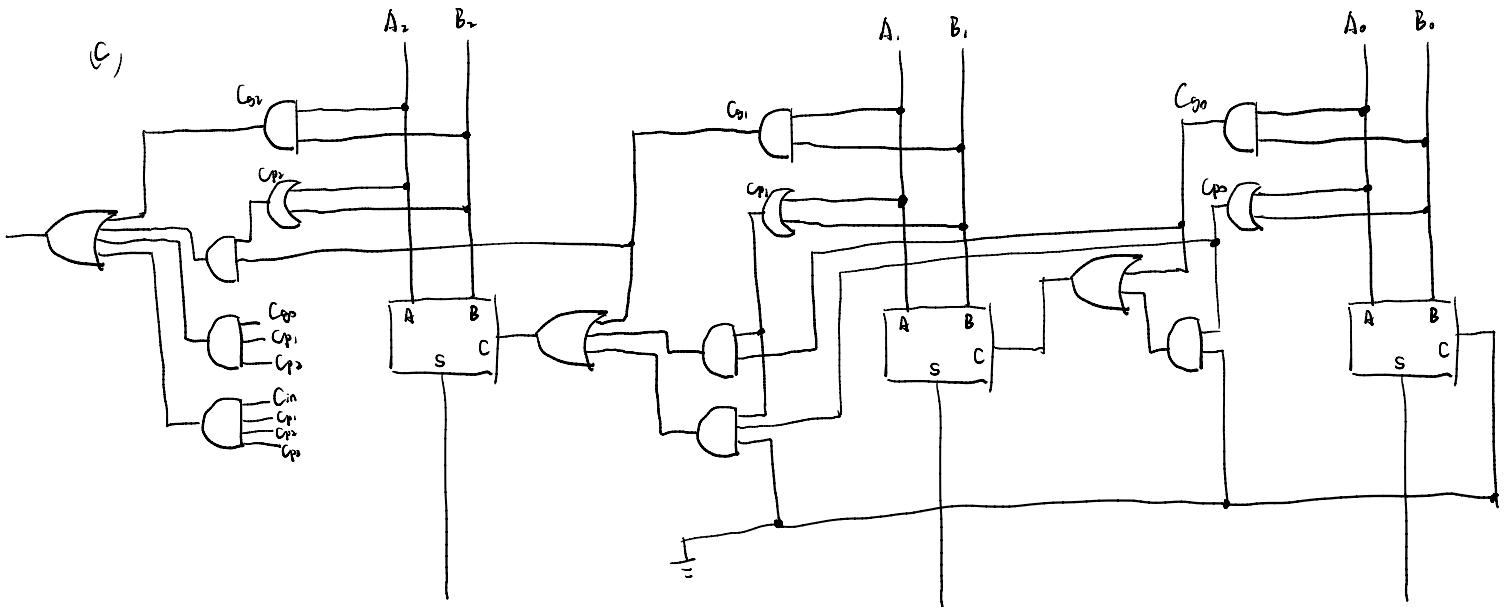
a) Write the logic expression for C_0 to C_2 . (5 marks)

b) Write the logic expression for sum. (5 marks)

c) Plot the circuit. (5 marks)

(b)

define $C_{gi} = A_i B_i$ $C_{pi} = A_i + B_i$ $\forall j \quad S_j = (A_j \oplus B_j) \oplus 0$
 $C_0 = C_{g0} + C_{in} C_{p0}$ $S_0 = (A_0 \oplus B_0) \oplus C_{in}$
 $C_1 = C_{g1} + C_{g0} C_{p1} + C_{in} C_{p0} C_{p1}$ $S_1 = (A_1 \oplus B_1) \oplus C_1$
 $C_2 = C_{g2} + C_{g1} C_{p2} + C_{g0} C_{p1} C_{p2} + C_{in} C_{p0} C_{p1} C_{p2}$



5. Design an 8-3 encoder. Only one input is allowed at a time. The inputs and outputs are low active. Use I_7' (LSB) to I_0' (MSB) to represent inputs, and Y_2' to Y_0' for outputs.

- Draw the truth table. (5 marks)
- Write the logic expressions for Y_2' to Y_0' . (5 marks)
- Draw the circuit. (5 marks)

(a)

\bar{I}_0	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	\bar{Y}_2	\bar{Y}_1	\bar{Y}_0
1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	0	1	1	0	1	0
1	1	1	1	0	1	1	1	0	0	0
1	1	1	0	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	0	1	0
1	0	1	1	1	1	1	1	0	0	1
0	1	1	1	1	1	1	1	0	0	0

(b)

$$\bar{Y}_2 = \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3$$

$$\bar{Y}_1 = \bar{I}_0 \bar{I}_1 \bar{I}_4 \bar{I}_5$$

$$\bar{Y}_0 = \bar{I}_0 \bar{I}_1 \bar{I}_4 \bar{I}_6$$

6. Design the binary-decimal decoder. Both the inputs (use A_i) and outputs (use Y_i) are active high.

- Draw the truth table. (5 marks)
- Write the logic expressions. (5 marks)

(a)

A_3	A_2	A_1	A_0	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0

(b)

$$Y_9 = \bar{A}_3 \bar{A}_2 \bar{A}_1 \bar{A}_0$$

$$Y_8 = \bar{A}_3 \bar{A}_2 \bar{A}_1 A_0$$

$$Y_7 = \bar{A}_3 \bar{A}_2 \bar{A}_1 \bar{A}_0$$

$$Y_6 = A_3 \bar{A}_2 \bar{A}_1 \bar{A}_0$$

$$Y_5 = \bar{A}_3 A_2 \bar{A}_1 \bar{A}_0$$

$$Y_4 = A_3 \bar{A}_2 \bar{A}_1 A_0$$

$$Y_3 = \bar{A}_3 A_2 \bar{A}_1 A_0$$

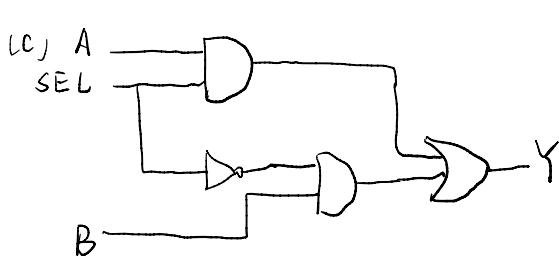
$$Y_2 = \bar{A}_3 A_2 \bar{A}_1 \bar{A}_0$$

7. Consider a 2-1 MUX

- draw the truth table of the MUX (5 marks)
- write the logic function of MUX (5 marks)
- draw the MUX using logic gate (5 marks)

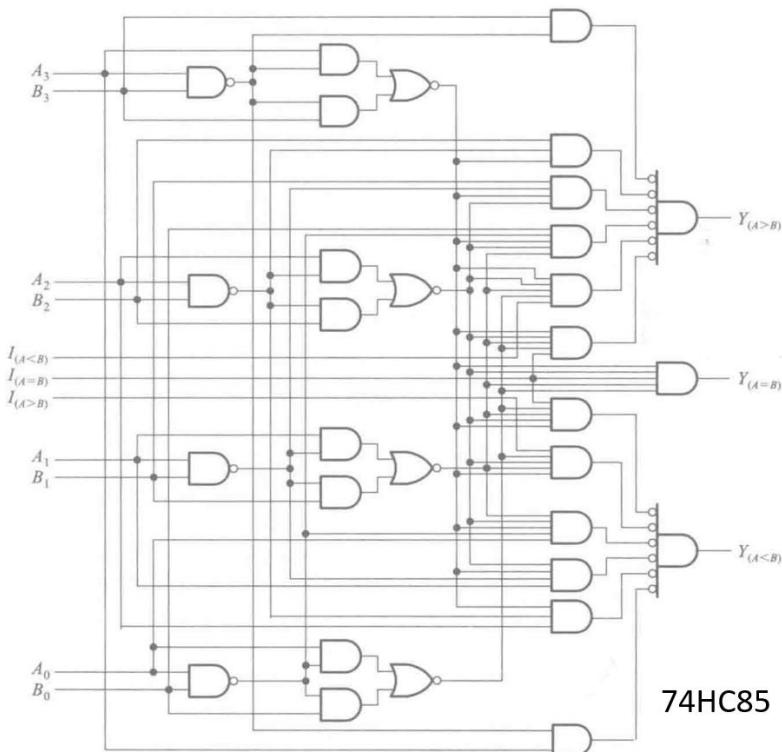
(a)

SEL	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



(b) $Y = SEL \cdot A + \overline{SEL} \cdot B$

8. Write the expression of $Y(A > B)$, $Y(A = B)$, and $Y(A < B)$ following the circuit below. (10 marks)



$$Y_{(A>B)} = (A_3' B_3)' \cdot (A_2' B_2 \cdot (A_3 \oplus B_3))' \cdot (A_1' B_1 \cdot (A_2 \oplus B_2) \cdot (A_3 \oplus B_3))' \cdot (A_0' B_0 \cdot (A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1))' \\ ((A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0) \cdot I_{(A>B)})' \cdot ((A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0) \cdot I_{(A=B)})'$$

$$Y_{(A=B)} = (A_3 B_3)' \cdot (A_2 B_2 \cdot (A_3 \oplus B_3))' \cdot (A_1 B_1 \cdot (A_2 \oplus B_2) \cdot (A_3 \oplus B_3))' \cdot (A_0 B_0 \cdot (A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1))' \\ ((A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0) \cdot I_{(A=B)})' \cdot ((A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0) \cdot I_{(A=B)})'$$

$$Y_{(A<B)} = (A_3 \oplus B_3) \cdot (A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \oplus B_0) \cdot I_{(A<B)}$$