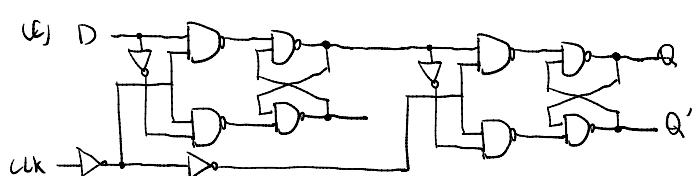
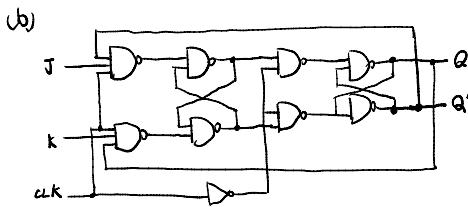
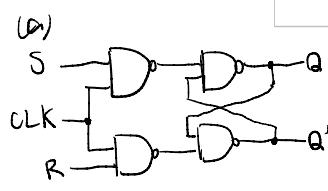
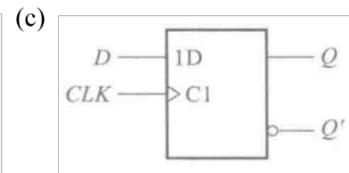
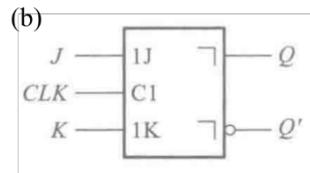
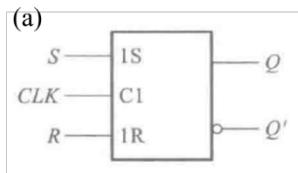


EE115B-Digital Circuits

HW3

Due on June. 12, 2024

1. Draw the circuit (using logic gates) and truth table of the flip-flop below. (15 points)



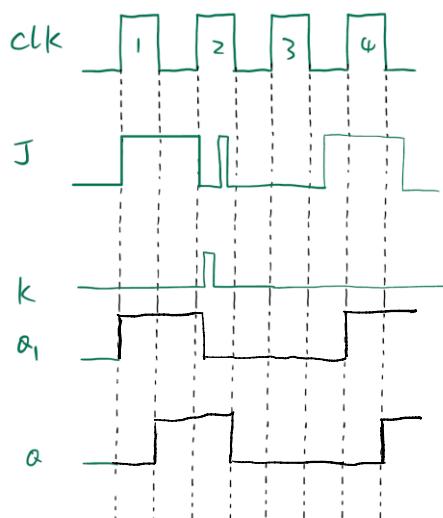
CLK	S	R	Q	Q*
0	x	x	0	0
0	x	x	1	1
1	0	0	0	0
1	0	0	1	-
1	0	0	-	-
1	0	1	1	1
1	0	1	0	0
1	0	1	-	-
1	1	0	0	0
1	1	0	1	1
1	1	1	1	0
1	1	1	0	1

CLK	J	K	Q	Q*
x	x	x	x	Q
0	0	0	0	0
0	0	0	1	1
1	0	0	0	0
1	0	0	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

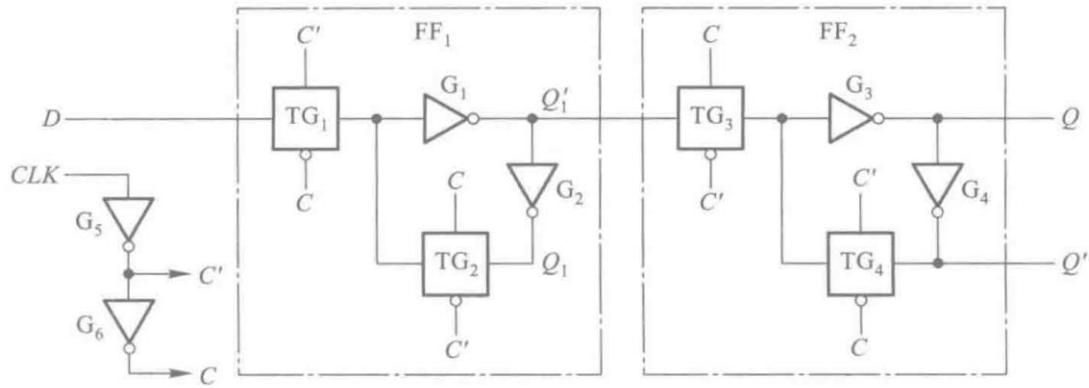
CLK	D	R	Q*
x	x	x	Q
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

① CLK 回到低电平后状态不定

2. Complete the following waveform based on the J-K flip-flop defined in 1(b). (10 points)



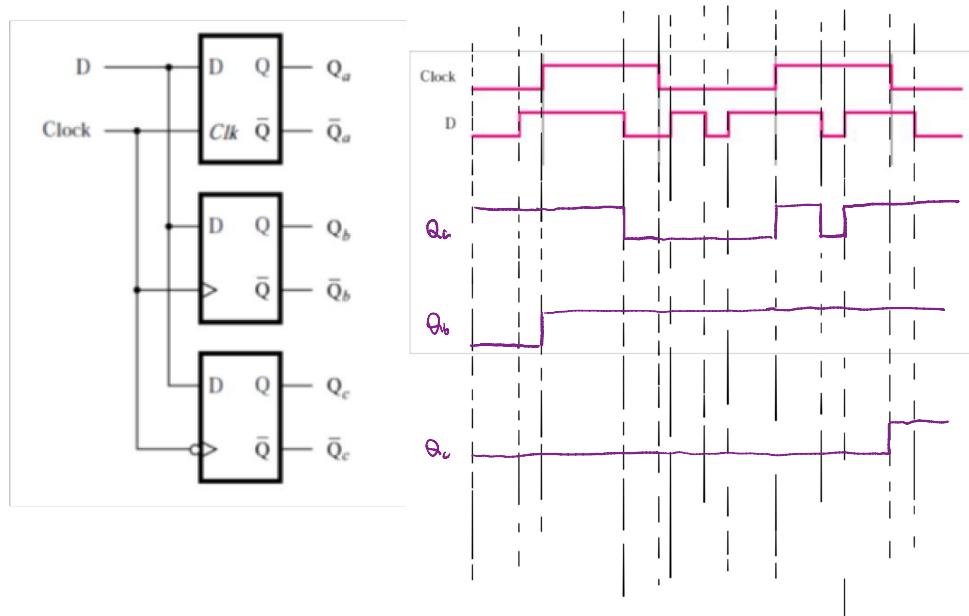
3. Determine the setup time and hold time of the following circuit. The propagation delay of the inverter and transmission gate is t_d and $2t_d$, respectively. (10 points)



$$t_{\text{setup}} = 2t_{\text{inv}} + t_{TG} - t_{\text{inv}} = t_{\text{inv}} + t_{TG} = 3t_d$$

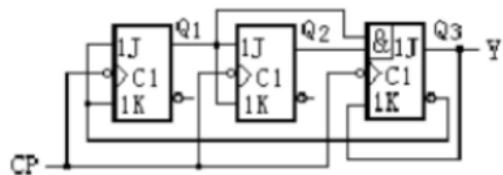
$$t_{\text{hold}} = 2t_{\text{inv}} = 2t_d$$

4. Assume that the D and Clock inputs shown below are applied to the circuits. Draw the waveforms for Q_a, Q_b , and Q_c . Assume that the initial states are $Q_a=1, Q_b=Q_c=0$. Ignore the propagation delays. (10 points)



5. For the logic functions of the circuit below,

- Determine it is Moore type or Mealy type. (5 points)
- Write down the excitation equation (驱动方程), state equation (状态方程) and output equations. (10 points)
- Draw the state transition diagram, and check whether the circuit can self-start. (10 points)



(a) There's no input and the output only depend on the current state, so it's Moore type

(b) excitation equation:

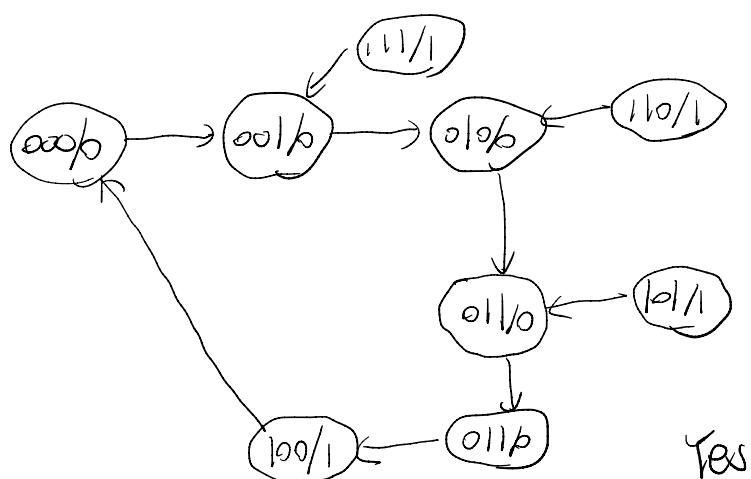
$$\begin{cases} J_1 = K_1 = \bar{Q}_2 \\ J_2 = K_2 = Q_1 \\ J_3 = Q_2 Q_3 \quad K_3 = Q_3 \end{cases}$$

state equation:

$$\begin{cases} Q_1^* = J_1 \bar{Q}_1 + \bar{K}_1 Q_1 = \bar{Q}_1 \bar{Q}_2 + Q_1 Q_2 = Q_1 \oplus Q_2 \quad Y = Q_3 \\ Q_2^* = J_2 \bar{Q}_2 + \bar{K}_2 Q_2 = Q_1 \bar{Q}_2 + \bar{Q}_2 Q_2 = Q_1 \oplus Q_2 \\ Q_3^* = J_3 \bar{Q}_3 + \bar{K}_3 Q_3 = Q_2 Q_3 \end{cases}$$

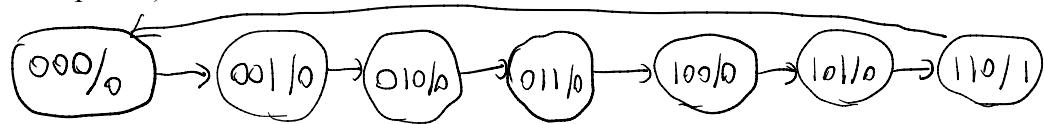
output equation:

J_1	Q_1	Q_2	Q_3	Q_1^*	Q_2^*	Q_3^*	Y
0	0	0	0	0	0	1	0
0	0	1	0	0	1	0	0
0	1	0	0	0	1	1	0
0	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1
1	0	1	0	0	1	1	1
1	1	0	0	1	0	0	1
1	1	1	0	0	0	1	1



Yes

6. Design a synchronized Modulo-7 counter using JK flip-flop and logic gates. (20 points)



$$Q^* = J\bar{Q} + \bar{K}Q$$

Q_2/Q_1	00	01	11	10
0	001/0	010/0	100/0	011/0
1	101/0	110/0	xxx/x	000/1

$$C = Q_2 Q_0$$

Q_2/Q_1	00	01	11	10
0	0	0	1	0
1	1	1	x	0

$$Q_0^*$$

Q_2/Q_1	00	01	11	10
0	0	0	0	0
1	0	1	x	0

$$Q_1^*$$

Q_2/Q_1	00	01	11	10
0	0	0	0	0
1	1	0	x	0

$$Q_0^*$$

Q_2/Q_1	00	01	11	10
0	0	0	0	0
1	0	0	x	0

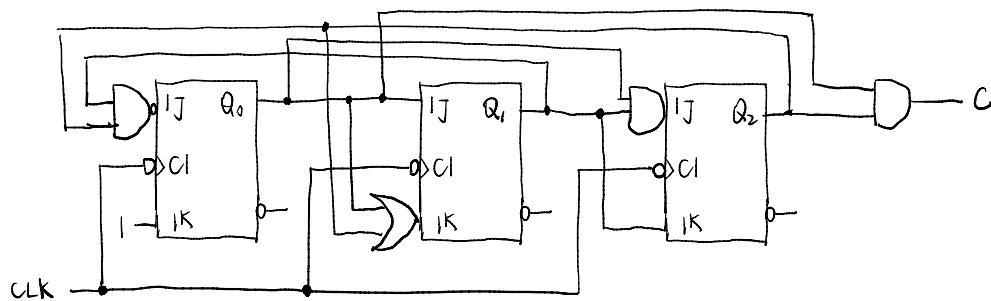
$$C$$

$$Q_0^* = Q_2 \bar{Q}_1 + Q_1 Q_0 = Q_2 \bar{Q}_1 + Q_1 Q_0 (Q_1 + \bar{Q}_1) = (Q_1 Q_0 + \bar{Q}_1) Q_2 + Q_1 Q_0 \bar{Q}_2 = Q_1 Q_0 \bar{Q}_2 + \bar{Q}_1 Q_2$$

$$J_1 = Q_0 \quad K_1 = Q_1 + Q_0$$

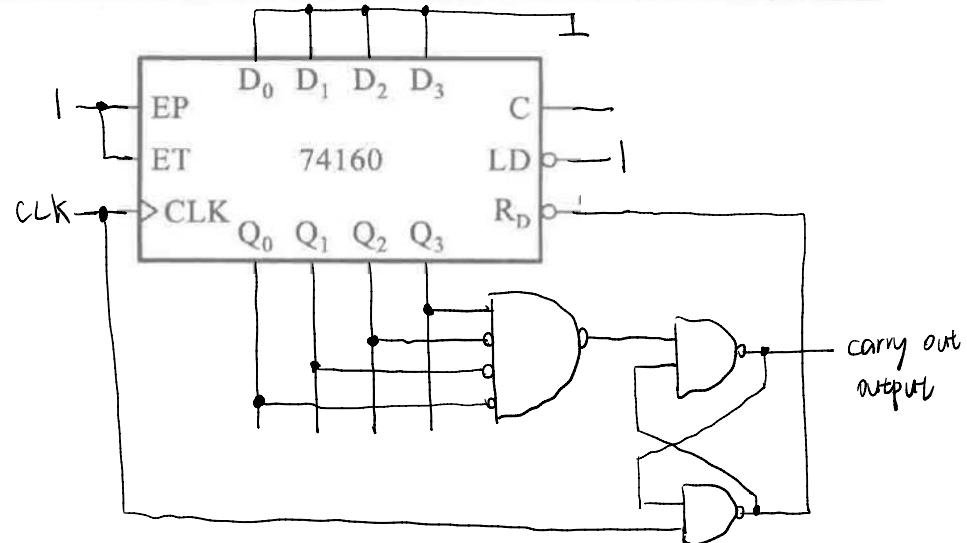
$$Q_1^* = \bar{Q}_1 Q_0 + \bar{Q}_2 Q_1 = \bar{Q}_1 Q_0 + \bar{Q}_2 \bar{Q}_1 Q_1 \quad J_2 = Q_0 \quad K_2 = Q_1 + Q_0$$

$$Q_0^* = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_2 \bar{Q}_1 = (\bar{Q}_1 + \bar{Q}_2) \bar{Q}_0 + \bar{T} \cdot \bar{Q}_0 \quad J_0 = \bar{Q}_1 \bar{Q}_2 \quad K_0 = 1$$



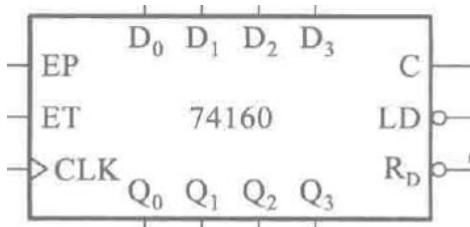
7. Design a synchronized octal counter using presetting method based on the 74160 chip, whose functional table is shown below. (10 points)

<i>CLK</i>	R'_D	LD'	<i>EP</i>	<i>ET</i>	工作状态
x	0	x	x	x	置零
↑	1	0	x	x	预置数
x	1	1	0	1	保持
x	1	1	x	0	保持(但 $C=0$)
↑	1	1	1	1	计数



7. Design a synchronized octal counter using presetting method based on the 74160 chip, whose functional table is shown below. (10 points)

CLK	R'_D	LD'	EP	ET	工作状态
x	0	x	x	x	置零
↑	1	0	x	x	预置数
x	1	1	0	1	保持
x	1	1	x	0	保持(但 $C=0$)
↑	1	1	1	1	计数



Handwritten logic expressions for the 74160 counter:

- $A \bar{B} + \bar{A} \bar{C} \bar{D}$
- $(\bar{A} + \bar{A}) \bar{B} \bar{C} \bar{D}$
- $\bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} \bar{C} \bar{D}$
- $AB + \bar{A} C$
- D (represented by a small square)