EE115B-Digital Circuits

LAB 3

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The circuit diagram of a 4-bit multiplier is shown below.

(1) Build this circuit using Verilog in vivado. Paste all your codes here (including the testbench).

codes

```
`timescale 1ns / 1ps
module FullAdder(
    input a,
    input b,
    input cin,
    output sum,
    output cout
);
    assign sum = a ^ b ^ cin;
    assign cout = (a & b) | (b & cin) | (a & cin);
endmodule

module FourBitMultiplier(
    input [3:0] multiplicand,
    input [3:0] multiplier,
    output [7:0] product
);
    wire [3:0] pp0, pp1, pp2, pp3;
    wire [3:0] s1, s2, s3;
    wire [3:0] c1, c2, c3;

    // Partial Products
    assign pp0 = multiplicand & {4{multiplier[0]}};
    assign pp1 = multiplicand & {4{multiplier[1]}};
    assign pp2 = multiplicand & {4{multiplier[2]}};
    assign pp3 = multiplicand & {4{multiplier[3]}};

    // First layer of full adders
    FullAdder fa11(pp1[0], pp0[1], 1'b0, s1[0], c1[0]);
```

```
    FullAdder fa12(pp1[1], pp0[2], c1[0], s1[1], c1[1]);
    FullAdder fa13(pp1[2], pp0[3], c1[1], s1[2], c1[2]);
    FullAdder fa14(pp1[3], 1'b0, c1[2], s1[3], c1[3]);

    // Second layer of full adders
    FullAdder fa21(pp2[0], s1[1], 1'b0, s2[0], c2[0]);
    FullAdder fa22(pp2[1], s1[2], c2[0], s2[1], c2[1]);
    FullAdder fa23(pp2[2], s1[3], c2[1], s2[2], c2[2]);
    FullAdder fa24(pp2[3], c1[3], c2[2], s2[3], c2[3]);

    // Third layer of full adders
    FullAdder fa31(pp3[0], s2[1], 1'b0, s3[0], c3[0]);
    FullAdder fa32(pp3[1], s2[2], c3[0], s3[1], c3[1]);
    FullAdder fa33(pp3[2], s2[3], c3[1], s3[2], c3[2]);
    FullAdder fa34(pp3[3], c2[3], c3[2], s3[3], c3[3]);

    // Assign final product
    assign product = {c3[3], s3[3], s3[2], s3[1], s3[0], s2[0], s1[0], pp0[0]};

endmodule
```

testbench

```
`timescale 1ns / 1ps
module tb();
    reg [3:0] multiplicand;
    reg [3:0] multiplier;
    wire [7:0] product;

    FourBitMultiplier uut (
        .multiplicand(multiplicand),
        .multiplier(multiplier),
        .product(product)
    );

    initial begin
        multiplicand = 4'b1000;
        multiplier = 4'b0101;
        #10
        multiplicand = 4'b1001;
        multiplier = 4'b0011;
        #10
        multiplicand = 4'b1011;
        multiplier = 4'b0011;
```

```
        #10
        multiplicand = 4'b1101;
        multiplier = 4'b0101;
        #10
        multiplicand = 4'b0101;
        multiplier = 4'b0111;
    end


endmodule
```

(2) Run the simulation, and show the wave diagram of 1000×0101, 1001×0011, 1011×0011, 1101×0101, 0101×0111.