# Wide Range Fuel Gauge with Impedance Track™ for Lead-Acid Batteries

**Check for Samples: bq34z110**

## FEATURES

- **Supports Lead-Acid Chemistries**
- **Capacity Estimation Using Patented Impedance Track™ Technology for Batteries from 4 V to 64 V**
  - **Aging Compensation**
  - **Self-Discharge Compensation**
- **Supports Battery Capacities Above 65 Ahr**
- **Supports Charge and Discharge Currents Above 32 A**
- **External NTC Thermistor Support**
- **Supports Two-Wire I²C™ and HDQ Single-Wire Communication Interfaces with Host System**
- **SHA-1, HMAC Authentication**
- **One- or Four-LED Direct Display Control**
- **Five-LED and Higher Display Through Port Expander**
- **Reduced Power Modes (Typical Battery Pack Operating Range Conditions)**
  - **Normal Operation: < 140 µA Average**
  - **Sleep: < 64 µA Average**
  - **Full Sleep: < 19 µA Average**
- **Package: 14-Pin TSSOP**

## APPLICATIONS

- **Light Electric Vehicles**
- **Power Tools**
- **Medical Instrumentation**
- **Uninterruptible Power Supplies (UPS)**
- **Mobile Radios**

## DESCRIPTION

The Texas Instruments bq34z110 is a fuel gauge solution that works independently of battery series-cell configurations, and supports Lead-Acid battery chemistries. Batteries from 4 V to 64 V can be supported through an external voltage translation circuit that can be controlled automatically to reduce system power consumption.

The bq34z110 device provides several interface options, including an I²C slave, an HDQ slave, one or four direct LEDs, and an Alert output pin. Additionally, the bq34z110 provides support for an external port expander for more than four LEDs.

**ORDERING INFORMATION**

| $T_A$ | PART NUMBER | PACKAGE (TSSOP) | TUBE | TAPE AND REEL |
|---|---|---|---|---|
| –40°C to 85°C | bq34z110PW or bq34z110PWR | 14-Pin | PW | PWR |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# PIN DETAILS

## PINOUT DIAGRAM

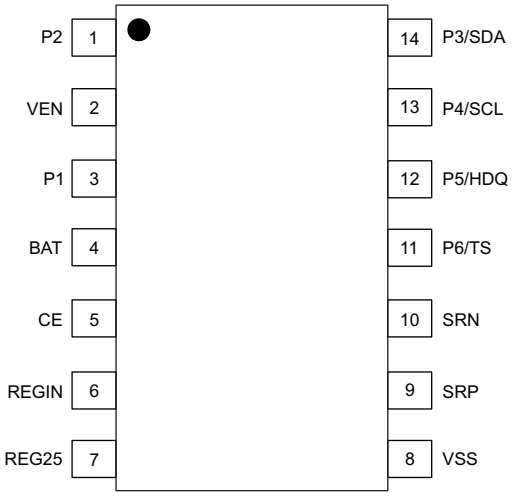


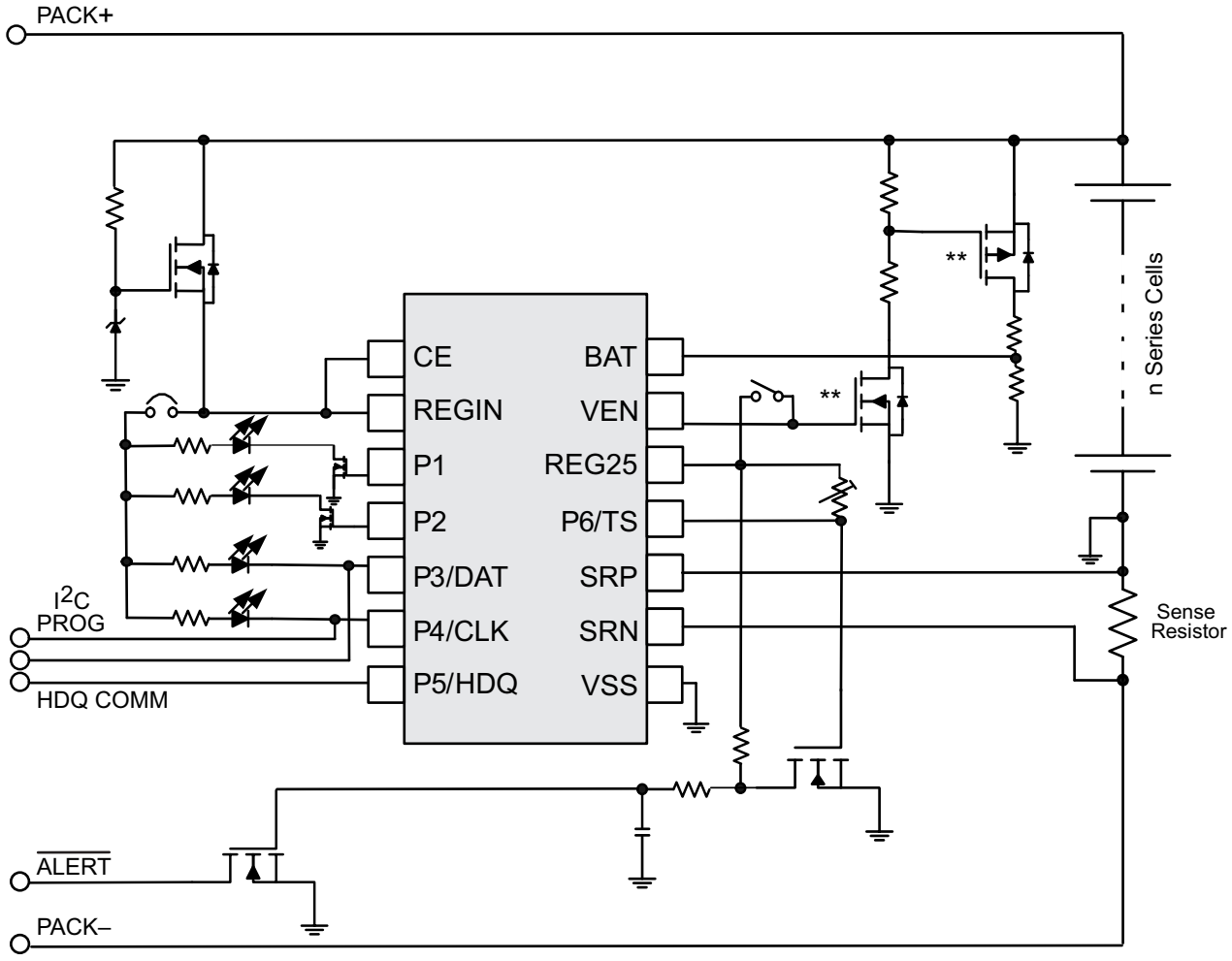

**Figure 1. bq34z110 Pinout Diagram**

**Table 1. bq34z110 External Pin Functions**

| PIN NAME | PIN NUMBER | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| P2 | 1 | O | LED 2 or Not Used (connect to Vss) |
| VEN | 2 | O | Active High Voltage Translation Enable. This signal is optionally used to switch the input voltage divider on/off to reduce the power consumption (typ 45 µA) of the divider network. |
| P1 | 3 | O | LED 1 or Not Used (connect to Vss). This pin is also used to drive an LED for single-LED mode. Use a small signal N-FET (Q1) in series with the LED as shown on Figure 9. |
| BAT | 4 | I | Translated Battery Voltage Input |
| CE | 5 | I | Chip Enable. Internal LDO is disconnected from REGIN when driven low. |
| REGIN | 6 | P | Internal integrated LDO input. Decouple with a 0.1-µF ceramic capacitor to Vss. |
| REG25 | 7 | P | 2.5-V Output voltage of the internal integrated LDO. Decouple with 1-µF ceramic capacitor to Vss. |
| VSS | 8 | P | Device ground |
| SRP | 9 | I | Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is nearest to the BAT– connection. |
| SRN | 10 | I | Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is nearest to the PACK– connection. |
| P6/TS | 11 | I | Pack thermistor voltage sense (use 103AT-type thermistor) |
| P5/HDQ | 12 | I/O | Open drain HDQ Serial communication line (slave) |
| P4/SCL | 13 | I | Slave $I^2C$ serial communication clock input. Use with a 10-K pull-up resistor (typical). Also used for LED 4 in the four-LED mode. |
| P3/SDA | 14 | I/O | Open drain slave $I^2C$ serial communication data line. Use with a 10-kΩ pull-up resistor (typical). Also used for LED 3 in the four-LED mode. |

(1) I = Input, O = Output, P = Power, I/O = Digital input/output

### TYPICAL IMPLEMENTATION




** optional to reduce divider power consumption

**Figure 2. bq34z110 Typical Implementation**

## THERMAL INFORMATION

| THERMAL METRIC(1) | | bq34z110 | UNITS |
|---|---|---|---|
| | | TSSOP (14-Pins) | |
| $\theta_{JA, High K}$ | Junction-to-ambient thermal resistance | 103.8 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 31.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 46.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 45.9 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{REGIN}$ | Regulator Input Range | –0.3 | 5.5 | V |
| $V_{CC}$ | Supply Voltage Range | –0.3 | 2.75 | V |
| $V_{IOD}$ | Open-drain I/O pins (SDA, SCL, HDQ) | –0.3 | 5.5 | V |
| $V_{BAT}$ | Bat Input pin | –0.3 | 5.5 | V |
| $V_I$ | Input Voltage range to all other pins (P1, P2, SRP, SRN) | –0.3 | VCC + 0.3 | V |
| ESD | Human-body model (HBM), BAT pin | | 1.5 | kV |
| | Human-body model (HBM), all other pins | | 2 | kV |
| $T_A$ | Operating free-air temperature range | –40 | 85 | °C |
| $T_F$ | Functional temperature range | –40 | 100 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

$T_A$ = 25ºC, $C_{LDO25}$ = 1 µF, and $V_{REGIN}$ = 3.6 V (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REGIN}$ | Supply Voltage | No operating restrictions | 2.7 | | 4.5 | V |
| | | No FLASH writes | 2.45 | | 2.7 | V |
| $C_{REGIN}$ | External input capacitor for internal LDO between REGIN and VSS | Nominal capacitor values specified. Recommend a 10% ceramic X5R type capacitor located close to the device. | | 0.1 | | µF |
| $C_{LDO25}$ | External output capacitor for internal LDO between VCC and VSS | | 0.47 | 1 | | µF |
| $I_{CC}$ | Normal operating-mode current | Gas Gauge in NORMAL mode, $I_{LOAD}$ > ***Sleep Current*** | | 140 | | µA |
| $I_{SLP}$ | SLEEP operating-mode current | Gas Gauge in SLEEP mode, $I_{LOAD}$ < Sleep Current | | 64 | | µA |
| $I_{SLP+}$ | FULL SLEEP operating-mode current | Gas Gauge in FULL SLEEP mode, $I_{LOAD}$ < ***Sleep Current*** | | 19 | | µA |
| $V_{OL}$ | Output voltage, low (SCL, SDA, HDQ) | $I_{OL}$ = 3 mA | | | 0.4 | V |
| $V_{OH(PP)}$ | Output voltage, high | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | | | V |
| $V_{OH(OD)}$ | Output voltage, high (SDA, SCL, HDQ) | External pull-up resistor connected to $V_{CC}$ | $V_{CC}$ – 0.5 | | | V |
| $V_{IL}$ | Input voltage, low | | –0.3 | | 0.6 | V |
| $V_{IH(OD)}$ | Input voltage, high (SDA, SCL, HDQ) | | 1.2 | | 6 | V |
| $V_{A1}$ | Input voltage range (TS) | | VSS – 0.05 | | 1 | V |
| $V_{A2}$ | Input voltage range (BAT) | | VSS – 0.125 | | 5 | V |
| $V_{A3}$ | Input voltage range (SRP, SRN) | | VSS – 0.125 | | 0.125 | V |
| $I_{LKG}$ | Input leakage current (I/O pins) | | | | 0.3 | µA |
| $t_{PUCD}$ | Power-up communication delay | | | 250 | | ms |

## POWER-ON RESET

$T_A$ = –40°C to 85°C; Typical Values at TA = 25°C and $V_{REGIN}$ = 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going battery voltage input at REG25 | | 2.05 | 2.20 | 2.31 | V |
| $V_{HYS}$ | Power-on reset hysteresis | | 45 | 115 | 185 | mV |

## LDO REGULATOR

$T_A$ = 25°C, $C_{LDO25}$ = 1 µF, $V_{REGIN}$ = 3.6 V (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REG25}$ | Regulator output voltage | 2.7 V ≤ $V_{REGIN}$ ≤ 4.5 V, $I_{OUT}$ ≤ 16 mA | $T_A$= –40°C to 85°C | 2.3 | 2.5 | 2.7 | V |
| | | 2.45 V ≤ $V_{REGIN}$ < 2.7 V (low battery), $I_{OUT}$ ≤ 3 mA | $T_A$ = –40°C to 85°C | 2.3 | | | |
| $I_{SHORT}$(2) | Short Circuit Current Limit | $V_{REG25}$ = 0 V | $T_A$ = –40°C to 85°C | | | 250 | mA |

(1) LDO output current, I, is the sum of internal and external load currents.
(2) Specified by design. Not production tested.

## INTERNAL TEMPERATURE SENSOR CHARACTERISTICS

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $G_{TEMP}$ | Temperature sensor voltage gain | | | –2 | | mV/°C |

## LOW-FREQUENCY OSCILLATOR

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(LOSC)}$ | Operating frequency | | | 32.768 | | kHz |
| $f_{(LEIO)}$ | Frequency error(1)(2) | $T_A$ = 0°C to 60°C | –1.5% | 0.25% | 1.5% | |
| | | $T_A$ = –20°C to 70°C | –2.5% | 0.25% | 2.5% | |
| | | $T_A$ = –40°C to 85°C | –4% | 0.25% | 4% | |
| $t_{(LSXO)}$ | Start-up time(2) | | | 500 | | µs |

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5 V, $T_A$ = 25°C.
(2) The startup time is defined as the time it takes for the frequency error is measured from 32.768 kHz.

## HIGH-FREQUENCY OSCILLATOR

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(OSC)}$ | Operating frequency | | | 8.389 | | MHz |
| $f_{(EIO)}$ | Frequency error(1) | $T_A$ = 0°C to 60°C | –2% | 0.38% | 2% | |
| | | $T_A$ = –20°C to 70°C | –3% | 0.38% | 3% | |
| | | $T_A$ = –40°C to 85°C | –4.5% | 0.38% | 4.5% | |
| $t_{(SXO)}$ | Start-up time(2) | | | 2.5 | 5 | ms |

(1) The frequency drift is included and measured from the trimmed frequency at $V_{CC}$ = 2.5 V, $T_A$ = 25°C.
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

## INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(SR)}$ | Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$ | $V_{(SR)}$ = $V_{(SRN)}$ – $V_{(SRP)}$ | –0.125 | | 0.125 | V |
| $t_{SR\_CONV}$ | Conversion time | Single conversion | | 1 | | s |
| | Resolution | | 14 | | 15 | bits |

## INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS (continued)

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OS(SR)}$ | Input offset | | | 10 | | µV |
| $I_{NL}$ | Integral nonlinearity error | | | ±0.007 | ±0.034 | % FSR |
| $Z_{IN(SR)}$ | Effective input resistance(1) | | 2.5 | | | MΩ |
| $I_{lkg(SR)}$ | Input leakage current(1) | | | | 0.3 | µA |

(1) Specified by design. Not tested in production.

## ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN(ADC)}$ | Input voltage range | | 0.05 | | 1 | V |
| $t_{ADC\_CONV}$ | Conversion time | | | | 125 | ms |
| | Resolution | | 14 | | 15 | bits |
| $V_{OS(ADC)}$ | Input offset | | | 1 | | mV |
| $Z_{ADC1}$ | Effective input resistance (TS)(1) | | 8 | | | MΩ |
| $Z_{ADC2}$ | Effective input resistance (BAT)(1) | bq34z110 not measuring cell voltage | 8 | | | MΩ |
| | | bq34z110 measuring cell voltage | | 100 | | KΩ |
| $I_{lkg(ADC)}$ | Input leakage current(1) | | | | 0.3 | µA |

(1) Specified by design. Not tested in production.

## DATA FLASH MEMORY CHARACTERISTICS

$T_A$ = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at $T_A$ = 25°C and REG25 = 2.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DR}$ | Data retention(1) | | 10 | | | Years |
| | Flash-programming write cycles(1) | | 20,000 | | | Cycles |
| $t_{WORDPROG}$ | Word programming time(1) | | | | 2 | ms |
| $I_{CCPROG}$ | Flash-write supply current(1) | | | 5 | 10 | mA |

(1) Specified by design. Not tested in production.

## HDQ COMMUNICATION TIMING CHARACTERISTICS

$T_A$ = –40°C to 85°C, $C_{REG}$ = 0.47 µF, 2.45 V < $V_{REGIN}$ = $V_{BAT}$ < 5.5 V; typical values at $T_A$ = 25°C and $V_{REGIN}$ = $V_{BAT}$ = 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(CYCH)}$ | Cycle time, host to bq34z110 | | 190 | | | µs |
| $t_{(CYCD)}$ | Cycle time, bq34z110 to host | | 190 | 205 | 250 | µs |
| $t_{(HW1)}$ | Host sends 1 to bq34z110 | | 0.5 | | 50 | µs |
| $t_{(DW1)}$ | bq34z110 sends 1 to host | | 32 | | 50 | µs |
| $t_{(HW0)}$ | Host sends 0 to bq34z110 | | 86 | | 145 | µs |
| $t_{(DW0)}$ | bq34z110 sends 0 to host | | 80 | | 145 | µs |
| $t_{(RSPS)}$ | Response time, bq34z110 to host | | 190 | | 950 | µs |
| $t_{(B)}$ | Break time | | 190 | | | µs |
| $t_{(BR)}$ | Break recovery time | | 40 | | | µs |
| $t_{(RISE)}$ | HDQ line rising time to logic 1 (1.2 V) | | | | 950 | ns |
| $t_{(RST)}$ | HDQ Reset | | 1.8 | | 2.2 | s |

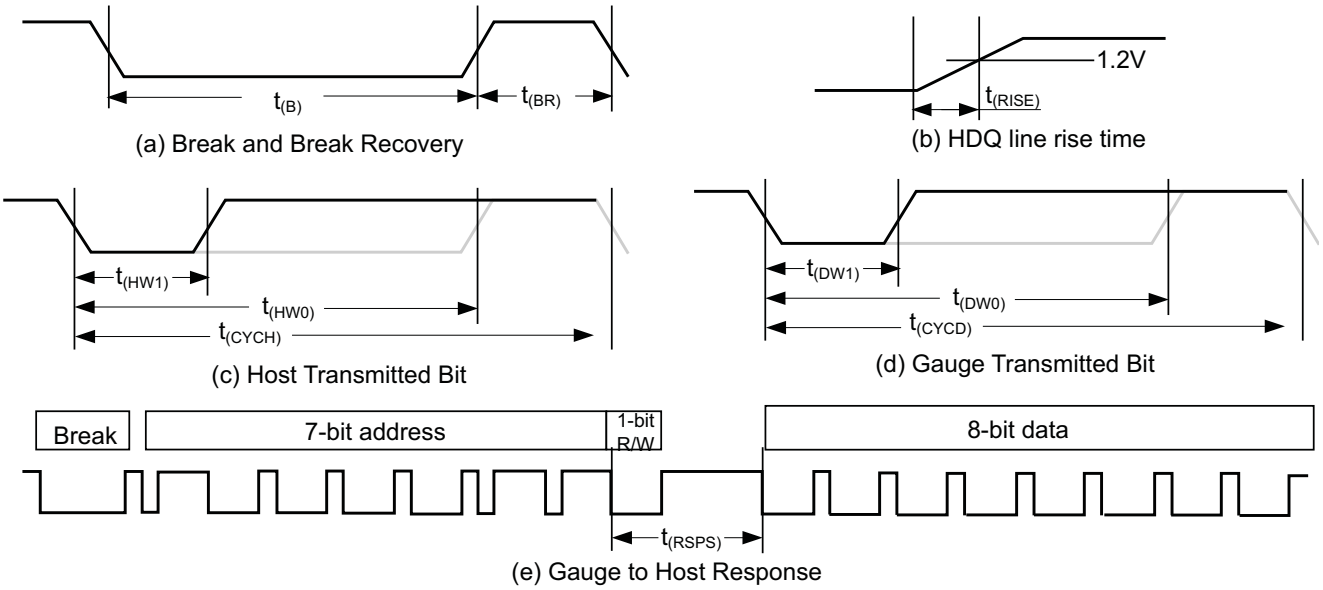



**Figure 3. Timing Diagrams**

## I²C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS

$T_A$ = –40°C to 85°C, $C_{REG}$ = 0.47 µF, 2.45 V < $V_{REGIN}$ = $V_{BAT}$ < 5.5 V; typical values at $T_A$ = 25°C and $V_{REGIN}$ = $V_{BAT}$ = 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | SCL/SDA rise time | | | | 300 | ns |
| $t_f$ | SCL/SDA fall time | | | | 300 | ns |
| $t_{w(H)}$ | SCL pulse width (high) | | 600 | | | ns |
| $t_{w(L)}$ | SCL pulse width (low) | | 1.3 | | | µs |
| $t_{su(STA)}$ | Setup for repeated start | | 600 | | | ns |
| $t_{d(STA)}$ | Start to first falling edge of SCL | | 600 | | | ns |
| $t_{su(DAT)}$ | Data setup time | | 100 | | | ns |
| $t_{h(DAT)}$ | Data hold time | | 0 | | | ns |
| $t_{su(STOP)}$ | Setup time for stop | | 600 | | | ns |
| $t_{BUF}$ | Bus free time between stop and start | | 66 | | | µs |
| $f_{SCL}$ | Clock frequency | | | | 400 | kHz |

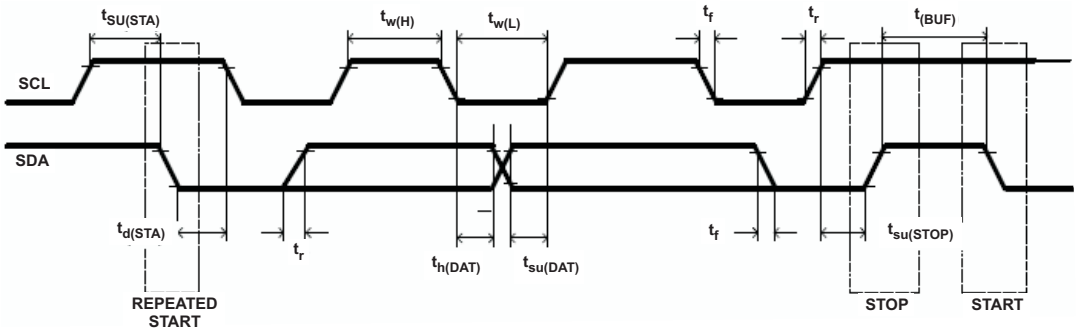



**Figure 4. I²C-Compatible Interface Timing Diagrams**

## GENERAL DESCRIPTION

The bq34z110 accurately predicts the battery capacity and other operational characteristics of multiple rechargeable cells blocks, which are voltage balanced when resting. It supports lead-acid chemistries. It can be interrogated by a host processor to provide cell information, such as Remaining Capacity, Full Charge Capacity, and Average Current.

Information is accessed through a series of commands, called Standard Commands. Further capabilities are provided by the additional Extended Commands set. Both sets of commands, indicated by the general format *Command()*, are used to read and write information contained within the bq34z110 device's control and status registers, as well as its data flash locations. Commands are sent from host to gauge using the bq34z110 serial communications engines, HDQ, and $I^2C$, and can be executed during application development, pack manufacture, or end-equipment operation.

Cell information is stored in the bq34z110 in non-volatile flash memory. Many of these data flash locations are accessible during application development and pack manufacture. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the bq34z110 device's companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The bq34z110 provides 32 bytes of user-programmable data flash memory. This data space is accessed through a data flash interface. For specifics on accessing the data flash, refer to DATA FLASH INTERFACE.

The key to the bq34z110 device's high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track algorithm. This algorithm uses voltage measurements, characteristics, and properties to create state-of-charge predictions that can achieve accuracy with as little as 1% error across a wide variety of operating conditions.

The bq34z110 measures charge and discharge activity by monitoring the voltage across a small-value series sense resistor connected in the low side of the battery circuit. When an application's load is applied, cell impedance is measured by comparing its Open Circuit Voltage (OCV) with its measured voltage under loading conditions.

The bq34z110 can use an NTC thermistor (default is Semitec 103AT or Mitsubishi BN35-3H103FB-50) for temperature measurement, or can also be configured to use its internal temperature sensor. The bq34z110 uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

To minimize power consumption, the bq34z110 has three power modes: NORMAL, SLEEP, and FULL SLEEP. The bq34z110 passes automatically between these modes, depending upon the occurrence of specific events.

Multiple modes are available for configuring from one to 16 LEDs as an indicator of remaining state of charge. More than four LEDs require the use of one or two inexpensive SN74HC164 shift register expanders.

A SHA-1 or HMAC-based battery pack authentication feature is also implemented on the bq34z110. When the IC is in UNSEALED mode, authentication keys can be (re)assigned. Alternatively, keys can also be programmed permanently in secure memory by Texas Instruments. A scratch pad area is used to receive challenge information from a host and to export SHA-1/HMAC encrypted responses. See the AUTHENTICATION section for further details.

**NOTE**

Formatting conventions in this document:

Commands: *italic* with parentheses and no breaking spaces, e.g. *RemainingCapacity()*.

Data Flash: *italic*, **bold**, and breaking spaces, e.g. ***Design Capacity***.

Register Bits and Flags: brackets only, e.g. [TDA] Data

Flash Bits: *italic* and **bold**, e.g. ***[LED1]***

Modes and states: ALL CAPITALS, e.g. UNSEALED mode.

# DATA COMMANDS

## STANDARD DATA COMMANDS

The bq34z110 uses a series of 2-byte standard commands to enable host reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in Table 2. Because each command consists of two bytes of data, two consecutive HDQ or $I^2C$ transmissions must be executed both to initiate the command function and to read or write the corresponding two bytes of data. Standard commands are accessible in NORMAL operation. Also, two block commands are available to read Manufacturer Name and Device Chemistry. Read and Write permissions depend on the active access mode.

**Table 2. Standard Commands**

| NAME | | COMMAND CODE | UNITS | SEALED ACCESS | UNSEALED ACCESS |
|---|---|---|---|---|---|
| *Control()* | CNTL | 0x00/0x01 | N/A | R/W | R/W |
| *StateOfCharge()* | SOC | 0x02/0x03 | % | R | R |
| *RemainingCapacity()* | RM | 0x04/0x05 | mAh | R | R |
| *FullChargeCapacity()* | FCC | 0x06/0x07 | mAh | R | R |
| *Voltage()* | VOLT | 0x08/0x09 | mV | R | R |
| *AverageCurrent()* | AI | 0x0a/0x0b | mA | R | R |
| *Temperature()* | TEMP | 0x0c/0x0d | 0.1ºK | R | R |
| *Flags()* | FLAGS | 0x0e/0x0f | N/A | R | R |
| *Mfr Date* | DATE | 0x6B/0x6c | N/A | R | R |
| *Mfr Name Length* | NAMEL | 0x6d | N/A | R | R |
| *Mfr Name* | NAME | 0x6e–0x78 | N/A | R | R |
| *Device Chemistry Length* | CHEML | 0x79 | N/A | R | R |
| *Device Chemistry* | CHEM | 0x7a–0x7d | N/A | R | R |
| *Serial Number* | SERNUM | 0x7e/0x7f | N/A | R | R |

### Control(): 0x00/0x01

Issuing a *Control()* command requires a subsequent two-byte sub-command. These additional bytes specify the particular control function desired. The *Control()* command allows the host to control specific features of the bq34z110 during normal operation, and additional features when the bq34z110 is in different access modes, as described in Table 3.

**Table 3. Control() Subcommands**

| CNTL FUNCTION | CNTL DATA | SEALED ACCESS | DESCRIPTION |
|---|---|---|---|
| CONTROL_STATUS | 0x0000 | Yes | Reports the status of DF Checksum, IT, for example. |
| DEVICE_TYPE | 0x0001 | Yes | Reports the device type of 0x0541 (indicating bq34z110) |
| FW_VERSION | 0x0002 | Yes | Reports the firmware version on the device type |
| HW_VERSION | 0x0003 | Yes | Reports the hardware version of the device type |
| RESET_DATA | 0x0005 | No | Returns reset data |
| PREV_MACWRITE | 0x0007 | No | Returns previous MAC command code |
| CHEM_ID | 0x0008 | Yes | Reports the chemical identifier of the Impedance Track configuration |
| BOARD_OFFSET | 0x0009 | No | Forces the device to measure and store the board offset |
| CC_OFFSET | 0x000A | No | Forces the device to measure the internal CC offset |
| CC_OFFSET_SAVE | 0x000B | No | Forces the device to store the internal CC offset |
| DF_VERSION | 0x000C | Yes | Reports the data flash version on the device |
| SET_FULLSLEEP | 0x0010 | No | Sets the [FULLSLEEP] bit in the control register to 1 |
| STATIC_CHEM_CHKSUM | 0x0017 | Yes | Calculates chemistry checksum |

**Table 3. Control() Subcommands (continued)**

| CNTL FUNCTION | CNTL DATA | SEALED ACCESS | DESCRIPTION |
|---|---|---|---|
| CURRENT | 0x0018 | Yes | Returns the instantaneous current measured by the gauge |
| SEALED | 0x0020 | No | Places the device in SEALED access mode |
| IT_ENABLE | 0x0021 | No | Enables the Impedance Track algorithm |
| CAL_ENABLE | 0x002D | No | Toggles calibration mode |
| RESET | 0x0041 | No | Forces a full reset of the bq34z110 |
| EXIT_CAL | 0x0080 | No | Exits calibration mode |
| ENTER_CAL | 0x0081 | No | Enters calibration mode |
| OFFSET_CAL | 0x0082 | No | Reports internal CC offset in calibration mode |

## CONTROL_STATUS: 0x0000

Instructs the fuel gauge to return status information to Control addresses 0x00/0x01. The status word includes the following information.

**Table 4. CONTROL_STATUS Flags**

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| High Byte | — | FAS | SS | CALMODE | CCA | BCA | CSV | — |
| Low Byte | — | — | FULLSLEEP | SLEEP | LDMD | RUP_DIS | VOK | QEN |

**FAS:** Status bit that indicates the bq34z110 is in FULL ACCESS SEALED state. Active when set.

**SS:** Status bit that indicates the bq34z110 is in the SEALED State. Active when set.

**CSV:** Status bit that indicates a valid data flash checksum has been generated. Active when set.

**CALMODE:** Status bit that indicates the bq34z110 calibration function is active. True when set. Default is 0.

**CCA:** Status bit that indicates the bq34z110 Coulomb Counter Calibration routine is active. Active when set.

**BCA:** Status bit that indicates the bq34z110 Board Calibration routine is active. Active when set.

**FULLSLEEP:** Status bit that indicates the bq34z110 is in FULLSLEEP mode. True when set. The state can only be detected by monitoring the power used by the bq34z110 because any communication will automatically clear it.

**SLEEP:** Status bit that indicates the bq34z110 is in SLEEP mode. True when set.

**LDMD:** Status bit that indicates the bq34z110 Impedance Track algorithm using constant-power mode. True when set. Default is 0 (constant-current mode).

**RUP_DIS:** Status bit that indicates the bq34z110 Ra table updates are disabled. True when set.

**VOK:** Status bit that indicates cell voltages are OK for Qmax updates. True when set.

**QEN:** Status bit that indicates the bq34z110 Qmax updates are enabled. True when set.

## DEVICE TYPE: 0x0001

Instructs the fuel gauge to return the device type to addresses 0x00/0x01.

## FW_VERSION: 0x0002

Instructs the fuel gauge to return the firmware version to addresses 0x00/0x01.

## HW_VERSION: 0x0003

Instructs the fuel gauge to return the hardware version to addresses 0x00/0x01.

### RESET_DATA: 0x0005

Instructs the fuel gauge to return the number of resets performed to addresses 0x00/0x01.

### PREV_MACWRITE: 0x0007

Instructs the fuel gauge to return the previous command written to addresses 0x00/0x01. The value returned is limited to less than 0x0020.

### CHEM ID: 0x0008

Instructs the fuel gauge to return the chemical identifier for the Impedance Track configuration to addresses 0x00/0x01.

### BOARD_OFFSET: 0x0009

Instructs the fuel gauge to calibrate board offset. During board offset calibration the [BCA] bit is set.

### CC_OFFSET: 0x000A

Instructs the fuel gauge to calibrate the coulomb counter offset. During calibration the [CCA] bit is set.

### CC_OFFSET_SAVE: 0x000B

Instructs the fuel gauge to save calibrate the coulomb counter offset after calibration.

### DF_VERSION: 0x000C

Instructs the fuel gauge to return the data flash version to addresses 0x00/0x01.

### SET_FULLSLEEP: 0x0010

Instructs the fuel gauge to set the FULLSLEEP bit in Control Status register to 1. This allows the gauge to enter the FULLSLEEP power mode after the transition to SLEEP power state is detected. In FULLSLEEP mode less power is consumed by disabling an oscillator circuit used by the communication engines. For HDQ communication one host message will be dropped. For $I^2C$ communications, the first $I^2C$ message will incur a 6 ms–8 ms clock stretch while the oscillator is started and stabilized. A communication to the device in FULLSLEEP will force the part back to the SLEEP mode.

### STATIC_CHEM_DF_CHKSUM: 0x0017

Instructs the fuel gauge to calculate chemistry checksum as a 16-bit unsigned integer sum of all static chemistry data. The most significant bit (MSB) of the checksum is masked yielding a 15-bit checksum. This checksum is compared with the value stored in the data flash Static Chem DF Checksum. If the value matches, the MSB is cleared to indicate pass. If it does not match, the MSB is set to indicate failure.

### SEALED: 0x0020

Instructs the fuel gauge to transition from UNSEALED state to SEALED state. The fuel gauge should always be set to SEALED state for use in customer's end equipment.

### IT ENABLE: 0x0021

Forces the fuel gauge to begin the Impedance Track algorithm, sets bit 2 of UpdateStatus and causes the [VOK] and [QEN] flags to be set in the CONTROL STATUS register. [VOK] is cleared if the voltages are not suitable for a Qmax update. Once set, [QEN] cannot be cleared. This command is only available when the fuel gauge is UNSEALED and is typically enabled at the last step of production after system test is completed.

### RESET: 0x0041

Instructs the fuel gauge to perform a full reset. This command is only available when the fuel gauge is UNSEALED.

### EXIT_CAL: 0x0080

Instructs the fuel gauge to exit calibration mode.

### ENTER_CAL: 0x0081

Instructs the fuel gauge to enter calibration mode.

### OFFSET_CAL: 0x0082

Instructs the fuel gauge to perform offset calibration.

### StateOfCharge(): 0x02 and 0x03

This read-only function returns an unsigned integer value of the predicted remaining battery capacity expressed as a percentage of *FullChargeCapacity()*, with a range of 0 to 100%.

### RemainingCapacity(): 0x04 and 0x05

This read-only command pair returns the compensated battery capacity remaining. Units are 1 mAh per bit.

### FullChargeCapacity(): 0x06 and 07

This read-only command pair returns the compensated capacity of the battery when fully charged. Units are 1 mAh per bit except if X10 mode is selected. In X10 mode, units are 10 mAh per bit. *FullChargeCapacity()* is updated at regular intervals, as specified by the Impedance Track algorithm.

### Voltage(): 0x08 and 0x09

This read-word function returns an unsigned integer value of the measured cell-pack voltage in mV with a range of 0 V to 65535 mV.

### AverageCurrent(): 0x0a and 0x0b

This read-only command pair returns a signed integer value that is the average current flow through the sense resistor. It is updated every 1 second. Units are 1 mA per bit except if X10 mode is selected. In X10 mode, units are 10 mA per bit.

### Temperature(): 0x0c and 0x0d

This read-word function returns an unsigned integer value of the temperature in units of 0.1ºK measured by the gas gauge and has a range of 0 to 6553.5 ºK. The source of the measured temperature is configured by the *[TEMPS]* bit in the Pack Configuration register (see EXTENDED DATA COMMANDS).

**Table 5. Temperature Sensor Selection**

| TEMPS | Temperature() Source |
|---|---|
| 0 | Internal Temperature Sensor |
| 1 | TS Input (default) |

### Flags(): 0x0e/0x0f

This read-word function returns the contents of the gas-gauge status register, depicting current operation status.

**Table 6. Flags Bit Definitions**

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| High Byte | OTC | OTD | BATHIGH | BATLOW | CHG_INH | RSVD | FC | CHG |
| Low Byte | OCVTAKEN | ISD | TDD | RSVD | RSVD | SOC1 | SOCF | DSG |

**OTC:** Over-Temperature in Charge condition is detected. True when set. OTD = Over-Temperature in Discharge condition is detected. True when set.

**BATHIGH:** Battery High bit that indicates a high battery voltage condition. Refer to the data flash ***BATTERY HIGH*** parameters for threshold settings.

**BATLOW:** Battery Low bit that indicates a low battery voltage condition. Refer to the data flash ***BATTERY LOW*** parameters for threshold settings.

**CHG_INH:** Charge Inhibit: unable to begin charging ***[Charge Inhibit Temp Low, Charge Inhibit Temp High]***. True when set.

**RSVD:** Reserved.

**FC:** Full-charge is detected. FC is set when charge termination is reached and FC Set% = –1 (see CHARGING AND CHARGE TERMINATION INDICATION for details) or State of Charge is larger than ***FC SET%*** and ***FC Set%*** is not –1. True when set.

**CHG:** (Fast) charging allowed. True when set.

**OCVTAKEN:** Cleared on entry to relax mode and set to 1 when OCV measurement is performed in relax mode.

**ISD:** Internal Short is detected. True when set. TDD = Tab Disconnect is detected. True when set.

**SOC1:** State-of-Charge Threshold 1 reached. True when set.

**SOCF:** State-of-Charge Threshold Final reached. True when set.

**DSG:** Discharging detected. True when set.

## DATA FLASH INTERFACE

### ACCESSING DATA FLASH

The bq34z110 data flash is a non-volatile memory that contains bq34z110 initialization, default, cell status, calibration, configuration, and user information. The data flash can be accessed in several different ways, depending on what mode the bq34z110 is operating in and what data is being accessed.

Commonly accessed data flash memory locations, frequently read by a host, are conveniently accessed through specific instructions (described in DATA COMMANDS). These commands are available when the bq34z110 is either in UNSEALED or SEALED modes.

Most data flash locations, however, can only accessible in UNSEALED mode by use of the bq34z110 evaluation software or by data flash block transfers. These locations should be optimized and/or fixed during the development and manufacture processes. They become part of a Golden Image File and can then be written to multiple battery packs. Once established, the values generally remain unchanged during end-equipment operation.

To access data flash locations individually, the block containing the desired data flash location(s) must be transferred to the command register locations, where they can be read to the host or changed directly. This is accomplished by sending the set-up command *BlockDataControl()* (code 0x61) with data 0x00. Up to 32 bytes of data can be read directly from the *BlockData()* command locations 0x40…0x5f, externally altered, then re-written to the *BlockData()* command space. Alternatively, specific locations can be read, altered, and re-written if their corresponding offsets are used to index into the *BlockData()* command space. Finally, the data residing in the command space is transferred to data flash, once the correct checksum for the whole block is written to *BlockDataChecksum()* (command number 0x60).

Occasionally, a data flash CLASS will be larger than the 32-byte block size. In this case, the *DataFlashBlock()* command is used to designate which 32-byte block the desired locations reside in. The correct command address is then given by 0x40 + offset modulo 32. For example, to access ***Terminate Voltage*** in the Gas Gauging class, *DataFlashClass()* is issued 80 (0x50) to set the class. Because the offset is 48, it must reside in the second 32-byte block. Hence, *DataFlashBlock()* is issued 0x01 to set the block offset, and the offset used to index into the *BlockData()* memory area is 0x40 + 48 *modulo* 32 = 0x40 + 16 = 0x40 + 0X10 = 0x50.

Reading and writing subclass data are block operations 32 bytes in length. Data can be written in shorter block sizes, however. Blocks can be shorter than 32 bytes in length. Writing these blocks back to data flash does not overwrite data that extend beyond the actual block length.

None of the data written to memory are bounded by the bq34z110—the values are not rejected by the gas gauge. Writing an incorrect value may result in hardware failure due to firmware program interpretation of the invalid data. The data written is persistent, so a Power-On Reset does resolve the fault.

### MANUFACTURER INFORMATION BLOCK

The bq34z110 contains 32 bytes of user programmable data flash storage: ***Manufacturer Info Block***. The method for accessing these memory locations is slightly different, depending on whether the device is in UNSEALED or SEALED modes.

When in UNSEALED mode and when and 0x00 has been written to *BlockDataControl()*, accessing the Manufacturer Info Block is identical to accessing general data flash locations. First, a *DataFlashClass()* command is used to set the subclass, then a *DataFlashBlock()* command sets the offset for the first data flash address within the subclass. The *BlockData()* command codes contain the referenced data flash data. When writing the data flash, a checksum is expected to be received by *BlockDataChecksum()*. Only when the checksum is received and verified is the data actually written to data flash.

As an example, the data flash location for ***Manufacturer Info Block*** is defined as having a Subclass = 58 and an Offset = 0 through 31 (32 byte block). The specification of Class = System Data is not needed to address Manufacturer Info Block, but is used instead for grouping purposes when viewing data flash info in the bq34z110 evaluation software.

When in SEALED mode or when 0x01 *BlockDataControl()* does not contain 0x00, data flash is no longer available in the manner used in UNSEALED mode. Rather than issuing subclass information, a designated ***Manufacturer Information Block*** is selected with the *DataFlashBlock()* command. Issuing a 0x01, 0x02, or 0x03 with this command causes the corresponding information block (A, B, or C, respectively) to be transferred to the command space 0x40…0x5f for editing or reading by the host. Upon successful writing of checksum information to *BlockDataChecksum()*, the modified block is returned to data flash.

**NOTE**

Manufacturer Info Block A is “read only” when in SEALED mode.

### ACCESS MODES

The bq34z110 provides three security modes which control data flash access permissions according to Table 7. Public Access refers to those data flash locations, specified in Table 20 that are accessible to the user. Private Access refers to reserved data flash locations used by the bq34z110 system. Care should be taken to avoid writing to Private data flash locations when performing block writes in Full Access mode by following the method outlined in ACCESSING DATA FLASH.

**Table 7. Data Flash Access**

| Security Mode | DF: Public Access | DF: Private Access |
|---|---|---|
| BOOTROM | N/A | N/A |
| FULL ACCESS | R/W | R/W |
| UNSEALED | R/W | R/W |
| SEALED | R | N/A |

Although FULL ACCESS and UNSEALED modes appear identical, FULL ACCESS mode allows the bq34z110 to directly transition to BOOTROM mode and also write access keys. The UNSEALED mode lacks these abilities.

### SEALING AND UNSEALING DATA FLASH ACCESS

The bq34z110 implements a key-access scheme to transition between SEALED, UNSEALED, and FULL-ACCESS modes. Each transition requires that a unique set of two keys be sent to the bq34z110 via the *Control()* command (these keys are unrelated to the keys used for SHA-1/HMAC authentication). The keys must be sent consecutively, with no other data being written to the *Control()* register in between. Note that to avoid conflict, the keys must be different from the codes presented in the CNTL DATA column of Table 3 subcommands.

When in SEALED mode the [SS] bit of *Control Status()* is set, but when the UNSEAL keys are correctly received by the bq34z110, the [SS] bit is cleared. When the full access keys are correctly received then the *Flags() [FAS]* bit is cleared.

Both the sets of keys for each level are 2 bytes each in length and are stored in data flash. The UNSEAL key (stored at ***Unseal Key 0*** and ***Unseal Key 1***) and the FULL-ACCESS key (stored at *Full Access Key 0* and ***Full Access Key 1***) can only be updated when in FULL-ACCESS mode. The order of the bytes entered through the *Control()* command is the reverse of what is read from the part. For example, if the 1st and 2nd word of the UnSeal Key 0 returns 0x1234 and 0x5678, then *Control()* should supply 0x3412 and 0x7856 to unseal the part.

# FUNCTIONAL DESCRIPTION

## FUEL GAUGING

The bq34z110 measures the cell voltage, temperature, and current to determine the battery SOC based in the Impedance Track algorithm (refer to the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application report [SLUA450] for more information). The bq34z110 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in-series with the cell. By integrating charge passing through the battery, the cell's SOC is adjusted during battery charge or discharge.

The total battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When an application load is applied, the impedance of the cell is measured by comparing the OCV obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and Chemical Capacity (Qmax). The initial *Qmax* value is taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. The parallel value is also used for the value programmed in ***Design Capacity***. The bq34z110 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the *Qmax* value, to determine *FullChargeCapacity()* and *StateOfCharge()*, specifically for the present load and temperature. *FullChargeCapacity()* is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage()* reaches the ***Terminate Voltage***. *NominalAvailableCapacity()* and *FullAvailableCapacity()* are the uncompensated (no or light load) versions of *RemainingCapacity()* and *FullChargeCapacity()*, respectively.

The bq34z110 has two flags accessed by the *Flags()* function that warns when the battery's SOC has fallen to critical levels. When *RemainingCapacity()* falls below the first capacity threshold, specified in ***SOC1 Set Threshold***, the *[SOC1]* (State of Charge Initial) flag is set. The flag is cleared once *RemainingCapacity()* rises above ***SOC1 Clear Threshold***. All units are in mAh.

When *RemainingCapacity()* falls below the second capacity threshold, ***SOCF Set Threshold***, the *[SOCF] (State of Charge Final)* flag is set, serving as a final discharge warning. If ***SOCF Set Threshold*** = –1, the flag is inoperative during discharge. Similarly, when *RemainingCapacity()* rises above ***SOCF Clear Threshold*** and the [SOCF] flag has already been set, the *[SOCF]* flag is cleared. All units are in mAh.

The bq34z110 has two additional flags accessed by the *Flags()* function that warn of internal battery conditions. The fuel gauge monitors the cell voltage during relaxed conditions to determine if an internal short has been detected When this condition occurs, [ISD] will be set. The bq34z110 also has the capability of detecting when a tab has been disconnected in a 2-cell parallel system by actively monitoring the state of health. When this condition occurs, [TDD] is set.

Lead-Acid gauging in the charge direction makes use of four *Charge Efficiency* factors to correct for energy lost due to heat. Lead-Acid charge efficiency is not linear throughout the charging process, as it drops with increasing state of charge.

## IMPEDANCE TRACK VARIABLES

The bq34z110 has several data flash variables that permit the user to customize the Impedance Track algorithm for optimized performance. These variables are dependent upon the power characteristics of the application as well as the cell itself.

### Load Mode

***Load Mode*** is used to select either the constant current or constant power model for the Impedance Track algorithm as used in ***Load Select***. See the Load Select section. When ***Load Mode*** is 0, the *Constant Current Model* is used (default). When Load Mode is 1, the *Constant Power Model* is used. The [LDMD] bit of CONTROL_STATUS reflects the status of Load Mode.

### Load Select

***Load Select*** defines the type of power or current model to be used to compute load-compensated capacity in the Impedance Track algorithm. If ***Load Mode*** = 0 (Constant Current) then the options presented in Table 8 are available.

**Table 8. Current Model Used when Load Mode = 0**

| Load Select Value | Current Model Used |
|---|---|
| 0 | Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register. |
| 1 (default) | Present average discharge current: This is the average discharge current from the beginning of this discharge cycle until present time. |
| 2 | Average Current: based on the *AverageCurrent()* |
| 3 | Current: based on a low-pass-filtered version of *AverageCurrent()* (τ=14s) |
| 4 | Design Capacity / 5: C Rate based off of Design Capacity /5 or a C / 5 rate in mA. |
| 5 | Use the value specified by *AtRate()* |
| 6 | Use the value in ***User_Rate-mA***: This gives a completely user configurable method. |

If ***Load Mode*** = 1 *(Constant Power)* then the following options are available:

**Table 9. Constant-Power Model Used when Load Mode = 1**

| Load Select Value | Power Model Used |
|---|---|
| 0 (default) | Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register. |
| 1 | Present average discharge power: This is the average discharge power from the beginning of this discharge cycle until present time. |
| 2 | Average Current × Voltage: based off the *AverageCurrent()* and *Voltage()*. |
| 3 | Current × Voltage: based on a low-pass-filtered version of *AverageCurrent()* (τ=14s) and *Voltage()* |
| 4 | Design Energy / 5: C Rate based off of Design Energy /5 or a C / 5 rate in mA . |
| 5 | Use whatever value specified by *AtRate()*. |
| 6 | Use the value in ***User_Rate-mW/cW***. This gives a completely user-configurable method. |

### *Reserve Cap-mAh*

***Reserve Cap-mAh*** determines how much actual remaining capacity exists after reaching 0 *RemainingCapacity()*, before ***Terminate Voltage*** is reached. A loaded rate or no-load rate of compensation can be selected for Reserve Cap by setting the [RESCAP] bit in the Pack Configuration register.

### *Reserve Cap-mWh/cWh*

***Reserve Cap-mWh*** determines how much actual remaining capacity exists after reaching 0 *AvailableEnergy()*, before ***Terminate Voltage*** is reached. A loaded rate or no-load rate of compensation can be selected for Reserve Cap by setting the [RESCAP] bit in the Pack Configuration register.

### *Design Energy Scale*

***Design Energy Scale*** is used to select the scale/unit of a set of data flash parameters. The value of ***Design Energy Scale*** can be either 1 or 10 only.

When using Design Energy Scale = 10, the value for each of the parameters in Table 10 must be adjusted to reflect the new units. See X10 MODE.

**Table 10. Data Flash Parameter Scale/Unit-Based on Design Energy Scale**

| Data Flash Parameter | Design Energy Scale = 1 (default) | Design Energy Scale = 10 |
|---|---|---|
| Design Energy | mWh | cWh |
| Reserve Energy-mWh/cWh | mWh | cWh |
| Avg Power Last Run | mW | cW |
| User Rate-mW/cW | mWh | cWh |
| T Rise | No Scale | Scaled by X10 |

### *Dsg Current Threshold*

This register is used as a threshold by many functions in the bq34z110 to determine if actual discharge current is flowing into or out of the cell. The default for this register should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

### *Chg Current Threshold*

This register is used as a threshold by many functions in the bq34z110 to determine if actual charge current is flowing into or out of the cell. The default for this register should be sufficient for most applications. This threshold should be set low enough to be below any normal charge current but high enough to prevent noise or drift from affecting the measurement.

### *Quit Current, Dsg Relax Time, Chg Relax Time, and Quit Relax Time*

The ***Quit Current*** is used as part of the Impedance Track algorithm to determine when the bq34z110 enters relaxation mode from a current flowing mode in either the charge direction or the discharge direction. The value of Quit Current is set to a default value that should be above the standby current of the host system.

Either of the following criteria must be met to enter relaxation mode:

1. |*AverageCurrent()*| < |***Quit Current***| for Dsg Relax Time.
2. |*AverageCurrent()*| > |***Quit Current***| for Chg Relax Time.

   After about 6 minutes in relaxation mode, the bq34z110 attempts to take accurate OCV readings. An additional requirement of dV/dt < 4 µV/s is required for the bq34z110 to perform Qmax updates. These updates are used in the Impedance Track algorithms. It is critical that the battery voltage be relaxed during OCV readings to and that the current is not higher than C/20 when attempting to go into relaxation mode.

   ***Quit Relax Time*** specifies the minimum time required for *AverageCurrent()* to remain above the QuitCurrent threshold before exiting relaxation mode.

### *Qmax*

***Qmax Cell 0*** contains the maximum chemical capacity of the cell and is determined by comparing states of charge before and after applying the load with the amount of charge passed. It also corresponds to capacity at low rate of discharge such as C/20 rate. For high accuracy, this value is periodically updated by the bq34z110 during operation.

Based on the battery cell capacity information, the initial value of chemical capacity should be entered in the ***Qmax Cell 0*** data flash parameter. The Impedance Track algorithm will update this value and maintain it internally in the gauge.

### *Update Status*

The Update Status register indicates the status of the Impedance Track algorithm.

**Table 11. Update Status Definitions**

| Update Status | Status |
|---|---|
| 0x02 | Qmax and Ra data are learned, but Impedance Track is not enabled. This should be the standard setting for a Golden Image File. |
| 0x04 | Impedance Track is enabled but Qmax and Ra data are not yet learned. |
| 0x05 | Impedance Track is enabled and only Qmax has been updated during a learning cycle. |
| 0x06 | Impedance Track is enabled. Qmax and Ra data are learned after a successful learning cycle. This should be the operation setting for end equipment. |

This register should only be updated by the bq34z110 during a learning cycle or when *IT_ENABLE()* subcommand is received. Refer to STEP 8: Run an Optimization Cycle.

### *Avg I Last Run*

The bq34z110 logs the current averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register. This register should never need to be modified. It is only updated by the bq34z110 when required.

### *Avg P Last Run*

The bq34z110 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading the bq34z110 continuously multiplies instantaneous current times *Voltage()* to get power. It then logs this data to derive the average power. This register should never need to be modified. It is only updated by the bq34z110 when the required.

### *Delta Voltage*

The bq34z110 stores the maximum difference of *Voltage()* during short load spikes and normal load, so the Impedance Track algorithm can calculate remaining capacity for pulsed loads. It is not recommended to change this value.

### *The Ra Tables*

This data is automatically updated during device operation. No user changes should be made except for reading the values from another pre-learned pack for creating Golden Image Files. Profiles have format *Cell0 R_a M*, where M is the number that indicates the state of charge to which the value corresponds.

## CHARGE EFFICIENCY

Tracking State of Charge during the charge phase is relatively easy with modern chemistries such as Lithium-Ion, where essentially none of the applied energy from the charger is lost to heat. However, lead-acid chemistries may demonstrate significant losses to heat during charging. Therefore, to more accurately track state of charge and Time-to-Full during the charge phase, the bq34z110 uses four charge-efficiency factors to compensate for charge acceptance. These factors are ***Charge Efficiency***, ***Charge Efficiency Reduction Rate***, ***Charge Efficiency Drop Off***, and ***Charge Efficiency Temperature Compensation***.

The bq34z110 applies the ***Charge Efficiency***, when RelativeStateOfCharge() is less than the value coded in ***Charge Efficiency Drop Off***. When RelativeStateOfCharge() is greater than or equal to the value coded in ***Charge Efficiency Drop Off***, ***Charge Efficiency*** and ***Charge Efficiency Reduction Rate*** determine the charge efficiency rate. ***Charge Efficiency Reduction Rate*** defines the percent efficiency reduction per percentage point of RelativeStateOfCharge() over ***Charge Efficiency Drop Off***. Note that the ***Charge Efficiency Reduction Rate*** has units of 0.1%.

The bq34z110 also adjusts the efficiency factors for temperature. ***Charge Efficiency Temperature Compensation*** defines the percent efficiency reduction per degree C over 25°C. Note that ***Charge Efficiency Temperature Compensation*** has units of 0.01%.

Applying the four factors:

Effective Charge Efficiency % = ***Charge Efficiency*** – ***Charge Efficiency Reduction Rate*** [RSOC() – ***Charge Efficiency Drop Off***] - ***Charge Efficiency Temperature Compensation*** [Temperature – 25°C]

Where:

RSOC() ≥ ***Charge Efficiency*** and Temperature ≥ 25°C

## PACK CONFIGURATION REGISTER

Some bq34z110 pins are configured via the ***Pack Configuration*** data flash register, as indicated in Table 12. This register is programmed/read via the methods described in ACCESSING DATA FLASH. The register is located at subclass = 64, offset = 0.

**Table 12. Pack Configuration Register Bits**

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| High Byte | RESCAP | CALEN | RSVD | RSVD | VOLTSEL | IWAKE | RSNS1 | RSNS0 |
| Low Byte | X10 | RESFACTSTEP | SLEEP | RMFCC | RSVD | RSVD | RSVD | TEMPS |

**RESCAP:** No-load rate of compensation is applied to the reserve capacity calculation. True when set. Default is 0.

**CALEN:** When enabled, entering calibration mode is permitted. For special use only. Default = 0.

**RSVD:** Reserved. Default = 0.

**VOLTSEL:** This bit selects between use of internal or external battery voltage divider. The internal divider is for single cell use only. 1 = external. 0 = internal. Default is 0.

**IWAKE/RSNS1/RSNS0:** These bits configure the current wake function (see Table 16). Default is 0/0/1.

**X10:** X10 Capacity and/or Current bit. The mA, mAh, and cWh settings and reports will take on a value of ten times normal. This setting has no actual effect within the gauge. It is the responsibility of the host to reinterpret the reported values. X10 current measurement is achieved by calibrating the current measurement to a value X10 lower than actual.

**RESFACTSTEP:** Enables Ra step up/down to Max/Min Res Factor before disabling Ra updates. Default is 1.

**SLEEP:** The fuel gauge can enter sleep, if operating conditions allow. True when set. Default is 1.

**RMFCC:** RM is updated with the value from FCC, on valid charge termination. True when set. Default is 1.

**RSVD:** Reserved. Do not use.

**TEMPS:** Selects external thermistor for *Temperature()* measurements. True when set. Uses internal temp when clear. Default is 1

## TEMPERATURE MEASUREMENT

The bq34z110 can measure temperature via the on-chip temperature sensor or via the TS input depending on the setting of the [TEMPS] bit *PackConfiguration()*. The bit is set by using the *PackConfiguration()* function, described in EXTENDED DATA COMMANDS.

Temperature measurements are made by calling the *Temperature()* function (see STANDARD DATA COMMANDS for specific information).

When an external thermistor is used, REG25 (pin 7) is used to bias the thermistor and TS (pin 11) is used to measure the thermistor voltage (a pull-down circuit is implemented inside the bq34z110). The bq34z110 then correlates the voltage to temperature, assuming the thermistor is a Semitec 103AT or similar device.

## OVERTEMPERATURE INDICATION

### Overtemperature: Charge

If during charging, *Temperature()* reaches the threshold of *DF:OT Chg* for a period of ***OT Chg Time*** and *AverageCurrent()* > ***Chg Current Threshold***, then the *[OTC]* bit of *Flags()* is set. Note: if *OT Chg Time* = 0 then feature is completely disabled.

When *Temperature()* falls to ***OT Chg Recovery***, the *[OTC]* of *Flags()* is reset.

### Overtemperature: Discharge

If, during discharging, *Temperature()* reaches the threshold of *OT Dsg* for a period of OT Dsg Time, and *AverageCurrent()* ≤ –Dsg Current Threshold, then the [OTD] bit of *Flags()* is set.

**NOTE**

If *OT Dsg Time* = 0, then the feature is completely disabled.

When *Temperature()* falls to OT Dsg Recovery, the *[OTD]* bit of *Flags()* is reset.

### CHARGING AND CHARGE TERMINATION INDICATION

For proper bq34z110 operation, the battery charging voltage must be specified by the user. The default value for this variable is ***Charging Voltage*** = 4200 mV. This parameter should be set to the recommended charging voltage for the entire battery stack.

The bq34z110 detects charge termination when (1) during two consecutive periods of *Current Taper Window*, the *AverageCurrent()* is < ***Taper Current*** and (2) during the same periods, the accumulated change in capacity > 0.25 mAh /***Taper Current Window*** and (3) *Voltage()* > ***Charging Voltage - Charging Taper Voltage***. When this occurs, the [CHG] bit of *Flags()* is cleared. Also, if the *[RMFCC]* bit of Pack Configuration is set, and *RemainingCapacity()* is set equal to *FullChargeCapacity()*.

### X10 MODE

The bq34z110 supports high current and high capacity batteries above 32.76 Amperes and 32.76 Ampere-Hours by switching to a times-ten mode where currents and capacities are internally handled correctly, but various reported units and configuration quantities are rescaled to tens of milliamps and tens of milliamp-hours. The need for this is due to the standardization of a two byte data command having a maximum representation of ±32767. When the X10 bit (Bit 7) is set in the Pack Configuration register, all of the mAh, cWh, and mWh settings will take on a value of ten times normal. When this bit is set, the actual units for all capacity and energy parameters will be 10 mAh or Wh. This includes reporting of Remaining Capacity. This bit will also be used to rescale the current reporting to 10 times normal, up to ±327 A. The actual resolution then becomes 10 mA.

It is important to know that setting the X10 flag does not actually change anything in the operation of the gauge. It serves as a notice to the host that the various reported values should be reinterpreted ten times higher. X10 Current measurement is achieved by calibrating the current gain to a value X10 lower than actually applied. Because the flag has no actual effect, it can be used to represent other scaling values. See Design Energy Scale.

### REMAINING STATE OF CHARGE LED INDICATION

The bq34z110 supports multiple options for using one to sixteen LEDs as an output device to display the remaining state of charge. The LED/Comm Configuration register determines the behavior.

**Table 13. LED/COMM Configuration Bits**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| XLED3 | XLED2 | XLED1 | XLED0 | LEDON | Mode2 | Mode1 | Mode0 |

Bits 0, 1, 2 are a code for one of five modes. 0 = No LED, 1 = Single LED, 2 = Four LEDs, 3 = External LEDs with $I^2C$ comm, 4 = External LEDs with HDQ comm.

Setting Bit 3, LEDON, will cause the LED display to be always on, except in Single LED mode. When clear (default), the LED pattern will only be displayed after holding an LED display button for one to two seconds. The button applies 2.5 V from REG25 pin 7 to VEN pin 2 (refer to ). The ***LED Hold Time*** parameter may be used to configure how long the LED display remains on if LEDON is clear. ***LED Hold Time*** configures the update interval for the LED display if LEDON is set.

Bits 4, 5, 6, and 7 are a binary code for number of external LEDs. Code 0 is reserved. Codes 1 through 15 represents 2~16 external LEDs. So, number of External LEDs is 1 + Value of the 4-bit binary code. Display of Remaining Capacity is evenly divided among the selected number of LEDs.

Upon detecting A/D value representing 2.5 V on VEN pin, Single LED mode toggles the LED as duty cycle on within a period of one second. So, for example 10% RSOC will have the LED on for 100 ms and off for 900 ms. 90% RSOC has the LED on for 900 ms and off for 100 ms. Any value >90% displays as 90%.

Upon detecting A/D value representing 2.5 V on VEN pin, Four-LED mode will display the RSOC by driving pins RC2(LED1), RC0(LED2), RA1(LED3),RA2(LED4) in a proportional manner where each LED represents 25% of the remaining state of charge. For example, if RSOC = 67%, three LEDs will be illuminated.

Upon detecting A/D value representing 2.5 V on the VEN pin, External LED mode will transmit the RSOC into an SN74HC164 (for 2~8 LEDs) or two SN74HC164 devices (for 9 to approximately 16 LEDs) using a bit-banged approach with RC2 as Clock and RC0 as Data (see Figure 9). LEDs are lit for number of seconds as defined in a data flash parameter. See the *SN54HC164, SN74HC164 8-Bit Parallel-Out Serial Shift Registers Data Sheet* (SCLS115E) for detail on these devices.

Extended commands are available to turn the LEDs on and off for test purposes.

### ALERT SIGNAL

Based on the selected LED mode, various options are available for the hardware implementation of an Alert signal. Software configuration of the Alert Configuration register determines which alert conditions will assert the Alert pin.

**Table 14. Alert Signal Pins**

| Mode | Description | Alert Pin | Alert Pin Name | Config Register Hex Code | Comment |
|---|---|---|---|---|---|
| 0 | No LED | 1 | P2 | 0 | |
| 1 | Single LED | 1 | P2 | 1 | |
| 2 | 4 LED | 11 | P6 | 2 | Filter and FETs are required to eliminate temperature sense pulses (see Figure 9). |
| 3 | 5-LED Expander with $I^2C$ Host Comm | 12 | P5 | 43 | |
| 3 | 10-LED Expander with $I^2C$ Host Comm | 12 | P5 | 93 | |
| 4 | 5-LED Expander with HDQ Host Comm | 13 | P4 | 44 | |
| 4 | 10-LED Expander with HDQ Host Comm | 13 | P4 | 94 | |

The port used for the Alert output depends on the mode setting in ***LED/Comm Configuration*** as defined in Table 14. The default mode is 0. The Alert pin will be asserted by driving LOW. However, note that in LED/COM mode 2, pin TS/P6, which has a dual purpose as temperature sense pin will be driven low except when temperature measurements are made each second. Refer to the reference schematic for filter implementation details if host alert sensing requires a continuous signal.

The Alert pin will be a logical OR of the selected bits in the new configuration register when asserted in the Flags register. Default value for Alert Configuration register is 0.

**Table 15. Alert Configuration Register Bit Definitions**

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| High Byte | OTC | OTD | BATHIGH | BATLOW | CHG_INH | RSVD | FC | CHG |
| Low Byte | RSVD | ISD | TDD | RSVD | RSVD | SOC1 | SOCF | DSG |

**OTC:** Overtemperature in Charge condition is detected. Alert enabled when set.

**OTD:** Overtemperature in Discharge condition is detected. Alert enabled when set.

**BATHIGH:** Battery High bit that indicates a high battery voltage condition. Refer to the data flash ***BATTERY HIGH*** parameters for threshold settings. Alert enabled when set.

**BATLOW:** Battery Low bit that indicates a low battery voltage condition. Refer to the data flash ***BATTERY LOW*** parameters for threshold settings. Alert enabled when set.

**CHG_INH:** Charge Inhibit: unable to begin charging ***[Charge Inhibit Temp Low, Charge Inhibit Temp High]***. Alert enabled when set.

**RSVD:** Reserved. Do not use.

**FC:** Full-charge is detected. FC is set when charge termination is reached and ***FC Set%*** = –1 (see CHARGING AND CHARGE TERMINATION INDICATION for details) or State of Charge is larger than ***FC Set%*** and ***FC Set%*** is not –1. Alert enabled when set.

**CHG:** (Fast) charging allowed. Alert enabled when set.

**RSVD:** Reserved. Do not use.

**ISD:** Internal Short is detected. Alert enabled when set.

**TDD:** Tab Disconnect is detected. Alert enabled when set.

**SOC1:** State-of-Charge Threshold 1 reached. Alert enabled when set.

**SOCF:** State-of-Charge Threshold Final reached. Alert enabled when set.

**DSG:** Discharging detected. Alert enabled when set.

## POWER MODES

The bq34z110 has three power modes: NORMAL mode, SLEEP mode, and FULLSLEEP mode.

- In NORMAL mode, the bq34z110 is fully powered and can execute any allowable task.
- In SLEEP mode, the gas gauge exists in a reduced-power state, periodically taking measurements and performing calculations.
- In FULLSLEEP mode, the high frequency oscillator is turned off, and power consumption is further reduced compared to SLEEP mode.

### NORMAL Mode

The gas gauge is in NORMAL mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()* and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

### SLEEP Mode

SLEEP mode is entered automatically if the feature is enabled (***Pack Configuration [SLEEP]*** = 1) and *Average Current()* is below the programmable level *Sleep Current*. Once entry to sleep has been qualified but prior to entry to SLEEP mode, the bq34z110 performs an ADC autocalibration to minimize offset. Entry to SLEEP mode can be disabled by the *[SLEEP]* bit of *Pack Configuration()*, where 0 = disabled and 1 = enabled. During SLEEP mode, the bq34z110 periodically wakes to take data measurements and updates the data set, after which it then returns directly to SLEEP. The bq34z110 exits SLEEP if any entry condition is broken, a change in protection status occurs, or a current in excess of $I_{WAKE}$ through $R_{SENSE}$ is detected.

### FULLSLEEP Mode

FULLSLEEP mode is entered automatically when the bq34z110 is in SLEEP mode and the timer counts down to 0 (*Full Sleep Wait Time* > 0). FULLSLEEP mode is disabled when *Full Sleep Wait Time* is set to 0.

During FULLSLEEP mode, the bq34z110 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The gauge exits the FULLSLEEP mode when there is any communication activity. Therefore, the execution of SET_FULLSLEEP sets *[FULLSLEEP]* bit, but the EVSW might still display the bit clear. The FULLSLEEP mode can be verified by measuring the current consumption of the gauge. In this mode, the high frequency oscillator is turned off. The power consumption is further reduced compared to the SLEEP mode.

While in FULLSLEEP mode, the fuel gauge can suspend serial communications as much as 4 ms by holding the communication line(s) low. This delay is necessary to correctly process host communication since the fuel gauge processor is mostly halted. For HDQ communication one host message will be dropped.

# POWER CONTROL

## RESET FUNCTIONS

When the bq34z110 detects either a hardware or software reset (/MRST pin driven low or the *[RESET]* bit of *Control()* initiated, respectively), it determines the type of reset and increments the corresponding counter. This information is accessible by issuing the command *Control()* function with the RESET_DATA subcommand.

As shown in Figure 5, if a partial reset was detected, a RAM checksum is generated and compared against the previously stored checksum. If the checksum values do not match, the RAM is reinitialized (a “Full Reset”). The stored checksum is updated every time RAM is altered.

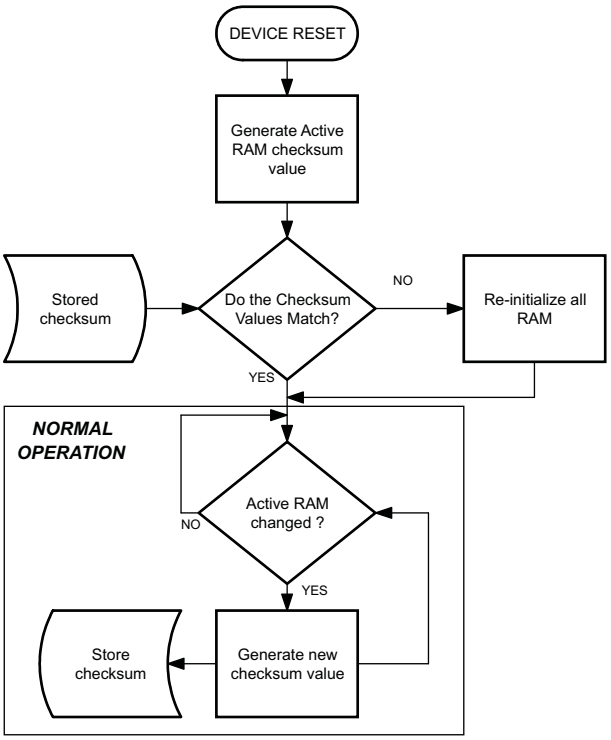



**Figure 5. Partial Reset Flow Diagram**

## WAKE-UP COMPARATOR

The wake up comparator is used to indicate a change in cell current while the bq34z110 is in SLEEP mode. *PackConfiguration()* uses bits [RSNS1–RSNS0] to set the sense resistor selection. *PackConfiguration()* uses the [IWAKE] bit to select one of two possible voltage threshold ranges for the given sense resistor selection. An internal interrupt is generated when the threshold is breached in either charge or discharge directions. A setting of 0x00 of RSNS1..0 disables this feature.

**Table 16. $I_{WAKE}$ t = Threshold Settings(1)**

| RSNS1 | RSNS0 | $I_{WAKE}$ | $V_{th}$ (SRP–SRN) |
|---|---|---|---|
| 0 | 0 | 0 | Disabled |
| 0 | 0 | 1 | Disabled |
| 0 | 1 | 0 | +1.25 mV or –1.25 mV |
| 0 | 1 | 1 | +2.5 mV or –2.5 mV |
| 1 | 0 | 0 | +2.5 mV or –2.5 mV |
| 1 | 0 | 1 | +5 mV or –5 mV |
| 1 | 1 | 0 | +5 mV or –5 mV |
| 1 | 1 | 1 | +10 mV or –10 mV |

(1) The actual resistance value vs. the setting of the sense resistor is not important just the actual voltage threshold when calculating the configuration.

## FLASH UPDATES

Data flash can only be updated if *Voltage()* ≥ *Flash Update OK Voltage*. Flash programming current can cause an increase in LDO dropout. The value of *Flash Update OK Voltage* should be selected such that the bq34z110 Vcc voltage does not fall below its minimum of 2.4 V during Flash write operations. The default value of 2800 mV is appropriate.

## VOLTAGE DIVISION AND CALIBRATION

The bq34z110 is shipped with factory configuration for the default case of 2-series lead-acid cell. This can be changed by setting the number of series cells in the data flash configuration section.

Multi-cell applications, with voltages up to 65535 mV may be gauged by using the appropriate input scaling resistors such that the maximum battery voltage, under all conditions, appears at the BAT input as approximately 900 mV. The actual gain function is determined by a calibration process and the resulting voltage calibration factor is stored in the data flash location ***Voltage Divider***.

For two-cell applications, an external divider network is not required. Inside the IC, behind the BAT pin is a nominal 5:1 voltage divider with 88 KΩ in the top leg and 22 KΩ in the bottom leg. This internal divider network is enabled by clearing the VOLTSEL bit in the Pack Configuration register. This ratio is optimum for directly measuring a dual cell lead-acid cell where charge voltage is limited to 5 V max.

For higher voltage applications, an external resistor divider network should be implemented as per the reference designs in this document. The quality of the divider resistors is very important to avoid gauging errors over time and temperature. It is recommended to use 0.1% resistors with 25 ppm temperature coefficient. Alternately, a matched network could be used that tracks its dividing ratio with temperature and age due to the similar geometry of each element. Calculation of the series resistor can be made per the equation below. Note that exceeding **$V_{IN}$ max mV** results in a measurement with degraded linearity.

The bottom leg of the divider resistor should be in the range of 15 KΩ to 25 KΩ. Assuming the use of 16.5 KΩ:

**Rseries = 16500 Ω ($V_{IN}$ max mV – 900 mV) / 900 mV**

For all applications, the ***Voltage Divider*** value in data flash is used by the firmware to calibrate the total divider ratio. The nominal value for this parameter is the maximum expected value for the stack voltage. The calibration routine adjusts the value to force the reported voltage to equal the actual applied voltage.

### 2S EXAMPLE

For stack voltages under 5 V max, it is not necessary to provide an external voltage divider network. The internal 5:1 divider should be selected by clearing the VOLTSEL bit in the Pack Configuration register. The default value for ***Voltage Divider*** is 5000 (representing the internal 5000:1000 mV divider) when no external divider resistor is used, and the default number of series cells = 2. In the 2S case, there is usually no requirement to calibrate the voltage measurement, since the internal divider is calibrated during factory test to within 2 mV.

### 6S EXAMPLE

In the multi-cell case, the hardware configuration is different. An external voltage divider network is calculated using the Rseries formula above. The bottom leg of the divider should be in the range of 15 KΩ to 25 KΩ. For more details on configuration, see DESIGN STEPS.

### AUTOCALIBRATION

The bq34z110 provides an autocalibration feature that will measure the voltage offset error across SRP and SRN from time-to-time as operating conditions change. It subtracts the resulting offset error from normal sense resistor voltage, $V_{SR}$, for maximum measurement accuracy.

The gas gauge performs a single offset calibration when (1) the interface lines stay low for a minimum of ***Bus Low Time*** and (2) Vsr > ***Deadband***.

The gas gauge also performs a single offset when (1) the condition of *AverageCurrent()* ≤ ***Autocal Min Current*** and (2) {voltage change since last offset calibration ≥ ***Delta Voltage***} or {temperature change since last offset calibration is greater than ***Delta Temperature*** for ≥ ***Autocal Time***}.

Capacity and current measurements should continue at the last measured rate during the offset calibration when these measurements cannot be performed. If the battery voltage drops more than ***Cal Abort*** during the offset calibration, the load current has likely increased considerably; hence, the offset calibration is aborted.

# COMMUNICATIONS

## AUTHENTICATION

The bq34z110 can act as a SHA-1 and HMAC authentication slave by using its internal engine. Sending a 160-bit SHA-1 challenge message to the bq34z110 causes the IC to return a 160-bit digest, based upon the challenge message and hidden plain-text authentication keys. When this digest matches an identical one, generated by a host or dedicated authentication master (operating on the same challenge message and using the same plain text keys), the authentication process is successful.

The bq34z110 contains a default plain-text authentication key of 0x0123456789ABCDEFFEDCBA987654321. If using the bq34z110 device's internal authentication engine, the default key can be used for development purposes, but should be changed to a secret key and the part immediately sealed, before putting a pack into operation.

## KEY PROGRAMMING

When the bq34z110 device's SHA-1 and HMAC internal engine is used, authentication keys are stored as plain-text in memory. A plain-text authentication key can only be written to the bq34z110 while the IC is in UNSEALED mode. Once the IC is UNSEALED, a 0x00 is written to *BlockDataControl()* to enable the authentication data commands. Next, subclass ID and offset are specified by writing 0x70 and 0x00 to *DataFlashClass()* and *DataFlashBlock()*, respectively. The bq34z110 is now prepared to receive the 16-byte plain-text key, which must begin at command location 0x4C. The key is accepted once a successful checksum has been written to *BlockDataChecksum()*, for the entire 32-byte block (0x40 through 0x5f), not just the 16-byte key.

## EXECUTING AN AUTHENTICATION QUERY

To execute an authentication query in UNSEALED mode, a host must first write 0x01 to the *BlockDataControl()* command, to enable the authentication data commands. If in SEALED mode, 0x00 must be written to *DataFlashBlock()*, instead.

Next, the host writes a 20-byte authentication challenge to the *AuthenticateData()* address locations (0x40 through 0x53). After a valid checksum for the challenge is written to *AuthenticateChecksum()*, the bq34z110 uses the challenge to perform it own the SHA-1/HMAC computation, in conjunction with its programmed keys. The resulting digest is written to *AuthenticateData()*, overwriting the pre-existing challenge. The host may then read this response and compare it against the result created by its own parallel computation.

## HDQ SINGLE-PIN SERIAL INTERFACE

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the bq34z110. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. Note that the DATA signal on pin 12 is open-drain and requires an external pull-up resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB Bit 7). The R/W field directs the bq34z110 either to

- Store the next 8 or 16 bits of data to a specified register or
- Output 8 or 16 bits of data from the specified register

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

The return-to-one data bit frame of HDQ consists of three distinct sections. The first section is used to start the transmission by either the host or by the bq34z110 taking the DATA pin to a logic-low state for a time $t_{STRH,B}$. The next section is for data transmission, where the data are valid for a time $t_{DSU}$, after the negative edge used to start communication. The data are held until a time $t_{DV}$, allowing the host or bq34z110 time to sample the data bit. The final section is used to stop the transmission by returning the DATA pin to a logic-high state by at least a time $t_{SSU}$, after the negative edge used to start communication. The final logic-high state is held until the end of $t_{CYCH,B}$, allowing time to ensure the transmission was stopped correctly. The timing for data and break communication is shown in HDQ COMMUNICATION TIMING CHARACTERISTICS.

HDQ serial communication is normally initiated by the host processor sending a break command to the bq34z110. A break is detected when the DATA pin is driven to a logic-low state for a time $t_B$ or greater. The DATA pin should then be returned to its normal ready high logic state for a time $t_{BR}$. The bq34z110 is now ready to receive information from the host processor.

The bq34z110 is shipped in the I²C mode. TI provides tools to enable the HDQ peripheral.

## I²C INTERFACE

The gas gauge supports the standard I²C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.

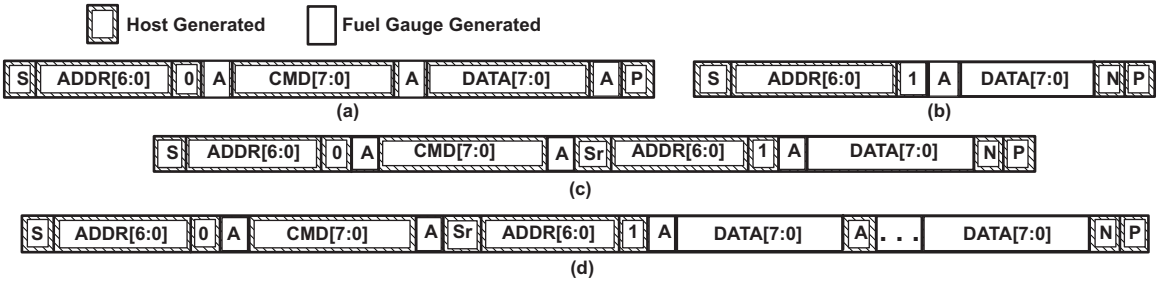



**Figure 6. Supported I²C formats: (a) 1-byte write, (b) quick read, ©) 1 byte-read, and (d) incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).**

The “quick read” returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the bq34z110 or the I²C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

Attempt to write a read-only address (NACK after data sent by master):


Attempt to read an address above 0x7F (NACK command):


Attempt at incremental writes (NACK all extra data bytes sent):


Incremental read at the maximum allowed read address:


The I²C engine releases both SDA and SCL if the I²C bus is held low for $t_{BUSERR}$. If the gas gauge was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power SLEEP mode.

## DESIGN STEPS

For additional design guidelines, see the *bq34z110EVM Wide Range Impedance Track Enabled Battery Fuel Gauge User's Guide* (SLUU904).

### STEP 1: Review and modify the Data Flash Configuration Data.

While many of the default parameters in the data flash will be suitable for most applications, the following should first be reviewed and modified to match the intended application.

- *Design Capacity*: Enter the value in mAh for the battery, even if you plan to treat your application from the "design energy" point of view.
- *Design Energy*: Enter the value in mWh.
- *Cell Charge Voltage Tx-Ty*: Enter the desired cell charge voltage for each JEITA temperature range.

### STEP 2: Review and modify the Data Flash Configuration Registers.

- *LED_Comm Configuration*: See Table 13 and Table 14 to aid in selection of an LED mode. Note that the pin used for the optional Alert signal is dependent upon the LED mode selected.
- *Alert Configuration*: See Table 15 to aid in selection of which faults will trigger the Alert pin.
- *Number of Series Cells*
- *Pack Configuration*: Ensure that the VOLSEL bit is set for multi-cell applications and cleared for single-cell applications.

### STEP 3: Design and Configure the Voltage Divider.

If the battery contains more than two series cells, a voltage divider network will be required. Design the divider network, based on the formula below. The voltage division required is from the highest expected battery voltage, down to approximately 900 mV. For example, using a lower leg resistor of 16.5 KΩ where the highest expected voltage is 32000 mV:

**Rseries = 16.5 KΩ (32000 mV – 900 mV) / 900 mV = 570.2 KΩ**

Based on price and availability, a 600 K resistor or pair of 300 K resistors could be used in the top leg along with a 16.5-K resistor in the bottom leg.

Set the *Voltage Divider* in the Data Flash Calibration section of the Evaluation Software to 32000 mV.

Use the Evaluation Software to calibrate to the applied nominal voltage, e.g.: 24000 mV. After calibration, a slightly different value will appear in the *Voltage Divider* parameter, which can be used as a default value for the project.

### STEP 4: Determine the Sense Resistor Value.

To ensure accurate current measurement, the input voltage generated across the current sense resistor should not exceed ±125 mV. For applications having high dynamic range, it is allowable to extend this range to absolute maximum of ±300 mV for overload conditions where a protector device will be taking independent protective action. In such an overloaded state, current reporting and gauging accuracy does not function correctly.

The value of the current sense resistor should be entered into both *CC Gain* and *CC Delta* parameters in the Data Flash Calibration section of the Evaluation Software.

### STEP 5: Review and Modify the Data Flash Gas Gauging Configuration, Data, and State.

- *Load Select*: See Table 8 and Table 9.
- *Load Mode*: See Table 8 and Table 9.
- *Cell Terminate Voltage*: This is the theoretical voltage where the system will begin to fail. It is defined as zero state of charge. Generally a more conservative level is used in order to have some reserve capacity. Note the value is for a single cell only.
- *Quit Current*: Generally should be set to a value slightly above the expected idle current of the system.
- *Qmax Cell 0*: Start with the C-rate value of your battery.

**STEP 6: Determine and Program the Chemical ID.**

Use the bqChem feature in the Evaluation Software to select and program the chemical ID matching your cell. If no match is found, use the procedure defined in TI's *Mathcad Chemistry Selection Tool* (SLUC138).

**STEP 7: Calibrate.**

Follow the steps on the Calibration screen in the Evaluation Software. Achieving the best possible calibration is important before moving on to STEP 8: Run an Optimization Cycle. For mass production, calibration is not required for single-cell applications. For multi-cell applications, only voltage calibration is required. Current and temperature may be calibrated to improve gauging accuracy if needed.

**STEP 8: Run an Optimization Cycle.**

1. Start with a fully charged and relaxed battery.
2. Temporarily Adjust the ***Cell BL Set Volt Threshold*** so as not to affect a full discharge.
3. Send the IT Enable command 0x21. The VOK and QEN flags should be set.
4. Discharge the battery at C/10 until the battery is empty.

**CAUTION**

It may be necessary to stop the load, check the rebound, then apply the load again to ensure that the rebounded voltage will not be significantly higher than the Cell Termination Voltage. For example, a Cell Termination Voltage of 1800 mV will be 10800 mV for a 12 V/six-cell battery. After stopping the load at 10500 mV, it can bounce all the way up to 11500 mV, which is too high for this procedure. However, if the load is continued until the battery voltage is 10000 mV, the resulting bounce back will be close to the intended termination voltage.

5. Allow the battery to relax. Wait for The OCV reading to be taken and the VOK flag to clear. The update status should now be set to 5.
6. Charge the battery until full. The VOK and QEN flags should be set during the charging operation.
7. Allow the battery to relax. The VOK flag will remain set.
8. Discharge the battery at C/10 until the battery is empty.
9. Allow the battery to relax. Wait for The OCV reading to be taken and the VOK flag to clear. The update status should now be set to 6.
10. Restore the ***Cell BL Set Volt Threshold*** to the desired value.

## APPLICATION SCHEMATICS

### 2-Cell Lead-Acid and 5-LED Display

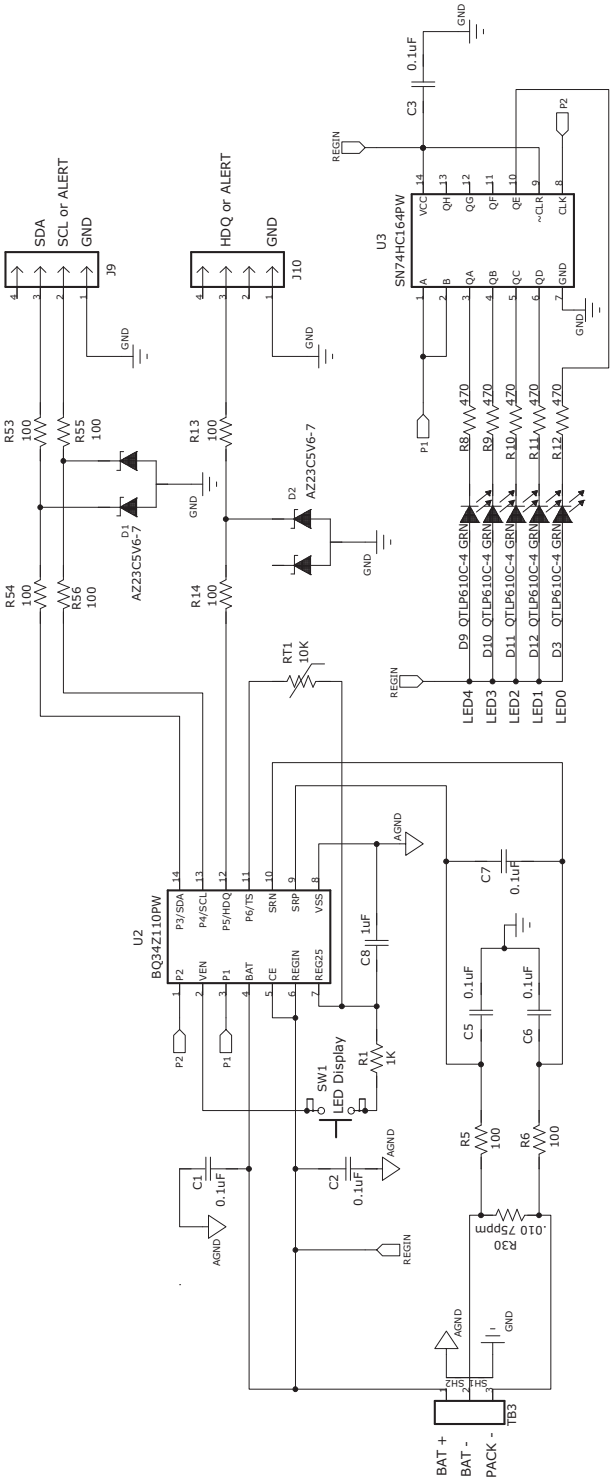



**Figure 7. 2-Cell Lead-Acid and 5-LED Display**

## Multi-Cell and 5-LED Display

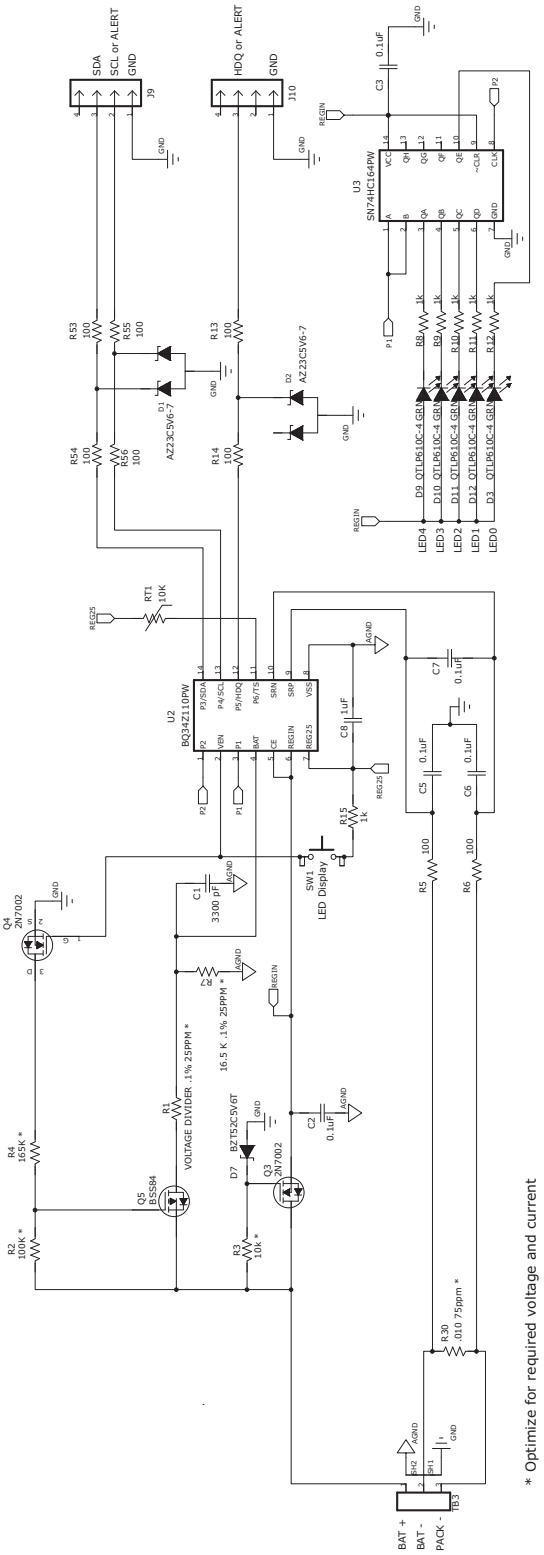



**Figure 8. Multi-Cell and 5-LED Display**

## Full-Featured Evaluation Module EVM

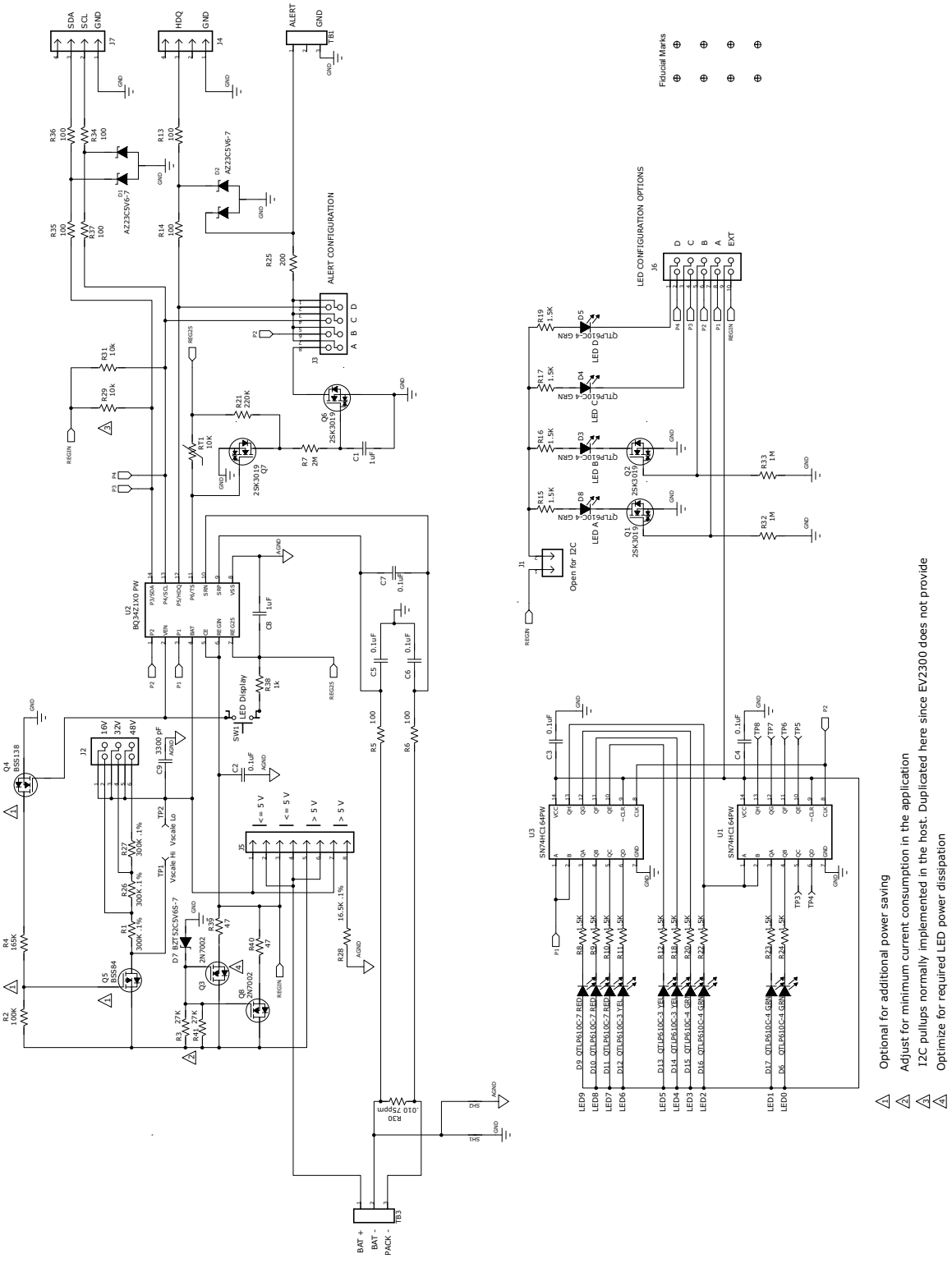



**Figure 9. Full-Featured Evaluation Module EVM**

## REFERENCE

### OPERATION CONFIGURATION B REGISTER

Some bq34z110 advanced features are rarely used. Operation Configuration registers B and C are available for configuring special applications. Default settings are recommended.

**Table 17. Operation Configuration B Bit Definition**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ChgDoDEoC | SE_TDD | VconsEN | SE_ISD | JEITA | LFPRelax | DoDWT | FConvEn |

**ChgDoDEoC:** Enable DoD at EoC during charging only. True when set. Default is 1. Default setting is recommended.

**SE_TDD:** Enable Tab Disconnection Detection. True when set. Default is 1.

**VconsEN:** Enable voltage consistency check. True when set. Default is 1. Default setting is recommended.

**SE_ISD:** Enable Internal Short Detection. True when set. Default is 1.

**JEITA:** Enable JEITA charge current and voltage settings based on temperature. True when set. Default is 1. When not set, values in T2–T3 ranges for charge current and voltage are used regardless of temperature.

**LFPRelax:** Enable LiFePO4 long RELAXATION mode when chemical ID 400 series is selected. True when set. Default is 1.

**DoDWT:** Enable Dod weighting for LiFePO4 support when chemical ID 400 series is selected. True when set. Default is 1.

**FConvEn:** Enable fast convergence algorithm. Default is 1. Default setting is recommended.

### OPERATION CONFIGURATION C REGISTER

**Table 18. Operation Configuration C Bit Definition**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| FastQmax | RsvdSBS | FF_Near_End | SleepWakeChg | RSVD | RSVD | RSVD | RSVD |

**FastQmax:** Enable Fast Qmax Update mode. True when set. Default is 0. Default setting is recommended.

**RsvdSBS**: Enable to activate debug information in command space 0x6d ~ 0x76. For special use only. Default setting is recommended.

**FF_Near_End**: Enable to use a fast voltage filter near the end of discharge only. Default setting is recommended.

**SleepWakeChg**: Enable for faster sampling in SLEEP mode. Default setting is recommended.

**RSVD:** Reserved. Default is 0.

### EXTENDED DATA COMMANDS

Extended commands offer additional functionality beyond the standard set of commands. They are used in the same manner; however unlike standard commands, extended commands are not limited to 2-byte words. The number of command bytes for a given extended command ranges in size from single to multiple bytes, as specified in Table 19. For details on the SEALED and UNSEALED states, refer to ACCESS MODES.

**Table 19. Extended Commands**

| NAME | | COMMAND CODE | UNITS | SEALED ACCESS (1), (2) | UNSEALED ACCESS (1), (2) |
|---|---|---|---|---|---|
| *AtRate()* | AR | 0X10, 0x11 | mA | R/W | R/W |
| *AtRateTimeToEmpty()* | ARTTE | 0x12, 0x13 | Minutes | R | R |
| *NominalAvailableCapacity()* | NAC | 0x14, 0x15 | mAh | R | R |
| *FullAvailableCapacity()* | FAC | 0x16, 0x17 | mAh | R | R |
| *TimeToEmpty()* | TTE | 0x18, 0x19 | Minutes | R | R |
| *TimeToFull()* | TTF | 0x1a, 0x1b | Minutes | R | R |
| *StandbyCurrent()* | SI | 0x1c, 0x1d | mA | R | R |
| *StandbyTimeToEmpty()* | STTE | 0x1e, 0x1f | Minutes | R | R |
| *MaxLoadCurrent()* | MLI | 0x20, 0x21 | mA | R | R |
| *MaxLoadTimeToEmpty()* | MLTTE | 0x22,0x23 | Minutes | R | R |
| *AvailableEnergy()* | AE | 0x24, 0x25 | 10 mWhr | R | R |
| *AveragePower()* | AP | 0x26, 0x27 | 10 mW | R | R |
| *TTEatConstantPower()* | TTECP | 0x28, 0x29 | Minutes | R | R |
| *Internal_Temp()* | INTTEMP | 0x2a, 0x2b | 0.1°K | R | R |
| *CycleCount()* | CC | 0x2c, 0x2d | Counts | R | R |
| *StateOfHealth()* | SOH | 0x2e, 0x2f | % / num | R | R |
| *ChargeVoltage()* | CHGV | 0x30, 0x31 | mV | R | R |
| *ChargeCurrent()* | CHGI | 0x32, 0x33 | mA | R | R |
| *PassedCharge()* | PCHG | 0x34, 0x35 | mAh | R | R |
| *DOD0()* | DOD0 | 0x36, 0x37 | HEX# | R | R |
| *SelfDischargeCurrent* | SDSG | 0x38, 0x39 | mA | R | R |
| *PackConfiguration()* | PKCFG | 0x3a, 0x3b | N/A | R | R |
| *DesignCapacity()* | DCAP | 0x3c, 0x3d | mAh | R | R |
| *DataFlashClass()* (2) | DFCLS | 0x3e | N/A | N/A | R/W |
| *DataFlashBlock()* (2) | DFBLK | 0x3f | N/A | R/W | R/W |
| *Authenticate()/BlockData()* | A/DF | 0x40…0x53 | N/A | R/W | R/W |
| *AuthenticateCheckSum()/BlockData()* | ACKS/DFD | 0x54 | N/A | R/W | R/W |
| *BlockData()* | DFD | 0x55…0x5f | N/A | R | R/W |
| *BlockDataCheckSum()* | DFDCKS | 0x60 | N/A | R/W | R/W |
| *BlockDataControl()* | DFDCNTL | 0x61 | N/A | N/A | R/W |
| *DeviceNameLength()* | DNAMELEN | 0x62 | N/A | R | R |
| *DeviceName()* | DNAME | 0x63...0x69 | N/A | R | R |
| Reserved | RSVD | 0x6a...0x7f | N/A | R | R |

(1) SEALED and UNSEALED states are entered via commands to CNTL 0x00 and 0x01
(2) In SEALED mode, data flash *cannot* be accessed through commands 0x3e and 0x3f.

### AtRate(): 0X10, 0x11

The *AtRate()* read-/write-word function is the first half of a two-function call-set used to set the AtRate value used in calculations made by the *AtRateTimeToEmpty()* function. The *AtRate()* units are in mA.

The *AtRate()* value is a signed integer and both positive and negative values will be interpreted as a discharge current value. The *AtRateTimeToEmpty()* function returns the predicted operating time at the AtRate value of discharge. The default value for *AtRate()* is zero and will force *AtRate()* to return 65535.

### AtRateTimeToEmpty(): 0x12, 0x13

This read-word function returns an unsigned integer value of the predicted remaining operating time if the battery is discharged at the *AtRate()* value in minutes with a range of 0 to 65534. A value of 65535 indicates *AtRate()* = 0.

The gas gauge updates *AtRateTimeToEmpty()* within 1s after the host sets the *AtRate()* value. The gas gauge automatically updates *AtRateTimeToEmpty()* based on the *AtRate()* value every 1 s.

**NominalAvailableCapacity(): 0x14, 0x15**

This read-only command pair returns the uncompensated (no or light load) battery capacity remaining. Units are 1 mAh per bit.

**FullAvailableCapacity(): 0x16, 0x17**

This read-only command pair returns the uncompensated (no or light load) capacity of the battery when fully charged. Units are 1 mAh per bit. *FullAvailableCapacity()* is updated at regular intervals, as specified by the Impedance Track algorithm.

**TimeToEmpty(): 0x18, 0x19**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the present rate of discharge, in minutes. A value of 65535 indicates battery is not being discharged.

**TimeToFull(): 0x1a, 0x1b**

This read-only function returns an unsigned integer value of predicted remaining time until the battery reaches full charge, in minutes, based upon *AverageCurrent()*. The computation should account for the taper current time extension from the linear TTF computation based on a fixed *AverageCurrent()* rate of charge accumulation. A value of 65535 indicates the battery is not being charged.

**StandbyCurrent(): 0x1c, 0x1d**

This read-only function returns a signed integer value of the measured standby current through the sense resistor. The *StandbyCurrent()* is an adaptive measurement. Initially it reports the standby current programmed in Initial Standby, and after spending some time in standby, reports the measured standby current.

The register value is updated every 1 second when the measured current is above the Deadband (3 mA default) and is less than or equal to 2 x Initial Standby. The first and last values that meet this criterion should not be averaged in, since they may not be stable values. To approximate a 1 minute time constant, each new *StandbyCurrent()* value is computed as follows:

$$StandbyCurrent()_{NEW} = (239/256) \times StandbyCurrent()_{OLD} + (17/256) \times AverageCurrent()$$

**StandbyTimeToEmpty(): 0x1e, 0x1f**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the standby rate of discharge, in minutes. The computation should use Nominal Available Capacity (NAC), the uncompensated remaining capacity, for this computation. A value of 65535 indicates battery is not being discharged.

**MaxLoadCurrent(): 0x20, 0x21**

This read-only function returns a signed integer value, in units of mA, of the maximum load conditions. The *MaxLoadCurrent()* is an adaptive measurement which is initially it reports the maximum load current programmed in Initial Max Load Current. If the measured current is ever greater than Initial Max Load Current, then *MaxLoadCurrent()* updates to the new current. *MaxLoadCurrent()* is reduced to the average of the previous value and Initial Max Load Current whenever the battery is charged to full after a previous discharge to an SOC less than 50%. This prevents the reported value from maintaining an unusually high value.

**MaxLoadTimeToEmpty(): 0x22, 0x23**

This read-only function returns an unsigned integer value of the predicted remaining battery life at the maximum load current discharge rate, in minutes. A value of 65535 indicates that the battery is not being discharged.

**AvailableEnergy(): 0x24, 0x25**

This read-only function returns an unsigned integer value of the predicted charge or energy remaining in the battery. The value is reported in units of mWh.

**AveragePower(): 0x26, 0x27**

This read-word function returns an unsigned integer value of the average power of the current discharge. A value of 0 indicates that the battery is not being discharged. The value is reported in units of mW.

**TimeToEmptyAtConstantPower(): 0x28, 0x29**

This read-only function returns an unsigned integer value of the predicted remaining operating time if the battery is discharged at the *AveragePower()* value in minutes. A value of 65535 indicates *AveragePower()* = 0. The gas gauge automatically updates *TimeToEmptyatContantPower()* based on the *AveragePower()* value every 1 s.

**InternalTemp(): 0x2a, 0x2b**

This read-only function returns an unsigned integer value of the measured internal temperature of the device in units of 0.1°K measured by the fuel gauge.

**CycleCount(): 0x2c, 0x2d**

This read-only function returns an unsigned integer value of the number of cycles the battery has experienced with a range of 0 to 65535. One cycle occurs when accumulated discharge ≥ *CC Threshold*.

**StateOfHealth(): 0x2e, 0x2f**

This read-only function returns an unsigned integer value, expressed as a percentage of the ratio of predicted FCC(25°C, SOH current rate) over the *DesignCapacity()*. The FCC(25°C, SOH current rate) is the calculated full charge capacity at 25°C and the SOH current rate which is specified in the data flash (State of Health Load). The range of the returned SOH percentage is 0x00 to 0x64, indicating 0% to 100% correspondingly.

**ChargeVoltage(): 0x30, 0x31**

This unsigned integer indicates the recommended charging voltage.

**ChargeCurrent(): 0x32, 0x33**

This signed integer indicates the recommended charging current.

**PassedCharge(): 0x34, 0x35**

This signed integer indicates the amount of charge passed through the sense resistor since the last IT simulation in mAh.

**DOD0(): 0x36, 0x37**

This unsigned integer indicates the depth of discharge during the most recent OCV reading.

**SelfDischargeCurrent(): 0x38, 0x39**

This read-only command pair returns a signed integer value that estimates the battery self discharge current.

**PackConfiguration(): 0x3a, 0x3b**

This Read-Word function allows the host to read the configuration of selected features of the bq34z110 pertaining to various features. Refer to PACK CONFIGURATION REGISTER.

**DesignCapacity(): 0x3c, 0x3d**

SEALED and UNSEALED Access: This command returns theoretical or nominal capacity of a new pack. The value is stored in ***Design Capacity*** and is expressed in mAh.

**DataFlashClass(): 0x3e**

UNSEALED Access: This command sets the data flash class to be accessed. The class to be accessed should be entered in hexadecimal.

SEALED Access: This command is not available in SEALED mode.

**DataFlashBlock(): 0x3f**

UNSEALED Access: If BlockDataControl has been set to 0x00, this command directs which data flash block will be accessed by the *BlockData()* command. Writing a 0x00 to *DataFlashBlock()* specifies the *BlockData()* command transfers authentication data. Issuing a 0x01 instructs the *BlockData()* command to transfer Manufacturer Data.

SEALED Access: This command directs which data flash block will be accessed by the *BlockData()* command. Writing a 0x00 to *DataFlashBlock()* specifies the BlockData() command transfers authentication data. Issuing a 0x01 instructs the *BlockData()* command to transfer ***Manufacturer Data***.

**AuthenticateData/BlockData(): 0x40…0x53**

UNSEALED Access: This data block has a dual function. It is used for the authentication challenge and response and is part of the 32-byte data block when accessing data flash.

SEALED Access: This data block is used for authentication challenge and response and is part of the 32-byte data block when accessing the ***Manufacturer Data***.

**AuthenticateChecksum/BlockData(): 0x54**

UNSEALED Access: This byte holds the authenticate checksum when writing the authentication challenge to the bq34z110 and is part of the 32-byte data block when accessing data flash.

SEALED Access: This byte holds the authentication checksum when writing the authentication challenge to the bq34z110 and is part of the 32-byte data block when accessing ***Manufacturer Data***.

**BlockData(): 0x55…0x5f**

UNSEALED Access: This data block is the remainder of the 32-byte data block when accessing data flash.

SEALED Access: This data block is the remainder of the 32-byte data block when accessing ***Manufacturer Data***.

**BlockDataChecksum(): 0x60**

UNSEALED Access: This byte contains the checksum on the 32 bytes of block data read or written to data flash.

SEALED Access: This byte contains the checksum for the 32 bytes of block data written to ***Manufacturer Data***.

**BlockDataControl(): 0x61**

UNSEALED Access: This command is used to control data flash access mode. Writing 0x00 to this command enables *BlockData()* to access general data flash. Writing a 0x01 to this command enables SEALED mode operation of *DataFlashBlock()*.

**DeviceNameLength(): 0x62**

UNSEALED and SEALED Access: This byte contains the length of the ***Device Name***.

**DeviceName(): 0x63…0x6A**

UNSEALED and SEALED Access: This block contains the device name that is programmed in ***Device Name***.

## DATA FLASH SUMMARY

Table 20 summarizes the data flash locations available to the user, including their default, minimum, and maximum values.

### Table 20. Data Flash Summary

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min Value | Max Value | Default Value | Units |
|---|---|---|---|---|---|---|---|---|---|
| Configuration | 2 | Safety | 0 | OT Chg | I2 | 0 | 1200 | 550 | 0.1°C |
| Configuration | 2 | Safety | 2 | OT Chg Time | U1 | 0 | 60 | 2 | s |
| Configuration | 2 | Safety | 3 | OT Chg Recovery | I2 | 0 | 1200 | 500 | 0.1°C |
| Configuration | 2 | Safety | 5 | OT Dsg | I2 | 0 | 1200 | 600 | 0.1°C |
| Configuration | 2 | Safety | 7 | OT Dsg Time | U1 | 0 | 60 | 2 | s |
| Configuration | 2 | Safety | 8 | OT Dsg Recovery | I2 | 0 | 1200 | 550 | 0.1°C |
| Configuration | 32 | Charge Inhibit Cfg | 0 | Chg Inhibit Temp Low | I2 | –400 | 1200 | 0 | 0.1°C |
| Configuration | 32 | Charge Inhibit Cfg | 2 | Chg Inhibit Temp High | I2 | –400 | 1200 | 450 | 0.1°C |
| Configuration | 32 | Charge Inhibit Cfg | 4 | Temp Hys | I2 | 0 | 100 | 50 | 0.1°C |
| Configuration | 34 | Charge | 0 | Suspend Low Temp | I2 | –400 | 1200 | –50 | 0.1°C |
| Configuration | 34 | Charge | 2 | Suspend High Temp | I2 | –400 | 1200 | 550 | 0.1°C |
| Configuration | 34 | Charge | 4 | Chg Eff | U1 | 0 | 100 | 100 | % |
| Configuration | 34 | Charge | 5 | Chg Eff Temp Comp | U1 | 0 | 255 | 25 | %/100 |
| Configuration | 34 | Charge | 6 | Chg Eff Drop Off | U1 | 0 | 100 | 96 | % |
| Configuration | 34 | Charge | 7 | Chg Eff Reduction rate | U1 | 0 | 100 | 10 | %/10 |
| Configuration | 34 | Charge | 8 | Maintenance Current | U1 | 0 | 100 | 0 | % |
| Configuration | 36 | Charge Termination | 0 | Taper Current | I2 | 0 | 1000 | 100 | mA |
| Configuration | 36 | Charge Termination | 2 | Min Taper Capacity | I2 | 0 | 1000 | 25 | 0.01 mAh |
| Configuration | 36 | Charge Termination | 4 | Cell Taper Voltage | I2 | 0 | 1000 | 100 | mV |
| Configuration | 36 | Charge Termination | 6 | Current Taper Window | U1 | 0 | 60 | 40 | s |
| Configuration | 36 | Charge Termination | 7 | TCA Set % | I1 | –1 | 100 | 99 | % |
| Configuration | 36 | Charge Termination | 8 | TCA Clear % | I1 | –1 | 100 | 95 | % |
| Configuration | 36 | Charge Termination | 9 | FC Set % | I1 | –1 | 100 | 100 | % |
| Configuration | 36 | Charge Termination | 10 | FC Clear % | I1 | –1 | 100 | 98 | % |
| Configuration | 36 | Charge Termination | 11 | DODatEOC Delta T | I2 | 0 | 1000 | 100 | 0.1°C |
| Configuration | 48 | Data | 0 | Rem Cap Alarm | I2 | 0 | 700 | 100 | mAh |
| Configuration | 48 | Data | 6 | Cell Design Voltage | I2 | 2000 | 5000 | 2000 | mV |
| Configuration | 48 | Data | 8 | Initial Standby | I1 | –256 | 0 | –10 | mA |
| Configuration | 48 | Data | 9 | Initial MaxLoad | I2 | –32767 | 0 | –500 | mA |
| Configuration | 48 | Data | 13 | Manufacture Date | U2 | 0 | 65535 | 0 | Date code |
| Configuration | 48 | Data | 15 | Serial Number | H2 | 0000 | ffff | 1 | num |
| Configuration | 48 | Data | 17 | Cycle Count | U2 | 0 | 65535 | 0 | Count |
| Configuration | 48 | Data | 19 | CC Threshold | I2 | 100 | 32767 | 900 | mAh |
| Configuration | 48 | Data | 21 | Design Capacity | I2 | 0 | 32767 | 4000 | mAh |
| Configuration | 48 | Data | 23 | Design Energy | I2 | 0 | 32767 | 8000 | mWh/cWh |
| Configuration | 48 | Data | 25 | SOH Load Current | I2 | –32767 | 0 | –400 | mA |
| Configuration | 48 | Data | 27 | TDD SOH Percent | I1 | 0 | 100 | 90 | % |
| Configuration | 48 | Data | 28 | Cell Charge Voltage T1–T2 | U2 | 0 | 4600 | 2200 | mV |
| Configuration | 48 | Data | 30 | Cell Charge Voltage T2–T3 | U2 | 0 | 4600 | 2450 | mV |
| Configuration | 48 | Data | 32 | Cell Charge Voltage T3–T4 | U2 | 0 | 4600 | 2350 | mV |
| Configuration | 48 | Data | 34 | Charge Current T1–T2 | U1 | 0 | 100 | 10 | % of des cap |
| Configuration | 48 | Data | 35 | Charge Current T2–T3 | U1 | 0 | 100 | 50 | % of des cap |
| Configuration | 48 | Data | 36 | Charge Current T3–T4 | U1 | 0 | 100 | 30 | % of des cap |

**Table 20. Data Flash Summary (continued)**

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min Value | Max Value | Default Value | Units |
|---|---|---|---|---|---|---|---|---|---|
| Configuration | 48 | Data | 37 | JEITA T1 | I1 | –128 | 127 | 0 | °C |
| Configuration | 48 | Data | 38 | JEITA T2 | I1 | –128 | 127 | 10 | °C |
| Configuration | 48 | Data | 39 | JEITA T3 | I1 | –128 | 127 | 45 | °C |
| Configuration | 48 | Data | 40 | JEITA T4 | I1 | –128 | 127 | 55 | °C |
| Configuration | 48 | Data | 41 | ISD Current | I2 | 0 | 32767 | 10 | HourRate |
| Configuration | 48 | Data | 43 | ISD Current Filter | U1 | 0 | 255 | 127 | — |
| Configuration | 48 | Data | 44 | Min ISD Time | U1 | 0 | 255 | 7 | Hour |
| Configuration | 48 | Data | 45 | Design Energy Scale | U1 | 1 | 10 | 1 | 1 or 10 only |
| Configuration | 48 | Data | 46 | Device Name | S9 | x | x | bq34z110 | — |
| Configuration | 48 | Data | 55 | Manufacturer Name | S12 | x | x | Texas Inst. | — |
| Configuration | 48 | Data | 67 | Device Chemistry | S5 | x | x | PbA | — |
| Configuration | 49 | Discharge | 0 | SOC1 Set Threshold | U2 | 0 | 65535 | 150 | mAh |
| Configuration | 49 | Discharge | 2 | SOC1 Clear Threshold | U2 | 0 | 65535 | 175 | mAh |
| Configuration | 49 | Discharge | 4 | SOCF Set Threshold | U2 | 0 | 65535 | 75 | mAh |
| Configuration | 49 | Discharge | 6 | SOCF Clear Threshold | U2 | 0 | 65535 | 100 | mAh |
| Configuration | 49 | Discharge | 9 | Cell BL Set Volt Threshold | I2 | 0 | 5000 | 1850 | mV |
| Configuration | 49 | Discharge | 11 | Cell BL Set Volt Time | U1 | 0 | 60 | 2 | s |
| Configuration | 49 | Discharge | 12 | Cell BL Clear Volt Threshold | I2 | 0 | 5000 | 1950 | mV |
| Configuration | 49 | Discharge | 14 | Cell BH Set Volt Threshold | I2 | 0 | 5000 | 2450 | mV |
| Configuration | 49 | Discharge | 16 | Cell BH Set Volt Time | U1 | 0 | 60 | 2 | s |
| Configuration | 49 | Discharge | 17 | Cell BH Clear Volt Threshold | I2 | 0 | 5000 | 2400 | mV |
| Configuration | 56 | Manufacturer Data | 0 | Pack Lot Code | H2 | 0 | 0xFFFF | 0000 | — |
| Configuration | 56 | Manufacturer Data | 2 | PCB Lot Code | H2 | 0 | 0xFFFF | 0000 | — |
| Configuration | 56 | Manufacturer Data | 4 | Firmware Version | H2 | 0 | 0xFFFF | 0000 | — |
| Configuration | 56 | Manufacturer Data | 6 | Hardware Revision | H2 | 0 | 0xFFFF | 0 | — |
| Configuration | 56 | Manufacturer Data | 8 | Cell Revision | H2 | 0 | 0xFFFF | 0 | — |
| Configuration | 56 | Manufacturer Data | 10 | DF Config Version | H2 | 0 | 0xFFFF | 0 | — |
| Configuration | 57 | Integrity Data | 6 | Static Chem DF Checksum | H2 | 00x7fff | 0x75F2 | 0 | — |
| Configuration | 59 | Lifetime Data | 0 | Lifetime Max Temp | I2 | 0 | 1400 | 300 | 0.1°C |
| Configuration | 59 | Lifetime Data | 2 | Lifetime Min Temp | I2 | –600 | 1400 | 200 | 0.1°C |
| Configuration | 59 | Lifetime Data | 4 | Lifetime Max Chg Current | I2 | –32767 | 32767 | 0 | mA |
| Configuration | 59 | Lifetime Data | 6 | Lifetime Max Dsg Current | I2 | –32767 | 32767 | 0 | mA |
| Configuration | 59 | Lifetime Data | 8 | Lifetime Max Pack Voltage | I2 | 0 | 32767 | 1500 | mV |
| Configuration | 59 | Lifetime Data | 10 | Lifetime Min Pack Voltage | I2 | 0 | 32767 | 2500 | mV |
| Configuration | 60 | Lifetime Temp Samples | 0 | Lifetime Flash Count | U2 | 0 | 65535 | 0 | — |
| Configuration | 64 | Registers | 0 | Pack Configuration | H2 | 0 | 0xFFFF | 0x0961 | — |
| Configuration | 64 | Registers | 2 | Pack Configuration B | H1 | 0 | 0xFF | 0xFF | Flgs |
| Configuration | 64 | Registers | 3 | Pack Configuration C | H1 | 0 | 0xFF | 0x30 | Flgs |
| Configuration | 64 | Registers | 4 | LED_Comm Configuration | H1 | 0 | 0xFF | 0x00 | Flgs |
| Configuration | 64 | Registers | 5 | Alert Configuration | H2 | 0 | 0xFFFF | 0x0000 | Flgs |
| Configuration | 64 | Registers | 7 | Number of Series Cells | U1 | 1 | 100 | 6 | — |
| Configuration | 66 | Lifetime Resolution | 3 | LT Update Time | U2 | 0 | 65535 | 60 | s |
| Configuration | 67 | LED Display | 0 | LED Hold Time | U1 | 0 | 255 | 4 | s |
| Configuration | 68 | Power | 0 | Flash Update OK Voltage Cell Volt | I2 | 0 | 4200 | 2800 | mV |
| Configuration | 68 | Power | 2 | Sleep Current | I2 | 0 | 100 | 10 | mA |
| Configuration | 68 | Power | 11 | Full Sleep Wait Time | U1 | 0 | 255 | 0 | s |
| System Data | 58 | Manufacturer Info | 0–31 | Manufacturer Info Block 0–31 | H1 | 0 | FF | 00 | — |

## Table 20. Data Flash Summary (continued)

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min Value | Max Value | Default Value | Units |
|---|---|---|---|---|---|---|---|---|---|
| Gas Gauging | 80 | IT Cfg | 0 | Load Select | U1 | 0 | 255 | 1 | — |
| Gas Gauging | 80 | IT Cfg | 1 | Load Mode | U1 | 0 | 255 | 0 | — |
| Gas Gauging | 80 | IT Cfg | 21 | Max Res Factor | U1 | 0 | 255 | 15 | num |
| Gas Gauging | 80 | IT Cfg | 22 | Min Res Factor | U1 | 0 | 255 | 3 | num |
| Gas Gauging | 80 | IT Cfg | 25 | Ra Filter | U2 | 0 | 1000 | 500 | — |
| Gas Gauging | 80 | IT Cfg | 42 | Fast Qmax Start DOD % | U1 | 0 | 255 | 92 | % |
| Gas Gauging | 80 | IT Cfg | 43 | Fast Qmax End DOD % | U1 | 0 | 255 | 96 | % |
| Gas Gauging | 80 | IT Cfg | 44 | Fast Qmax Start Volt Delta | I2 | 0 | 4200 | 100 | mV |
| Gas Gauging | 80 | IT Cfg | 67 | Cell Termination Voltage | I2 | 2500 | 3700 | 1800 | mV |
| Gas Gauging | 80 | IT Cfg | 69 | Cell Termination Voltage Delta | I2 | 0 | 4200 | 25 | mV |
| Gas Gauging | 80 | IT Cfg | 72 | Simulation Res Relax Time | U2 | 0 | 65534 | 200 | s |
| Gas Gauging | 80 | IT Cfg | 76 | User Rate-mA | I2 | –32767 | 32767 | 0 | mA |
| Gas Gauging | 80 | IT Cfg | 78 | User Rate-mW/cW | I2 | –32767 | 32767 | 0 | mW/cW |
| Gas Gauging | 80 | IT Cfg | 80 | Reserve Cap-mAh | I2 | 0 | 9000 | 0 | mAh |
| Gas Gauging | 80 | IT Cfg | 82 | Reserve Energy | I2 | 0 | 14000 | 0 | mWh/cWh |
| Gas Gauging | 80 | IT Cfg | 86 | Max Scale Back Grid | U1 | 0 | 15 | 4 | — |
| Gas Gauging | 80 | IT Cfg | 87 | Cell Max Delta V | U2 | 0 | 65535 | 100 | mV |
| Gas Gauging | 80 | IT Cfg | 89 | Cell Min Delta V | U2 | 0 | 65535 | 0 | mV |
| Gas Gauging | 80 | IT Cfg | 91 | Max Sim Rate | U1 | 0 | 255 | 2 | C/rate |
| Gas Gauging | 80 | IT Cfg | 92 | Min Sim Rate | U1 | 0 | 255 | 20 | C/rate |
| Gas Gauging | 80 | IT Cfg | 93 | Ra Max Delta | U2 | 0 | 32767 | 44 | mΩ |
| Gas Gauging | 80 | IT Cfg | 95 | Qmax Max Delta % | U1 | 0 | 100 | 5 | mAh |
| Gas Gauging | 80 | IT Cfg | 96 | Cell DeltaV Max Delta | U2 | 0 | 65535 | 10 | mV |
| Gas Gauging | 80 | IT Cfg | 102 | Fast Scale Start SOC | U1 | 0 | 100 | 10 | % |
| Gas Gauging | 80 | IT Cfg | 107 | Charge Hys Voltage Shift | I2 | 0 | 2000 | 40 | mV |
| Gas Gauging | 81 | Current Thresholds | 0 | Dsg Current Threshold | I2 | 0 | 2000 | 60 | mA |
| Gas Gauging | 81 | Current Thresholds | 2 | Chg Current Threshold | I2 | 0 | 2000 | 75 | mA |
| Gas Gauging | 81 | Current Thresholds | 4 | Quit Current | I2 | 0 | 1000 | 40 | mA |
| Gas Gauging | 81 | Current Thresholds | 6 | Dsg Relax Time | U2 | 0 | 8191 | 60 | s |
| Gas Gauging | 81 | Current Thresholds | 8 | Chg Relax Time | U1 | 0 | 255 | 60 | s |
| Gas Gauging | 81 | Current Thresholds | 9 | Quit Relax Time | U1 | 0 | 63 | 1 | s |
| Gas Gauging | 81 | Current Thresholds | 10 | Max IR Correct | U2 | 0 | 1000 | 400 | mV |
| Gas Gauging | 82 | State | 0 | Qmax Cell 0 | I2 | 0 | 32767 | 4000 | mAh |
| Gas Gauging | 82 | State | 2 | Cycle Count | U2 | 0 | 65535 | 0 | — |
| Gas Gauging | 82 | State | 4 | Update Status | H1 | 0x00 | 0x06 | 0x00 | — |
| Gas Gauging | 82 | State | 5 | Cell V at Chg Term | I2 | 0 | 5000 | 2400 | mV |
| Gas Gauging | 82 | State | 7 | Avg I Last Run | I2 | –32768 | 32767 | –299 | mA |
| Gas Gauging | 82 | State | 9 | Avg P Last Run | I2 | –32768 | 32767 | –1131 | mW/cW |
| Gas Gauging | 82 | State | 11 | Cell Delta Voltage | I2 | –32768 | 32767 | 2 | mV |
| Gas Gauging | 82 | State | 15 | T Rise | I2 | 0 | 32767 | 0 | — |
| Gas Gauging | 82 | State | 17 | T Time Constant | I2 | 0 | 32767 | 32767 | — |
| OCV Table | 83 | OCV Table | 0 | Chem ID | H2 | 0 | 0xFFFF | 0107 | — |
| Ra Tables | 88 | Data | 0–31 | Cell0 R_a Table | See Note 1 | | | | |
| Ra Tables | 89 | Data | 0–31 | xCell0 R_a Table | See Note 1 | | | | |
| Calibration | 104 | Data | 0 | CC Gain (Note 4) | F4 | 1.00E–01 | 4.00E+01 | 0.47095 | num |
| Calibration | 104 | Data | 4 | CC Delta Note 4) | F4 | 2.98E+04 | 1.19E+06 | 5.595e5 | num |
| Calibration | 104 | Data | 8 | CC Offset (Note 4) | I2 | –32768 | 32767 | –1200 | num |
| Calibration | 104 | Data | 10 | Board Offset (Note 4) | I1 | –128 | 127 | 0 | num |

**Table 20. Data Flash Summary (continued)**

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Min Value | Max Value | Default Value | Units |
|---|---|---|---|---|---|---|---|---|---|
| Calibration | 104 | Data | 11 | Int Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | 104 | Data | 12 | Ext Temp Offset | I1 | –128 | 127 | 0 | 0.1°C |
| Calibration | 104 | Data | 13 | Pack V Offset | I1 | –128 | 127 | 0 | mV |
| Calibration | 104 | Data | 14 | Voltage Divider | U2 | 0 | 65535 | 20000 | mV |
| Calibration | 107 | Current | 1 | Deadband | U1 | 0 | 255 | 5 | mA |
| Security | 112 | Codes | 0 | Sealed to Unsealed | H4 | 0 | ffffffff | 36720414 | — |
| Security | 112 | Codes | 4 | Unsealed to Full | H4 | 0 | ffffffff | ffffffff | — |
| Security | 112 | Codes | 8 | Authen Key3 | H4 | 0 | ffffffff | 01234567 | — |
| Security | 112 | Codes | 12 | Authen Key2 | H4 | 0 | ffffffff | 89ABCDEF | — |
| Security | 112 | Codes | 16 | Authen Key1 | H4 | 0 | ffffffff | FEDCBA98 | — |
| Security | 112 | Codes | 20 | Authen Key0 | H4 | 0 | ffffffff | 76543210 | — |
| 1. Encoded battery profile information created by bqEasy software. | | | | | | | | | |
| 2. Part number and/or part specific | | | | | | | | | |
| 3. Not IEEE floating point | | | | | | | | | |
| 4. Display as data flash value; value displayed in EVSW is different. See Table 21 for the conversion table. | | | | | | | | | |

**Table 21. Data Flash (DF) to EVSW Conversion**

| Class | Subclass ID | Subclass | Offset | Name | Data Type | Data Flash Default | Data Flash Unit | EVSW Default | EVSW Unit | DF to EVSW Conversion |
|---|---|---|---|---|---|---|---|---|---|---|
| Data | 48 | Data | 13 | Manufacture Date | U2 | 0 | code | 1-Jan-1980 | | Day+Mo*32+(Yr -1980)*256 |
| Gas Gauging | 80 | IT Cfg | 59 | User Rate mW | I2 | 0 | cW | 0 | mW | DF × 10 |
| Gas Gauging | 80 | IT Cfg | 63 | Reserve Cap mWh | I2 | 0 | cWh | 0 | mWh | DF × 10 |
| Calibration | 104 | Data | 0 | CC Gain | F4 | 0.47095 | Num | 10.124 | mΩ | 4.768/DF |
| Calibration | 104 | Data | 4 | CC Delta | F4 | 5.595e5 | Num | 10.147 | mΩ | 5677445/DF |
| Calibration | 104 | Data | 8 | CC Offset | I2 | –1200 | Num | –0.576 | mV | DF × 0.00048 |
| Calibration | 104 | Data | 10 | Board Offset | I1 | 0 | Num | 0 | µV | DF × 16/0.48 |

## REVISION HISTORY

**Changes from Original (June 2012) to Revision A** **Page**

- Added additional information starting at the General Description section ..... 1
- Changed a word (editorial) ..... 1
- Changed document to Production Data ..... 1
- Changed the Typical Implementation graphic ..... 3
- Changed SLEEP Mode section ..... 23
- Changed FULLSLEEP Mode section ..... 23
- Changed figure ..... 33
- Changed Data Flash Summary ..... 39

**Changes from Revision A (December 2012) to Revision B** **Page**

- Changed Figure 2 ..... 3

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ34Z110PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 34Z110 | Samples |
| BQ34Z110PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 34Z110 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

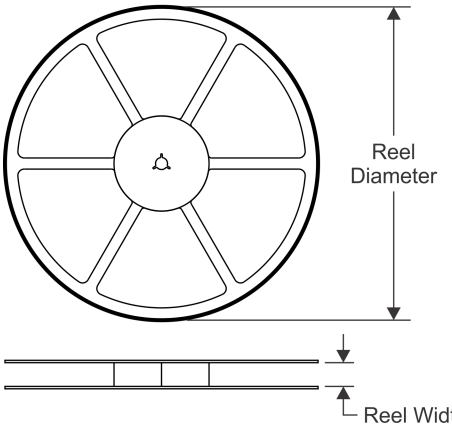
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

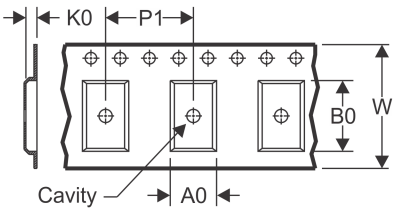
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

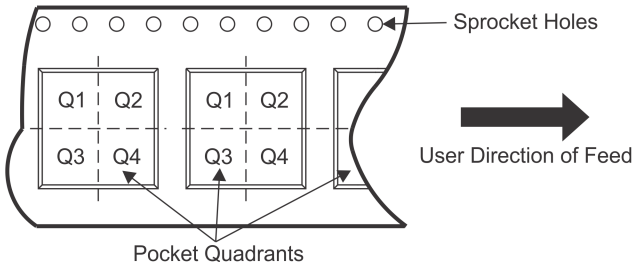



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

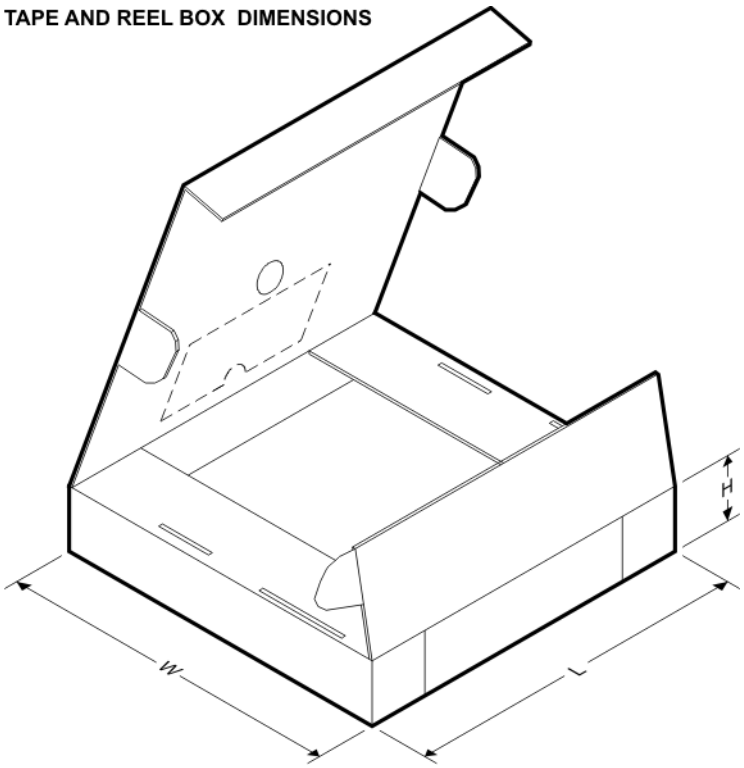
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ34Z110PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

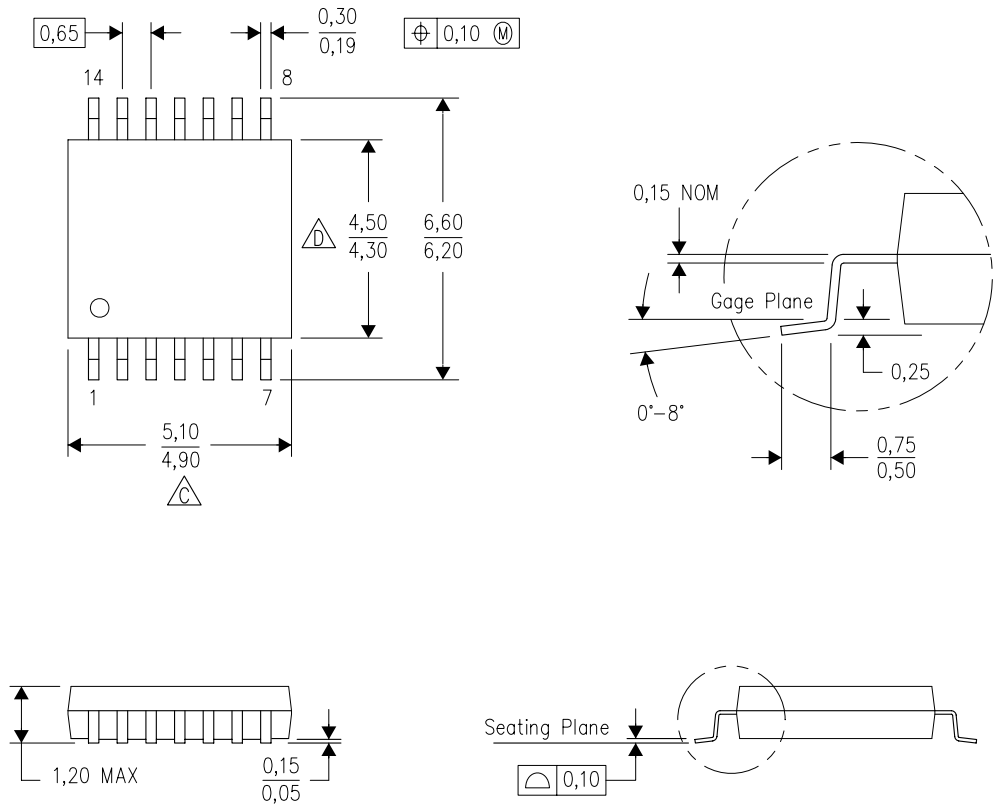
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ34Z110PWR | TSSOP | PW | 14 | 2000 | 338.1 | 338.1 | 20.6 |

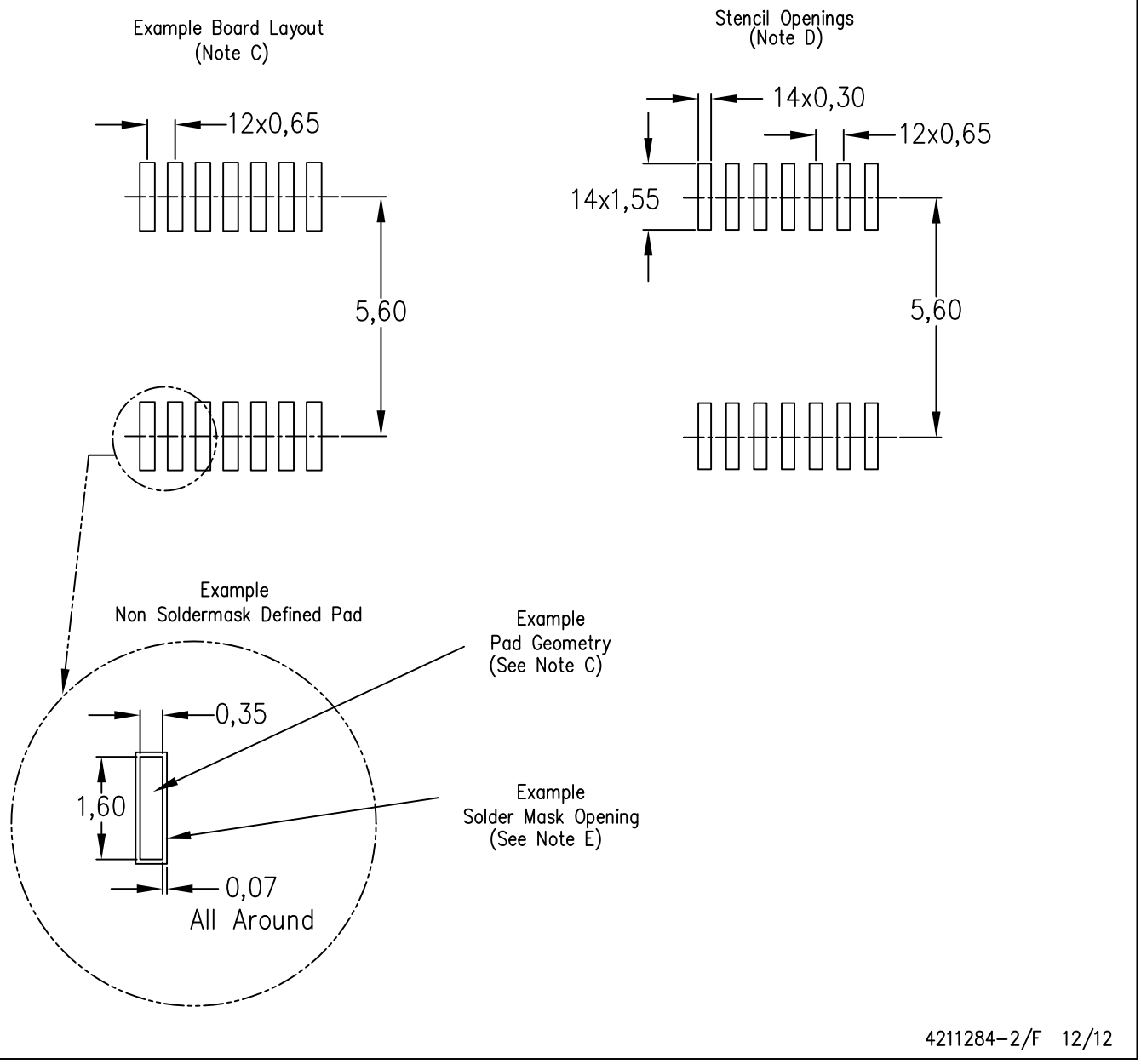
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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