

EPT SPICE Modeling Kit

Prepared by

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ON Semiconductor

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<http://onsemi.com>

APPLICATION NOTE

Objective

The objective of this kit is to provide customers with enough schematic and SPICE parameter information to perform system level interconnect modeling with the ON Semiconductor ECLinPS Plus™ Translator EPT family. The EPT devices MC100EPT2xD are single or dual supply 1 or 2 Bit translators between the TTL and ECL/PECL worlds. Single supply devices translate between TTL and PECL, dual supply devices translate to or from negative supplied ECL. All devices are designed as 100K compatible 100EPT2x.

The kit contains representative schematics and model files for the I/O circuits used by the EPT20 and EPT22 devices. The package model should be placed on all external inputs, outputs and supply pins.

Input and Output Schematics

The TTL-PECL Translator function uses circuit schematics LVTTL01 and LVTTL02 for references diagrams to the SPICE netlists.

All inputs and outputs of the ELT family are protected by ESD protection circuitry. The ESD circuit, IN_ESD, is used for TTL Input and OUT_ESD for PECL outputs.

If the user would like to just simulate the output behavior of an TTL output the TTL_OUT circuit can be stimulated with internal signals.

To all external pins the package model, LINES, needs to be added. If users want to reduce simulation time and just simulate 1 channel or only the output of a circuit, they need to take care of the correct power supply management. The channels share power supply pins. Dynamic ICC current will add up at power pins. When a simulation is performed with only one channel, the package models of the power pins

need to be adjusted. The parasitic capacitance and inductance should be adjusted accordingly.

Modeling

The bias driver schematics for VCS and V1 generation are not included in this kit, as they are unnecessary for interconnection simulation. In addition their use would result in a relatively large in simulation time. Alternatively the internal reference voltages should be driven with ideal constant voltage sources.

Parameter	Typical Level	Worst Case
VCS	VEE+1.3V	±50mV
V1	VEE+2.1V	±50mV

This model kit is intended for simulations within the specified power supply range. If supply voltages drop below minimum specification, VCS and V1 can no longer be assumed to be constant. Thus, this model kit can not be used for power up or power down simulations. The 10K ohm resistor should NOT be simulated as simple SPICE resistor because it is fabricated by a diffusion step in wafer processing and there is an associated parasitic. The following subcircuit should be used to enhance the performance of the simulation.

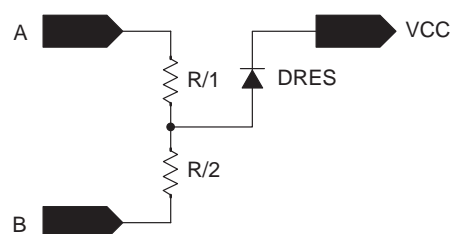


Figure 1. Resistor Model

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```
.SUBCKT RESK A B VCC params: R=10000
* Assumes Sheet Rho=500OHM, Resistor Width=10U, and Cap in Farads.
Ra A 1 {R/2} TC=900U
Rb 1 B {R/2} TC=900U
D1 1 VCC DRES
.MODEL DRES D
+ (IS=3.7E-16
+ CJO=0.265E-16*R+29E-16)
.ENDS RESK
```

The nodes in the model files and the schematics are:

Name	Node	Description
Root	1	Root of the tree
Node 1	2	Left child of Root
Node 2	3	Right child of Root
Node 3	4	Left child of Node 1
Node 4	5	Right child of Node 1
Node 5	6	Left child of Node 2
Node 6	7	Right child of Node 2
Node 7	8	Left child of Node 3
Node 8	9	Right child of Node 3
Node 9	10	Left child of Node 4
Node 10	11	Right child of Node 4
Node 11	12	Left child of Node 5
Node 12	13	Right child of Node 5
Node 13	14	Left child of Node 6
Node 14	15	Right child of Node 6
Node 15	16	Left child of Node 7
Node 16	17	Right child of Node 7
Node 17	18	Left child of Node 8
Node 18	19	Right child of Node 8
Node 19	20	Left child of Node 9
Node 20	21	Right child of Node 9
Node 21	22	Left child of Node 10
Node 22	23	Right child of Node 10
Node 23	24	Left child of Node 11
Node 24	25	Right child of Node 11
Node 25	26	Left child of Node 12
Node 26	27	Right child of Node 12
Node 27	28	Left child of Node 13
Node 28	29	Right child of Node 13
Node 29	30	Left child of Node 14
Node 30	31	Right child of Node 14
Node 31	32	Left child of Node 15
Node 32	33	Right child of Node 15
Node 33	34	Left child of Node 16
Node 34	35	Right child of Node 16
Node 35	36	Left child of Node 17
Node 36	37	Right child of Node 17
Node 37	38	Left child of Node 18
Node 38	39	Right child of Node 18
Node 39	40	Left child of Node 19
Node 40	41	Right child of Node 19
Node 41	42	Left child of Node 20
Node 42	43	Right child of Node 20
Node 43	44	Left child of Node 21
Node 44	45	Right child of Node 21
Node 45	46	Left child of Node 22
Node 46	47	Right child of Node 22
Node 47	48	Left child of Node 23
Node 48	49	Right child of Node 23
Node 49	50	Left child of Node 24
Node 50	51	Right child of Node 24
Node 51	52	Left child of Node 25
Node 52	53	Right child of Node 25
Node 53	54	Left child of Node 26
Node 54	55	Right child of Node 26
Node 55	56	Left child of Node 27
Node 56	57	Right child of Node 27
Node 57	58	Left child of Node 28
Node 58	59	Right child of Node 28
Node 59	60	Left child of Node 29
Node 60	61	Right child of Node 29
Node 61	62	Left child of Node 30
Node 62	63	Right child of Node 30
Node 63	64	Left child of Node 31
Node 64	65	Right child of Node 31
Node 65	66	Left child of Node 32
Node 66	67	Right child of Node 32
Node 67	68	Left child of Node 33
Node 68	69	Right child of Node 33
Node 69	70	Left child of Node 34
Node 70	71	Right child of Node 34
Node 71	72	Left child of Node 35
Node 72	73	Right child of Node 35
Node 73	74	Left child of Node 36
Node 74	75	Right child of Node 36
Node 75	76	Left child of Node 37
Node 76	77	Right child of Node 37
Node 77	78	Left child of Node 38
Node 78	79	Right child of Node 38
Node 79	80	Left child of Node 39
Node 80	81	Right child of Node 39
Node 81	82	Left child of Node 40
Node 82	83	Right child of Node 40
Node 83	84	Left child of Node 41
Node 84	85	Right child of Node 41
Node 85	86	Left child of Node 42
Node 86	87	Right child of Node 42
Node 87	88	Left child of Node 43
Node 88	89	Right child of Node 43
Node 89	90	Left child of Node 44
Node 90	91	Right child of Node 44
Node 91	92	Left child of Node 45
Node 92	93	Right child of Node 45
Node 93	94	Left child of Node 46
Node 94	95	Right child of Node 46
Node 95	96	Left child of Node 47
Node 96	97	Right child of Node 47
Node 97	98	Left child of Node 48
Node 98	99	Right child of Node 48
Node 99	100	Left child of Node 49
Node 100	101	Right child of Node 49
Node 101	102	Left child of Node 50
Node 102	103	Right child of Node 50
Node 103	104	Left child of Node 51
Node 104	105	Right child of Node 51
Node 105	106	Left child of Node 52
Node 106	107	Right child of Node 52
Node 107	108	

VCC 100 3.3V High rail power supply

VEE 200 0.0V Lowest Rail Power supply

VCS 300 1.24 Current Source Base Voltage (VEE+1.3V)V

V1	400	2.1 Internal TTL Transfer Reference Supply
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VTT 500 1.3V External termination sink supply ($\bar{V}_{CC}=2V$)

VIN 51 PULSE (.8 to 2.0, tr/tf 5NS, PW 20NS, PER 50NS)

Temperature coefficients are annotated (* TC=).

For typical load ECL and PECL outputs should be terminated 50ohm to VTT=VCC—2V. TTL outputs are loaded with 20pF to GROUND and 500OHM to GROUND.

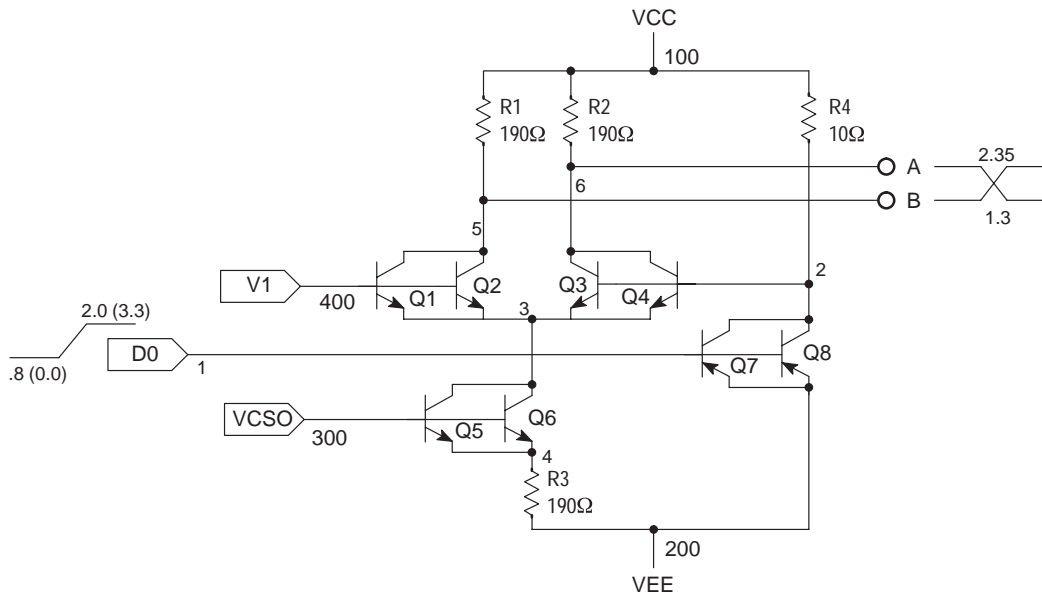
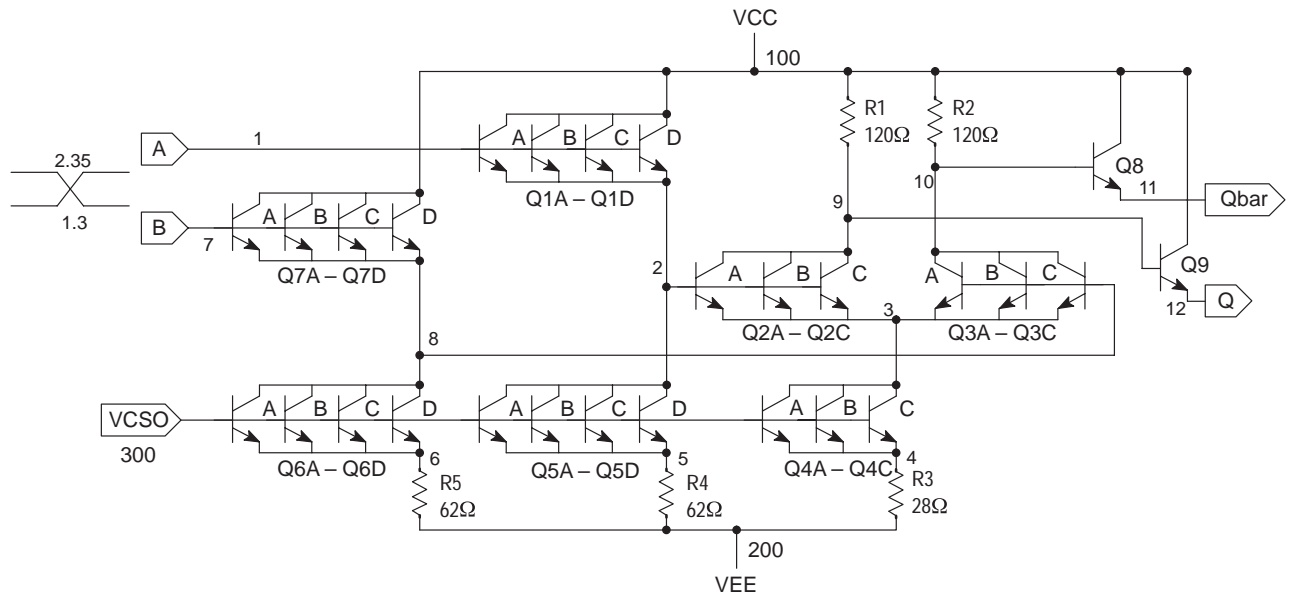


Figure 2. LVTTL–LVPECL Translator
EPT20/22
LVPECL output

For LVTTL01, the following transitors are used:

Q1	TRANA
Q2	TRANA
Q3	TRANA
Q4	TRANA
Q5	TRANA
Q6	TRANA
Q7	TRANE
Q8	TRANE

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**Figure 3. LVTTTL-LVPECL Translator
EPT20/22
LVPECL output**

For LVTTTL02 the following transistors are used:

Q1A-D	TRANA
Q2A-C	TRANB
Q3A-C	TRANB
Q4A-C	TRANB
Q5A-D	TRANA
Q6A-D	TRANA
Q7A-D	TRANA
Q8	TRANB
Q9	TRANB

```
.TRAN 0.2NS 120NS
XLVTTTL01 100 200 300 400 1 5 6 LVTTTL01
XLVTTTL02 100 200 300 5 6 11 12 LVTTTL02
XINESD 100 200 51 1 IN_ESD
XOUTESD 100 200 11 OUT_ESD
XOUTESDB 100 200 12 OUT_ESD
XQBTERM 500 12 RTERM
XQTERM 500 11 RTERM
```

```
.SUBCKT LVTTTL01 100 200 300 400 1 5 6
Q1 5 400 3 200 TRANA
Q2 5 400 3 200 TRANA
Q3 6 2 3 200 TRANA
Q4 6 2 3 200 TRANA
Q5 3 300 4 200 TRANA
Q6 3 300 4 200 TRANA
Q7 2 1 200 200 TLS
Q8 2 1 200 200 TLS
R1 100 5 190
* TC=0.26M, 0.9U
R2 100 6 190
```

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```
* TC=0.26M, 0.9U
R3  4    200 190
* TC=0.26M, 0.9U
R4 100  2    10000
* TC=0.26M, 0.9U
.ENDS LVTTL01
```

```
.SUBCKT LVTTL02 100 200 300 1 7 11 12
Q1A 100  1  2  200 TRANA
Q1B 100  1  2  200 TRANA
Q1C 100  1  2  200 TRANA
Q1D 100  1  2  200 TRANA
Q2A  9  2  3  200 TRANB
Q2B  9  2  3  200 TRANC
Q2C  9  2  3  200 TRANC
Q3A 10  8  3  200 TRANB
Q3B 10  8  3  200 TRANC
Q3C 10  8  3  200 TRANC
Q4A  3 300  4  200 TRANB
Q4B  3 300  4  200 TRANB
Q4C  3 300  4  200 TRANB
Q5A  2 300  5  200 TRANA
Q5B  2 300  5  200 TRANA
Q5C  2 300  5  200 TRANA
Q5D  2 300  5  200 TRANA
Q6A  8 300  6  200 TRANA
Q6B  8 300  6  200 TRANA
Q6C  8 300  6  200 TRANA
Q6D  8 300  6  200 TRANA
Q7A 100  7  8  200 TRANA
Q7B 100  7  8  200 TRANA
Q7C 100  7  8  200 TRANA
Q7D 100  7  8  200 TRANA
Q8  100 10 11  200 TRAND
Q9  100  9 12  200 TRAND
R1  100  9 120
* TC=0.26M, 0.9U
R2  100 10 120
* TC=0.26M, 0.9U
R3  4    200 28
* TC=0.26M, 0.9U
R4  5    200 62
* TC=0.26M, 0.9U
R5  6    200 62
* TC=0.26M, 0.9U
.ENDS LVTTL02
```

```
* INPUT ESD 51 = in, 61 out
.SUBCKT IN_ESD 100 200 51 61
D1  51    100    ES14X19M
D2  51    100    ES14X19M
D3  51    100    ES14X19M
D4  200    51    ES14X19M
D5  200    51    ES14X19S
D6  200    51    ES14X19M
D7  200    51    ES14X19S
D8  200    51    ES14X19M
D9  200    51    ES14X19S
RB1  51  61 1000
* TC=0.26M, 0.9U
.ENDS IN_ESD
```

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```
* OUTPUT ESD
.SUBCKT OUT_ESD 100 200 81
D1      81      100      ES14X19M
D2      81      100      ES14X19M
D3      200     81       ES14X19M
D4      200     81       ES14X19S
D5      200     81       ES14X19M
D6      200     81       ES14X19S
.ENDS OUT_ESD

.SUBCKT RTERM 500 91
R1 91 500 50
.ENDS

.END

.MODEL TRANA NPN (IS=8.12E-18 BF=192 NF=1 VAF=75.6 IKF=1.49E-02
+ ISE=9.14E-17 NE=2 BR=15.8 VAR=2.76 IKR=2.2E-03 ISC=2.62E-16
+ NC=1.578 RB=327 IRB=4.8E-05 RBM=0.001 RE=10 RC=15 CJE=2.0E-14
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=7.6E-03 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=5.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=4.8E-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)

.MODEL TRANC NPN (IS=1.36E-17 BF=180 NF=1 VAF=87.6 IKF=2.19E-02
+ ISE=6.65E-16 NE=2 BR=16.9 VAR=2.76 IKR=1.5E-03 ISC=1.11E-16
+ NC=1.578 RB=136 IRB=3.24E-05 RBM=0.001 RE=6 RC=8 CJE=1.02E-13
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=1.27E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=10.3E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=9.94E-15 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)

.MODEL TRAND NPN (IS=6.55E-17 BF=103 NF=1 VAF=90 IKF=2.91E-01
+ ISE=8.85E-15 NE=2 BR=15.7 NR=1 VAR=3.82 IKR=2.01E-02 ISC=1.48E-15
+ NC=2 RB=10.5 IRB=4.39E-04 RBM=0.29 RE=0.351 RC=9 CJE=3.5E-13
+ VJE=.8167 MJE=.1973 TF=8.99E-12 ITF=1.3E-01 XTF=5.67 VTF=1.86 PTF=41.43 TR=6.405E-10
+ CJC=1.4E-13 VJC=.6401 MJC=.2674 XCJC=1 CJS=9.3E-14 VJS=.5002 MJS=.1706
+ EG=1.135 XTI=4.177 XTB=0.6322 FC=0.961)

.MODEL TRANB NPN (IS=2.71E-17 BF=172 NF=1 VAF=71.4 IKF=4.38E-02
+ ISE=1.33E-15 NE=2 BR=17.9 VAR=2.76 IKR=3.0E-03 ISC=2.22E-16
+ NC=1.578 RB=67 IRB=6.47E-05 RBM=0.001 RE=3 RC=4 CJE=5.09E-14
+ VJE=.8867 MJE=.2868 TF=9.02E-12 ITF=2.53E-02 XTF=2.8 VTF=3.4 PTF=41.56 TR=1NS
+ CJC=20.6E-15 VJC=.6324 MJC=.3006 XCJC=.3 CJS=1.7E-14 VJS=.4193 MJS=.2563
+ EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)

.MODEL TRANEPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05
+ ISE=7.75e-17 NE=1.813 BR=210 VAR=5.68 IKR=6.51e-05 ISC=7.75e-17
+ NC=1.813 RB=349 IRB=1.77e-07 RBM=53 RE=119 RC=158 CJE=7.04e-15
+ VJE=0.6578 MJE=0.149 TF=6.33e-10 ITF=2.2e-08 XTF=2.8 VTF=1.4
+ PTF=41.56 TR=1e-9 CJC=7.04e-15 VJC=0.8034 MJC=0.1773 XCJC=.3
+ CJS=4.79e-15 VJS=.4193 MJS=0.0902
+ EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9)

.MODEL TLS LPNP (IS=1.65e-17 BF=210 NF=1 VAF=7.5 IKF=6.51e-05
+ ISE=7.75e-17 NE=1.813 BR=210.1 NR=1 VAR=5.68 IKR=2.61e-04 ISC=7.75e-17
+ NC=1.813 RB=349 IRB=1.8e-07 RBM=53 RE=119 RC=158 CJE=7.0e-15
+ VJE=.6578 MJE=.149 TF=6.33e-10 ITF=2.2e-08 XTF=.5356 VTF=.2365 PTF=0 TR=6.33e-10
+ CJC=7.0e-15 VJC=.8034 MJC=.1773 XCJC=1 CJS=4.8e-15 VJS=.5 MJS=.09022
+ EG=1.158 XTI=2.015 XTB=0.1208 FC=0.9)
```

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.MODEL ES14X19M D (IS=1.55E-14 CJO=160FF RS=12 VJ=.58 M=.25 BV=9)

.MODEL ES14X19S D (IS=1.55E-14 CJO=29FF VJ=.624 M=.571)
.END

* PACKAGE: 8SOIC
* SPICE SUBCIRCUIT FILE OF COUPLED TRANSMISSION LINES
* CREATED FRI APR 25 16:47:54 1997
* BY PMG VERSION 3.6.2
*

* TRANSMISSION LINE MODEL

* CONDUCTOR	PIN
* 1	1
* 2	2
* 3	3
* 4	4
* 5	5
* 6	6
* 7	7
* 8	8

* NUMBER OF LUMPS: 1
* FASTEST APPLICABLE EDGE RATE: 0.076 NS
* CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
*


.SUBCKT LINES N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O

L01WB	N01I	N01M	1.367E-09
L01	N01M	N01O	7.794E-10
C01	N01M	0	2.445E-13
L02WB	N02I	N02M	1.287E-09
L02	N02M	N02O	5.473E-10
C02	N02M	0	1.888E-13
L03WB	N03I	N03M	1.287E-09
L03	N03M	N03O	5.473E-10
C03	N03M	0	1.901E-13
L04WB	N04I	N04M	1.367E-09
L04	N04M	N04O	7.723E-10
C04	N04M	0	2.443E-13
L05WB	N05I	N05M	1.367E-09
L05	N05M	N05O	7.710E-10
C05	N05M	0	2.478E-13
L06WB	N06I	N06M	1.287E-09
L06	N06M	N06O	5.489E-10
C06	N06M	0	1.916E-13
L07WB	N07I	N07M	1.287E-09
L07	N07M	N07O	5.495E-10
C07	N07M	0	1.930E-13
L08WB	N08I	N08M	1.367E-09
L08	N08M	N08O	7.786E-10
C08	N08M	0	2.451E-13
K0102	L01	L02	0.1687
K0102WB	L01WB	L02WB	0.3400
C0102	N01O	N02O	3.674E-14
K0103	L01	L03	0.0702
K0103WB	L01WB	L03WB	0.1847
K0203	L02	L03	0.1822
K0203WB	L02WB	L03WB	0.3505
C0203	N02O	N03O	3.521E-14
K0204	L02	L04	0.0682
K0204WB	L02WB	L04WB	0.1847

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K0304	L03	L04	0.1694
K0304WB	L03WB	L04WB	0.3400
C0304	N03O	N04O	3.675E-14
K0305WB	L03WB	L05WB	0.1847
K0405WB	L04WB	L05WB	0.3455
K0406WB	L04WB	L06WB	0.1847
K0506	L05	L06	0.1697
K0506WB	L05WB	L06WB	0.3400
C0506	N05O	N06O	3.720E-14
K0507	L05	L07	0.0682
K0507WB	L05WB	L07WB	0.1847
K0607	L06	L07	0.1824
K0607WB	L06WB	L07WB	0.3505
C0607	N06O	N07O	3.570E-14
K0608	L06	L08	0.0702
K0608WB	L06WB	L08WB	0.1847
K0708	L07	L08	0.1691
K0708WB	L07WB	L08WB	0.3400
C0708	N07O	N08O	3.632E-14
.ENDS LINES			

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