NC STATE UNIVERSITY Electrical and Computer Engineering

FreePDK3

Design Rule Manual

Revision: 1.0

Process Node: 3nm

Release Date: August 30, 2021

1.Layer Information

1.1 Front-End-of-Line (FEOL) Layers

Layer	Description	Lithography	Patterning
NW	N – Well	193i	**SE**
BPR	Buried Power Rail	193i	LE2
VBPR	Via connecting BPR to M0A	193i	LE2
ACT	Active for Nanosheet Layers	193i	SADP
GATE	Gate Metal	EUV	SADP
GCUT	Gate Cut Metal	193i	SPT
DUMMY	Dummy Poly	EUV	SAQP
NIM	N - implant	193i	SE
PIM	P - implant	193i	SE

1.2 Middle-of-Line (MOL) Layers

Layer	Description	Lithography	Patterning
M0A	Metal M0A interconnect layer	EUV	DPT
V0A	Via connecting M0A to M0B	EUV	DPT
GCON	Gate interconnect layer	EUV	DPT
M0B	Metal M0B interconnect layer	EUV	SALELE
V0B	Via connecting M0B to M1	EUV	DPT

1.3 Back-End-of-Line (BEOL) Layers

Layer	Description	Lithography	Patterning
M1	Metal 1 interconnect layer	EUV	DPT
V1	Via connecting M1 to M2	EUV	DPT
M2	Metal 2 interconnect layer	EUV	DPT
V2	Via connecting M2 to M3	EUV	DPT
M3	Metal 3 interconnect layer	EUV	DPT
V3	Via connecting M3 to M4	EUV	DPT
M4	Metal 4 interconnect layer	EUV	SPT
V4	Via connecting M4 to M5	EUV	SPT

M5	Metal 5 interconnect layer	EUV	SPT
V5	Via connecting M5 to M6	EUV	SPT
M6	Metal 6 interconnect layer	EUV	SPT
V6	Via connecting M6 to M7	EUV	SPT
M7	Metal 7 interconnect layer	193i	LE2
V7	Via connecting M7 to M8	193i	LE2
M8	Metal 8 interconnect layer	193i	LE2
V8	Via connecting M8 to M9	193i	LE2
M9	Metal 9 interconnect layer	193i	LE2
V9	Via connecting M9 to M10	193i	LE2
M10	Metal 10 interconnect layer	193i	SE
V10	Via connecting M10 to M11	193i	SE
M11	Metal 11 interconnect layer	193i	SE
V11	Via connecting M11 to M12	193i	SE
M12	Metal 12 interconnect layer	193i	SE
V12	Via connecting M12 to M13	193i	SE
M13	Metal 13 interconnect layer	193i	SE
VRDL	Via connecting M13 to RDL	193i	SE
RDL	Metal RDL interconnect layer	193i	SE

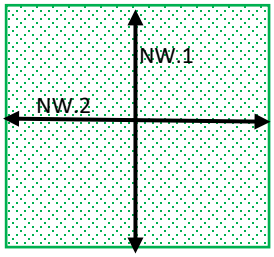
2. Physical Design Rules

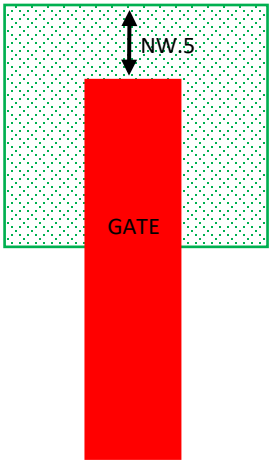
2.1 Geometry Check

Rule	Value	Description
1	-	Non-orthogonal shapes are not allowed

2.2 N-Well (NW) Rules

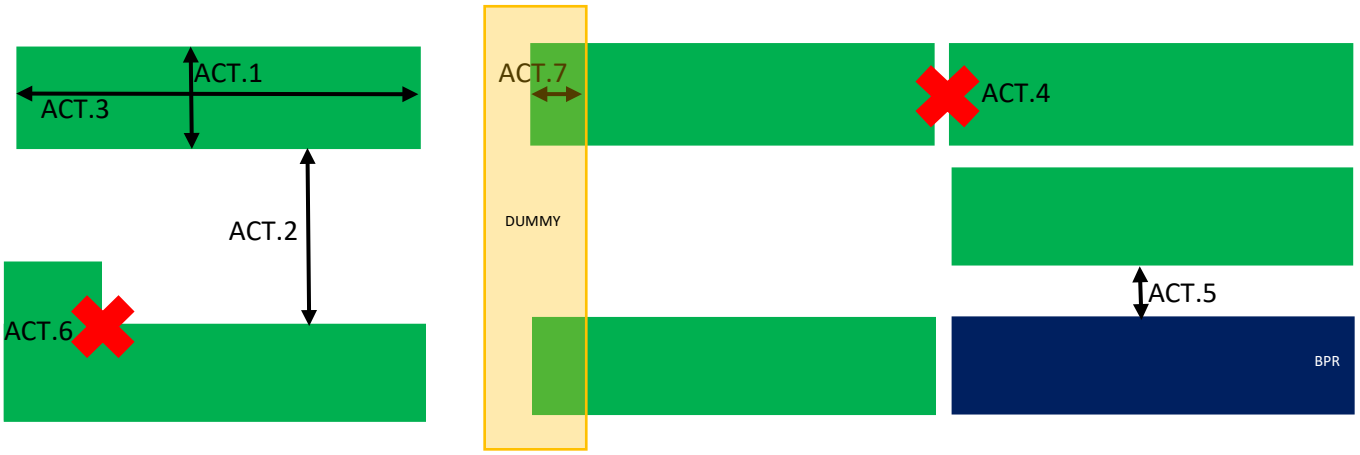
Rule	Value	Description
NW.1	57.5 nm	Minimum vertical width of NW
NW.2	84 nm	Minimum horizontal width of NW
NW.3	6237 nm^2	Minimum area/enclosed area of NW
NW.4	-	NW must be orthogonal
NW.5	7 nm	Minimum extension of NW past GATE (not cut by GCUT)





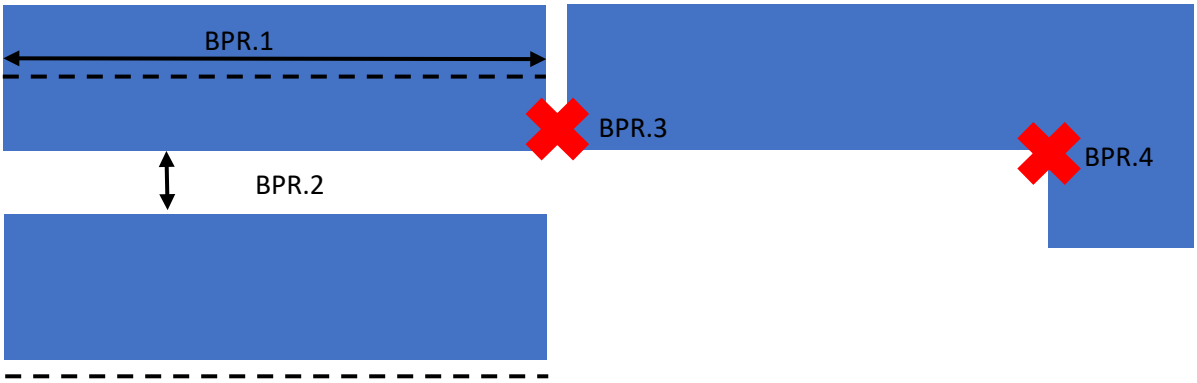
2.3 Active (ACT) Rules

Rule	Value	Description
ACT.1	21 nm	Minimum vertical width of ACT
ACT.2	21.5 nm	Minimum vertical spacing of ACT
ACT.3	84 nm	Minimum horizontal width of ACT
ACT.4		ACT should be continuous
ACT.5	10 nm	Minimum vertical spacing between ACT and BPR
ACT.6		ACT may not bend
ACT.7		ACT must end inside DUMMY layer.



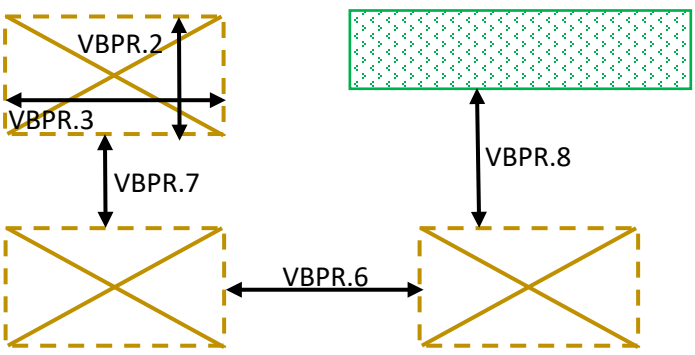
2.4 Buried Power Rail (BPR) Rules

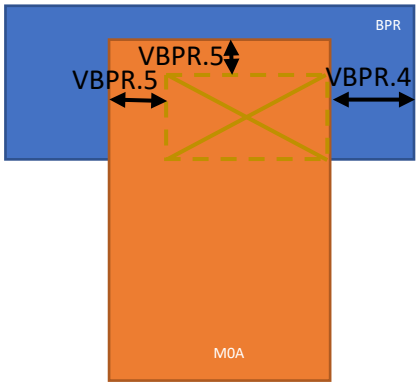
Rule	Value	Description
BPR.1	31.5 nm	BPR Vertical Width
BPR.2	84 nm	Minimum vertical spacing between BPR layers
BPR.3		BPR must be continuous
BPR.4		BPR might not bend



2.5 Via Buried Power Rail (VBPR) Rules

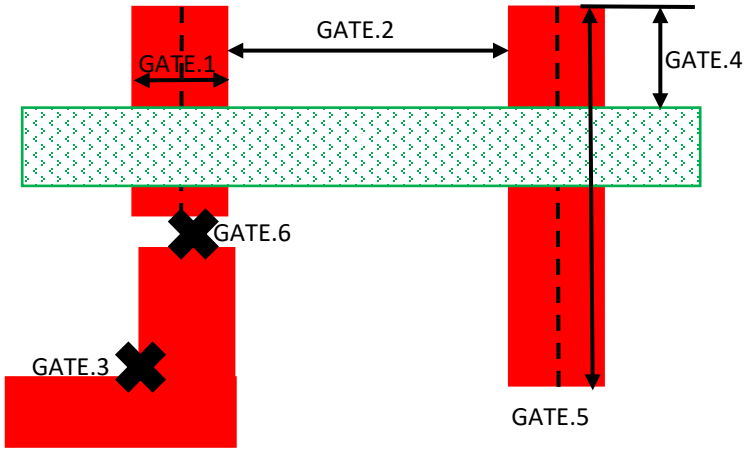
Rule	Value	Description
VBPR.1		VBPR Must be rectangle
VBPR.2	10.5 nm	Exact VERTICAL width of VBPR
VBPR.3	15 nm	Exact HORIZONTAL length of VBPR
VBPR.4	13.5 nm	VBPR enclosure by BPR on two opposite sides, horizontal direction
VBPR.5	0 nm	VBPR enclosure by M0A on two opposite sides, vertical direction
VBPR.6	27 nm	Minimum horizontal spacing between two VBPR layer
VBPR.7	10 nm	Minimum vertical spacing between two VBPR layer
VBPR.8	10 nm	Minimum spacing between VBPR and ACTIVE layer polygons not on the same net
VBPR.9		VBPR may not interact with GCUT or GATE or DUMMY





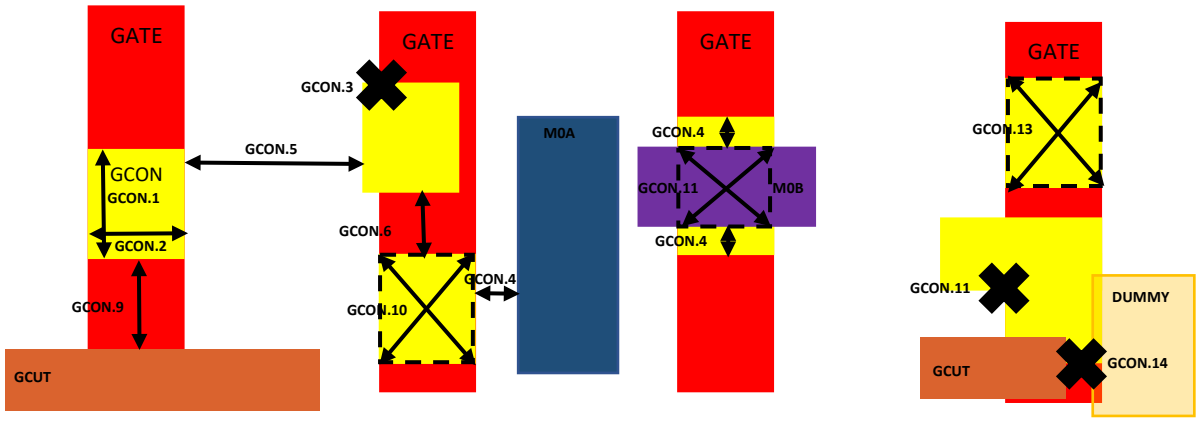
2.6 Gate Layer

Rule	Value	Description
GATE.1	15 nm	GATE exact horizontal width
GATE.2	27 nm	Minimum horizontal spacing between GATE or DUMMY layers
GATE.3		GATE may not bend
GATE.4	21.5 nm	GATE min extension past ACT
GATE.5	40 nm	GATE minimum vertical length
GATE.6		GATE may not be discontinuous along the vertical axis. Use GCUT layer to mark cuts in the GATE
GATE.7		ACT layer vertical edge may not lie inside, or coincide with, the GATE layer
GATE.8	6 nm	Minimum horizontal spacing between ACT and GATE (not cut by GCUT and not interacting with ACT)



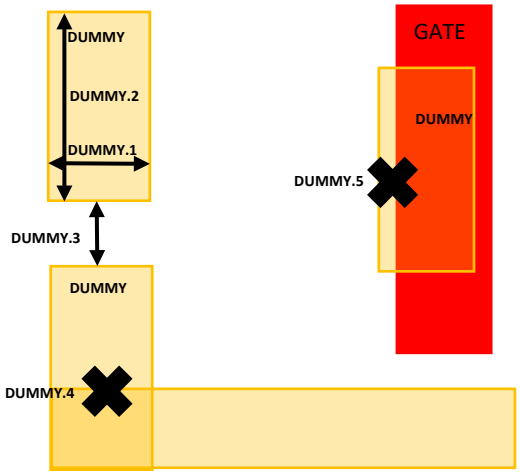
2.7 Gate Contact (GCON) Layer

Rule	Value	Description
GCON.1	13 nm	Exact VERTICAL width of GCON
GCON.2	15 mn	Exact HORIZONTAL length of GCON
GCON.3		GCON must overlap gate
GCON.4	1 nm	Extension past M0B in vertical direction
GCON.5	25 nm	Minimum horizontal spacing between two GCON layer
GCON.6	28 nm	Minimum vertical spacing between two GCON layer
GCON.7	6 nm	Minimum spacing between GCON and M0A layer polygons
GCON.8	25 nm	Minimum horizontal spacing between GCON and GATE layer
GCON.9	13.5 nm	Minimum vertical spacing between GCON and GCUT
GCON.10	180 nm^2	Minimum GCON Area
GCON.11		GCON may not bend
GCON.12	165 nm^2	Minimum area of overlap between GCON and M0B
GCON.13	180 nm^2	Minimum area of overlap between GCON and GATE
GCON.14		GCON may not interact with GCUT or DUMMY



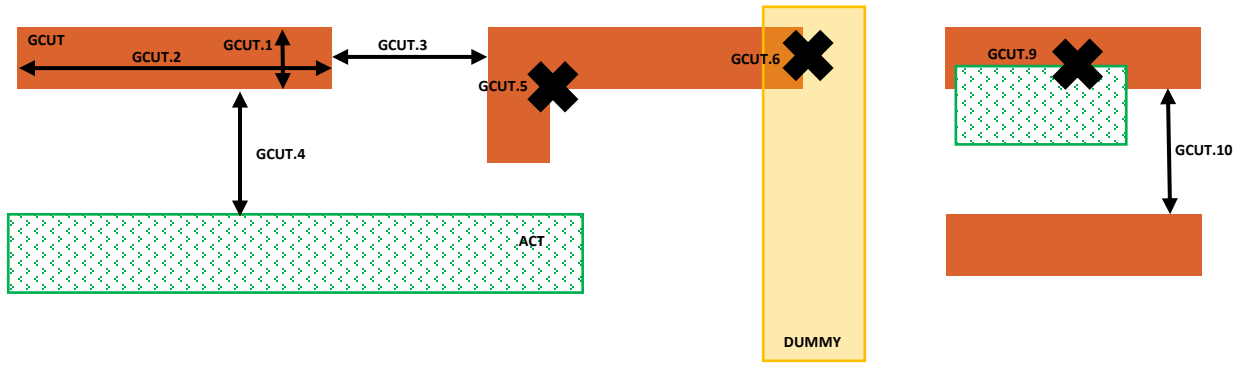
2.8 Dummy Layer

Rule	Value	Description
DUMMY.1	15 nm	DUMMY exact horizontal width
DUMMY.2	40 nm	DUMMY minimum vertical length
DUMMY.3	115.5 nm	Minimum vertical space
DUMMY.4		DUMMY may not bend
DUMMY.5		DUMMY must completely overlap GATE



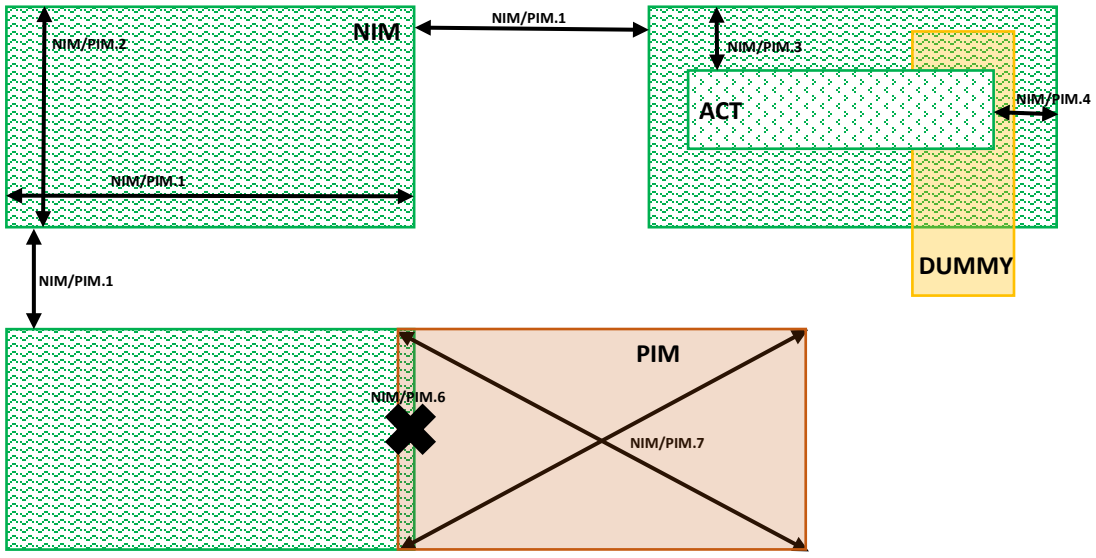
2.9 Gate Metal Cut (GCUT) Layer

Rule	Value	Description
GCUT.1	10.5 nm	Exact vertical width of GCUT (shape is oriented horizontally)
GCUT.2	42 nm	Minimum horizontal length of GCUT(shape is oriented horizontally)
GCUT.3	69 nm	Minimum horizontal space of GCUT
GCUT.4	20.5 nm	GCUT minimum space to ACT (must be 20.5 = 10 + 10.5 //)
GCUT.5		GCUT may not bend
GCUT.6		GCUT vertical edge must coincide with DUMMY vertical edge
GCUT.7		GCUT layer may not exist without the layer GATE
GCUT.8		GCUT layer vertical edge may not lie inside, or coincide with, the GATE layer
GCUT.9		GCUT may not interact with ACT
GCUT.10	105 nm	Minimum vertical spacing between two GCUT layer



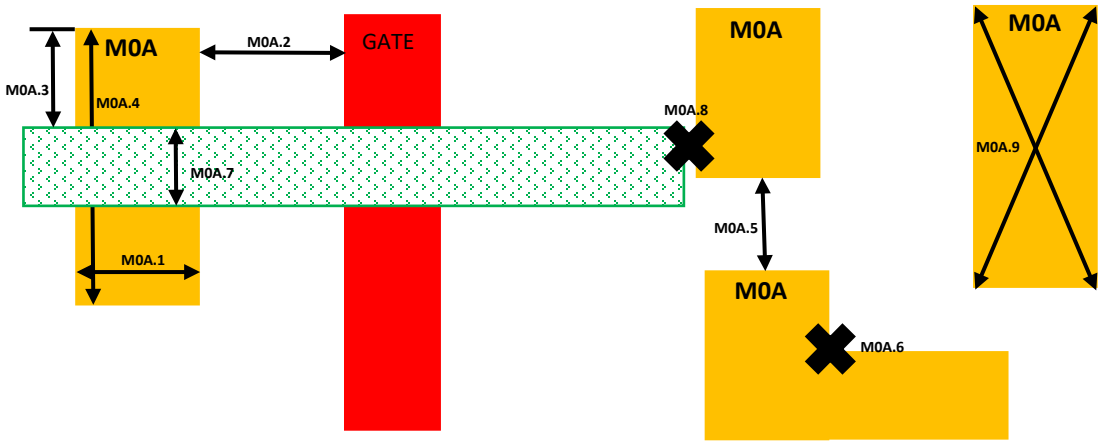
2.10 NIM/PIM Layer

Rule	Value	Description
NIM/PIM.1	84 nm	Minimum width/spacing/notch of NIM/PIM
NIM/PIM.2	57.5 nm	Minimum vertical width of NIM/PIM
NIM/PIM.3	20 nm	Minimum enclose of ACT by NIM/PIM on vertical direction
NIM/PIM.4	13.5 nm	Minimum enclose of ACT by NIM/PIM on horizontal direction
NIM/PIM.5	4830 nm^2	Minimum NIM/PIM area/enclosed area
NIM/PIM.6		NIM and PIM may not overlap



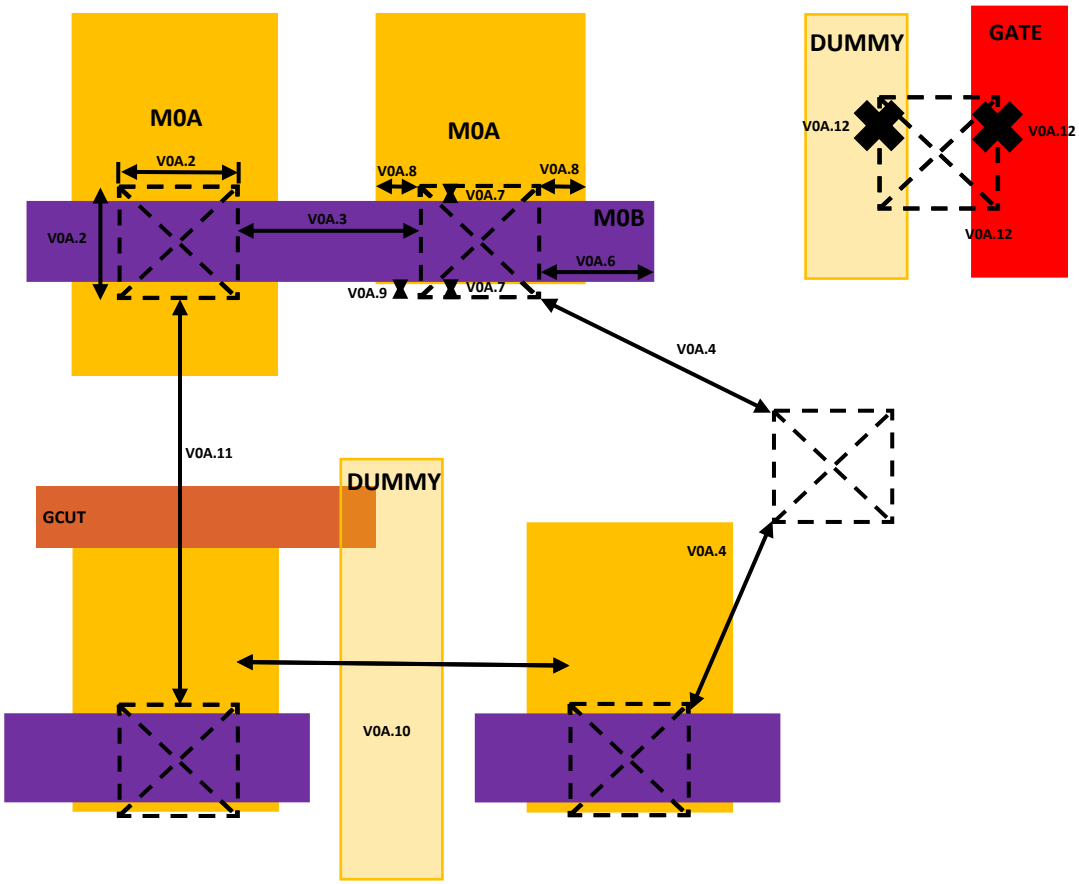
2.11 M0A Layer

Rule	Value	Description
M0A.1	15 nm	Minimum width of M0A
M0A.2	6 nm	Minimum spacing of M0A to GATE
M0A.3	5 nm	Minimum extension of ACT past M0A (horizontal direction)
M0A.4	21.5 nm	Vertical length of M0A
M0A.5	10 nm	Vertical spacing of M0A
M0A.6		M0A may not bend
M0A.7	11 nm	Minimum vertical overlap between M0A and ACTIVE
M0A.8		M0A may not be outside ACTIVE
M0A.9	322.5 nm^2	Minimum M0A area



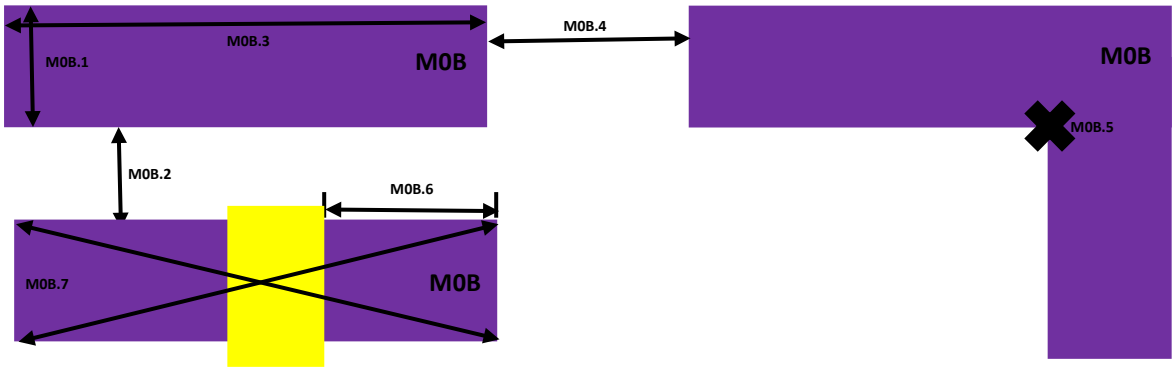
2.12 V0A Layer

Rule	Value	Description
V0A.1		V0A shape is a square
V0A.2	13 nm	V0A is a square with 13nm edge length
V0A.3	29 nm	Minimum spacing of V0A - Full alignment
V0A.4	30 nm	Minimum corner-to-corner spacing between two V0A instances
V0A.5		V0A must always interact with M0A and M0B
V0A.6	6 nm	V0A enclosure by M0B on two opposite sides, horizontal direction
V0A.7	-1 nm	V0A enclosure by M0B on two opposite sides, vertical direction
V0A.8	1 nm	V0A enclosure by M0A on two opposite sides, horizontal direction
V0A.9	-1 nm	V0A enclosure by M0A on opposite sides, vertical direction
V0A.10	8 nm	Minimum space of V0A and M0B of different net
V0A.11	16.5 nm	Minimum space of V0A and M0A of different net
V0A.12		V0A may not interact with DUMMY or GATE layer
V0A.13	156 nm^2	Minimum area overlap between M0A and V0A



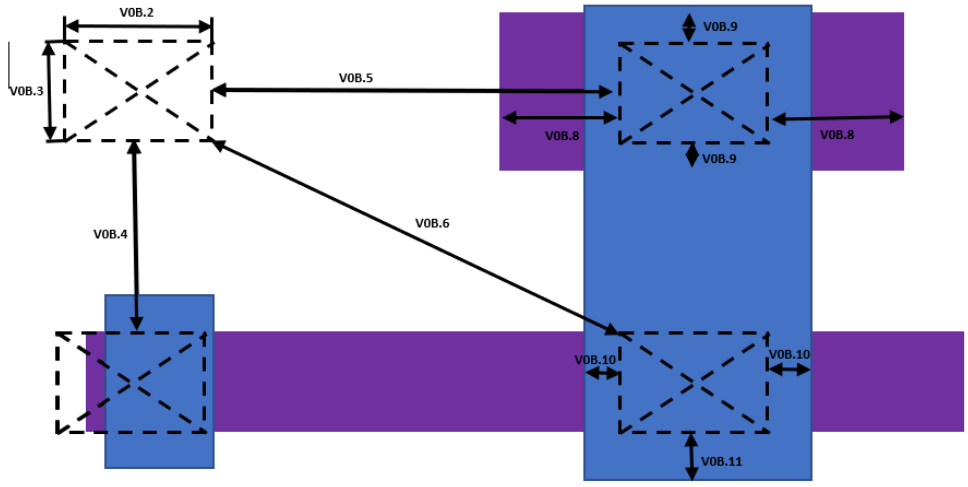
2.13 M0B Layer

Rule	Value	Description
M0B.1	11 nm	Minimum Vertical width of M0B
M0B.2	10 nm	Minimum Vertical spacing of M0B
M0B.3	22 nm	Minimum Horizontal width of M0B
M0B.4	20 nm	M0B minimum horizontal spacing
M0B.5		M0B may not bend
M0B.6	3.5 nm	Minimum extension of MOB past GCON
M0B.7	242 nm^2	Minimum M0B area



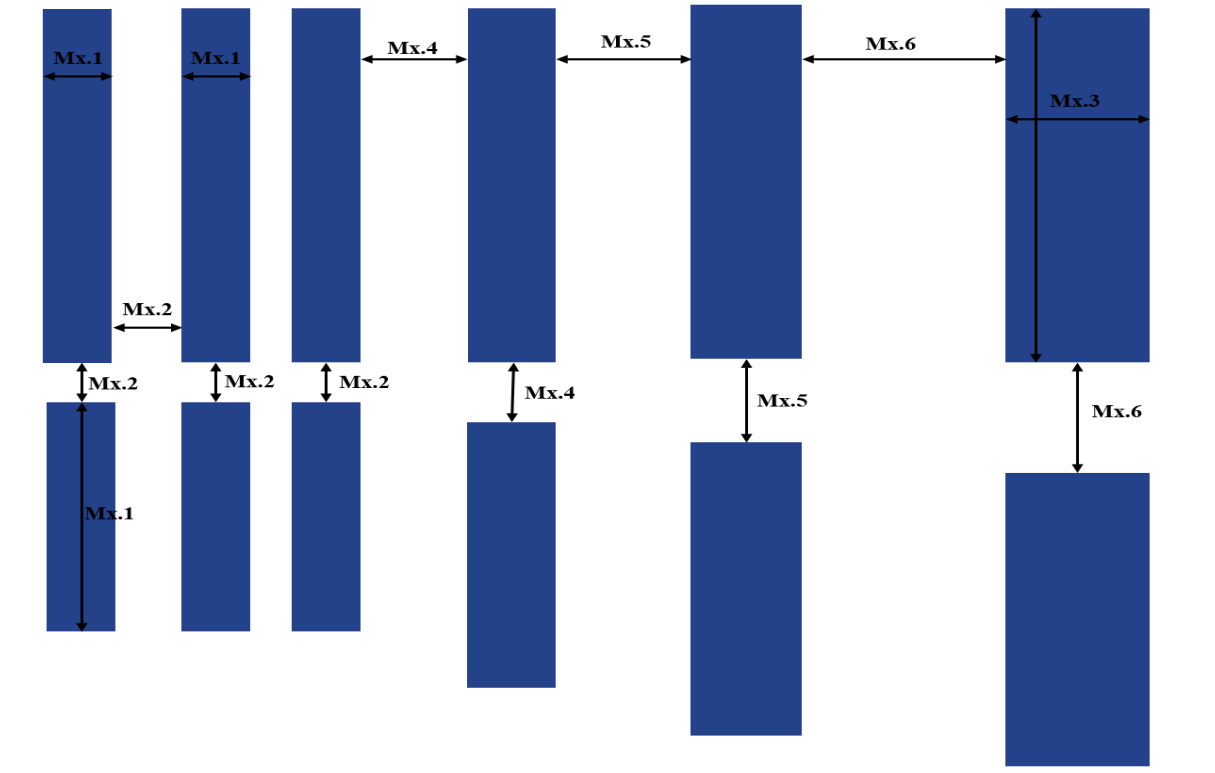
2.14 V0B Layer

Rule	Value	Description
V0B.1		V0B shape is a rectangle
V0B.2	14 nm	V0B exact horizontal width
V0B.3	10 nm	V0B exact vertical width
V0B.4	10.5 nm	Minimum vertical spacing of V0B - Full alignment
V0B.5	20 nm	Minimum horizontal spacing of V0B - Full alignment
V0B.6	22 nm	Minimum corner-to-corner spacing between two V0B instances
V0B.7		V0B must always interact with M0B and M1
V0B.8	4 nm	V0B enclosure by M0B on two opposite sides, horizontal direction
V0B.9	0 nm	V0B enclosure by M0B on two opposite sides, VERTICAL direction
V0B.10	0 nm	V0B enclosure by M1 on two opposite sides, horizontal direction
V0B.11	2.5 nm	V0B enclosure by M1 on two opposite sides, VERTICAL direction



2.15 Metalx (Mx) Layers

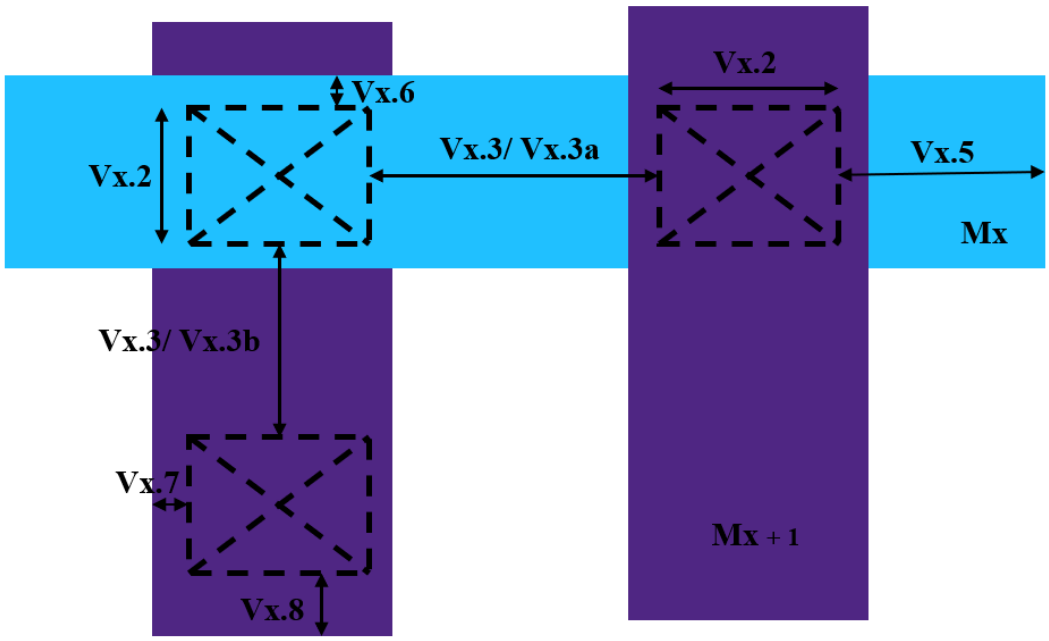
Rule	Value	Description
Mx.1 (x=1,2)	14 nm	METALx width minimum
Mx.1 (x=3)	15 nm	METALx width minimum
Mx.1 (x=4-6)	24 nm	METALx width minimum
Mx.1 (x=7-9)	40 nm	METALx width minimum
Mx.1 (x=10-11)	80 nm	METALx width minimum
Mx.1 (x=12-13)	160 nm	METALx width minimum
Mx.2 (x=1-3)	15 nm	METALx spacing minimum
Mx.2 (x=4-6)	24 nm	METALx spacing minimum
Mx.2 (x=7-9)	40 nm	METALx spacing minimum
Mx.2 (x=10-11)	80 nm	METALx spacing minimum
Mx.2 (x=12-13)	160 nm	METALx spacing minimum
Mx.3 (x=2-3)	750 nm	METALx maximum width
Mx.3 (x=4-6)	1200 nm	METALx maximum width
Mx.3 (x=7-9)	2000 nm	METALx maximum width
Mx.3 (x=10-11)	4000 nm	METALx maximum width
Mx.3 (x=12-13)	8000 nm	METALx maximum width
Mx.4 (x=1-3)	45 nm	Minimum spacing of METALx wider than 45nm and longer than 45nm
Mx.4 (x=4-6)	72 nm	Minimum spacing of METALx wider than 72nm and longer than 72nm
Mx.4 (x=7-9)	120 nm	Minimum spacing of METALx wider than 120nm and longer than 120nm
Mx.4 (x=10-11)	240 nm	Minimum spacing of METALx wider than 240nm and longer than 240nm
Mx.4 (x=12-13)	480 nm	Minimum spacing of METALx wider than 480nm and longer than 480nm
Mx.5 (x=1-3)	135 nm	Minimum spacing of METALx wider than 135nm and longer than 135nm
Mx.5 (x=4-6)	216 nm	Minimum spacing of METALx wider than 216nm and longer than 216nm
Mx.5 (x=7-9)	360 nm	Minimum spacing of METALx wider than 360nm and longer than 360nm
Mx.5 (x=10-11)	720 nm	Minimum spacing of METALx wider than 720nm and longer than 720nm
Mx.5 (x=12-13)	1440 nm	Minimum spacing of METALx wider than 1440nm and longer than 1440nm
Mx.6 (x=1-3)	405 nm	Minimum spacing of METALx wider than 405nm and longer than 405nm
Mx.6 (x=4-6)	648 nm	Minimum spacing of METALx wider than 648nm and longer than 648nm
Mx.6 (x=7-9)	1080 nm	Minimum spacing of METALx wider than 1080nm and longer than 1080nm
Mx.6 (x=10-11)	2160 nm	Minimum spacing of METALx wider than 2160nm and longer than 2160nm
Mx.6 (x=12-13)	4320 nm	Minimum spacing of METALx wider than 4320nm and longer than 4320nm
Mx.7(x=1-3,7-9)		Double patterning Error
Mx.8(x=1-3,7-9)		Density Balancing Rule: The density of decomposed metals should be between 23 and 77%



2.16 ViaX (Vx) Layers

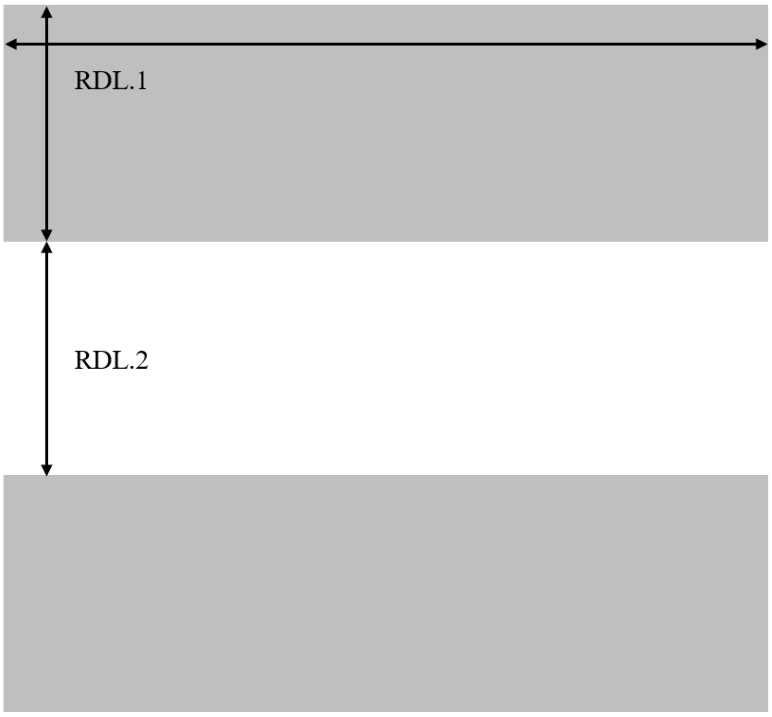
Rule	Value	Description
Vx.1 (x=1,2, 4,5,7,8,10,12,VRDL)		Vx shape is square
Vx.1 (x=3,6,9,11)		Vx shape is rectangle
Vx.2 (x=1,2)	14 nm	Vx is a square with 14nm edge length
Vx.2 (x=3)	15, 24 nm	Vx is a rectangle with 15nm horizontal edge and 24nm vertical edge
Vx.2 (x=4,5)	24 nm	Vx is a square with 24nm edge length
Vx.2 (x=6)	40,24 nm	Vx is a rectangle with 40nm horizontal edge and 24nm vertical edge
Vx.2 (x=7,8)	40 nm	Vx is a square with 40nm edge length
Vx.2 (x=9)	40,80 nm	V9 is a rectangle with 40nm horizontal edge and 80nm vertical edge
Vx.2 (x=10)	80nm	V10 is a square with 80nm edge length
Vx.2 (x=11)	80, 160 nm	V11 is a rectangle with 80nm horizontal edge and 160nm vertical edge
Vx.2 (x=12,VRDL)	160 nm	V12 is a square with 160nm edge length
Vx.3 (x=1,2)	14 nm	Minimum spacing of Vx - Full alignment
Vx.3a (x=3)	15 nm	Minimum horizontal spacing of Vx - Full alignment
Vx.3b (x=3)	24 nm	Minimum vertical spacing of Vx - Full alignment
Vx.3 (x=4,5)	24 nm	Minimum spacing of Vx - Full alignment
Vx.3a (x=6)	40 nm	Minimum horizontal spacing of Vx - Full alignment
Vx.3b (x=6)	24 nm	Minimum vertical spacing of Vx - Full alignment
Vx.3 (x=7,8)	40 nm	Minimum spacing of Vx - Full alignment
Vx.3a (x=9)	40 nm	Minimum horizontal spacing of Vx - Full alignment
Vx.3b (x=9)	80 nm	Minimum vertical spacing of V9 - Full alignment
Vx.3 (x=10)	80 nm	Minimum spacing of V10 - Full alignment
Vx.3a (x=11)	80 nm	Minimum horizontal spacing of V11 - Full alignment
Vx.3b (x=11)	160 nm	Minimum vertical spacing of V11 - Full alignment
Vx.3 (x=12,VRDL)	160 nm	Minimum spacing of V12 - Full alignment
Vx.4 (x=1-12)		V_x should be enclosed between M_x and M_{x+1}
Vx.4 (x=VRDL)		V_x should be enclosed between M13 and RDL
Vx.5 (x=1,3,5,7,9,11,VRDL)	0 nm	Vx enclosure by Mx on two opposite sides, horizontal direction
Vx.5 (x=2)	3 nm	Vx enclosure by Mx on two opposite sides, horizontal direction
Vx.5 (x=4,6,8,10,12)	10 nm	Vx enclosure by Mx on two opposite sides, horizontal direction
Vx.6 (x=1,3)	3 nm	Vx enclosure by Mx on two opposite sides, vertical direction
Vx.6 (x=2,4,6,8,10,12)	0 nm	Vx enclosure by Mx on two opposite sides, vertical direction
Vx.6 (x=5,7,9,11,VRDL)	10 nm	Vx enclosure by Mx on two opposite sides, vertical direction
Vx.7 (x=1,3)	3 nm	Vx enclosure by M_{x+1} on two opposite sides, horizontal direction
Vx.7 (x=2,4,6,8,10,12)	0 nm	Vx enclosure by M_{x+1} on two opposite sides, horizontal direction
Vx.7 (x=5,7,9,11)	10 nm	Vx enclosure by M_{x+1} on two opposite sides, horizontal direction
Vx.7 (x=VRDL)	80 nm	VRDL enclosure by RDL in horizontal direction
Vx.8 (x=1,3,5,7,9,11)	0 nm	Vx enclosure by M_{x+1} on two opposite sides, vertical direction
Vx.8 (x=2)	3 nm	Vx enclosure by M_{x+1} on two opposite sides, vertical direction
Vx.8 (x=4,6,8,10,12)	10 nm	Vx enclosure by M_{x+1} on two opposite sides, vertical direction

Vx.8 (x=VRDL)	80 nm	VRDL enclosure by RDL in vertical direction
Vx.9 (x=1,2)	196 nm^2	Minimum area overlap between Mx and Vx
Vx.9 (x=3)	360 nm^2	Minimum area overlap between Mx and Vx
Vx.9 (x=4,5)	576 nm^2	Minimum area overlap between Mx and Vx
Vx.9 (x=6)	960 nm^2	Minimum area overlap between Mx and Vx
Vx.9 (x=7,8)	1600 nm^2	Minimum area overlap between M7 and V7
Vx.9 (x=9)	3200 nm^2	Minimum area overlap between M9 and V9
Vx.9 (x=10)	6400 nm^2	Minimum area overlap between M10 and V10
Vx.9 (x=11)	12800 nm^2	Minimum area overlap between M11 and V11
Vx.9 (x=12,VRDL)	25600 nm^2	Minimum area overlap between M12 and V12



2.17 RDL Layer

Rule	Value	Description
RDL.1	1.6 µm	RDL width minimum
RDL.2	1.6 µm	RDL spacing minimum



2.18 Other Rules

Rule	Value	Description
GRID	0.5 nm	Shapes on all layers must be on a 0.5 nm grid
ANTENNA	50:1	Ratio of Maximum Allowed (GATE or Metal Layer Area) to transistor Gate Area