ISSN 1063-7826, Semiconductors, 2016, Vol. 50, No. 1, pp. 66–82. © Pleiades Publishing, Ltd., 2016.
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SEMICONDUCTOR STRUCTURES, LOW-DIMENSIONAL SYSTEMS, AND QUANTUM PHENOMENA

Vertical Heterostructures Based on Graphene and Other 2D Materials

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Submitted April 1, 2015; accepted for publication April 2, 2015

Abstract—Recent advances in the fabrication of vertical heterostructures based on graphene and other dielectric and semiconductor single-layer materials, including hexagonal boron nitride and transition-metal dichalcogenides, are reviewed. Significant progress in this field is discussed together with the great prospects for the development of vertical heterostructures for various applications, which are associated, first of all, with reconsideration of the physical principles of the design and operation of device structures based on graphene combined with other 2D materials.

DOI: 10.1134/S106378261601005X

1. INTRODUCTION

Studying graphene-based heterostructures, especially vertical heterostructures, is currently the main direction in the development of thin-film (graphene) electronics [1, 2]. In recent times, vertical graphene-based heterostructures have been referred to as van der Waals heterostructures [3], since they are assumed to be formed by the sequential transfer of layers, which are retained in a single structure by van der Waals forces only. The first heterostructures involved hexagonal boron nitride (hBN) and graphene layers [4–7]. In recent studies [8–10], heterostructures with transition-metal dichalcogenides ($NbSe_2$, MoS_2, WS_2, WSe_2, TaS_2, etc.) have been investigated [8–10]. Several types of such heterostructures fabricated and studied to date have already revealed the huge potential for development in this direction. An important achievement of the developed heterostructures is their demonstration of the possibilities of new physical approaches and principles in device-structure fabrication, which differ from traditional approaches of silicon electronics and, using proper design solutions, make it possible to easily eliminate the limitation imposed on the fabrication of transistors based on graphene due to the lack of a band gap in it.

In addition, here we discuss another approach to the fabrication of heterostructures which uses multilayer (up to 10 layers) graphene with a thickness of a few nanometers, intercalation, and chemical functionalization to modify the properties of graphene [11–14]. Such an approach makes it possible to form certain functional units from several single layers of graphene (multilayer graphene) to fabricate more complex heterostructures.

We review the main experimental studies on the creation of vertical heterostructures based on graphene and other 2D materials.

2. HETEROSTRUCTURES CONTAINING GRAPHENE AND HEXAGONAL BORON NITRIDE

At present, hexagonal (graphite-like) boron nitride is considered the main complementary material to graphene, which, in particular, is used as a substrate to ensure high carrier mobility in graphene. The presence of defects and tunneling currents through hBN layers of different thicknesses were studied in [6]. Figure 1 shows the measurement scheme used in [6], atomic force microscopy (AFM) data, and a plot of the tunneling current through 1–4 hBN layers. One can observe atomic smoothness of the hBN surface, the absence of defects, high homogeneity of the tunneling currents through hNB, and an exponential decrease in the current with increasing number of singlelayers. Atomic force microscopy and scanning tunneling spectroscopy investigations [15] showed smoothness and homogeneity of the surface, and also low ($\sim 3 \times 10^{10}$ cm^{-2}), as compared with SiO_2, and hBN charge uniformly distributed at the nanoscale. As was shown in [16], the roughness of hBN or graphene on hBN is lower than that of SiO_2 by a factor of three. The barrier for carrier tunneling through hBN (3.07 eV) and the dielectric strength of the layer (7.94 MV/cm) were determined in [17]. For comparison, the height of the barrier for carrier tunneling through SiO_2 is 3.25 eV [18] and the dielectric strength is 8–10 MV/cm [19]. The band gap of hNB is 5.2–6.0 eV [19, 20], the dif-

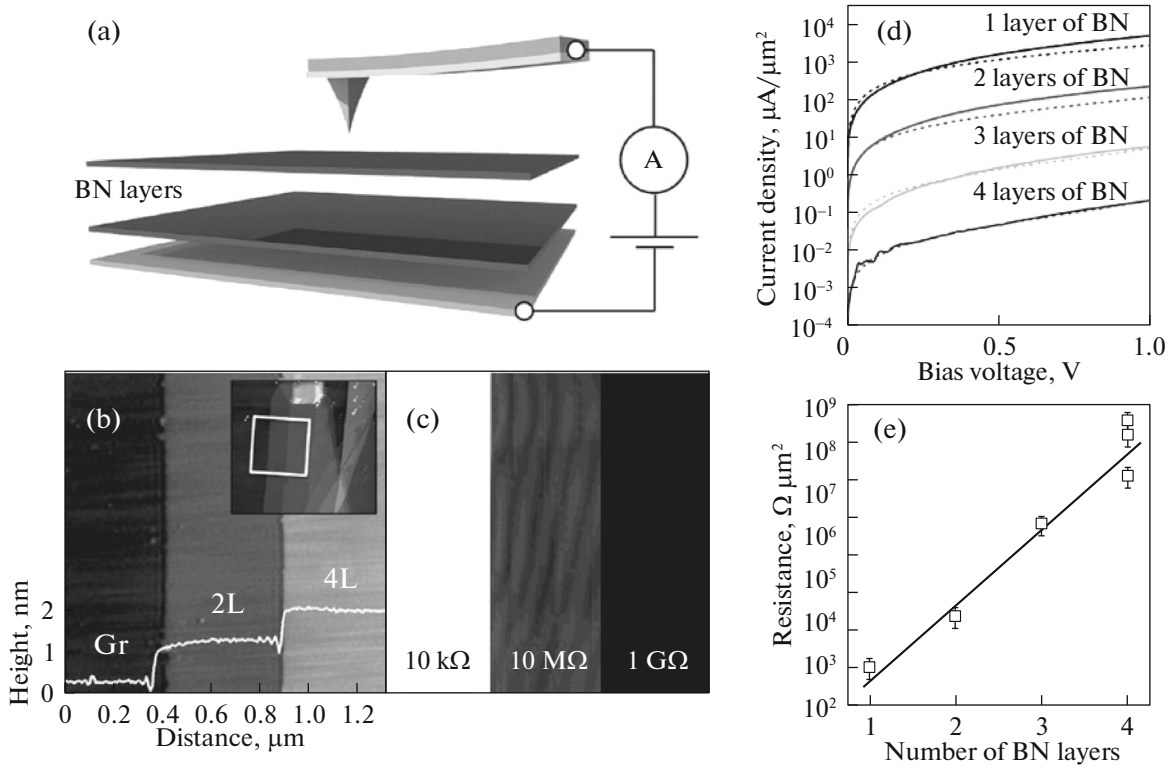

Fig. 1. (a) Scheme for AFM study of the properties of hBN. hBN layers were formed by mechanical stratification from a bulk crystal. (b) Surface morphology of graphite/hBN heterostructures with thicknesses of 2 and 4 SLs. The insets show an enlarged image of the structure and surface profile demonstrating the layer thickness. (c) Leakage-current map for the same structure. (d) I–V characteristics for the graphite/hBN/graphite structures with different hBN thicknesses [6].

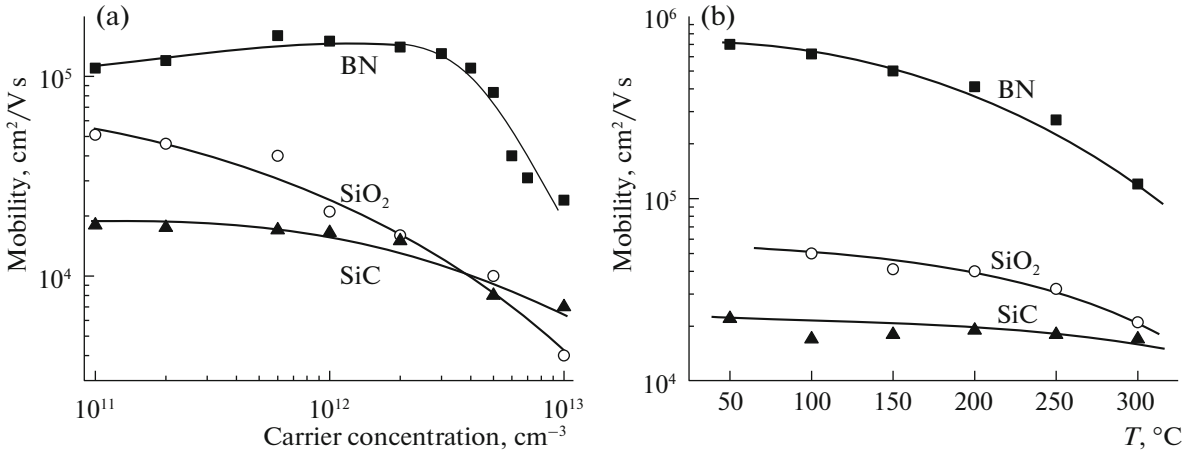

Fig. 2. Calculated dependences of the carrier mobility in graphene on substrates of three types on (a) the carrier concentration and (b) temperature. Calculation was performed using the Monte Carlo method taking into account scattering at phonons and interaction with the substrate [22].

ference between the lattice parameters of hBN and graphene is merely 1.7% (the lattice constants of hBN and graphene are 2.50 and 2.46 Å, respectively) [21], and the estimated hBN single-layer thickness is 0.33 nm [6, 15]. In addition, it is worth noting that the properties of this material are stable.

The deposition of graphene onto hBN substrates leads to a significant increase in the carrier mobility in graphene. The extent of this effect depends on the quality of graphene and hBN. The calculated dependences of the mobility on temperature, the carrier density, and the structure type from [22] are presented

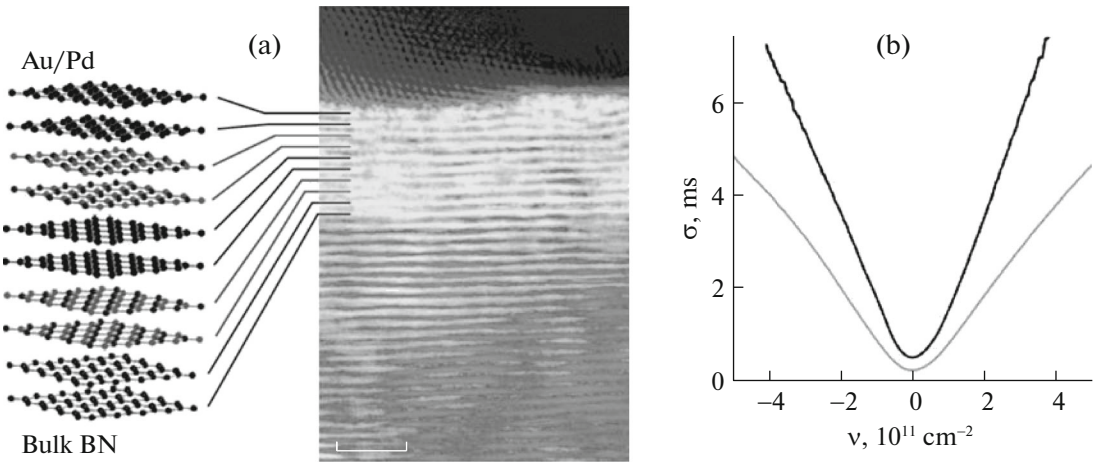

Fig. 3. (a) Cross section of a multilayer heterostructure with graphene and hBN layers (the total structure thickness is 40 nm and the hBN layer thickness is 4–5 nm) and (b) conductivity of the lower graphene layer (black curve) and upper graphene layer (red curve) in the structure [7].

in Fig. 2. The experimental room-temperature carrier mobility in the case where layers are formed by mechanical stratification lies, as a rule, between 35000–100000 $cm^2/(V\ s)$ [5, 23, 24]. For graphene with large (100–300 μm) single-crystal domains grown by the chemical vapor deposition (CVD), the carrier mobility within a domain is 20000–45000 $cm^2/(V\ s)$ [16, 25, 26].

In a polycrystalline CVD graphene film, the carrier mobility is significantly lower and usually is no larger than few thousand [27, 28]. It is worth noting study [29] on growing graphene on CVD hBN, which will hopefully allow the required heterostructures to be grown in the future.

The first multilayer heterostructure consisting of alternating graphene (or bigraphene) and hBN layers was fabricated and investigated previously [7]. The total structure thickness was 40 nm and the hBN layer thickness varied between 4–5 nm (Fig. 3). To measure the conductivities of the layers and determine the carrier mobility, contacts to the lower and upper graphene layers were formed. The carrier mobility was found to be 60000 $cm^2/(V\ s)$ in the upper layer and 120000 $cm^2/(V\ s)$ in the lower layer (the measurement temperature was $T = 4.2$ K). Thus, if graphene has hBN layers on both sides, its carrier mobility is significantly (by a factor of about two) higher than when graphene simply lies on a hBN layer. The authors of [5] proposed a new approach for creating graphene-based transistors with the use of multilayer hBN/graphene heterostructures. In transistor structures with a graphene channel in the conventional device configuration, the absence of a band gap in graphene, high conductivity near the neutrality point, and the Klein effect led to high currents in the OFF state and did not allow significant current modulation to be obtained (the current ratio in the transistor ON and OFF states is, as a rule, $I_{on}/I_{off} < 10$). The transistor design proposed in [5] involves two graphene layers separated by a tunneling-transparent boron nitride or MoS_2 (Fig. 4) layer. The authors showed that current flow is ensured by the tunneling of holes with an effective mass of $\sim 0.5m_0$, where m_0 is the free-electron mass, which corresponds to the effective hole mass in hBN. Investigation of the current flowing across the structure showed that current modulation by the voltage at the silicon substrate (gate) is much stronger than in the planar transistor structure. The time of carrier tunneling through the hBN layer was a few femtoseconds, which is much shorter than the time of electron passage in silicon field-effect transistors. Varying the hBN-layer thickness the authors found that the optimal thickness is 4–7 SLs (single layers). It was shown that at this thickness the current ratio I_{on}/I_{off} can reach $\sim 10^4$. However, structures with a hBN thickness of 4–7 SLs require a high gate voltage (up to 50 V). The structures with a hBN layer thickness of 2–4 SLs allow the gate voltage to be reduced, but, in this case, the ratio I_{on}/I_{off} is reduced as well.

Britnell et al. [30] investigated carrier tunneling through a hBN layer located between two graphene layers and showed the possibility of creating tunneling-diode structures with nonlinear current–voltage (I–V) characteristics. Figure 5a shows a schematic representation of the obtained structure and the circuit of voltage application to it. The hBN layer with the formed structure incompletely screens graphene electrodes from the substrate; therefore, the graphene-electrode potential can be controlled by voltage applied to the silicon substrate. Figures 5b and 5c show the I–V characteristics as functions of the voltage between the graphene electrodes at temperatures of 6–300 K and different voltages at the silicon substrate. The most important feature of these characteristics is

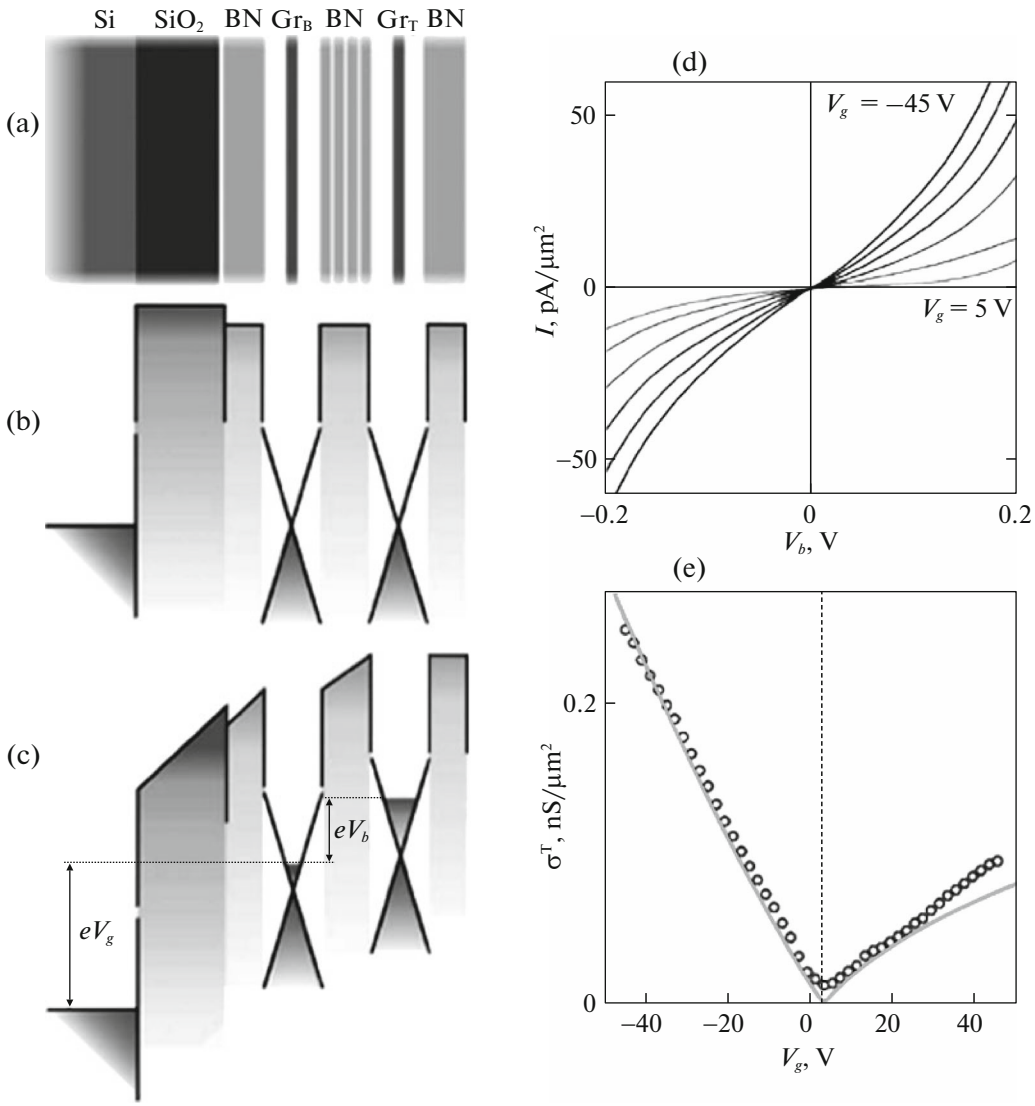

Fig. 4. (a) Cross section of a field-effect transistor. Band diagram of this transistor in (b) zero and (c) nonzero applied voltage. (d) Characteristics of the device with 6 hBN single layers: the drain–source current at different gate voltages and (e) transfer functions measured at zero drain voltage. Circles correspond to the experiment and the curve corresponds to the simulation. The measurement temperature was 240 K [5].

their nonlinearity, i.e., negative differential voltage regions, whose position depends on the substrate voltage. Depending on the substrate voltage, the maxima in the I–V characteristics are observed at positive or negative voltages between the graphene electrodes under conditions when the positions of the Dirac points in the graphene electrodes are equalized in terms of their potential (the resonance condition, see the inset in Fig. 5b). Depending on the combination of voltages V_b and V_g, resonance conditions are met twice at positive or negative and zero V_b (see the simulation results in Fig. 5c, modes (i) and (ii)) and the maximum current is observed only at high electron density at one of the graphene electrodes (see the inset in Fig. 5b, mode (ii)). The nonlinear room-temperature characteristics make these structures interesting for application. In addition, it is worth noting that the absence of current peaks in similar structures investigated in [5] is related to lower voltages. The nonlinear I–V characteristics of tunneling-diode structures were theoretically predicted by Feenstra et al. [31, 32], where the graphene structure (size and planar misorientation of single-crystal grains) was taken into account. It was shown there that the positions of the current maxima depend only slightly on temperature, which was confirmed experimentally.

The generally good combination of graphene and hBN in terms of high carrier mobility in graphene and the interesting properties of vertical structures formed from graphene and hexagonal boron nitride have

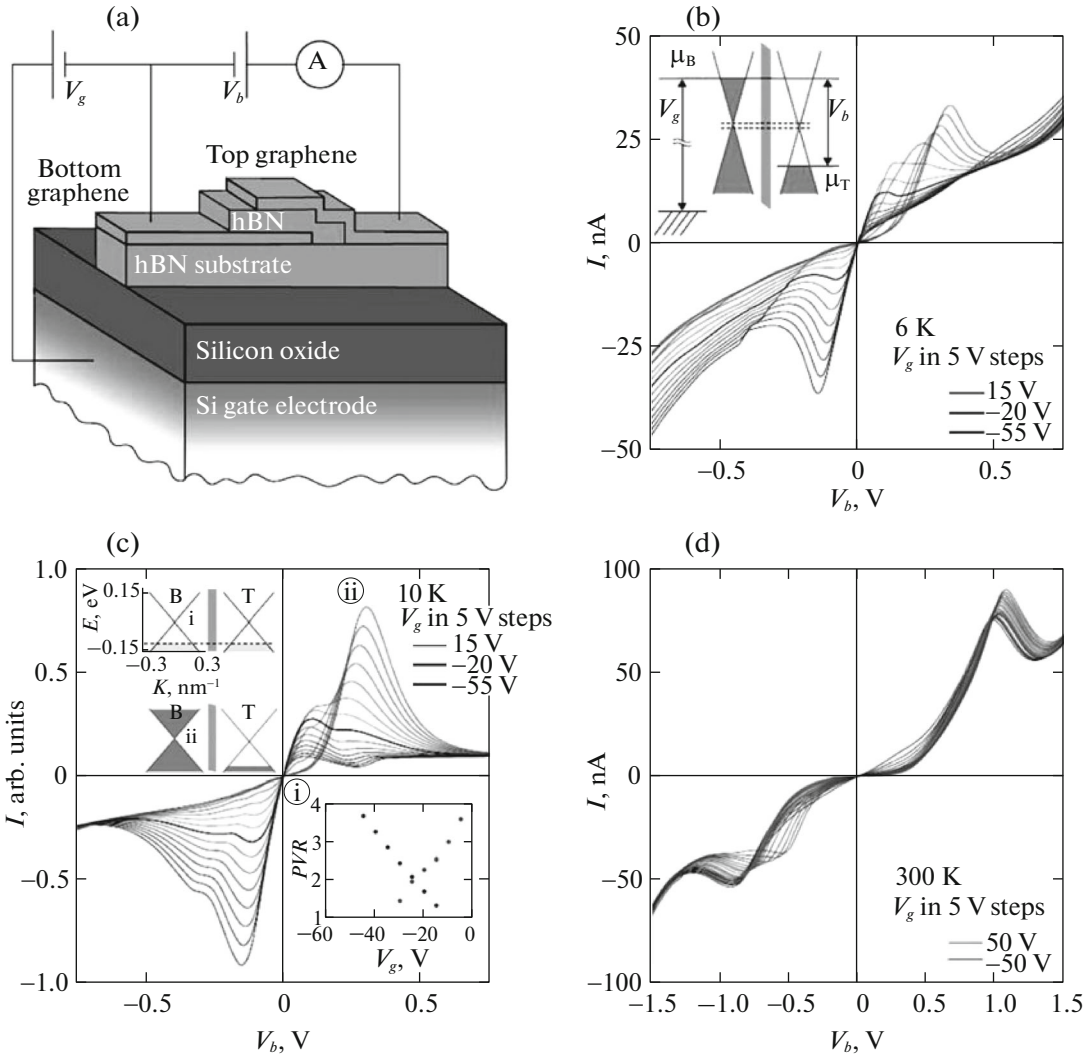

Fig. 5. (a) Schematic representation of the investigated device structure. (b) I–V characteristics of the tunneling current through a hBN layer with a thickness of 4 SLs as measured at a temperature of 6 K and (d) the same characteristics for a structure with a thickness of 5 SLs as measured at a temperature of 300 K. The inset in Fig. 5b: schematic of the origination of the resonance current, when the positions of the Dirac points in the graphene electrodes are equalized in potential at a certain gate (silicon substrate) voltage. (c) Simulated currents in the structure. The inset in Fig. 5c: band diagrams for zero voltage and maximum current and dependences of the maximum current on the silicon-substrate voltage [30].

caused great interest in this system. As a result, taking into account advances in the CVD growth of graphene and hBN layers and in the growth of lateral heterostructures with abrupt boundaries [33, 34], significant progress in the fabrication and application of graphene–hBN heterostructures can be expected in the near future.

Low-temperature investigations showed that the weak van der Waals interlayer interaction in the heterostructures consisting of graphene and hexagonal boron nitride makes the two graphene sublattices nonequivalent. As a result, the linear electron dispersion law changes from linear to quadratic (electrons acquire mass) and an energy gap of ~30 meV arises in the energy spectrum [35]. It is believed that the possibility of local variation in the effective carrier mass opens up a new way of fabricating quantum dots and wires in graphene.

3. HYBRID HETEROSTRUCTURES FORMED BY INTERCALATION

Let us consider an alternative to high-resistivity hybrid substrates, which ensure high carrier mobility in graphene. As is known, the maximum carrier mobility (up to 100000–200000 cm^2 V^{-1} s^{-1}) is observed in suspended graphene [36, 37]. A SiO_2 substrate which is the easiest to manufacture haltscarrier mobility in graphene because of carrier scattering at relatively large nonuniformly distributed SiO_2 charge

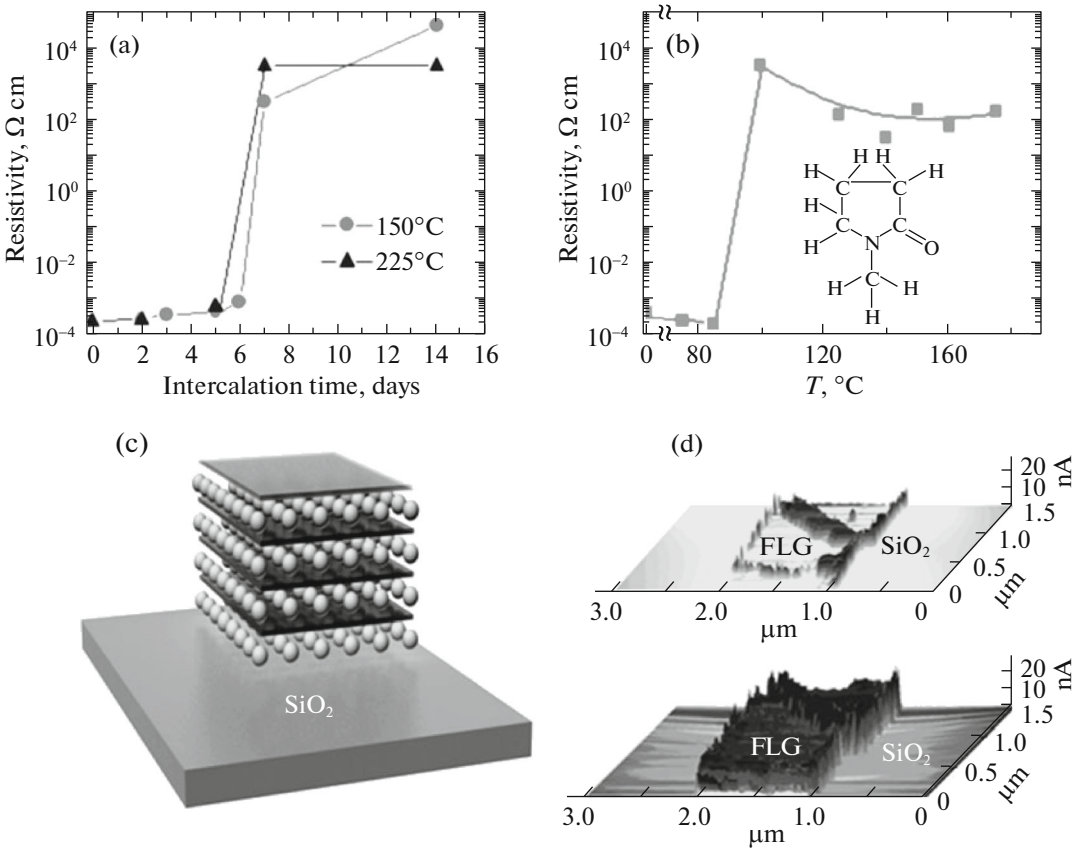

Fig. 6. (a) Resistivity of the intercalated multilayer-graphene layer with a thickness of 5 μm as a function of intercalation time at different annealing temperatures. (b) Annealing–temperature dependence of the layer resistivity for an annealing time of 5 min. Inset: schematic representation of an *N*-methylpyrrolidone molecule. (c) Schematic representation of graphene with a high carrier mobility on the high-resistivity hybrid substrate. (d) Current maps measured with an AFM probe before (at the top) and after (at the bottom) treatment in HF vapors. The probe voltage during measurements of the current maps was 50 mV and the threshold current was 25 nA.

[38, 39], surface phonons [40, 41], and surface roughness [42, 43]. Typical carrier-mobility values for polycrystalline graphene on SiO_2 are 2000–6000 $cm^2/(V s)$ [44, 45] and the record values for graphene single crystals are 10000 and 16000 $cm^2/(V s)$ [46, 47]. As was shown above, at present hexagonal boron nitride is considered the most suitable substrate for graphene.

We proposed the use of other substrates for graphene, which ensure high carrier mobility. Such substrates are high-resistivity layers obtained by the intercalation of *N*-methylpyrrolidone (NMP) molecules with subsequent annealing at temperatures of 100–180°C [11, 48]. Figure 6 shows the schematic representation of such a substrate and the results of investigations of its properties. The initial material used for implementing our approach was multilayer graphene with a thickness of a few nanometers. Figure 6a shows that it is necessary to form single layers from NMP molecules in order to ensure a sharp increase in the resistivity of graphene upon subsequent annealing. It is worth noting that, from the technological point of view, it is more convenient to form the desired elements first by lithography to obtain a certain multilayer-graphene width for structure formation and then perform intercalation and annealing. The resistivity of the layers annealed at temperatures of 100–180°C is higher than that of graphene by six–seven orders of magnitude. The resistivity increase is caused by the interaction between NMP and the multilayer-graphene layers. As a result, we obtain a stable atomically smooth high-resistivity substrate. Then, to form a graphene layer on the hybrid substrate, it is sufficient simply to clean the upper layer and recover its conductivity [14]. The NMP was removed in hydrofluoric-acid HF vapors or an aqueous solution.

When the initial material was graphene, its conductivity was completely recovered after cleaning of the single-layer surface (the resistivity decreased from 3.5×10^8 to 32 Ω/□, i.e., by seven orders of magnitude). The measurements performed on these structures using two- and four-contact circuits showed a resistance difference of less than 10%. The mobility determined from the transfer characteristics increased from 650 to 11000 $cm^2/(V s)$ for holes and from 50 to

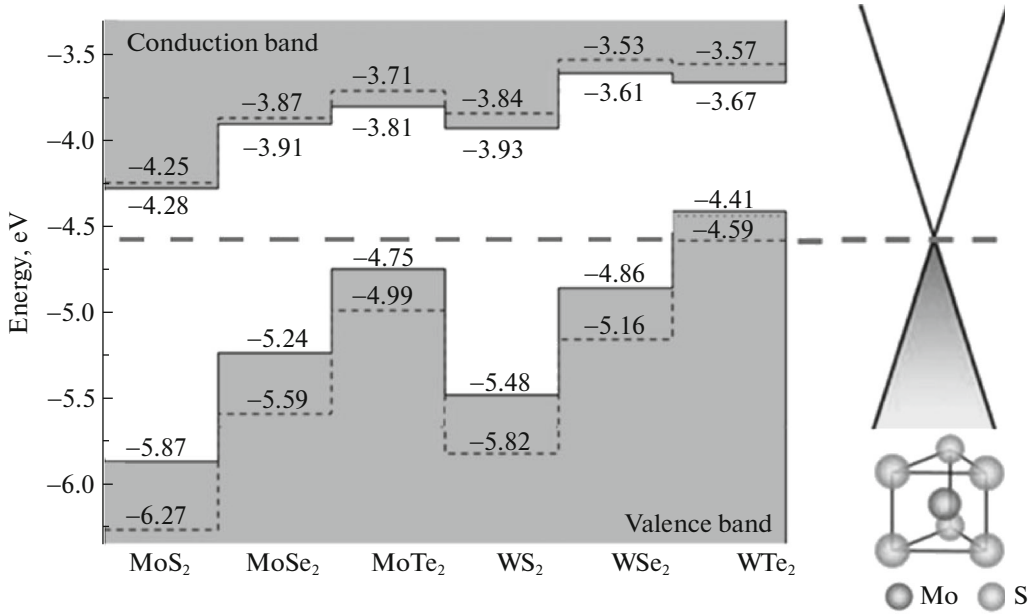

Fig. 7. Calculated energy-band structure for single layers of different transition-metal dichalcogenides and graphene. Blue and black numerals and band boundaries correspond to the different calculation techniques [55]. Energies are calculated from the level of an electron in free space. The inset shows the MoS_2 single-layer structure. The MoS_2 monolayer thickness is ~0.65 nm.

40000 cm^2/(V s) for electrons. For layers with thicknesses of 2–4 nm treated in HF vapors or an aqueous solution, the resistance of the structure decreased by two–four orders of magnitude, which indicates incomplete (one-sided) cleaning of the upper layer. The best maximum mobility values for electrons (17000–41000 cm^2 V^{-1} s^{-1}) were observed in the structures annealed at temperatures of 140–160°C [14]. The hole mobilities were somewhat lower. It is worth noting that, after recovery of the conductivity in the upper layer, current modulation by the gate (silicon substrate) voltage by four orders of magnitude was observed, which is related to the residual chemical modification of graphene. Figure 6c shows direct evidence of the increase in the surface conductivity after HF treatment: current maps obtained using an AFM probe. Raman scattering and scanning-electron and atomic-force microscopy data showed that the recovered layers are almost free of defects and have a conventional surface morphology after the complete cycle of chemical and temperature treatments, which makes them promising for further application. The high current modulation in the recovered graphene layer originates, most likely, from incomplete cleaning of the layer (the presence of tunneling-transparent barriers for carriers) or, possibly, from carrier tunneling between the hybrid substrate layers under applied silicon-gate voltage.

The observed considerable growth in the carrier mobility in the upper graphene layer on the hybrid substrate after recovery of its conductivity is related to the low charge in the hybrid substrate and the screening of charges in the SiO_2/Si substrate by this layer. It is of interest to compare the mobilities obtained by us with the values for the hBN substrates: our values of 17000–41000 cm^2/(V s) are close to the room-temperature mobilities for the hBN substrate. In addition, it should be noted that our approach allows the formation of a functional unit (substrate ensuring high mobility and a graphene layer on its surface) straightaway, which is convenient for the creation of more complex vertical heterostructures.

Another variant of hybrid heterostructures formed by the intercalation of NMP in multilayer-graphene is a superlattice of hydrogenated graphene and NMP single layers [11, 49]. Hydrogenated layers after intercalation were formed by annealing at higher temperatures (200–250°C). During such heat treatments, NMP oligomers formed and the molecules were dehydrogenated. This resulted in the occurrence of free hydrogen atoms in the graphene interlayer space, which interact with the nearest graphene layers and lead to its hydrogenation. The maximum degree of hydrogenation was observed at annealing temperatures of 225–250°C. It was found that such structures have a band gap (up to 2.7 eV) and are characterized by relatively high mobility (up to 10000 cm^2 V^{-1}). However, the long-term stability of such structures, as in ordinary hydrogenated graphene [50], is limited.

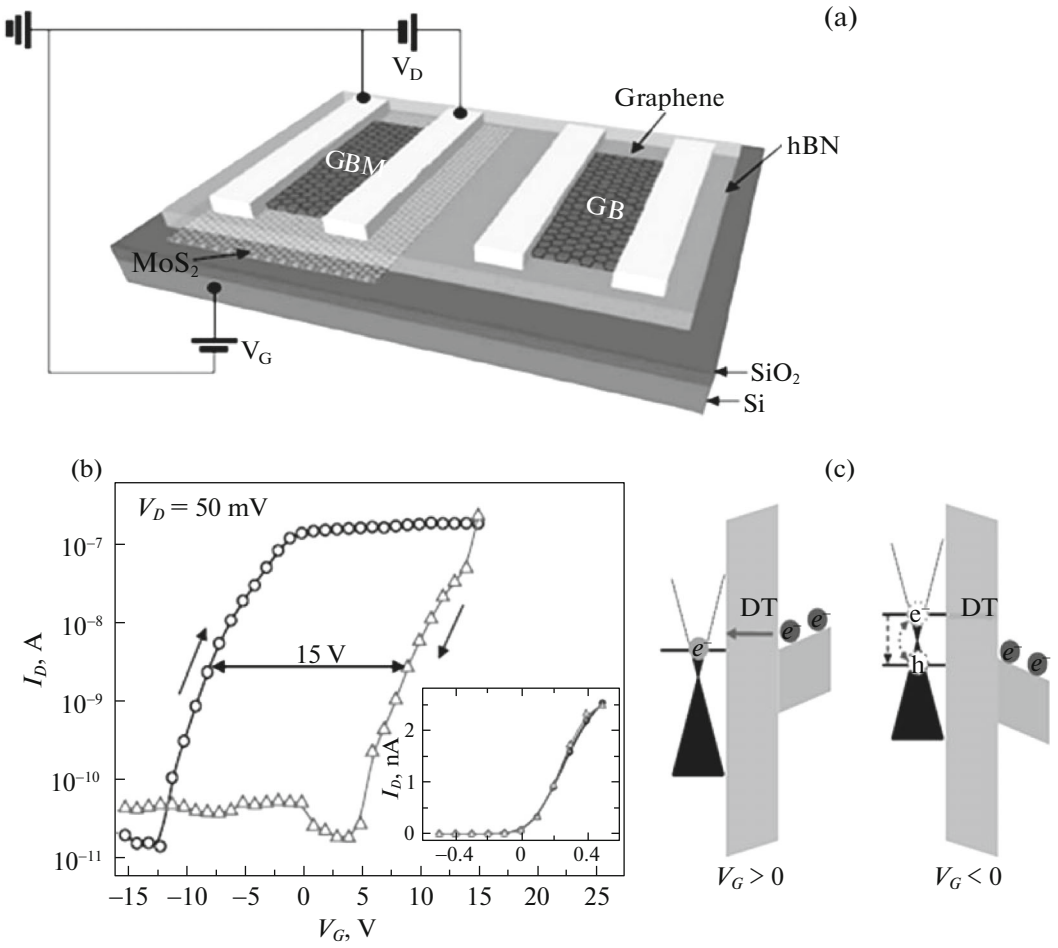

Fig. 8. (a) Schematic representation of the MoS_2/hBN/graphene heterostructure and hBN/graphene test structure. (b) Current in graphene as a function of the gate (silicon substrate) voltage for the investigated and test (inset) structures as measured in two voltage scan directions. The hBN and MoS_2 layer thicknesses are 12 nm and 3 SLs, respectively. (c) Band diagrams of the structure for the recording ($V_g > 0$) and erasing ($V_g < 0$) m odes [63].

4. HETEROSTRUCTURES WITH TRANSITION-METAL DICHALCOGENIDES

Transition-metal dichalcogenides ($NbSe_2$, MoS_2, WS_2, WSe_2, TaS_2, etc.) belong to layered compounds, which, similar to graphite, can be divided into separate single layers. Transition-metal dichalcogenides have the same structure: a single layer includes three layers, among which the two edge layers consist of sulfur or selenium atoms and the intermediate layer, of transition-metal atoms [51]. The estimated single-layer thickness is 0.65 nm. The properties depend on the composition and thickness and change from metal to semiconductor ones. In particular, it was shown that the transition to a single layer is accompanied by a transition from the indirect to direct energy-band structure with some band-gap broadening [52], which manifests itself in considerable enhancement of the photoluminescence of the single layers observed in MoS_2, $MoSe_2$, WS_2, and WSe_2 [53, 54]. The calculated band gaps for some of these compounds, their mutual arrangement, and compatibility with graphene are illustrated in Fig. 7 using the data reported in [55].

First, MoS_2 layers and transistors fabricated on their basis were investigated. The mobility values obtained for the transistor structures were no larger than 200–350 $cm^2/(V\ s)$, whereas the current ratios I_{on}/I_{off} reached 10^7–10^{10} [56, 57]. For MoS_2 layers on a SiO_2/Si substrate, a pronounced hysteresis was observed in the I–V characteristics of the structures [58, 59]. Attempts to enhance the carrier mobility in the MoS_2 layers showed that the use of polymethylmethacrylate (PMMA) as a substrate for MoS_2 increases the carrier mobility to 480 $cm^2/(V\ s)$ [59]. This value is characteristic of relatively thick (~50 nm) MoS_2 layers. The use of PMMA substrates allows hysteresis in the I–V characteristics to be avoided. Thus, transistors on flexible PMMA substrates are currently the best versions for the realization of a transistor

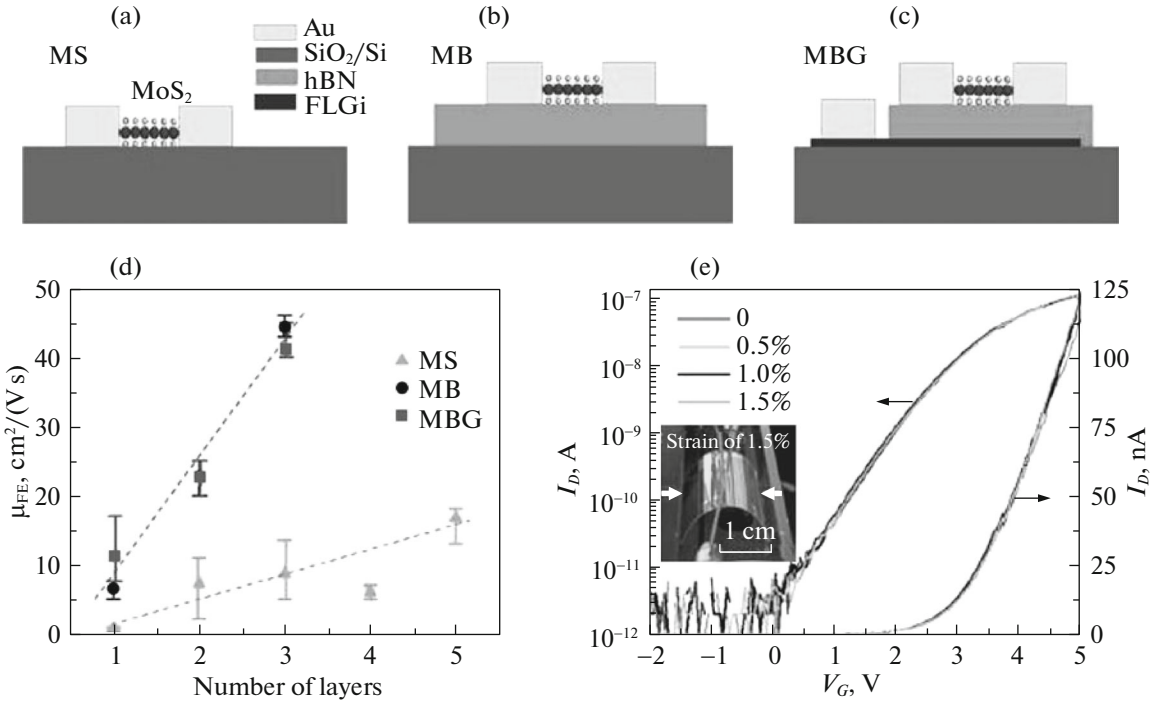

Fig. 9. (a–c) Schematic representations of the investigated MS, MB, and MBG field-effect transistors on a flexible substrate. (d) Dependences of mobility in the channel of a transistor on a SiO_2/Si substrate on the number of MoS_2 monolayers. (e) *I–V* characteristics of a transistor on a flexible substrate as measured upon substrate bending to a value corresponding to 1.5% extension. The inset shows the device structure bent to a stress of 1.5% [65].

based on MoS_2 layers [59]. Other device structures successfully implemented on the basis of MoS_2 layers are logic elements [60], a phototransistor [61], and a high-sensitivity photodetector [62].

The MoS_2 single layer in combination with graphene was used to fabricate heterostructures with the memory effect [63]. Figure 8a shows the schematic representation of a MoS_2/hBN/graphene structure. The second test structure formed for comparison contained no MoS_2 layer. As is known, the MoS_2 work function is 4.6–4.9 eV, the MoS_2 band gap is 1.3 eV, the MoS_2 electron affinity is 4.2 eV, the hBN electron affinity is 2–2.3 eV, the hBN band gap is 5.2–5.9 eV, and the graphene work function is 4.6 eV. According to these data, the carrier exchange between MoS_2 and hBN layers should occur via electron tunneling. To facilitate hole tunneling, extremely high voltages are required. The band diagrams for the recording ($V_g > 0$) and erasing ($V_g < 0$) modes are presented in Fig. 8c. In the structure containing the MoS_2 layer, significant current hysteresis is observed (Fig. 8b), which is related to the trapping or emission of a charge at/from the MoS_2 layer. In the test structure without a MoS_2 layer, hysteresis was not observed. The MoS_2- and hBN-layer thicknesses were 3–5 SLs and 6–12 nm, respectively. The MoS_2 layer serves as an electron source or drain during recording and erasing. The use of voltage pulses with a duration from 1 ms to 6 s for recording allowed us to determine the rate of carrier trapping at the MoS_2 layer. It was found to be 10^{11}–10^{13} cm^{-2} s^{-1}, which is higher than values of 10^9 cm^{-2} s^{-1} typical of metal–insulator–semiconductor systems [64]. The authors believe that such heterostructures can be created and applied in memory cells on flexible substrates [63].

A field-effect transistor with a MoS_2 channel, a hBN gate dielectric, and a graphene gate was fabricated and studied in [65]. This transistor and other test transistors were formed on both SiO_2/Si and flexible substrates. Schematic representations of the structures and dependences of the carrier mobility in the channel on the channel thickness (number of MoS_2 layers) for the case of the SiO_2/Si substrate are presented in Fig. 9. It can be seen that the carrier mobility increased with the MoS_2-layer thickness, but was no higher than 45 cm^2/(V s), although, in general, placement of the MoS_2 on the hBN layer yielded higher mobility values than on SiO_2/Si. In addition, structures on a polyethylene naphthalate (PEN) substrate with a thickness of 127 μm were fabricated and investigated. It was an MBG structure with three MoS_2 monolayers and a hBN thickness of 35 nm. The carrier mobility in such a structure was 29 cm^2/(V s). The working ability of the structure was tested by substrate

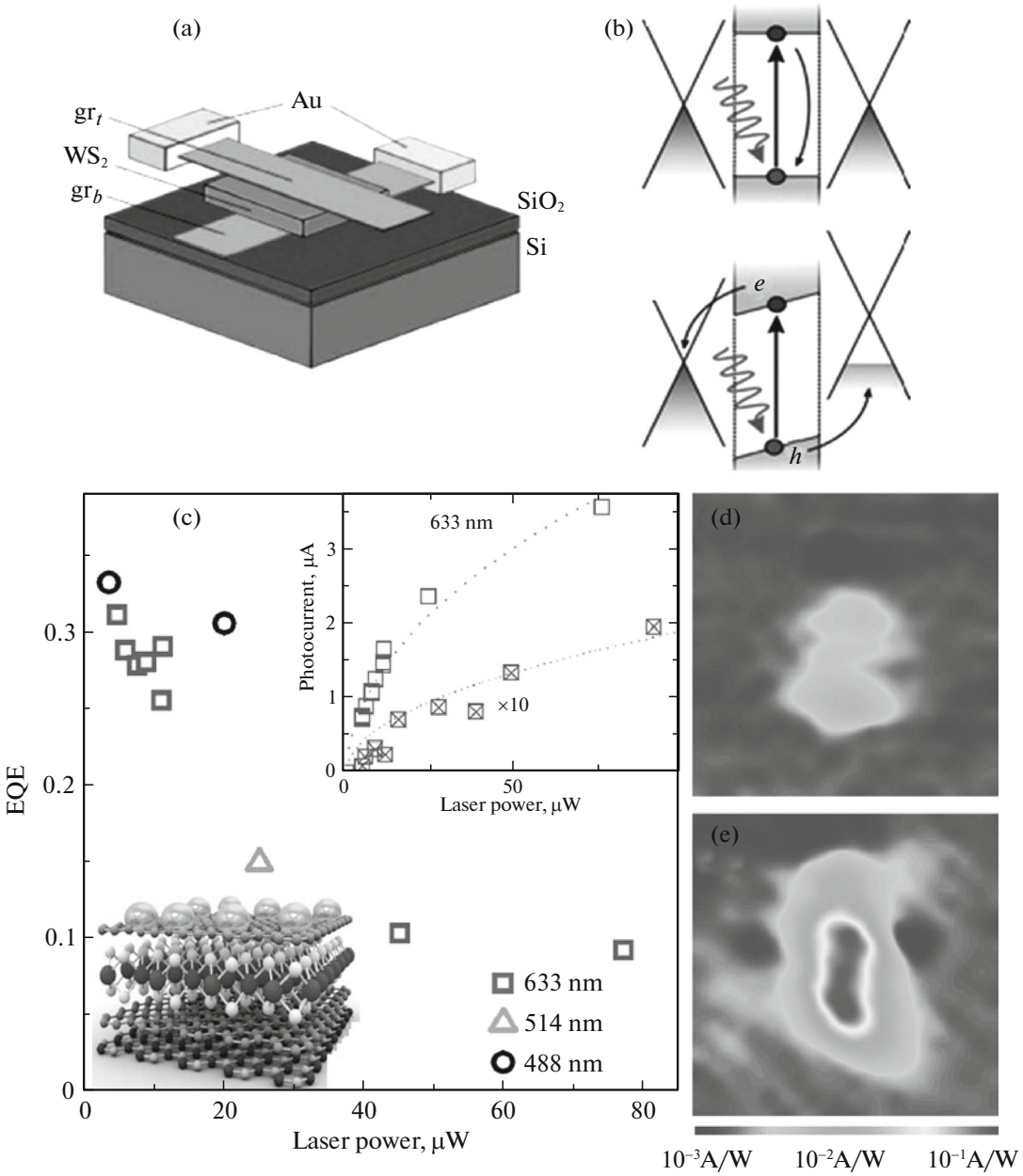

Fig. 10. (a) Schematic representation of the graphene/WS2/graphene structure. The hBN layer placed between the SiO_2/Si substrate and graphene is not shown. (b) Band diagram of the structure with an applied voltage for the separation of carriers and without voltage. (c) External quantum efficiency (EQE) as a function of the excitation-laser power. First inset: dependence of the photocurrent on the excitation-laser power (open symbols correspond to structures on a SiO_2/Si substrate and crosses correspond to structures on a flexible substrate). Second inset: hBN/graphene/MoS_2/graphene structure (upward) with a cavity made of gold nanoparticles. (d, e) Photocurrent map for the hBN/graphene/MoS_2/graphene structure without (at the top) and with (at the bottom) gold particles on the surface. The map size is 14 × 14 μm [10].

bending (see the inset in Fig. 9e). It was shown that bending corresponding to 1.5% extension does not change the parameters of the transistor. In addition, the analysis showed that the transparency of such structures was ~95% (2.3% is absorption in graphene and 2–5% is absorption in MoS_2; absorption in hBN in the visible range can be disregarded [66]). Such structures can be used in flexible electronics and, in particular, can replace logic elements in flexible displays. At present, logic elements in flexible displays are formed using amorphous silicon structures with a required carrier mobility of no lower than 10 $cm^2/(Vs)$. In addition, it is worth noting that the carrier mobility in transistors on a flexible substrate obtained in [65]

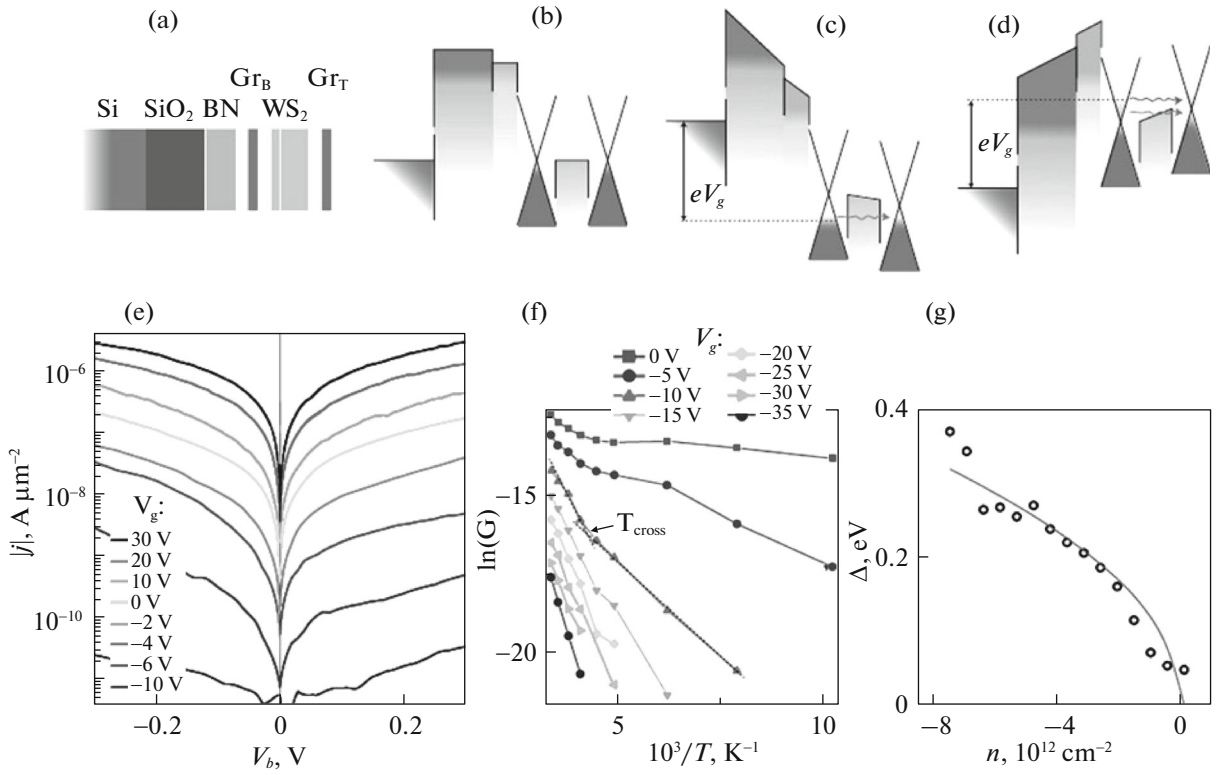

Fig. 11. (a) Schematic representation of a vertical transistor and (b, c, d) its energy-band diagrams at different applied voltages. A gate voltage V_g was applied between the silicon substrate and lower graphene layer; voltage V_b was applied between the two graphene layers. (e) The I–V characteristics of the structure measured at different gate voltages. (f) Temperature dependences of the current at different gate voltages. Using the slope of these dependences, the effective tunneling-barrier height (Fig. 11g) was calculated as a function of the carrier density Gr_B in the lower graphene layer [71].

and their transparency are at a record high as compared with a frequently observed mobility of 4–12 $cm^2/(V\,s)$ and a transparency of ~60% [67, 68].

Britnell et al. [10] demonstrated the possibility of creating photovoltaic heterostructures with a high quantum efficiency using WS_2, WSe_2, or MoS_2 layers. The heterostructures had the composition of graphene/WS_2 (WSe_2 or MoS_2)/graphene insulated by a hBN layer from below. A schematic representation of the fabricated structures and an energy-band diagram for one of the structures are presented in Fig. 10. Charge carriers are generated by a laser in the semiconductor (WS_2, WSe_2, or MoS_2) layer and, if a voltage is applied to the structure, they are separated and accumulate in different graphene layers. The internal quantum efficiency, i.e., the ratio between the number of separated electron–hole pairs and the number of incident photons) for the graphene/WS2/graphene structures was 0.2–0.3 at an excitation-laser power of up to 10 μW (Fig. 10c). A similar effect was observed in the hBN/graphene/MoS_2/graphene structure. In addition, it was shown in [10, 69] that the photocurrent can be increased even more by using an optical cavity to enhance the absorption of light. The cavity was formed from a hBN layer on a SiO_2/Si substrate and gold nanoparticles on the surface of a hBN/graphene/MoS_2/graphene heterostructure. A simple increase in the thickness of the absorbing substance (WS_2 or MoS_2) does not yield a significant effect, since the field separating the carriers weakens and recombination channels are enhanced. The deposition of gold nanoparticles onto the structure surface results in photocurrent growth by about an order of magnitude. A similar technique was used in [70] for creating a high-sensitivity graphene phototransistor. A layer of PbS quantum dots of different sizes was deposited onto the surface of graphene. The obtained phototransistor yielded a gain of up to 10^8 electrons per incident photon.

A vertical tunneling transistor for flexible electronics was fabricated using a hBN/graphene/WS2/graphene heterostructure in [71]. A schematic representation and band diagrams with and without voltage applied to the structure are shown in Fig. 11. The current in this structure consists of tunneling current through the barrier formed in WS_2 and thermionic current in WS_2. Upon transition to a single layer, WS_2 changes from an indirect-gap material with a band gap of 1.4 eV to a direct-gap material with a band gap of 2.1 eV [55, 72]. The use of

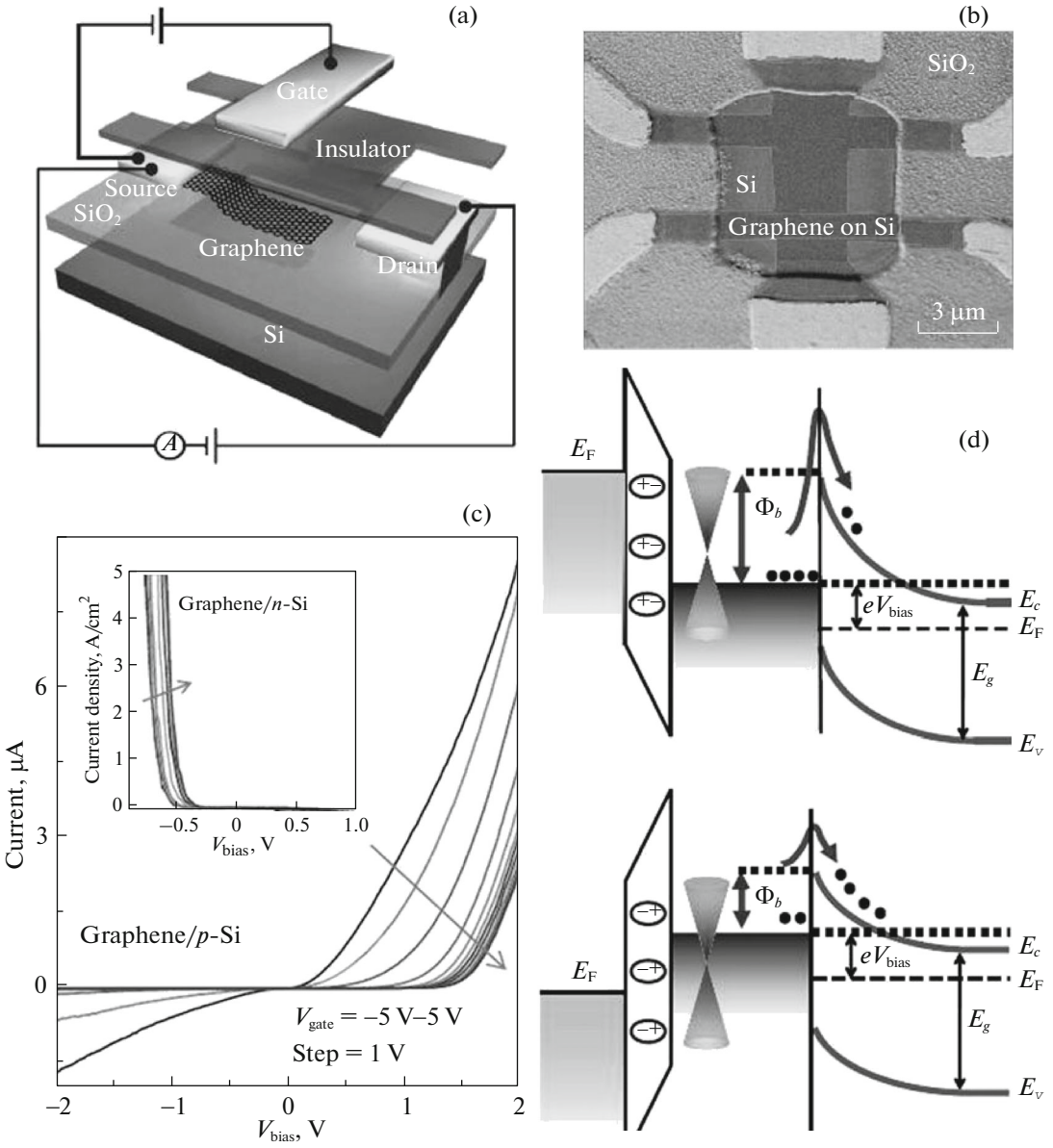

Fig. 12. (a) Schematic and (b) external appearance of graphene-on-silicon heterostructures. (c) Current in graphene for *p*- and *n*-Si (inset) at different gate voltages. (d) Energy-band diagrams of the barrier structure at different gate-voltage polarities [74].

such a tunneling-barrier material with a narrower band gap as compared with hBN allowed the transistor characteristics to be significantly improved. Depending on the applied voltage, the effective height (Fermi-level shift in graphene) and width (shape variation) of the tunneling barrier change. Thus, a current modulation of 10^6 and high current in the transistor ON state were observed for the first time. The currents observed in the transistor at different gate voltages are presented in Fig. 11d. The effective barrier height, which determines the current in the structure, was obtained from temperature dependences of the current (Fig. 11e) and the dependence of the effective barrier height on the carrier density in the lower graphene layer is shown in Fig. 11. The vertical tunneling transistor was formed not only on a SiO_2/Si substrate, but also on a flexible polymer (polyethylene terephthalate (PET)) substrate. In the latter case, the gate was sputtered onto the rear side of the polymer substrate. The conductivity of such a structure appeared to be stable against substrate bending up to extensions of ~2% and then somewhat decreased. The current modulation in such a transistor was weaker due to the larger thickness of the flexible substrate, which served as a gate insulator. In general, transistors with the WS_2 barrier showed better characteristics as compared with those of structures with MoS_2 or hBN barriers.

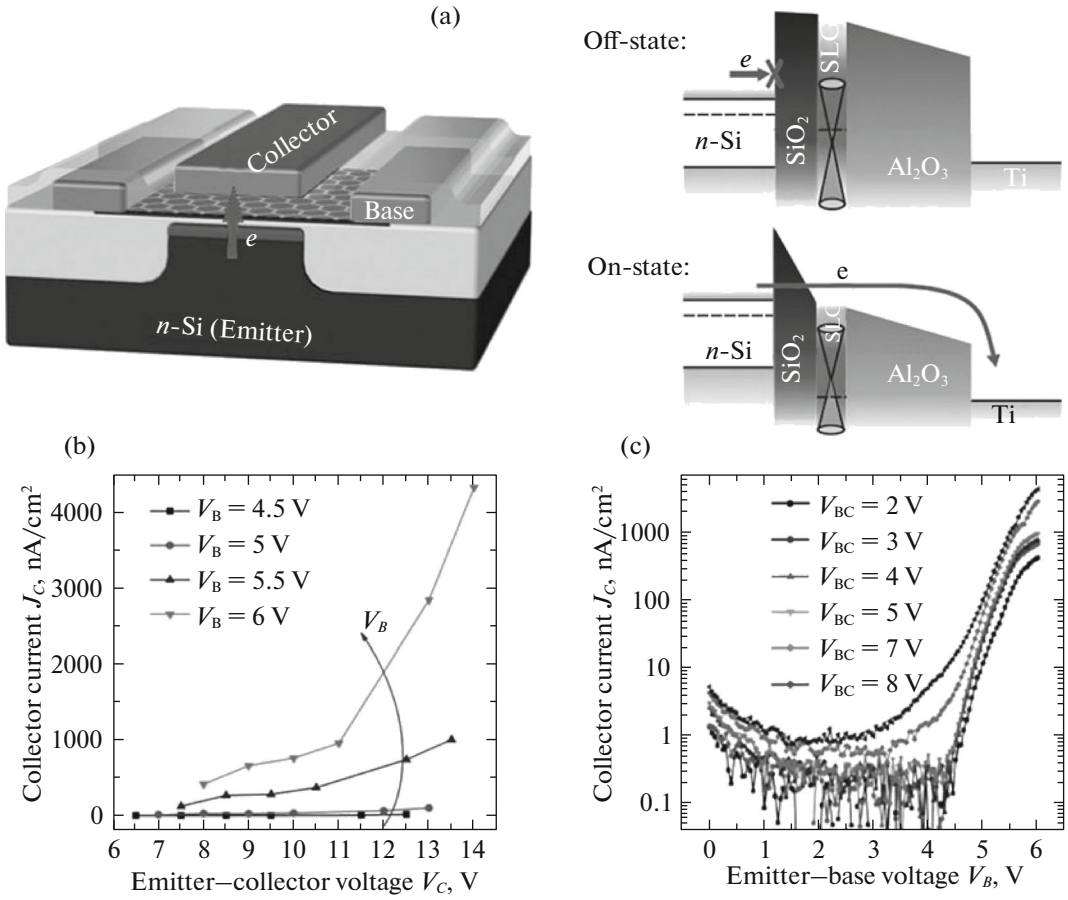

Fig. 13. (a) Schematic representation of a transistor for hot electrons and energy-band diagrams of the transistor in the ON and OFF states. (b) Output characteristics of the transistor at different base voltages. (c) Transfer characteristics of the transistor at different voltages V_{BC} between the base and collector. The insulator-layer thicknesses were 5 nm for the SiO_2 layer and 25 nm for the Al_2O_3 layer [84].

In [73], an ordinary field-effect transistor made entirely of 2D materials was reported. The drain, source, and gate were made of graphene; the transistor channel was made of MoS_2; and the gate insulator was hBN. For this transistor, a high (six orders of magnitude) current ratio I_{on}/I_{off} was obtained and the carrier mobility in the channel was merely 33 $cm^2/(V\ s)$. In addition, a diode with MoS_2, WS_2, and graphene electrodes was fabricated [73] and exhibited excellent rectification (the direct and reverse current ratio is $\sim 10^5$) and a low current in the OFF state. It is especially important that both devices exhibit a low density of states at the heterointerfaces formed without lattice matching by the transfer of single layers retained in one structure by van der Waals forces.

5. GRAPHENE–SILICON BARRIER HETEROSTRUCTURES

Interesting heterostructures were obtained by placing graphene on silicon [74]. The graphene work function is 4.6 eV and the Si electron affinity is 4.0 eV. This leads to the formation of a barrier between graphene and *p*- and *n*-Si. The barrier height changes when a voltage is applied. The *I–V* characteristics for heterostructures with *p*- and *n*-Si are presented in Fig. 12c and band diagrams of the barrier structure for different gate-voltage polarities are shown in Fig. 12d. It can be seen that the current modulation for these heterostructures reaches 10^5. Yang et al. [74] showed the possibility of forming complementary barristors, i.e., auxiliary devices for switching off the current in graphene, logic elements, and inverters on whole silicon wafers 150 nm in diameter. These structures are an example of reconsideration of the main operating principles of digital switches in the case of using the multilayer materials.

6. COMPARISON OF THE LATERAL AND VERTICAL HETEROSTRUCTURES

The use of conventional planar constructions in the fabrication of field-effect transistors with graphene as the working channel showed [75–77] that the absence

of a band gap leads to weak current control in the channel by the gate voltage: as a rule, the current only varies several times. This limits the use of graphene in transistor structures. The transition to bigraphene, nanoribbons, or other materials based on functionalized graphene with a band gap allows the channel current to be controlled, but significantly reduces the carrier mobility in the structure and, thus, limits the working-frequency range of device structures [78–80]. In a number of studies [79–83], Iannaccone et al. demonstrated the operation of lateral and vertical graphene-based heterostructures. It was shown that the overlap of the drain, source, and gate electrodes in vertical heterostructures leads to the mutual screening of electric fields, which degrades the subthreshold characteristics of the transistors and their operation speed and somewhat reduces the ratio I_{on}/I_{off} [81]. A new version of the lateral transistor with a tunneling-transparent barrier built in a planar graphene channel was suggested in [82, 83]. This can be simply a gap with a width of a few nanometers or a strip of hBN or other material forming a barrier to carrier motion. Such a construction is the next step in the development of new principles for the creation of device structures, which combines the advantages of vertical and lateral constructions. It was shown that the use of such a structure makes it possible to significantly improve the parameters of transistors, but the formation of a tunneling-transparent barrier is a relatively difficult technological problem. In addition, since multilayer materials are attractive for use just in vertical constructions, the next step will, it seems, be a vertical construction with a weaker degree of overlap of the control electrodes.

Recently, a transistor for hot electrons with a graphene base was fabricated. The construction is compatible with existing planar silicon technology. Figure 13 shows a schematic representation of the transistor and some of its characteristics from [84]. Earlier, a similar device was formed using a metal base [85], but its optimization required a reduction in the base thickness and enhancement of the layer conductivity. Therefore, graphene was found to be a perfect base material. It was theoretically predicted [86] that the use of graphene should ensure a ratio I_{on}/I_{off} of up to five orders of magnitude and the operation-frequency range is bound to extend into the terahertz region. Thus far, a current ratio I_{on}/I_{off} of over four–five orders of magnitude has been demonstrated [84, 87].

7. CONTACTS TO SINGLE LAYERS IN THE HETEROSTRUCTURES

An important problem in the fabrication and investigation of vertical heterostructures based on graphene and semiconductor and insulator layers is the provision of a good contact to the single layers. Different contacts to graphene (Ti/Au, Al/Au, Ni/Au, Cu/Au, Pd/Au, and Pt/Au) were analyzed in [88]. It was shown that the minimum resistance is obtained when using Ti/Au. This problem was also considered by Wang et al. [89], in which case, after optimization of the single-layer transfer technology for assembling heterostructures and contact-fabrication technology, the carrier mobility in graphene placed between two hBN layers was ~140000 $cm^2/(V\ s)$, the layer resistance was about 40 Ω/□ at room temperature and the carrier density was over 4×10^{12} cm^{-2}. These carrier mobility values are close to the theoretical limit related to scattering at acoustic phonons. At temperatures below 40 K, Wang et al. [89] observed ballistic transport to distances of over 15 μm in such samples. The single-layer transfer technology was optimized using an additional protective polypropylene carbonate layer to avoid direct contact between graphene and hBN with polydimethylsiloxane (PDMS) usually used for the transfer of CVD graphene grown from a copper foil [90, 91], as in assembling the heterostructures [4–7]. As is known, PDMS cannot be completely removed from graphene [90, 92]. The use of similar polycarbonate (poly(biphenol-A carbonate)) films was proposed for "pure" transfer of the grown graphene [93]; its modified variant was used in [94] and, indeed, yielded transferred layers with good parameters. Along with ensuring layer purity during assembly, Wang et al. [89] applied plasma treatment before sputtering contacts of 1 nm Cr/15 nm Pd/60 nm Au. A combination of the optimized technologies made it possible to obtain good 1D contacts to the graphene single layer and record high room-temperature carrier mobilities.

8. CONCLUSIONS

Significant progress, in recent years, in the development, fabrication, and investigation of graphene-based vertical heterostructures reflects the huge potential and prospects for the development of this direction. The obtained heterostructures exhibit intriguing and interesting properties and possibilities of new designs of device structures, they remove limitations imposed on the application of graphene in electronics, which are related to the absence of a band gap, and considerably broaden the prospects of the application of graphene and other single-layer materials. Further development in this area relies, on one hand, on the development of new, more complex and interesting heterostructures and, on the other hand, on the development of techniques for fabricating single-layer materials and assembling them in a common structure. So far, the layers are assembled by mechanical transfer, but in future it is necessary to develop methods for growing (synthesizing) the required multilayer heterostructure. Generally, as follows from the reviewed data, the principles of the organization of various graphene-based device structures and prospects in this direction are currently being reconsidered.

ACKNOWLEDGMENTS

This study was supported by the Ministry of Education and Science of the Russian Federation.

REFERENCES

1. K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, Nature **490**, 192 (2012).
2. K. S. Novoselov, Rev. Mod. Phys. **83**, 837 (2011).
3. A. K. Geim and I. V. Grigorieva, Nature **499**, 419 (2013).
4. H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios, IEEE Electron. Dev. Lett. **32**, 1209 (2011).
5. L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, Science **335**, 947 (2012).
6. L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. Castro Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, Nano Lett. **12**, 1707 (2012).
7. S. J. Haigh, A. Gholinia, R. Jalil, S. Romani, L. Britnell, D. C. Elias, K. S. Novoselov, L. A. Ponomarenko, A. K. Geim, and R. Gorbachev, Nature Mater. **11**, 764 (2012).
8. J. Kang, S. Tongay, J. Zhou, J. Li, and J. Wu, Appl. Phys. Lett. **102**, 012111 (2013).
9. M. S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. H. Lee, P. Kim, J. Hone, and W. J. Yoo, Nature Commun. **4**, 1624 (2013).
10. L. Britnell, R. M. Ribeiro, A. Eckmann, R. Jalil, B. D. Belle, A. Mishchenko, Y.-J. Kim, R. V. Gorbachev, T. Georgiou, S. V. Morozov, A. N. Grigorenko, A. K. Geim, C. Casiraghi, A. H. Castro Neto, and K. S. Novoselov, Science **340**, 1311 (2013).
11. I. V. Antonova, I. A. Kotin, R. A. Soots, and V. Ya. Prinz, Nanotechnology **23**, 315601 (2012).
12. I. V. Antonova, S. V. Mutilin, V. A. Seleznev, R. A. Soots, V. A. Volodin, and V. Ya. Prinz, Nanotechnology **22**, 285502 (2011).
13. N. A. Nebogatikova, I. V. Antonova, V. A. Volodin, and V. Y. Prinz, Physica E **52**, 106 (2013).
14. I. A. Kotin, I. V. Antonova, A. I. Komonov, V. A. Seleznev, R. A. Soots, and V. Ya. Prinz, J Phys. D: Appl. Phys. **46**, 285303 (2013).
15. R. Decker, Y. Wang, V. W. Brar, W. Regan, H.-Z. Tsai, Q. Wu, W. Gannett, A. Zettl, and M. F. Crommie, Nano Lett. **11**, 2291 (2011).
16. C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone, Nature Nanotechnol. **5**, 722 (2010).
17. G.-H. Lee, Y.-J. Yu, C. Lee, C. Dean, K. L. Shepard, P. Kim, and J. Hone, Appl. Phys. Lett. **99**, 243114 (2011).
18. M. Hirose, Mater. Sci. Eng. B **41**, 35 (1996).
19. S. N. Mohammad, F. J. Kub, and C. R. Eddy, J. Vac. Sci. Technol. B **29**, 021021 (2011).
20. K. Watanabe, T. Taniguchi, and H. Kanda, Nature Mater. **3**, 404 (2004).
21. G. Giovannetti, P. A. Khomyakov, G. Brocks, P. J. Kelly, and J. van den Brink, Phys. Rev. B **76**, 073103 (2007).
22. D. K. Ferry, IEEE Nanotech. **12**, 1932 (2012).
23. W. Gannett, W. Regan, K. Watanabe, T. Taniguchi, M. F. Crommie, and A. Zettl, Appl. Phys. Lett. **98**, 242105 (2011).
24. A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, Nano Lett. **11**, 2396 (2011).
25. N. Petrone, C. Dean, I. Meric, A. M. van der Zande, P. Y. Huang, L. Wang, D. Muller, K. L. Shepard, and J. Hone, Nano Lett. **12**, 275 (2012).
26. Yi. Zhang, L. Zhang, P. Kim, M. Ge, Z. Li, and C. Zhou, Nano Lett. **12**, 2810 (2012).
27. E. Kim, T. Yu, E. S. Song, and B. Yu, Appl. Phys. Lett. **98**, 262103 (2011).
28. K. H. Lee, H. J. Shin, J. Lee, I. Y. Lee, G. H. Kim, J. Y. Choi, and S. W. Kim, Nano Lett. **12**, 714 (2012).
29. M. Wang, S. K. Jang, W.-J. Jang, M. Kim, S.-Y. Park, S.-W. Kim, S.-J. Kahng, J.-Y. Choi, R. S. Ruoff, Y. J. Song, and S. Lee, Adv. Mater. **25**, 2746 (2013).
30. L. Britnell, R. V. Gorbachev, A. K. Geim, L. A. Ponomarenko, A. Mishchenko, M. T. Greenaway, T. M. Fromhold, K. S. Novoselov, and L. Eaves, Nature Commun. **4**, 1794 (2013).
31. P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, IEEE Trans. Electron Dev. **60**, 951 (2013).
32. R. M. Feenstra, D. Jena, and G. Gu, J. Appl. Phys. **111**, 043711 (2012).
33. M. P. Levendorf, C.-J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. A. Muller, and J. Park, Nature **488**, 627 (2012).
34. Z. Liu, L. Ma, G. Shi, W. Zhou, Y. Gong, S. Lei, X. Yang, J. Zhang, J. Yu, K. P. Hackenberg, A. Babakhani, J.-C. Idrobo, R. Vajtai, J. Lou, and P. M. Ajayan, Nature Nanotechnol. **8**, 119 (2013).
35. B. Hunt, J. D. Sanchez-Yamagishi, A. F. Young, M. Yankowitz, and B. J. Le Roy, Science **340**, 1427 (2013).
36. K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, Solid State Commun. **146**, 351 (2008).
37. X. Du, A, Barker, I. Skachko, and E. Y. Andrei, Nature Nanotechnol. **3**, 491 (2008).

38. J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhre, Nature Nanotechnol. **3**, 206 (2008).

39. E. H. Hwang, S. Adam, and S. Das Sarma, Phys. Rev. Lett. **98**, 186806 (2007).

40. L. Wang, Z. Chen, C. R. Dean, T. Taniguchi, K. Watanabe, L. Brus, and J. Hone, ACS Nano **6**, 9314 (2012).

41. S. Fratini and F. Guinea, Phys. Rev. B **77**, 195415 (2008).

42. A. K. Geim and K. S. Novoselov, Nature Mater. **6**, 183 (2007).

43. S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, Phys. Rev. Lett. **100**, 016602 (2008).

44. V. Singh, D. Joung, L. Zhai, S. Das, S. I. Khondaker, and S. Seal, Progr. Mater. Sci. **56**, 1178 (2011).

45. S. Chen, H. Ji, H. Chou, Q. Li, H. Li, J. W. Suk, R. Piner, L. Liao, W. Cai, and R. S. Ruoff, Adv. Mater. **25**, 2062 (2013).

46. D. R. Cooper, B. D'Anjou, and N. Ghattamaneni, Condens. Matter Phys. **2**, 56 (2012).

47. H. Zhou, W. J. Yu, L. Liu, R. Cheng, Y. Chen, X. Huang, Y. Liu, Y. Wang, Y. Huang, and X. Duan, Nature Commun. **4**, 2096 (2013).

48. I. V. Antonova, I. A. Kotin, R. A. Soots, and V. Ya. Prinz, Fullerenes, Nanotubes, Carbon Nanostruct. **20**, 543 (2012).

49. I. A. Kotin, I. V. Antonova, R. A. Soots, V. A. Volodin, and V. Ya. Prints, Nanotechnol. Russ. **8**, 621 (2013).

50. A. I. Podlivaev and L. A. Openov, Semiconductors **45**, 958 (2011).

51. K. F. Mak, M. Y. Sfeir, Y. Wu, C. H. Lui, J. A. Misewich, and T. F. Heinz, Phys. Rev. Lett. **105**, 136805 (2010).

52. R. Gordon, D. Yang, E. Crozier, D. Jiang, and R. Frind, Phys. Rev. B **65**, 125407 (2002).

53. W. Zhao, Z. Ghorannevis, L. Chu, M. Toh, C. Kloc, P.-H. Tan, and G. Eda, ACS Nano **7**, 791 (2013).

54. P. Tonndorf, R. Schmidt, P. Böttger, X. Zhang, J. Börner, A. Liebig, M. Albrecht, C. Kloc, O. Gordan, D. R. T. Zahn, S. M. de Vasconcellos, and R. Bratschitsch, Opt. Express **21**, 4908 (2013).

55. J. Kang, S. Tongay, J. Zhou, J. Li, and J. Wu, Appl. Phys. Lett. **102**, 012111 (2013).

56. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nature Nanotechnol. **6**, 147 (2011).

57. Y. Yoon, K. Ganapathi, and S. Salahuddin, Nano Lett. **11**, 3768 (2011).

58. D. J. Late, B. Liu, H. S. S. R. Matte, V. P. Dravid, and C. N. R. Rao, ACS Nano **6**, 5635 (2012).

59. W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhre, Appl. Phys. Lett. **102**, 042104 (2013).

60. B. Radisavljevic, M. B. Whitwick, and A. Kis, ACS Nano **5**, 9934 (2011).

61. Z. Y. Yin, H. Li, H. Li, L. Jiang, Y. M. Shi, Y. H. Sun, G. Lu, Q. Zhang, X. D. Chen, and H. Zhang, ACS Nano **6**, 74 (2012).

62. O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, and A. Kis, Nature Nanotechnol. **8**, 497 (2013).

63. M. S. Choi, G. H. Lee, Y. J. Yu, D. Y. Lee, S. H. Lee, P. Kim, J. Hone, and W. J. Yoo, Nature Commun. **4**, 1624 (2013).

64. Y. C. Kong, L. Q. Hu, Y. D. Zheng, C. H. Zhou, C. Chen, S. L. Gu, R. Zhang, P. Han, R. L. Jiang, and Y. Shi, Appl. Phys. A **90**, 545 (2008).

65. G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, ACS Nano **5**, 9934 (2011).

66. Z. Remes, M. Nesladek, K. Haenen, K. Watanabe, and T. Taniguchi, Phys. Status Solidi A **202**, 2229 (2005).

67. J. Pu, Y. J. Zhang, Y. Wada, J. T. W. Wang, L. J. Li, Y. Iwasa, and T. Takenobu, Nano Lett. **12**, 4013 (2012).

68. J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee, and H. C. Ko, Small **9**, 3295 (2013).

69. J. M. Hamm and O. Hess, Science **340**, 1298 (2013).

70. G. Konstantatos, M. Badioli, L. Gaudreau, J. Osmond, M. Bernechea, F. P. Garcia de Arquer, F. Gatti, and F. H. L. Koppens, Nature Nanotechnol. **7**, 363 (2012).

71. T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, Nature Nanotechnol. **8**, 100 (2013).

72. A. Kuc, N. Zibouche, and T. Heine, Phys. Rev. B **83**, 245213 (2011).

73. T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, ACS Nano **8**, 6259 (2014).

74. H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, Science **336**, 1140 (2012).

75. D. B. Farmer, A. Valdes-Garcia, C. Dimitrakopoulos, and P. Avouris, Appl. Phys. Lett. **101**, 143503 (2012).

76. Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and Ph. Avouris, Science **327**, 662 (2010).

77. C.-C. Lu, Y.-C. Lin, C.-H. Yeh, J.-C. Huang, and P.-W. Chiu, ACS Nano **6**, 4469 (2012).

78. F. Schwierz, Nature Nanotechnol. **5**, 487 (2010).

79. G. Fiori and G. Iannaccone, Proc. IEEE **101**, 1653 (2013).

80. G. Fiori, D. Neumaier, B. N. Szafranek, and G. Iannaccone, IEEE Trans. Electron Dev. **61**, 729 (2014).

81. G. Fiori, S. Bruzzone, and G. Iannaccone, IEEE Trans. Electron Dev. **60**, 268 (2013).

82. G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, ACS Nano **6**, 2642 (2012).

83. A. Paussa, G. Fiori, P. Palestri, M. Geromel, D. Esseni, G. Iannaccone, and L. Selmi, IEEE Trans. Electron Dev. **61**, 1567 (2014).

84. S. Vaziri, G. Lupina, C. Henke, A. D. Smith, M. Ostling, J. Dabrowski, G. Lippert, W. Mehr, and M. C. Lemme, Nano Lett. **13**, 1435 (2013).

85. T. Yajima, Y. Hikita, and H. Y. Hwang, Nature Mater. **10**, 198 (2011).

86. W. Mehr, J. Dabrowski, J. C. Scheytt, G. Lippert, Y.-H. Xie, M. C. Lemme, M. Ostling, and G. Lupina, IEEE Electron Dev. Lett. **33**, 691 (2012).

87. C. Zeng, E. B. Song, M. Wang, S. Lee, C. M. Torres, Jr., J. Tang, B. H. Weiller, and K. L. Wang, Nano Lett. **13**, 2370 (2013).

88. J. A. Robinson, M. La Bella, M. Zhu, M. Hollander, R. Kasurda, Z. Hughes, K. Trumbull, R. Cavalero, and D. Snyder, Appl. Phys. Lett. **98**, 053103 (2011).

89. L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean, Science **342**, 614 (2013).

90. J. W. Suk, A. Kitt, C. W. Magnuson, Y. Hao, S. Ahmed, J. An. A. K. Swan, B. B. Goldberg, and R. S. Ruoff, ACS Nano **5**, 6916 (2011).

91. Y. Lee, S. Bae, H. Jang, S. Jang, S.-E. Zhu, S. H. Sim, Y. I. Song, B. H. Hong, and J.-H. Ahn, Nano Lett. **10**, 490 (2010).

92. M. Ishigami, Shaul Aloni, and A. Zettl, Nano Lett. **7**, 1643 (2007).

93. Y. C. Lin, C. H. Jin, J. C. Lee, S. F. Jen, and P. W. Chiu, ACS Nano **5**, 2362 (2011).

94. I. V. Antonova, S. V. Golod, R. A. Soots, A. I. Komonov, V. A. Seleznev, M. A. Sergeev, V. A. Volodin, and V. Ya. Prints, Semiconductors **48**, 804 (2014).

Translated by E. Bondareva