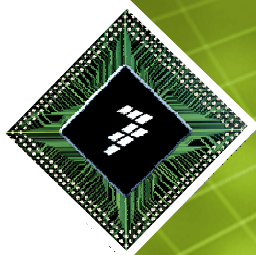




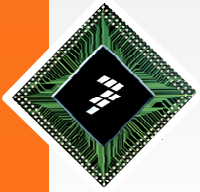
# I<sup>2</sup>C

## Inter-Integrated Circuit

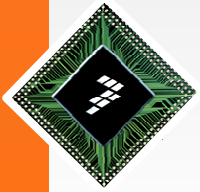


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Alí Piña  
Technical Support Engineer

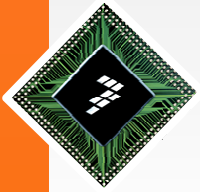


- Overview
  - Communication interfaces allow systems with different architectures to communicate with each other. In the previous lab, you learned how to use the serial port. In this lab, you will about I<sup>2</sup>C and how it is used to communicate with a variety of devices.
- Learning Objectives
  - This module will help you learn how to use the KL25's I<sup>2</sup>C module with the MMA8451Q accelerometer.
- Success Criteria
  - At the end of this module, you will be able to use the KL25 to communicate with various I2C devices such as the MMA8451Q Accelerometer from Freescale.



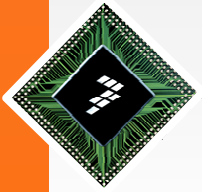
## Overview

- Only two bus line are required:
  - SDA: Data Line
  - SCL: Clock Line
- No strict baud rate requirements
  - Master generates the clock signal
- Simple master/slave relationships exist between all components
  - Each slave has a unique bus address
- I2C is a true multi-master bus
  - Provides arbitration and collision detection



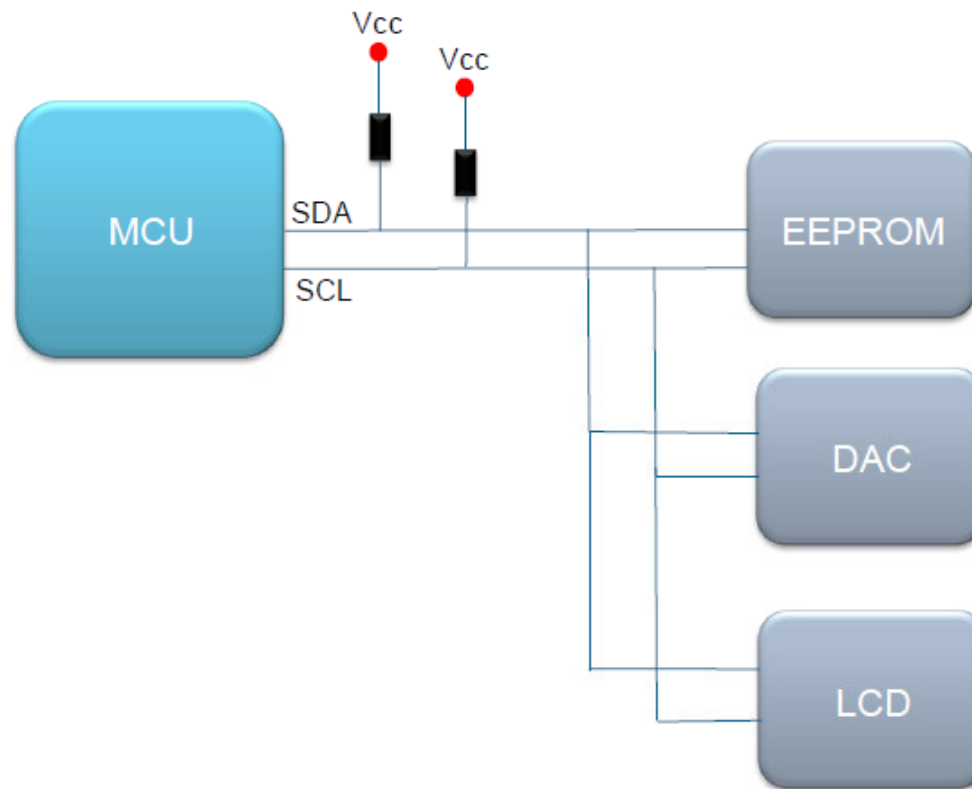
## Overview

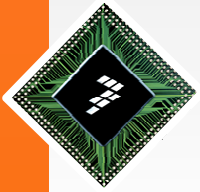
- Three top speeds
  - 100KHz
  - 400KHz(Fast Mode)
  - 3.4MHz(High Speed)



# Overview

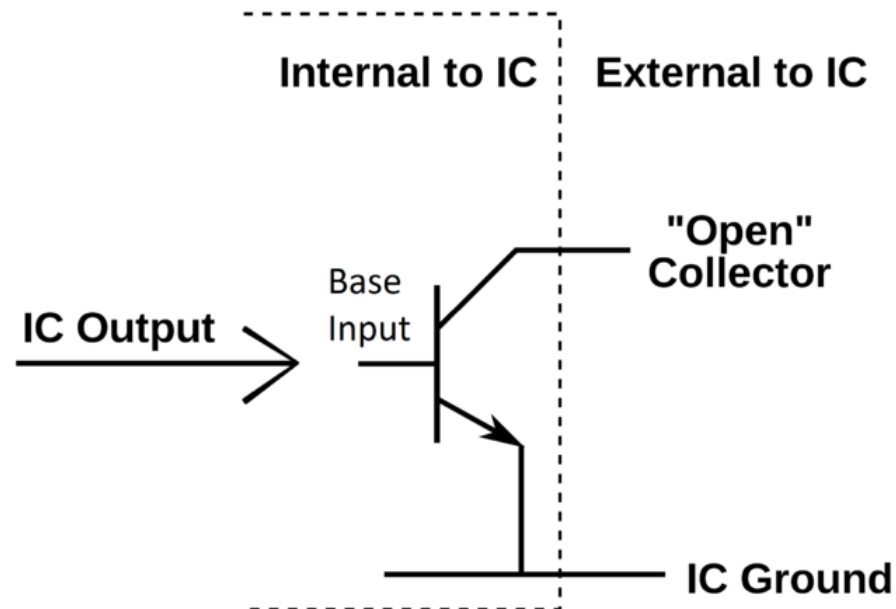
- Single Master connection

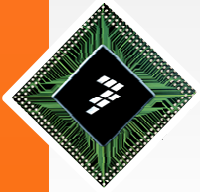




## Overview

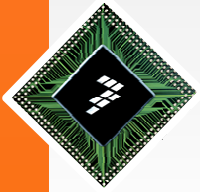
- I2C pins are open drain and external pull-up resistors are required.
- Pull-up typical values from 1K to 10K.





## Overview

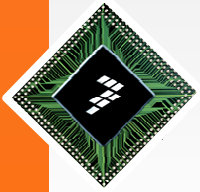
- Also known as open collector
- This means the device just can pull down the line or leave it open.
- The pull up will get the line to  $V_{cc}$  to get the 1's
- A capacitance of 400pF is allowed for correct behavior
  - Between the lines and GND
  - Also known as wire capacitance



## I<sup>2</sup>C Glossary

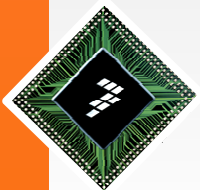
- **Start signal:** Is defined as a high-to-low transition of SDA while SCL is on high
- **Acknowledge:** The slave keeps SDA low during the ninth clock of SCL
- **Stop signal:** Is defined as a low-to-high transition of SDA while SCL is on high
- **Slave address:** 7-bit data which represents the name of the specific device. Is part of the first byte sent
- **R /W bit:** represents the operation to be performed on the slave. Is sent as the LSB of the first byte. If 1 is a read, if 0 is a write.
- **Repeated Start:** A Start signal without first generating a Stop signal



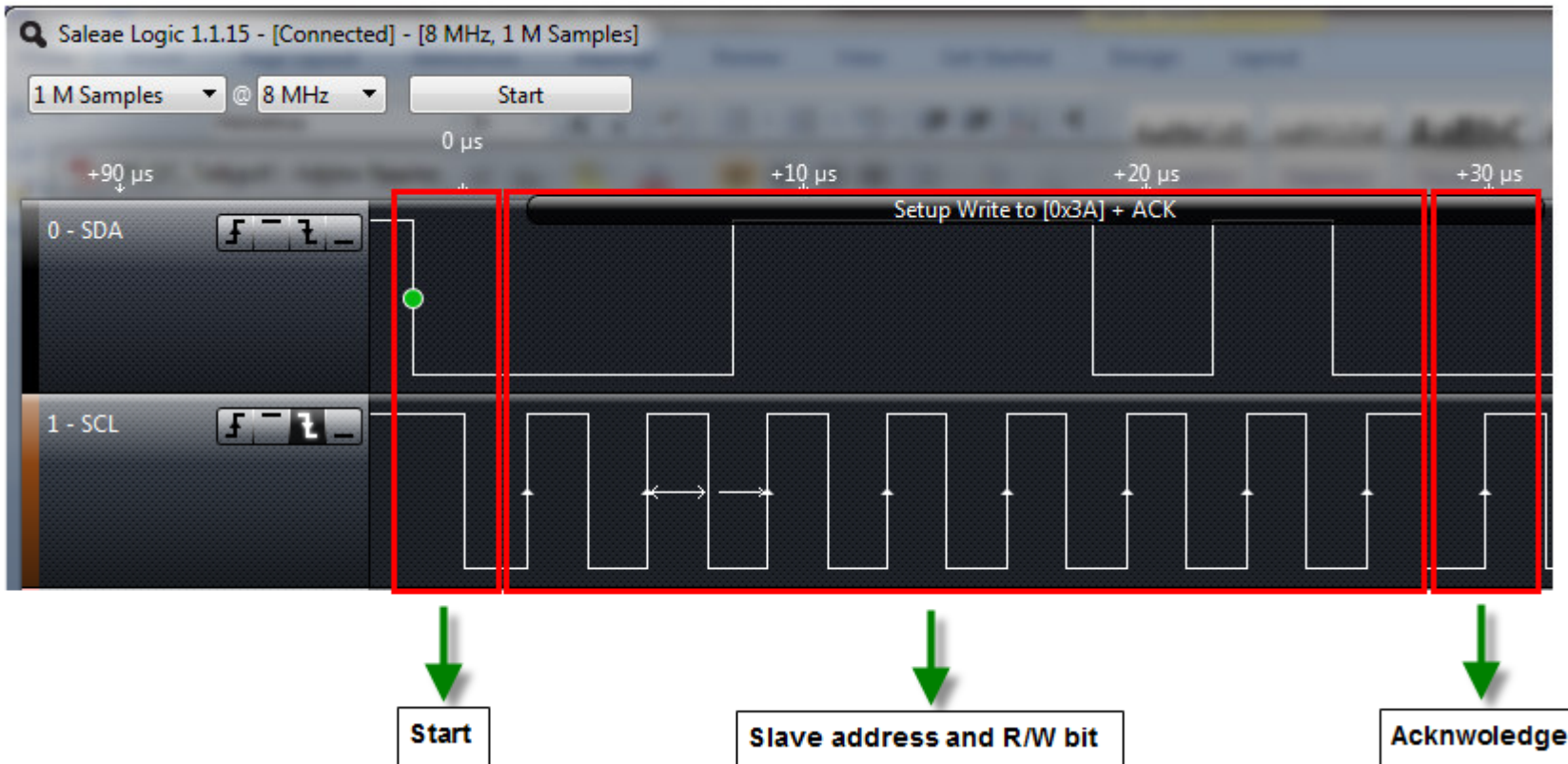


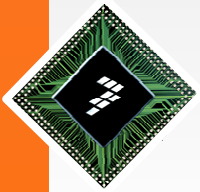
## I<sup>2</sup>C operations

- There are 3 operations on I2C
  - Write: Master writes to the slave
  - Read: Master reads from slave
  - Random read: Perform a write and read on the same operation

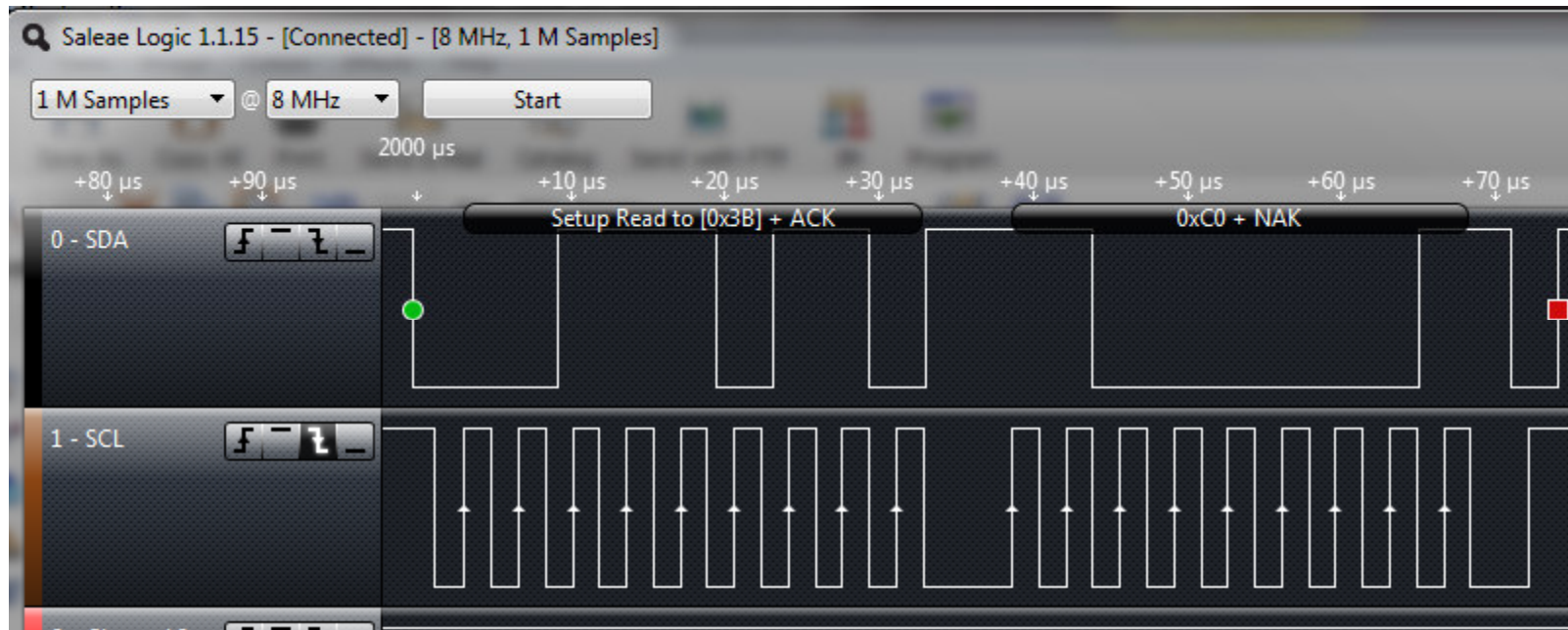


# I<sup>2</sup>C Write





# I<sup>2</sup>C Read



# Hands-On



