Laboratory Assignment
ALU Design and Implementation

1 Design and Implementation

- Write a VHDL code that implements the ALU given in Fig. 1 that does arithmetic operations (addition, subtraction, comparation etc.) and logic operations (and, or, invert, xor) with the use of 3 selection bits (e.g. for "001" subtraction operation is performed).

  Since there is only a single data input bus, two inputs are loaded separately into PIPO registers (Fig. 2) using Load input (e.g. for Load=1, A is loaded in corresponding PIPO register).

  PIPO registers, Arithmetic Unit, Logic Unit and MUX are discrete components that are used in this ALU design. Each unit (Arithmetic and Logic) has own multiplexed implementations of required operations (Table 1).

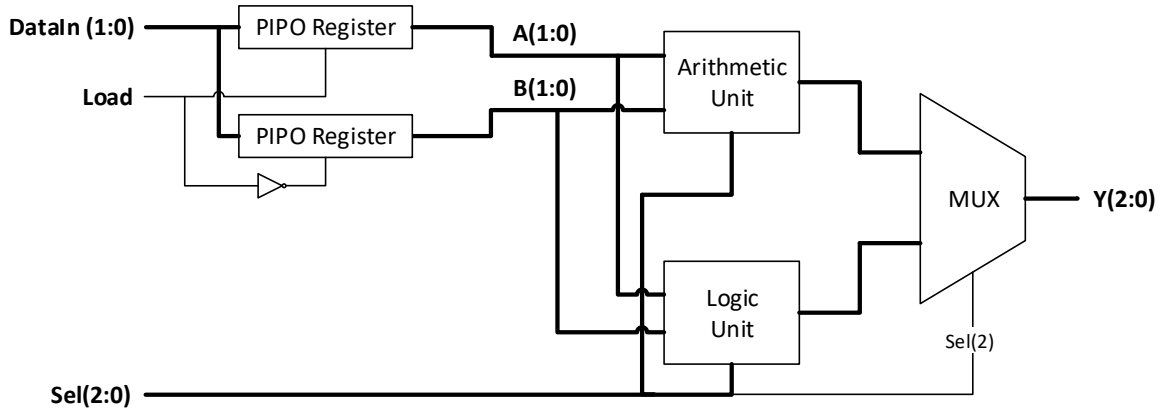

Figure 1: ALU Schematic

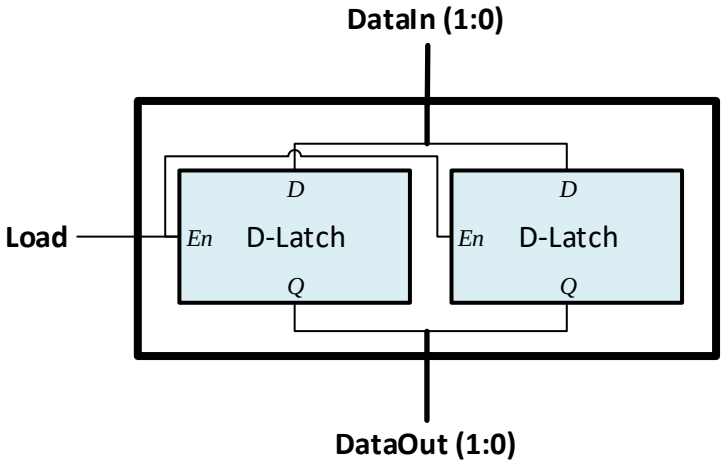

Figure 2: PIPO Schematic

Sel	**Operation**	Type
000	**A + B**	Arithmetic Unit
001	**A - B**	
010	**A + 1**	
011	**max(A,B)**	
100	**A AND B**	Logic Unit
101	**A OR B**	
110	**NOT A**	
111	**A XOR B**	

Table 1: ALU opcodes

2 Testing

- Synthesize and check your RTL Schematic for consistency of your components and connections.
- Test your design in test bench with all possible operations and at least two different sets of inputs for A and B.