HACETTEPE UNIVERSITY
ELECTRICAL & ELECTRONICS ENGINEERING
ELE227 FUNDAMENTALS OF DIGITAL SYSTEMS

Experiment 3 – Implementation of Combinational Circuits with VHDL

Preliminaries:

1) Students who will attend this experiment are assumed to know:
    a. Basic number systems and Boolean algebra
    b. Basic combinational logic operations and Gates
    c. Basic VHDL operators and operands
2) Study related pages in the textbook.

Work:

- Basic Logic Functions are "**and, or, not, nand, nor, xor, xnor**"
- For each question first design your circuit on the paper. Then write the VHDL code of each module and test bench of the overall circuit. Include the RTL schematics and test bench graphs. Insert comments in your code.

1) Decoder: First design a 3-to-8 decoder with active-high outputs. Then using the 3-to-8 decoder, design a full subtractor.

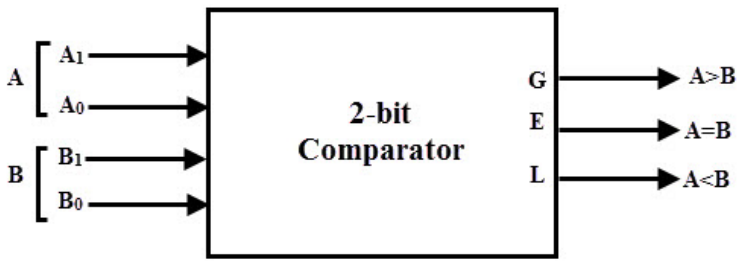
2) Multiplexer: First design a 4-to-1 multiplexer (mux). Then ***just*** using the 4-to-1 mux implement the function $f(x, y, z)$ given below.

$$f(x, y, z) = xy' + y'z' + x'z$$

3) Magnitude Comparator: Design a combinational circuit that compares two 2-bit numbers and gives following outputs:

- A>B
- A=B
- A<B

You need to implement this device using 2-to-4 decoders and minimum number of basic logic functions. Input bits A_1 A_0 B_1 B_0 should be inputs for decoders, you need to design remaining circuitry. You can use more than two decoders if you need.



4) Decimal to BCD Converter: Design a combinational circuit that converts a 6-bit binary number into a 2-digit decimal number represented in the BCD form.