HACETTEPE UNIVERSITY
ELECTRICAL AND ELECTRONICS ENGINEERING
ELE227 FUNDAMENTALS OF DIGITAL SYSTEMS

Experiment 2 – Implementation of Combinational Circuits with VHDL

Preliminaries:

1) Students who will attend to this experiment are assumed to know:
- Basic number systems and Boolean algebra
- Basic combinational logic operations and gates
- Basic VHDL operators and operands

2) Please study the related pages on the book.

Work:

- **Basic Logic Functions are "and, nand, or, nor, not, xor, xnor"**
- **Write Test Bench Programs for all questions, and test your VHDL module.**
- **Add RTL schematics for all designs.**

1) Write a VHDL code to implement a half-adder by using only basic logic functions. Test your design with all possible inputs.

2) Draw a full-adder logic circuit on the paper by hand. Write a VHDL code to implement a full-adder by using the half-adder written at Q1, and basic logic functions. Compare your drawing with RTL schematic. Test your design with all possible inputs.

3) Write a VHDL code to implement a 3-bit adder-subtractor by using only the full adder written at Q2 and basic logic functions. There will be a select bit to choose the add or subtract operation. Test your design with at least 5 different cases of inputs

4) Write a VHDL code to implement a multiplier that can multiply a 3-bit number with a 2-bit number by using the full adder written in Q2 and basic logic functions. Test your design with at least 5 different cases of inputs. (There will be 2 unsigned numbers at the input (one 3-bit, one 2-bit), and an unsigned 5-bit number at the output.)