Problem Design Statement — Digital Front End (DFE) Filter Array

1 Title

Design and implementation of a multistage Digital Front End (DFE) for radio/ADC preprocessing: fractional polyphase decimator (9 MHz → 6 MHz), dual 2nd-order IIR notch filters (2.4 MHz and 5 MHz), and a configurable CIC decimator chain (decimation factors 1,2,4,8,16).

2 Context & Motivation

An incoming digitized RF/intermediate-frequency stream is sampled at 9 MHz (or equivalent sample clock) but the downstream processing chain (demodulator/decoder) requires a 6 MHz sample rate and/or multiple lower-rate streams. The channel environment contains narrowband interferers centered at 2.4 MHz and 5 MHz that must be deeply suppressed. A multi-stage architecture—fractional polyphase decimation → narrowband IIR notches → CIC decimation—offers the best trade-off between computational cost, latency, and spectral performance.

3 High-Level Functional Requirements

1. Fractional Decimation (9 MHz → 6 MHz)
    - Implement a polyphase fractional decimator that converts a 9 MHz sampled stream to 6 MHz (i.e., decimation by factor 3/2) while meeting stringent aliasing requirements.
    - Must be streaming, fixed-latency, and suitable for hardware (FPGA/ASIC) implementation.
2. Notch Filtering
    - Two cascaded 2nd-order IIR notch (biquad) filters to remove narrowband interferers at 2.4 MHz and 5.0 MHz (center frequencies relative to the 6 MHz sampling rate after fractional stage).
    - Notches shall be deeply attenuating and stable in fixed point.

3. CIC Decimation

   - Provide a CIC decimation stage with configurable decimation factor selectable among powers-of-two: 1, 2, 4, 8, 16.
   - The CIC output rate = 6 MHz / D, where $D \in \{1, 2, 4, 8, 16\}$.
   - Include an optional compensation / final FIR stage if required to meet passband ripple requirements.

4. Control & Observability

   - Run-time control registers to: enable/disable stages, set CIC decimation factor, bypass notches, freeze/unfreeze adaptation (if any), and read status (overflow, ready).
   - Probe points or debug outputs for tap coefficients, SNR/AGC metrics, and diagnostic signals.