



For the SI Clash Digital Hackathon

Organized by IEEE SSCS AUSC

Digital Design and Verification of a Digital Front End (DFE) Filter Array

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Proposal

Please note that this is out of our hands as the report was so big it passed 10 MB.

I hope you accept our proposal to check our GitHub for the Report and all the source codes and flow.

Link: [DFE_GitHub](#)