CLRM701

Mifare® & ICODE contactless reader module

Rev. 3.2 — 24 May 2007
101432

Product data sheet
PUBLIC

1. General description

This document describes the functionality of the CLRM701 reader module. It includes the functional and electrical specifications and gives the needed details to use this reader module as a reference design.
This reader module is designed for an easy adaptation of a contactless reader to a PC and it is ready to design a new application giving the basic hints for a reader hardware development.

The CLRM701 contactless reader module is part of the CLRD701, the Mifare® PEGODA reader. It uses the CLRC632 reader IC for the contactless communication. The CLRC632 is member of a family for highly integrated reader ICs for contactless communication at 13.56 MHz.

2. Features

- contactless smart card reader module
- based on the CLRC632
- contactless operating frequency 13.56 MHz
- Supports Mifare® Dual Interface Card ICs and ISO 14443A part 1- 4
- Supports ISO 14443B
- Supports Mifare® Classic crypto
- Supports ISO 15693
- Supports NXP ICODE
- Supports higher data rates of up to 424 kbit/s
- Typical operating distance: 75 - 100mm
- CE and FCC compliant
- USB host interface
- USB bus powered 5 VDC power supply
- Unique serial number of each reader device
- Supported by Windows 2000 and Windows XP.

3. Ordering information

This module is part of the CLRD701 reader. It cannot be ordered separately.

4. Block diagram

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The CLRD701 PEGODA reader is a complete reader based on the CLRM701. The reader itself is divided in two parts:

- CLRM701, This reader module is the basic print including the CLRC632, a µ-Controller and all interfaces to a host.
- MF AN700 (flexible PEGODA antenna), This antenna is described in the application note Ref. 2.

CLRD701 block diagram (Figure 1) shows the CLRD701 PEGODA's basic functional components

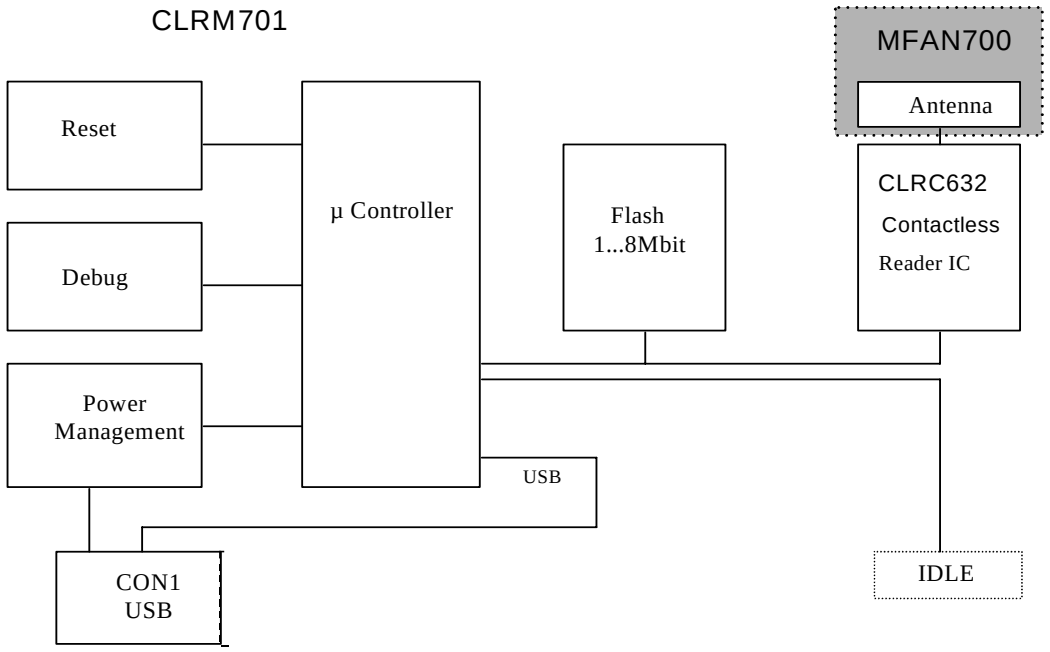

Fig 1. CLRD701 PEGODA block diagram

The PEGODA reader is designed to offer the user a great freedom to design an application. Several functional blocks can be identified.
Core component of the PEGODA is the CLRC632, the highly integrated ISO 14443, ISO 15693 reader IC. For detailed information concerning the CLRC632 please refer to the data sheet Ref. 1. The CLRC632 is used as an analog front-end unit to communicate via the antenna to a contactless chip card. All relevant data coding to send and receive data according to the ISO 14443 and ISO 15693 is done internally by the CLRC632. The CLRC632 itself is controlled by a µ-controller.
The µ-controller handles the communication to the host PC via USB. The µ-Controller translates the serial protocol via USB into remote function calls and executes the appropriate command. To be able to implement the complete Mifare® Classic protocol, the ISO 14443-4 open protocol commands as well as ISO 15693 and the host communication protocol is implemented in a 1.8 Mbit flash device.
Furthermore, a reset and a power management circuit and several ports are provided for debug purposes.

5. Functional description

The default configuration for the PEGODA reader offers an USB interface to the host. Table 1 defines possible interface connection types of CLRM701 module and CLRD701 PEGODA reader.

Table 1. Host interface types

Host interface type	CLRD701 PEGODA reader	CLRM701 reader module
USB Type B plug	yes	yes

5.1 USB Type B Plug

The USB type B plug is the default configuration of the PEGODA reader to connect the reader to a host PC.

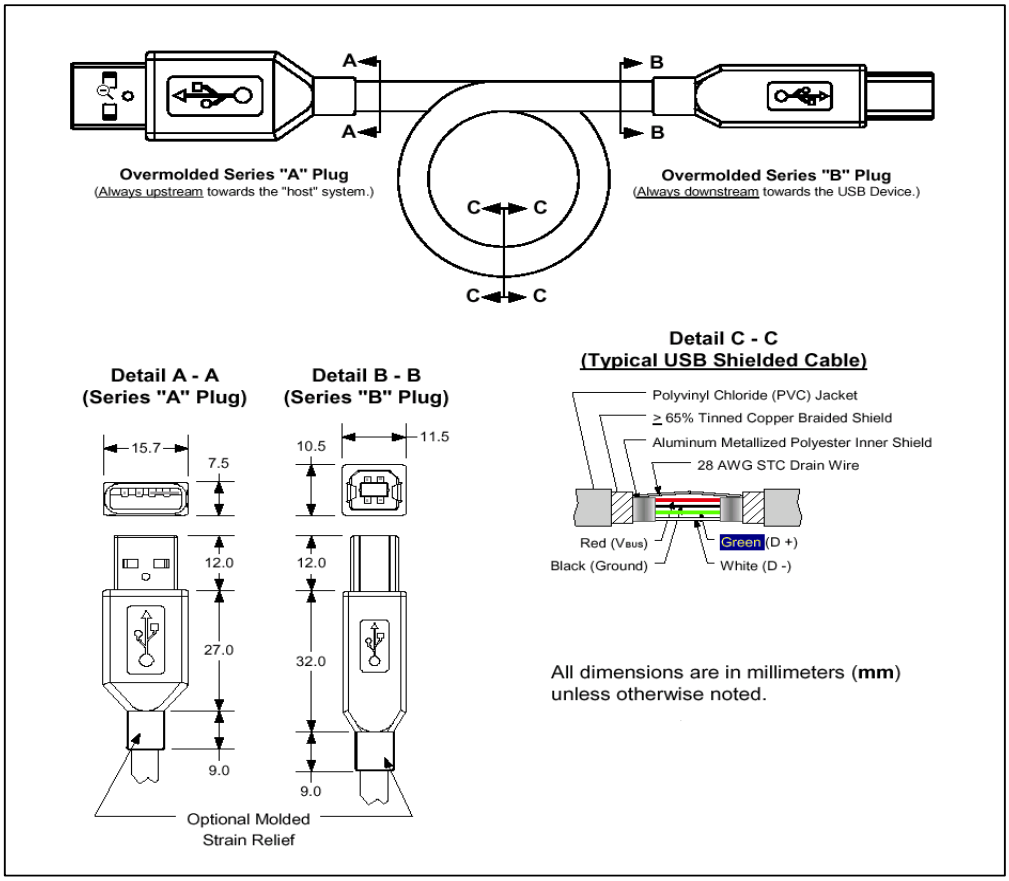

Fig 2. USB Type B connectors

The default configuration uses the USB cable to communicate to the PEGODA as well as to supply the 5 V supply voltage.

5.2 Power supply

The controller board supports various power supply sources, which have to provide a regulated 5V DC voltage. Figure 3 shows the possible power supply on the CLRM701. In the default configuration, the PEGODA reader is a USB bus powered reader. No external power supply has to be connected.

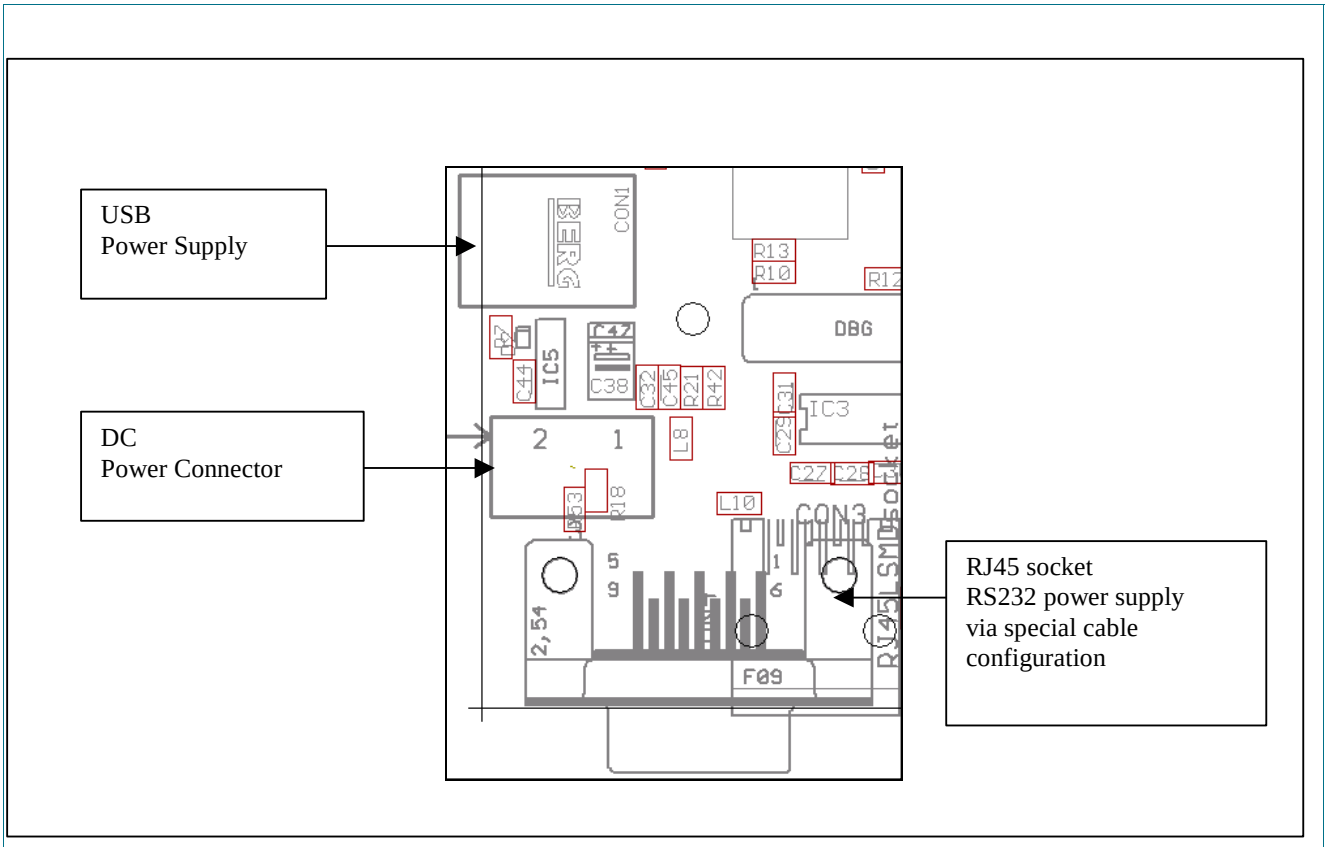

Fig 3. Interface and power supply

Remark: In order to fulfil the USB specification version 1.1, the reader module behaves like a low power device after power on. Having sent an ACTIVATE command, the PEGODA is activated and the reader module switches to an idle state resulting in an increased power consumption. Only one power source must be connected to the board.

5.3 Boot jumper and serial I/O

The PEGODA reader offers a boot jumper to enable a firmware update as well as several serial I/O pins to fulfil different user and application specific requirements. Figure 4 shows the location of the boot jumper and the serial I/O pins.

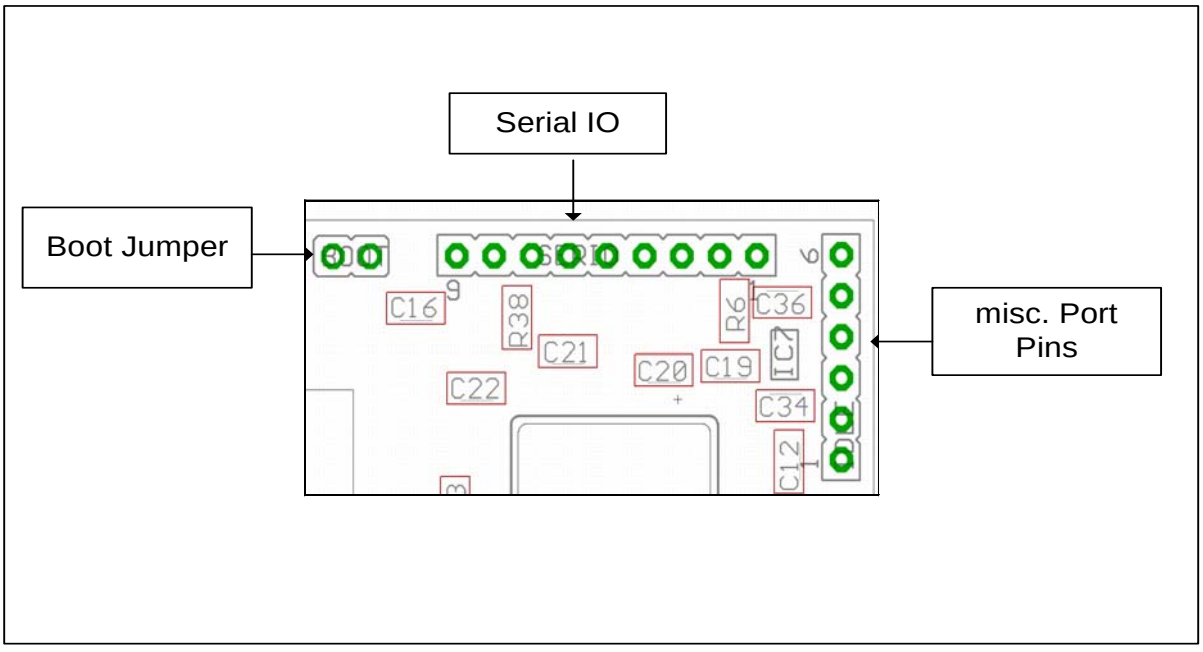

Fig 4. Boot jumper and I/O pins location

5.3.1 Boot jumper

Setting the boot jumper before the board is connected to the power supply, the µ-controller enables the internal bootstrap mechanism. This might be used to download new firmware via the serial interface without additional hardware changes. For detailed description of the µ-controller please refer to the controller's data sheet.

5.3.2 Serial I/O

The serial I/O pins allow the user to monitor additional controller lines to fulfil application-related requirements. Table 2 describes the I/O pins.

Table 2. I/O pin description

Pin No.	Description
1	+ 3.3 V regulated; Controller power supply
2	RxD; asynchronous receive pin; TTL level
3	TxD; asynchronous transmit pin; TTL level
4	DSR; data set ready; asynchronous serial handshake pin; TTL level; synchronous serial Master-Receive/Slave-Transmit
5	DTR; data terminal ready; asynchronous serial hand shake pin; TTL level
6	GND
7	port 3.9; synchronous serial Master-Transmit/Slave-Receive
8	port 3.13; synchronous serial Master-Clock-Out/Slave-Clock-In
9	reset out; microcontroller reset out pin

5.3.3 Miscellaneous Port Pins

In addition to the I/O pins several miscellaneous port pins can be used to monitor and control the µ-controllers behaviour. Table 3 lists the miscellaneous port pins.

Table 3. Miscellaneous port pins

Pin No.	Description
1	+ 3.3 V regulated; Controller power supply
2	port 6.2; Chip Select Line 2;
3	port 2.1; fast external interrupt line 2
4	port 6.3; Chip Select Line 3;
5	Reset In; microcontroller reset in; negative logic
6	GND

6. CLRM701 PCB description

The following parts describe the CLRM701 schematic, the part list and the layout of the PCB completely in order to give the user the possibility to take the PEGODA reader as a reference design for an own reader development.

6.1 Schematic

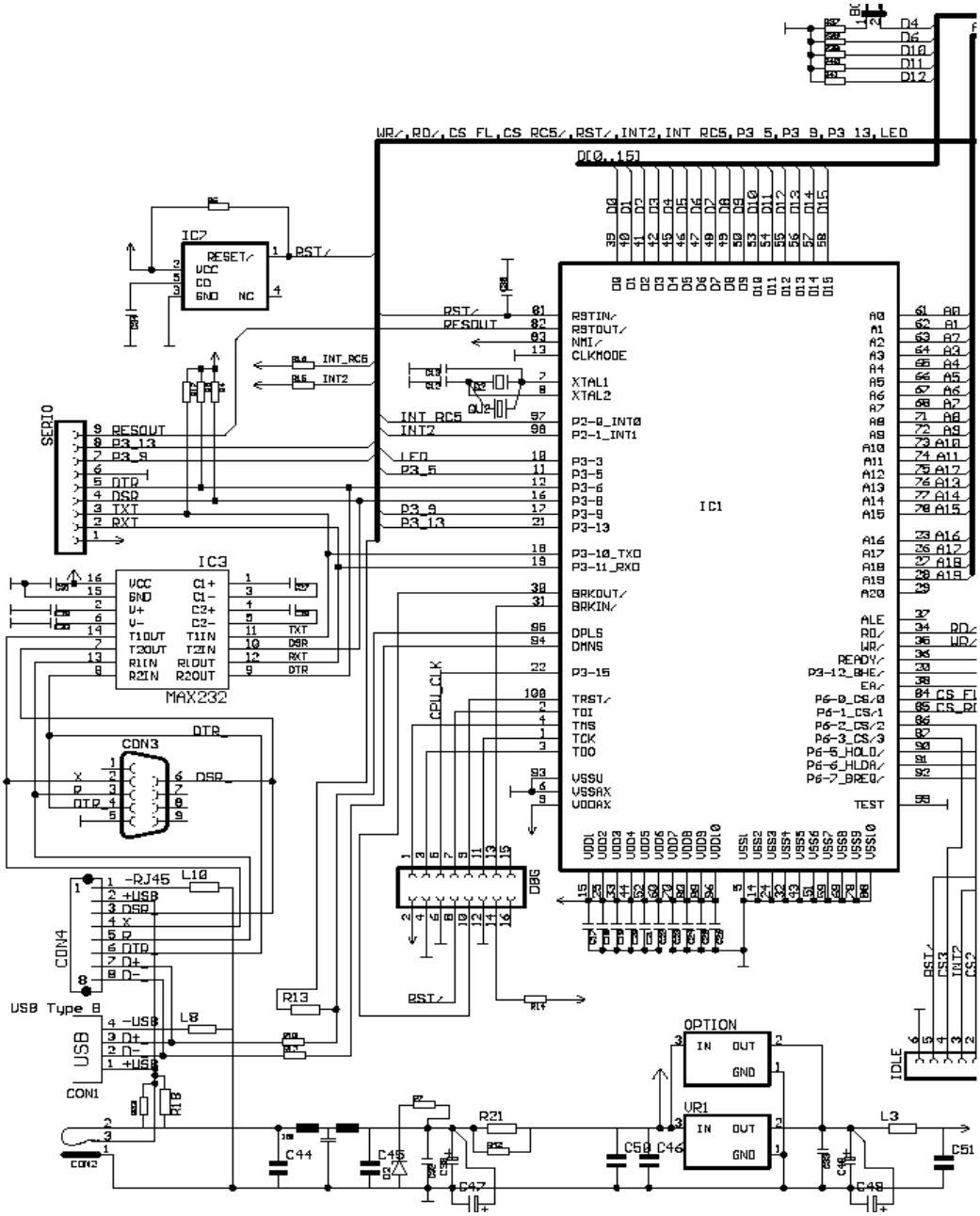

Fig 5. CLRM701 Schematic left part

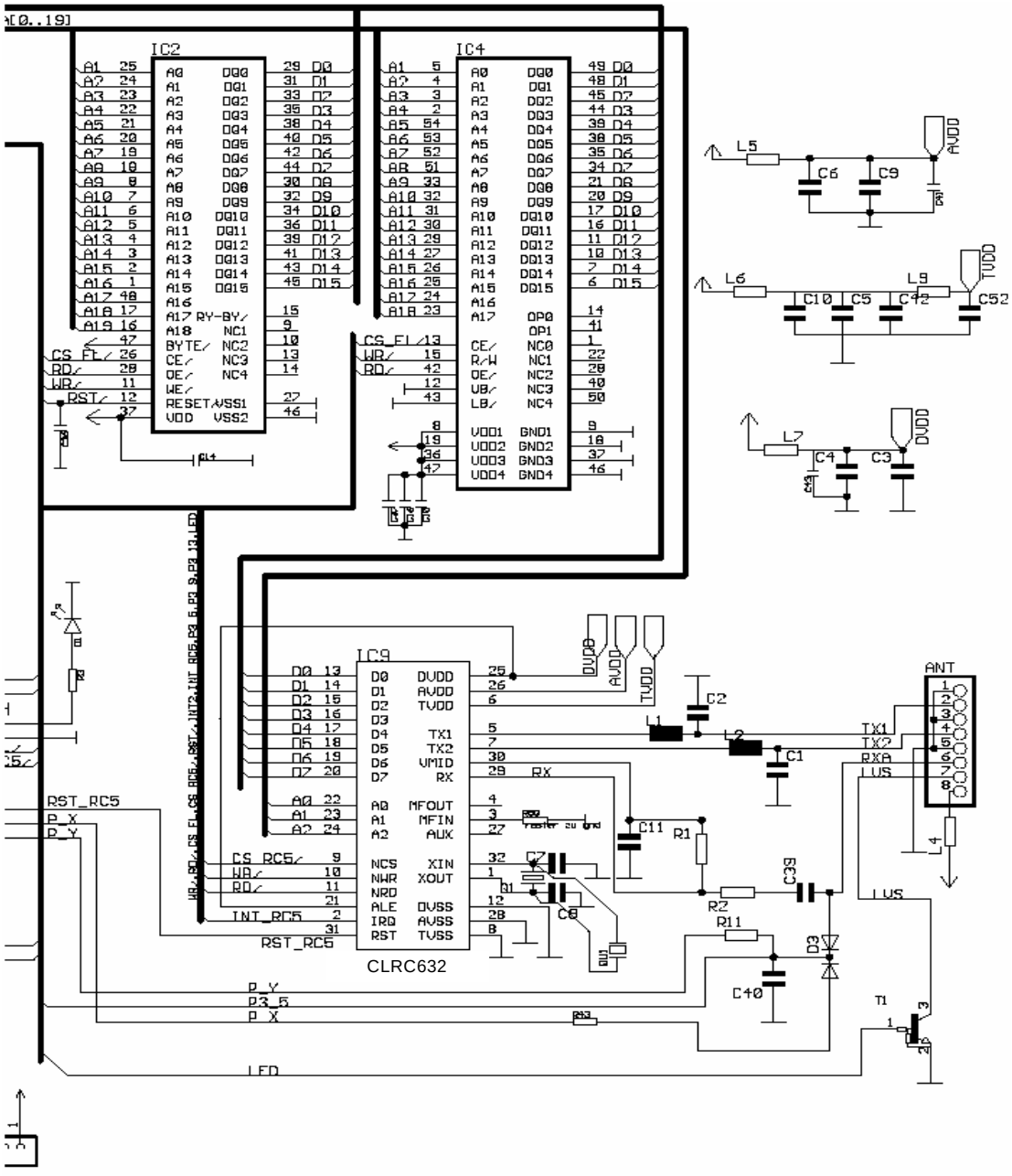

Fig 6. CLRM701 Schematic right part

6.2 Part list

The part list gives a complete overview about the used components. If no supplier or order number is given these parts are standard components.

Parts are subject to multi-sourcing and can be replaced with equivalent part without notice.

Table 4. Part list CLRM701

Qty	Part	Value	Package	Remarks	CLRM701
1	PCB	72x72		scratched edges	X
1	ANT	PHD1x8	1X08	single pin row	X
1	BOOT	PHD1x2	JP1	bootstrap jumper	X
2	C1, C2	68p	C0805	NPO, 2 %	X
2	C3, C6	100p	C0805	NPO, 5 %	X
2	C4, C5	10n	C0805	X7R	X
2	C7, C8	33p	C0805	NPO, 5 %	X
1	C9	10n	C0805	X7R	X
1	C10	100p	C0805	NPO, 5 %	X
1	C11	100n	C0805	NPO, 10 %	X
1	C12	47p	C0805	NPO, 5 %	X
17	C14, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C41, C42, C43, C44, C45	100n	C0805	X7R	X
7	C15, C27, C28, C29, C30, C37, C46	100n	C0805	X7R	n.a.
1	C31	4.7n	C0805	X7R	X
2	C32, C33	2.2µ	C0805	ceramic decoupling capacitance 6,3 V 10 %	X
1	C34	220n	C0805	X7R	X
4	C35, C36, C50, C51	10n	C0805	X7R	X
2	C38, C48	33µ,10V	TANTAL-D	Tantal	X
1	C39	1n	C0805	NPO, 10 %	X
1	C40	22n	C0805	NPO, 5 %	n.a.
2	C47, C49	option	ES-2,5	optional to part C38, C48	X
1	C52	10p	C0805	NPO, 5 %	X
1	CON1	USB Type B	RWD61729	USB, Type B, socket	X
1	CON2	DC PWR socket	HOHLB02	DC power socket, outer diam. 5,5 mm inner diam. 2,5 mm	n.a.
1	CON3	DB9 socket	F09H	9 pol. DSub Socket	n.a.
1	CON4	RJ45LSMD socket	555764-1	RJ45 Connector for RS232, Power, USB	n.a.
1	D1	TOP-LED	PLCC2	SMD LED green, PLCC2 package	X
1	D2	5,6	DIO-MINI	BZV55C 5,6 V SOD-80, MINIMELF	X
1	D3	DKKSOT23	SOT23C	Schottky Diode 30 V SOT23 BAT64-05	n.a.

Table 4. Part list CLRM701

Qty	Part	Value	Package	Remarks	CLRM701
1	DBG	PHD2x8	FE08-2		n.a.
1	IC1	C161U_M	TQFP-100	SAB-C161U-LF V1.3	X
1	IC2	AM29F800B	TSOP48	(A)M29F400B	X
1	IC3	MAX232	SO16	MAX232ECSE	n.a.
1	IC4	TC554161	TSOPII54	SRAM, TC554161AFT-V	n.a.
1	IC5	DSS30655	EMI	EMI filter, DSS30655Y5S102M100	X
1	IC7	MC33465N	SOT-23-5	Reset IC, MC33465N-27atr	X
1	IC9	RC632	SO-32L	CL RC 632	X
1	IDLE	PHD1x6	FE06		n.a.
2	L1, L2	1µH	L_NL322	NL322522T-1R0J, 5%	X
2	L3, L4	470nH			X
3	L5, L6, L7	0		Substitute Resistor 0R	X
2	L8, L10	100nH			X
1	L9	22nH			X
1	OPTION	option	TO220V	optional equipment for part VR1	X
1	Q1	13.56MHz	HC49U-V	SMD-Quarz, HC 49 US SMD, 13,56 MHz SMD or through hole contacts	X
1	QU1	option	HC49U-V	optional for part Q1	X
1	Q2	8MHz	SD3	SMD-Quarz, HC 49 US SMD, 8MHz, SMD or through hole contacts	X
1	QU2	option	SD3	optional for part Q2	X
1	R1	820	R0805	NPO, 1 %	X
1	R2	560	R0805	NPO, 1 %	X
1	R3	470	R0805	5 %	X
12	R4, R5, R6, R14, R15, R16, R17, R37, R38, R39, R40, R41	10k	R0805	5 %	X
1	R7	82	R0805	5 %	X
2	R10, R12	27	R0805	1 %	X
1	R11	11k	R0805	2 %	n.a.
1	R13	1k5	R0805	5 %	X
5	R18, R21, R42, R50, R53	0	R0805		X
1	R43	820	R0805	1 %	n.a.
2	S1, S2	Screw		2.5x7 mm tin screw	X
2	S1I, S2I	Isolate		screw isolation foil	X
1	SERIO	PHD1x9	FE09		n.a.
1	T1	BCR108	SOT-23	switching transistor	X
1	VR1	LT1086_SMD	DDPAK	voltage regulator 3.3 V SMD (LT1086CM-3.3) or through hole contacts (LT1086CT-3.3)	X

6.3 Layout

The CLRM701 is designed using a four layer PCB. The following Figure 7 to Figure 12 show the component placements and all other layers.

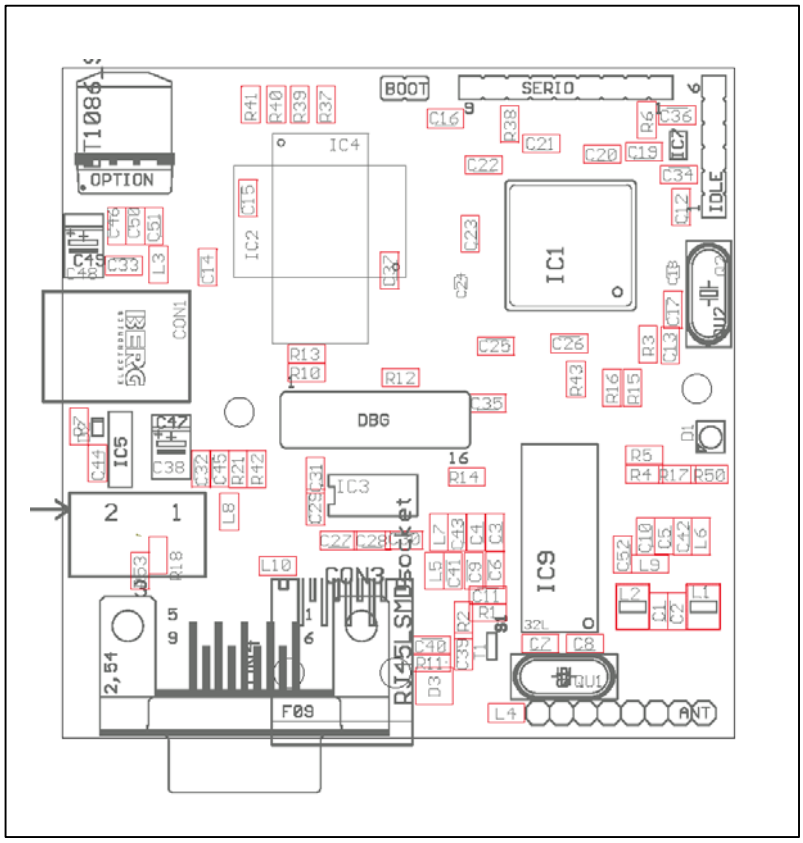

Fig 7. CLRM701 Complete Component Placement

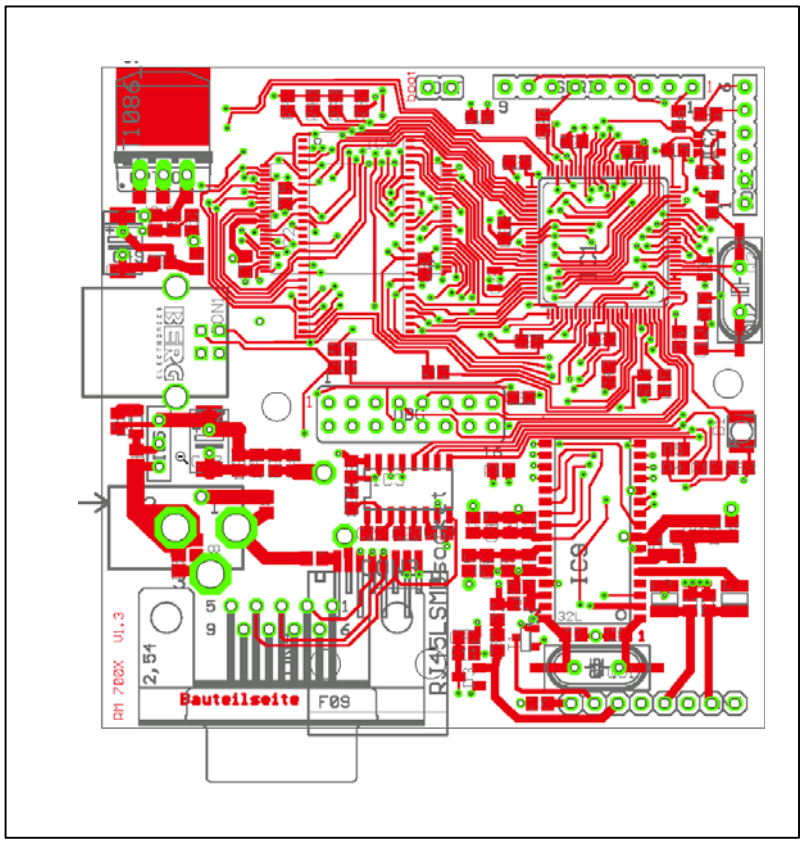

Fig 8. CLRM701 Top Layer

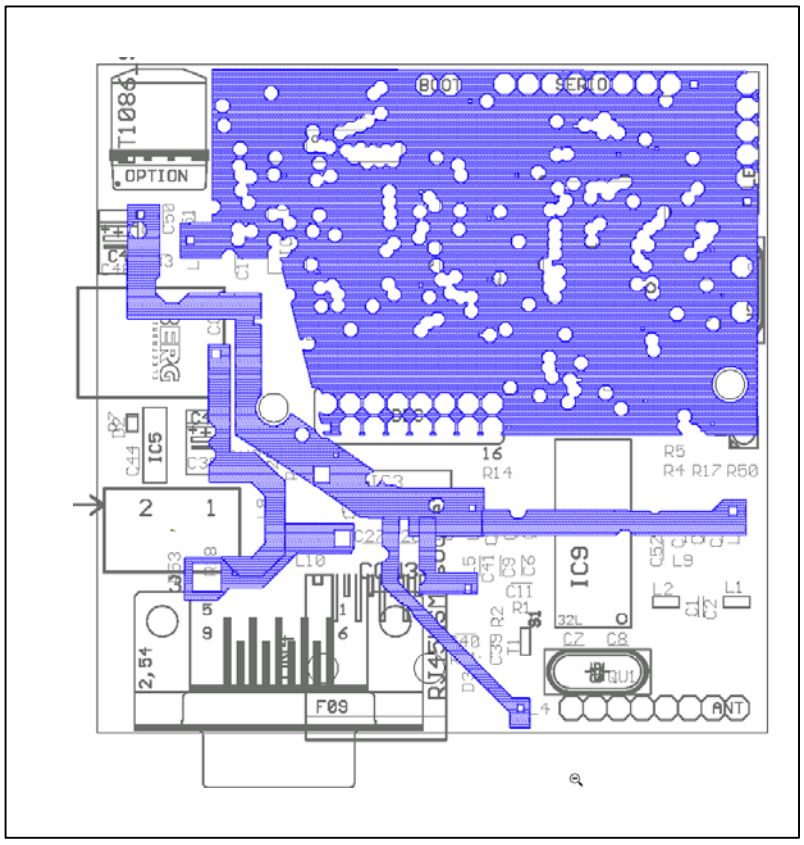

Fig 9. CLRM701 Supply Layer

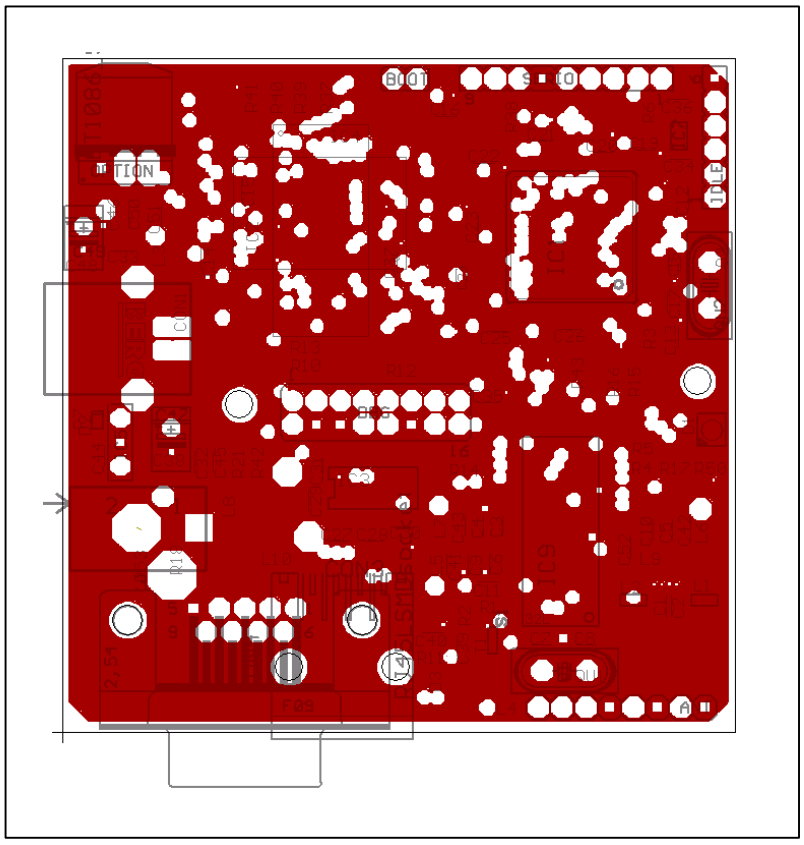

Fig 10. CLRM701 Ground Layer

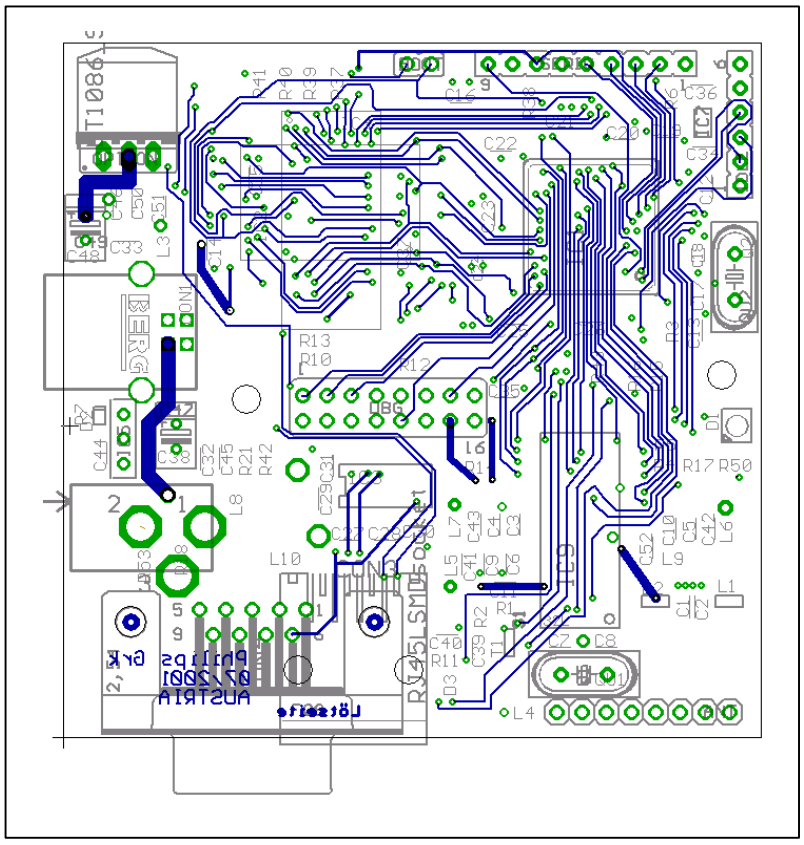

Fig 11. CLRM701 Bottom Layer

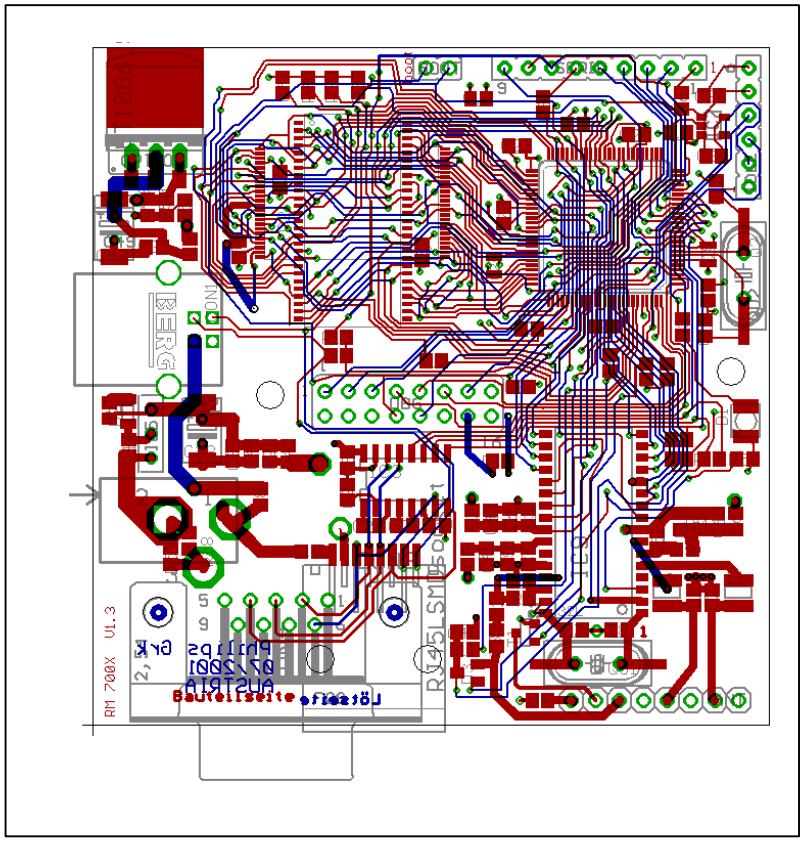

Fig 12. CLRM701 Top and Bottom View

7. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Type	Max	Unit
T_{amb}	ambient temperature		-10	+25	+70	°C
VDD	DC Supply Voltage	DVSS = 0V	4.5	5.0	5.5	V

8. Characteristics

Table 6. USB- characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
USB- baud	USB- baudrate	cable length max. 3 m	-	12	-	Mbaud

9. Current consumption

Table 7. Current consumption

Symbol	Parameter	Conditions	Min	Type	Max	Unit
I_{DVDD}	supply current	StandBy	-	70	-	mA
I_{DVDD}	supply current	Idle, RF off	-	160	-	mA
I_{DVDD}	supply current	Idle, RF on	-	250	-	mA

10. Operating distance

Table 8. Operating distance

Symbol	Parameter	Conditions	Min	Type	Max	Unit
OD	operating distance	used antenna : MFAN700, measured from the middle of the reader surface	-	75	-	mm

11. Support information

For additional information, please visit http.//www.nxp.com

12. References

[1] Mifare® & ICODE CLRC632 Multiple protocol contactless reader IC

[2] Mifare® MFRM700 Antenna and matching adapter description

To download referred documents please visit http://www.nxp.com

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
101432	24 May 2007	Product data sheet		3.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name.			
101431	November 2004	Product data sheet	Add ordering info, Addition to feature set	3.0
101430	July 2004	Product data sheet		2.0
101420	April 2004	initial version		

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 24 May 2007
Document identifier: 101432