PSoC® Creator™
Project Datasheet for CDBAssistNextGen

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5 device. For details on all the systems listed above, please refer to the PSoC 5 Technical Reference Manual .

Figure 1. CY8C58LP Device Family Block Diagram

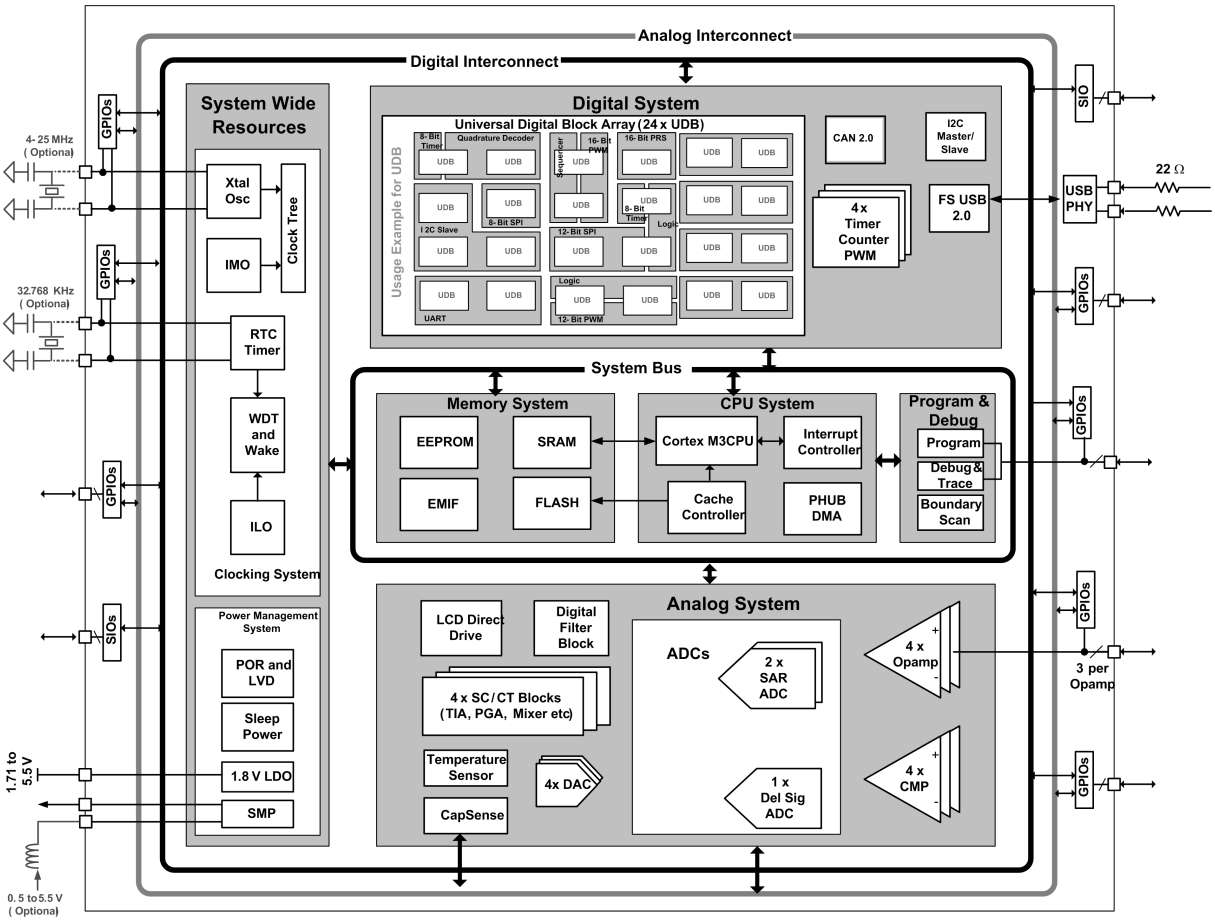


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5888AXI-LP096
Package Name	100-TQFP
Architecture	PSoC 5
Family	CY8C58LP
CPU speed (MHz)	80
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E160069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

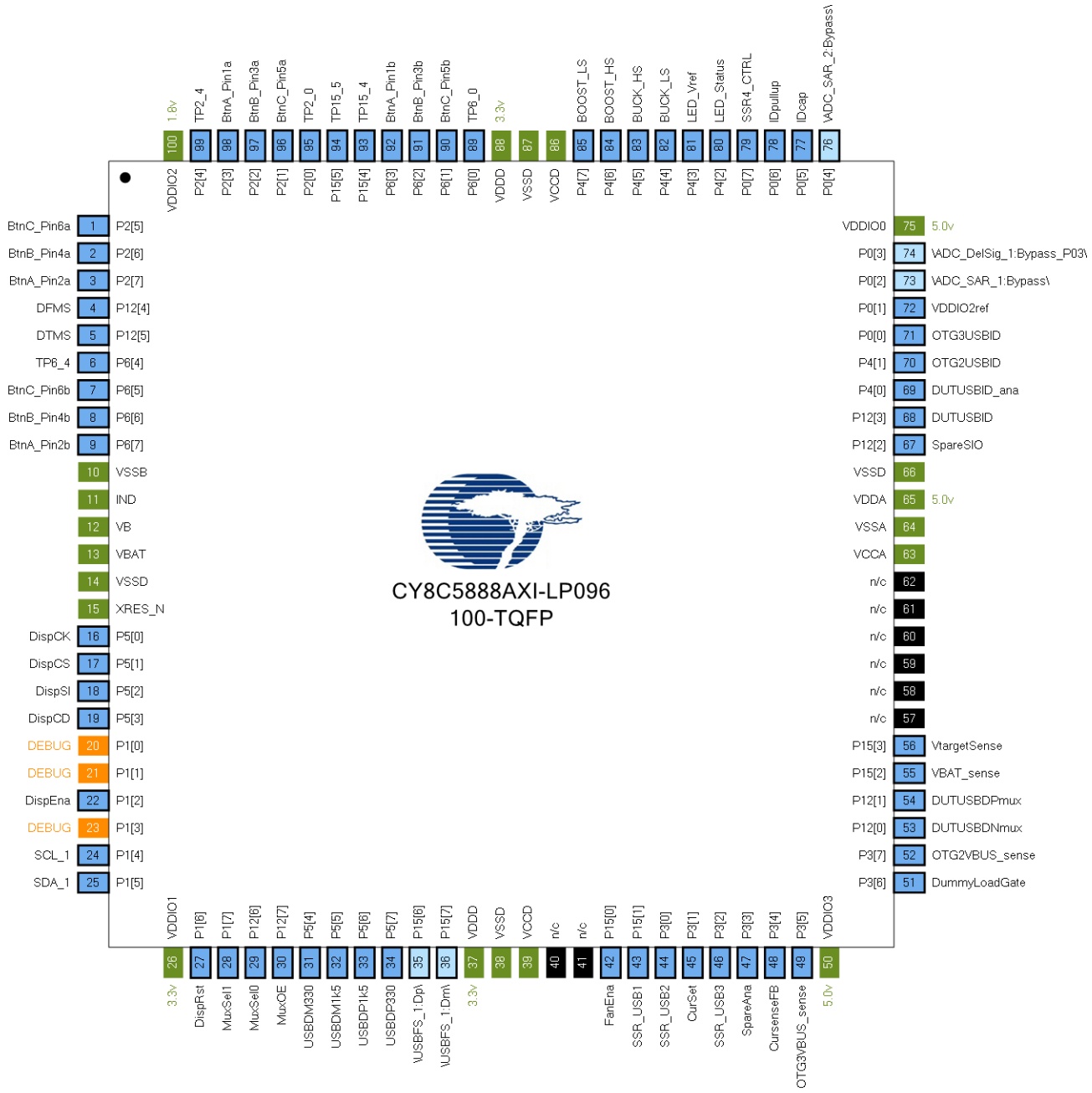
Resource Type	Used	Free	Max	% Used
Digital Clocks	4	4	8	50.00 %
Analog Clocks	1	3	4	25.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	18	14	32	56.25 %
IO	76	-4	72	105.56 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	1	0	1	100.00 %
USB	1	0	1	100.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	61	131	192	31.77 %
Unique P-terms	147	237	384	38.28 %
Total P-terms	172			
Datapath Cells	9	15	24	37.50 %
Status Cells	11	13	24	45.83 %
StatusI Registers	5			
Sync Cells (x15)	4			
Routed Count7 Load/Enable	2			
Control Cells	6	18	24	25.00 %
Control Registers	4			
Count7 Cells	2			
Opamp	2	2	4	50.00 %
Comparator	0	4	4	0.00 %
Delta-Sigma ADC	1	0	1	100.00 %
LPF	0	2	2	0.00 %
SAR ADC	2	0	2	100.00 %
Analog (SC/CT) Blocks	1	3	4	25.00 %

Resource Type	Used	Free	Max	% Used
DAC				
VIDAC	4	0	4	100.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	BtnC_Pin6a	Analog	HiZ analog	HiZ Analog Unb
2	P2[6]	BtnB_Pin4a	Analog	HiZ analog	HiZ Analog Unb
3	P2[7]	BtnA_Pin2a	Analog	HiZ analog	HiZ Analog Unb
4	P12[4]	DFMS	Dgtl I/O	HiZ digital	HiZ Analog Unb
5	P12[5]	DTMS	Dgtl I/O	HiZ digital	HiZ Analog Unb
6	P6[4]	TP6_4	Software In/Out	OD, DL	HiZ Analog Unb
7	P6[5]	BtnC_Pin6b	Dgtl I/O	HiZ digital	HiZ Analog Unb
8	P6[6]	BtnB_Pin4b	Dgtl I/O	HiZ digital	HiZ Analog Unb
9	P6[7]	BtnA_Pin2b	Dgtl I/O	HiZ digital	HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	DispCK	Dgtl Out	Strong drive	HiZ Analog Unb
17	P5[1]	DispCS	Dgtl Out	Strong drive	HiZ Analog Unb
18	P5[2]	DispSI	Dgtl Out	Strong drive	HiZ Analog Unb
19	P5[3]	DispCD	Software Output	Strong drive	HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	DispEna	Software Output	Strong drive	HiZ Analog Unb
23	P1[3]	Debug:SWV	Reserved		
24	P1[4]	SCL_1	Dgtl I/O	OD, DL	HiZ Analog Unb
25	P1[5]	SDA_1	Dgtl I/O	OD, DL	HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	DispRst	Software Output	Strong drive	HiZ Analog Unb
28	P1[7]	MuxSel1	Software Output	Strong drive	HiZ Analog Unb
29	P12[6]	MuxSel0	Software Output	Strong drive	HiZ Analog Unb
30	P12[7]	MuxOE	Software Output	Strong drive	HiZ Analog Unb
31	P5[4]	USBDM330	Software Input	HiZ digital	HiZ Analog Unb
32	P5[5]	USBDM1k5	Software Input	HiZ digital	HiZ Analog Unb
33	P5[6]	USBDP1k5	Software Input	HiZ digital	HiZ Analog Unb
34	P5[7]	USBDP330	Software Input	HiZ digital	HiZ Analog Unb
35	P15[6]	USB:D+	Reserved		
36	P15[7]	USB:D-	Reserved		

Pin	Port	Name	Type	Drive Mode	Reset State
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	FanEna	Software Output	Strong drive	HiZ Analog Unb
43	P15[1]	SSR_USB1	Software Output	Strong drive	HiZ Analog Unb
44	P3[0]	SSR_USB2	Software Output	Strong drive	HiZ Analog Unb
45	P3[1]	CurSet	Analog	HiZ analog	HiZ Analog Unb
46	P3[2]	SSR_USB3	Software Output	Strong drive	HiZ Analog Unb
47	P3[3]	SpareAna	Analog	HiZ analog	HiZ Analog Unb
48	P3[4]	CursenseFB	Analog	HiZ analog	HiZ Analog Unb
49	P3[5]	OTG3VBUS_sense	Analog	HiZ analog	HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GPIO [unused]	Reserved		
52	P3[7]	OTG2VBUS_sense	Analog	HiZ analog	HiZ Analog Unb
53	P12[0]	DUTUSBDNmux	Dgtl I/O	HiZ digital	HiZ Analog Unb
54	P12[1]	DUTUSBDPmux	Dgtl I/O	HiZ digital	HiZ Analog Unb
55	P15[2]	VBAT_sense	Analog	HiZ analog	HiZ Analog Unb
56	P15[3]	VtargetSense	Analog / Dgtl In	HiZ digital	HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	SpareSIO	Dgtl I/O	HiZ digital	HiZ Analog Unb
68	P12[3]	DUTUSBID	Dgtl I/O	HiZ digital	HiZ Analog Unb
69	P4[0]	DUTUSBID_ana	Analog	HiZ analog	HiZ Analog Unb
70	P4[1]	OTG2USBID	Analog	HiZ analog	HiZ Analog Unb
71	P0[0]	OTG3USBID	Analog	HiZ analog	HiZ Analog Unb
72	P0[1]	GPIO [unused]	Reserved		
73	P0[2]	\ADC_SAR_1:Bypass\	Analog	HiZ analog	HiZ Analog Unb
74	P0[3]	\ADC_DelSig_1:Bypass_P03\	Analog	HiZ analog	HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	\ADC_SAR_2:Bypass\	Analog	HiZ analog	HiZ Analog Unb
77	P0[5]	IDcap	Analog	HiZ analog	HiZ Analog Unb
78	P0[6]	IDpullup	Analog	HiZ analog	HiZ Analog Unb
79	P0[7]	SSR4_CTRL	Software Output	Res pull up	HiZ Analog Unb
80	P4[2]	LED_Status	Software Output	OD, DL	HiZ Analog Unb
81	P4[3]	LED_Vref	Software Output	OD, DL	HiZ Analog Unb
82	P4[4]	BUCK_LS	Dgtl Out	Strong drive	HiZ Analog Unb
83	P4[5]	BUCK_HS	Dgtl Out	Strong drive	HiZ Analog Unb
84	P4[6]	BOOST_HS	Dgtl Out	Strong drive	HiZ Analog Unb
85	P4[7]	BOOST_LS	Dgtl Out	Strong drive	HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	TP6_0	Software In/Out	OD, DL	HiZ Analog Unb
90	P6[1]	BtnC_Pin5b	Dgtl I/O	HiZ digital	HiZ Analog Unb

2 Pins

Pin	Port	Name	Type	Drive Mode	Reset State
91	P6[2]	BtnB_Pin3b	Dgtl I/O	HiZ digital	HiZ Analog Unb
92	P6[3]	BtnA_Pin1b	Dgtl I/O	HiZ digital	HiZ Analog Unb
93	P15[4]	TP15_4	Software In/Out	OD, DL	HiZ Analog Unb
94	P15[5]	TP15_5	Software In/Out	OD, DL	HiZ Analog Unb
95	P2[0]	TP2_0	Software In/Out	OD, DL	HiZ Analog Unb
96	P2[1]	BtnC_Pin5a	Analog	HiZ analog	HiZ Analog Unb
97	P2[2]	BtnB_Pin3a	Analog	HiZ analog	HiZ Analog Unb
98	P2[3]	BtnA_Pin1a	Analog	HiZ analog	HiZ Analog Unb
99	P2[4]	TP2_4	Software In/Out	OD, DL	HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ analog = High impedance analog
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl I/O = Digital In/Out
- HiZ digital = High impedance digital
- OD, DL = Open drain, drives low
- Dgtl Out = Digital Output
- Analog / Dgtl In = Analog / Digital Input
- Res pull up = Resistive pull up

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	OTG3USBID	Analog	HiZ analog	HiZ Analog Unb
P0[1]	72	GPIO [unused]	Reserved		
P0[2]	73	\ADC_SAR_1:Bypass\	Analog	HiZ analog	HiZ Analog Unb
P0[3]	74	\ADC_DelSig_1:Bypass_P03\	Analog	HiZ analog	HiZ Analog Unb
P0[4]	76	\ADC_SAR_2:Bypass\	Analog	HiZ analog	HiZ Analog Unb
P0[5]	77	IDcap	Analog	HiZ analog	HiZ Analog Unb
P0[6]	78	IDpullup	Analog	HiZ analog	HiZ Analog Unb
P0[7]	79	SSR4_CTRL	Software Output	Res pull up	HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	DispEna	Software Output	Strong drive	HiZ Analog Unb
P1[3]	23	Debug:SWV	Reserved		
P1[4]	24	SCL_1	Dgtl I/O	OD, DL	HiZ Analog Unb
P1[5]	25	SDA_1	Dgtl I/O	OD, DL	HiZ Analog Unb
P1[6]	27	DispRst	Software Output	Strong drive	HiZ Analog Unb
P1[7]	28	MuxSel1	Software Output	Strong drive	HiZ Analog Unb
P12[0]	53	DUTUSBDNmux	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[1]	54	DUTUSBDPmux	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[2]	67	SpareSIO	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[3]	68	DUTUSBID	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[4]	4	DFMS	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[5]	5	DTMS	Dgtl I/O	HiZ digital	HiZ Analog Unb
P12[6]	29	MuxSel0	Software Output	Strong drive	HiZ Analog Unb
P12[7]	30	MuxOE	Software Output	Strong drive	HiZ Analog Unb
P15[0]	42	FanEna	Software Output	Strong drive	HiZ Analog Unb
P15[1]	43	SSR_USB1	Software Output	Strong drive	HiZ Analog Unb
P15[2]	55	VBAT_sense	Analog	HiZ analog	HiZ Analog Unb
P15[3]	56	VtargetSense	Analog / Dgtl In	HiZ digital	HiZ Analog Unb
P15[4]	93	TP15_4	Software In/Out	OD, DL	HiZ Analog Unb
P15[5]	94	TP15_5	Software In/Out	OD, DL	HiZ Analog Unb
P15[6]	35	USB:D+	Reserved		
P15[7]	36	USB:D-	Reserved		
P2[0]	95	TP2_0	Software In/Out	OD, DL	HiZ Analog Unb
P2[1]	96	BtnC_Pin5a	Analog	HiZ analog	HiZ Analog Unb
P2[2]	97	BtnB_Pin3a	Analog	HiZ analog	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P2[3]	98	BtnA_Pin1a	Analog	HiZ analog	HiZ Analog Unb
P2[4]	99	TP2_4	Software In/Out	OD, DL	HiZ Analog Unb
P2[5]	1	BtnC_Pin6a	Analog	HiZ analog	HiZ Analog Unb
P2[6]	2	BtnB_Pin4a	Analog	HiZ analog	HiZ Analog Unb
P2[7]	3	BtnA_Pin2a	Analog	HiZ analog	HiZ Analog Unb
P3[0]	44	SSR_USB2	Software Output	Strong drive	HiZ Analog Unb
P3[1]	45	CurSet	Analog	HiZ analog	HiZ Analog Unb
P3[2]	46	SSR_USB3	Software Output	Strong drive	HiZ Analog Unb
P3[3]	47	SpareAna	Analog	HiZ analog	HiZ Analog Unb
P3[4]	48	CursenseFB	Analog	HiZ analog	HiZ Analog Unb
P3[5]	49	OTG3VBUS_sense	Analog	HiZ analog	HiZ Analog Unb
P3[6]	51	GPIO [unused]	Reserved		
P3[7]	52	OTG2VBUS_sense	Analog	HiZ analog	HiZ Analog Unb
P4[0]	69	DUTUSBID_ana	Analog	HiZ analog	HiZ Analog Unb
P4[1]	70	OTG2USBID	Analog	HiZ analog	HiZ Analog Unb
P4[2]	80	LED_Status	Software Output	OD, DL	HiZ Analog Unb
P4[3]	81	LED_Vref	Software Output	OD, DL	HiZ Analog Unb
P4[4]	82	BUCK_LS	Dgtl Out	Strong drive	HiZ Analog Unb
P4[5]	83	BUCK_HS	Dgtl Out	Strong drive	HiZ Analog Unb
P4[6]	84	BOOST_HS	Dgtl Out	Strong drive	HiZ Analog Unb
P4[7]	85	BOOST_LS	Dgtl Out	Strong drive	HiZ Analog Unb
P5[0]	16	DispCK	Dgtl Out	Strong drive	HiZ Analog Unb
P5[1]	17	DispCS	Dgtl Out	Strong drive	HiZ Analog Unb
P5[2]	18	DispSI	Dgtl Out	Strong drive	HiZ Analog Unb
P5[3]	19	DispCD	Software Output	Strong drive	HiZ Analog Unb
P5[4]	31	USBDM330	Software Input	HiZ digital	HiZ Analog Unb
P5[5]	32	USBDM1k5	Software Input	HiZ digital	HiZ Analog Unb
P5[6]	33	USBDP1k5	Software Input	HiZ digital	HiZ Analog Unb
P5[7]	34	USBDP330	Software Input	HiZ digital	HiZ Analog Unb
P6[0]	89	TP6_0	Software In/Out	OD, DL	HiZ Analog Unb
P6[1]	90	BtnC_Pin5b	Dgtl I/O	HiZ digital	HiZ Analog Unb
P6[2]	91	BtnB_Pin3b	Dgtl I/O	HiZ digital	HiZ Analog Unb
P6[3]	92	BtnA_Pin1b	Dgtl I/O	HiZ digital	HiZ Analog Unb
P6[4]	6	TP6_4	Software In/Out	OD, DL	HiZ Analog Unb
P6[5]	7	BtnC_Pin6b	Dgtl I/O	HiZ digital	HiZ Analog Unb
P6[6]	8	BtnB_Pin4b	Dgtl I/O	HiZ digital	HiZ Analog Unb
P6[7]	9	BtnA_Pin2b	Dgtl I/O	HiZ digital	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Res pull up = Resistive pull up
- Dgtl I/O = Digital In/Out

- OD, DL = Open drain, drives low
- HiZ digital = High impedance digital
- Analog / Dgtl In = Analog / Digital Input
- Dgtl Out = Digital Output

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\ADC_DelSig_1:Bypass_P03\	P0[3]	Analog	HiZ Analog Unb
\ADC_SAR_1:Bypass\	P0[2]	Analog	HiZ Analog Unb
\ADC_SAR_2:Bypass\	P0[4]	Analog	HiZ Analog Unb
BOOST_HS	P4[6]	Dgtl Out	HiZ Analog Unb
BOOST_LS	P4[7]	Dgtl Out	HiZ Analog Unb
BtnA_Pin1a	P2[3]	Analog	HiZ Analog Unb
BtnA_Pin1b	P6[3]	Dgtl I/O	HiZ Analog Unb
BtnA_Pin2a	P2[7]	Analog	HiZ Analog Unb
BtnA_Pin2b	P6[7]	Dgtl I/O	HiZ Analog Unb
BtnB_Pin3a	P2[2]	Analog	HiZ Analog Unb
BtnB_Pin3b	P6[2]	Dgtl I/O	HiZ Analog Unb
BtnB_Pin4a	P2[6]	Analog	HiZ Analog Unb
BtnB_Pin4b	P6[6]	Dgtl I/O	HiZ Analog Unb
BtnC_Pin5a	P2[1]	Analog	HiZ Analog Unb
BtnC_Pin5b	P6[1]	Dgtl I/O	HiZ Analog Unb
BtnC_Pin6a	P2[5]	Analog	HiZ Analog Unb
BtnC_Pin6b	P6[5]	Dgtl I/O	HiZ Analog Unb
BUCK_HS	P4[5]	Dgtl Out	HiZ Analog Unb
BUCK_LS	P4[4]	Dgtl Out	HiZ Analog Unb
CursenseFB	P3[4]	Analog	HiZ Analog Unb
CurSet	P3[1]	Analog	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
DFMS	P12[4]	Dgtl I/O	HiZ Analog Unb
DispCD	P5[3]	Software Output	HiZ Analog Unb
DispCK	P5[0]	Dgtl Out	HiZ Analog Unb
DispCS	P5[1]	Dgtl Out	HiZ Analog Unb
DispEna	P1[2]	Software Output	HiZ Analog Unb
DispRst	P1[6]	Software Output	HiZ Analog Unb
DispSI	P5[2]	Dgtl Out	HiZ Analog Unb
DTMS	P12[5]	Dgtl I/O	HiZ Analog Unb
DUTUSBDNmux	P12[0]	Dgtl I/O	HiZ Analog Unb
DUTUSBDPmux	P12[1]	Dgtl I/O	HiZ Analog Unb
DUTUSBID	P12[3]	Dgtl I/O	HiZ Analog Unb
DUTUSBID_ana	P4[0]	Analog	HiZ Analog Unb
FanEna	P15[0]	Software Output	HiZ Analog Unb
IDcap	P0[5]	Analog	HiZ Analog Unb
IDpullup	P0[6]	Analog	HiZ Analog Unb
LED_Status	P4[2]	Software Output	HiZ Analog Unb

Name	Port	Type	Reset State
LED_Vref	P4[3]	Software Output	HiZ Analog Unb
MuxOE	P12[7]	Software Output	HiZ Analog Unb
MuxSel0	P12[6]	Software Output	HiZ Analog Unb
MuxSel1	P1[7]	Software Output	HiZ Analog Unb
OTG2USBID	P4[1]	Analog	HiZ Analog Unb
OTG2VBUS_sense	P3[7]	Analog	HiZ Analog Unb
OTG3USBID	P0[0]	Analog	HiZ Analog Unb
OTG3VBUS_sense	P3[5]	Analog	HiZ Analog Unb
SCL_1	P1[4]	Dgtl I/O	HiZ Analog Unb
SDA_1	P1[5]	Dgtl I/O	HiZ Analog Unb
SpareAna	P3[3]	Analog	HiZ Analog Unb
SpareSIO	P12[2]	Dgtl I/O	HiZ Analog Unb
SSR_USB1	P15[1]	Software Output	HiZ Analog Unb
SSR_USB2	P3[0]	Software Output	HiZ Analog Unb
SSR_USB3	P3[2]	Software Output	HiZ Analog Unb
SSR4_CTRL	P0[7]	Software Output	HiZ Analog Unb
TP15_4	P15[4]	Software In/Out	HiZ Analog Unb
TP15_5	P15[5]	Software In/Out	HiZ Analog Unb
TP2_0	P2[0]	Software In/Out	HiZ Analog Unb
TP2_4	P2[4]	Software In/Out	HiZ Analog Unb
TP6_0	P6[0]	Software In/Out	HiZ Analog Unb
TP6_4	P6[4]	Software In/Out	HiZ Analog Unb
USB:D-	P15[7]	Reserved	
USB:D+	P15[6]	Reserved	
USBDM1k5	P5[5]	Software Input	HiZ Analog Unb
USBDM330	P5[4]	Software Input	HiZ Analog Unb
USBDP1k5	P5[6]	Software Input	HiZ Analog Unb
USBDP330	P5[7]	Software Input	HiZ Analog Unb
VBAT_sense	P15[2]	Analog	HiZ Analog Unb
VtargetSense	P15[3]	Analog / Dgtl In	HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl I/O = Digital In/Out
- Analog / Dgtl In = Analog / Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x1000
Stack Size (bytes)	0x1000
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

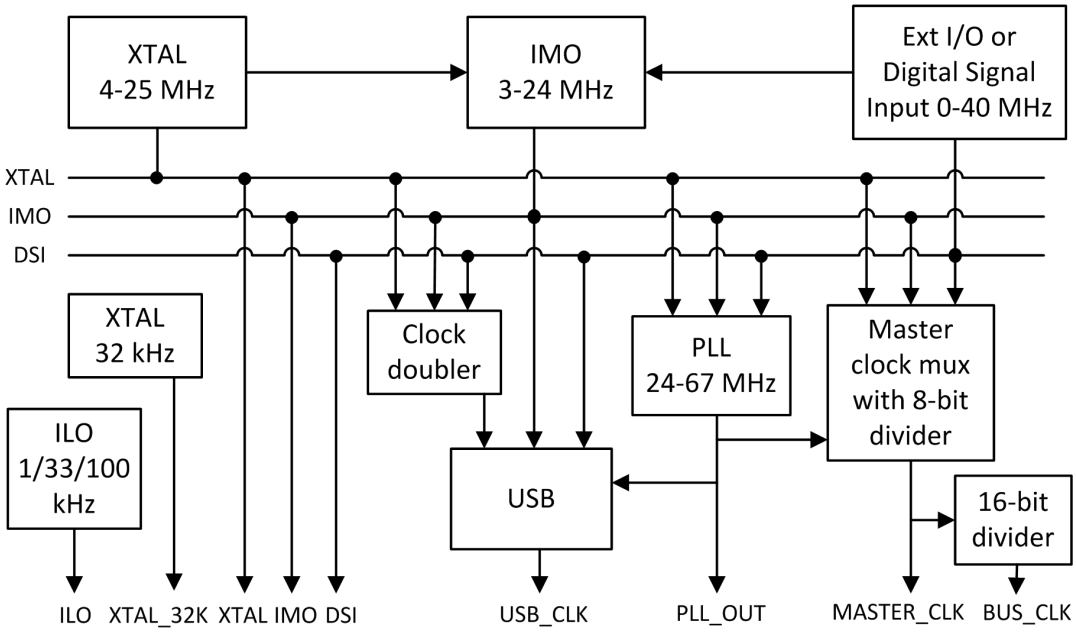
Name	Value
Variable VDDA	False
VDDA (V)	5.0
VDDD (V)	3.3
VDDIO0 (V)	5.0
VDDIO1 (V)	3.3
VDDIO2 (V)	1.8
VDDIO3 (V)	5.0
Temperature Range	0C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	64 MHz	±0.25	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	64 MHz	±0.25	True	True
PLL_OUT	DIGITAL	IMO	64 MHz	64 MHz	±0.25	True	True
USB_CLK	DIGITAL	IMO	48 MHz	48 MHz	±0.25	False	True
IMO	DIGITAL		24 MHz	24 MHz	±0.25	True	True
ILO	DIGITAL		? MHz	100 kHz	-55,+100	True	True
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

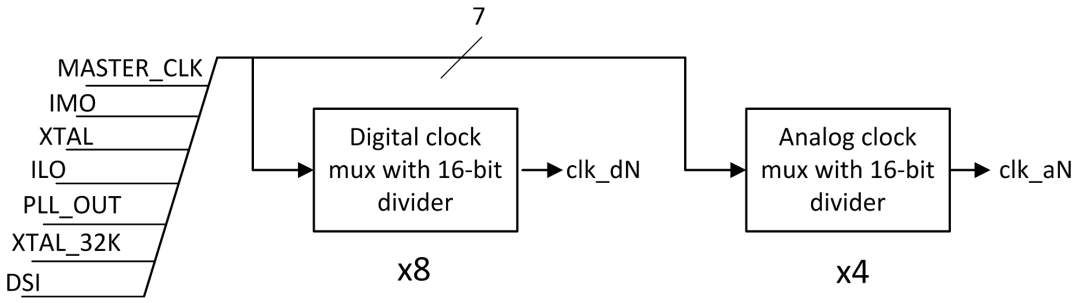


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
USBFS_1_-Clock_vbus	DIGITAL	BUS_CLK	? MHz	64 MHz	±0.25	True	True
Clock_1	DIGITAL	BUS_CLK	? MHz	64 MHz	±0.25	True	True
ADC_DelSig_-1_Ext_CP_Clk	DIGITAL	MASTER_CLK	? MHz	64 MHz	±0.25	True	True
Clock_2	DIGITAL	BUS_CLK	? MHz	64 MHz	±0.25	True	True
IntI2C_-BusClock	DIGITAL	BUS_CLK	? MHz	64 MHz	±0.25	True	True
DispSPI_-IntClock	DIGITAL	MASTER_CLK	16 MHz	16 MHz	±0.25	True	True

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ADC_SAR_1_-theACLK	DIGITAL	MASTER_CLK	1 MHz	1 MHz	±0.25	True	True
ADC_SAR_2_-theACLK	DIGITAL	MASTER_CLK	1 MHz	1 MHz	±0.25	True	True
ADC_DelSig_-1_theACLK	ANALOG	MASTER_CLK	128 kHz	128 kHz	±0.25	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
ADC_DelSig_1_IRQ	7	29
ADC_SAR_1_IRQ	7	0
ADC_SAR_2_IRQ	7	1
IntI2C_I2C_IRQ	7	15
TargetUART_1_-RXInternalInterrupt	7	2
TargetUART_1_-TXInternalInterrupt	7	3
USBFS_1_arb_int	7	22
USBFS_1_bus_reset	7	23
USBFS_1_dp_int	7	12
USBFS_1_ep_0	7	24
USBFS_1_ep_1	7	4
USBFS_1_ep_2	7	5
USBFS_1_ep_3	7	6
USBFS_1_ep_5	7	7
USBFS_1_ep_6	7	8
USBFS_1_ep_7	7	9
USBFS_1_ep_8	7	10
USBFS_1_sof_int	7	21

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

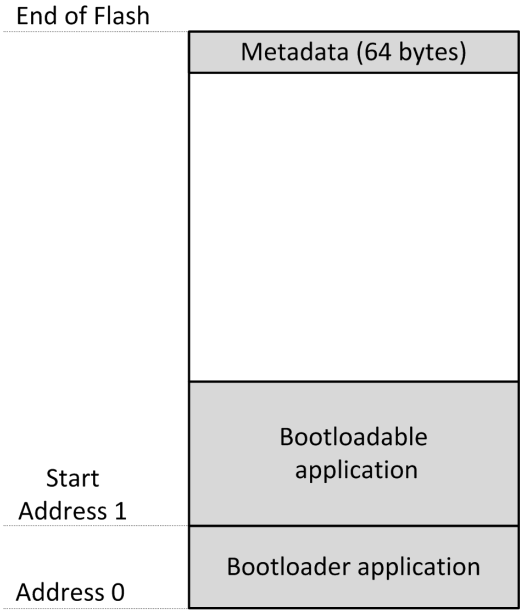
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 5 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 13. Bootloadable Settings

Name	Value
Application Version	0x8013
Application ID	0xCDB3
Application Custom ID	0x43444233
Application Image 1 Start Address	0x4000
Application Image 1 End Address	0x3FEFF
Manual Application Image Placement	True

7.2 Bootloader Application

Table 14. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x8013
Bootloader Start Address	0x0
Bootloader End Address	0x0

For more information on the bootloader and startup please refer to:

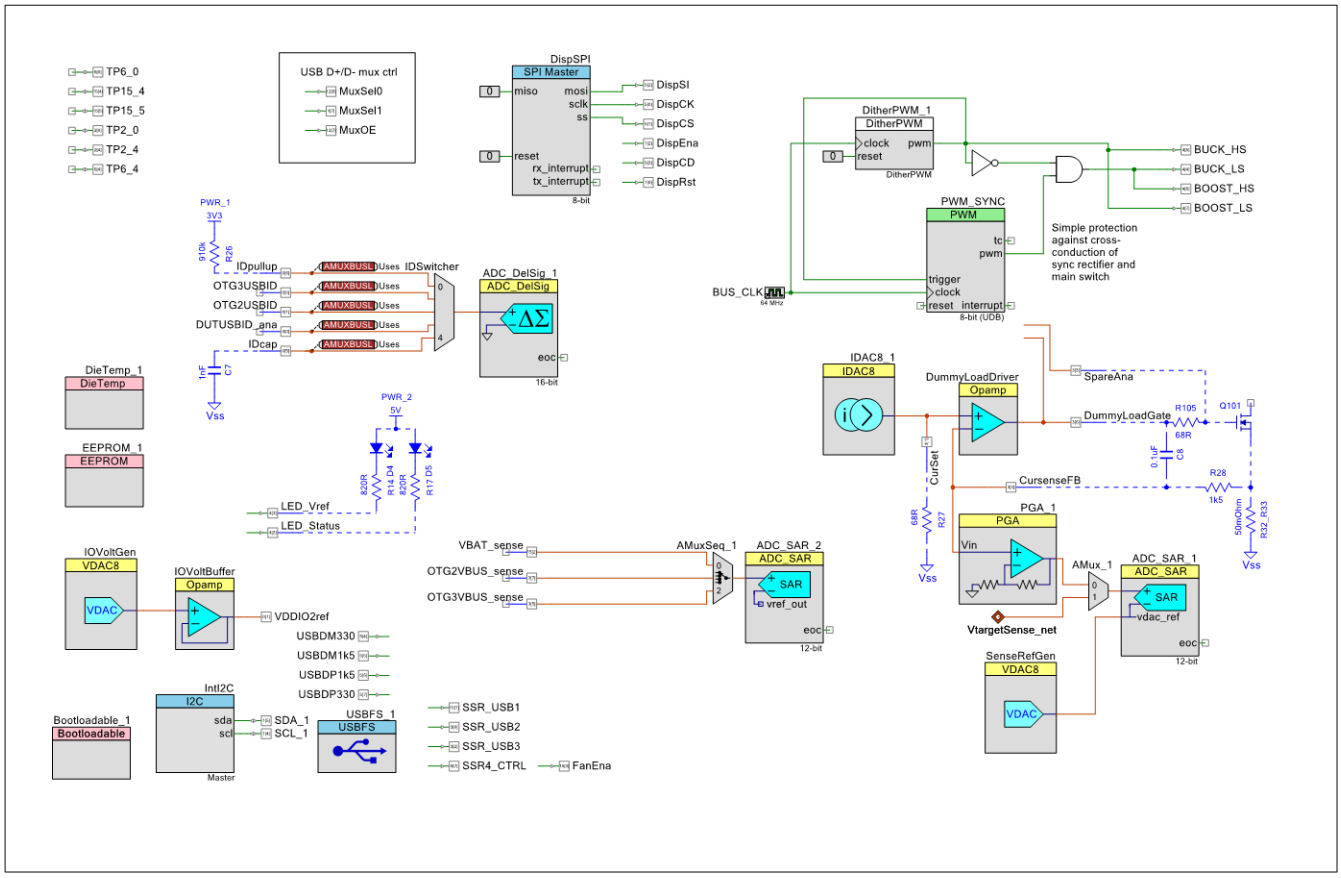
- Startup and Linking chapter in the System Reference Guide
- Datasheet for Bootloader and Bootloadable component

8 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

8.1 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1



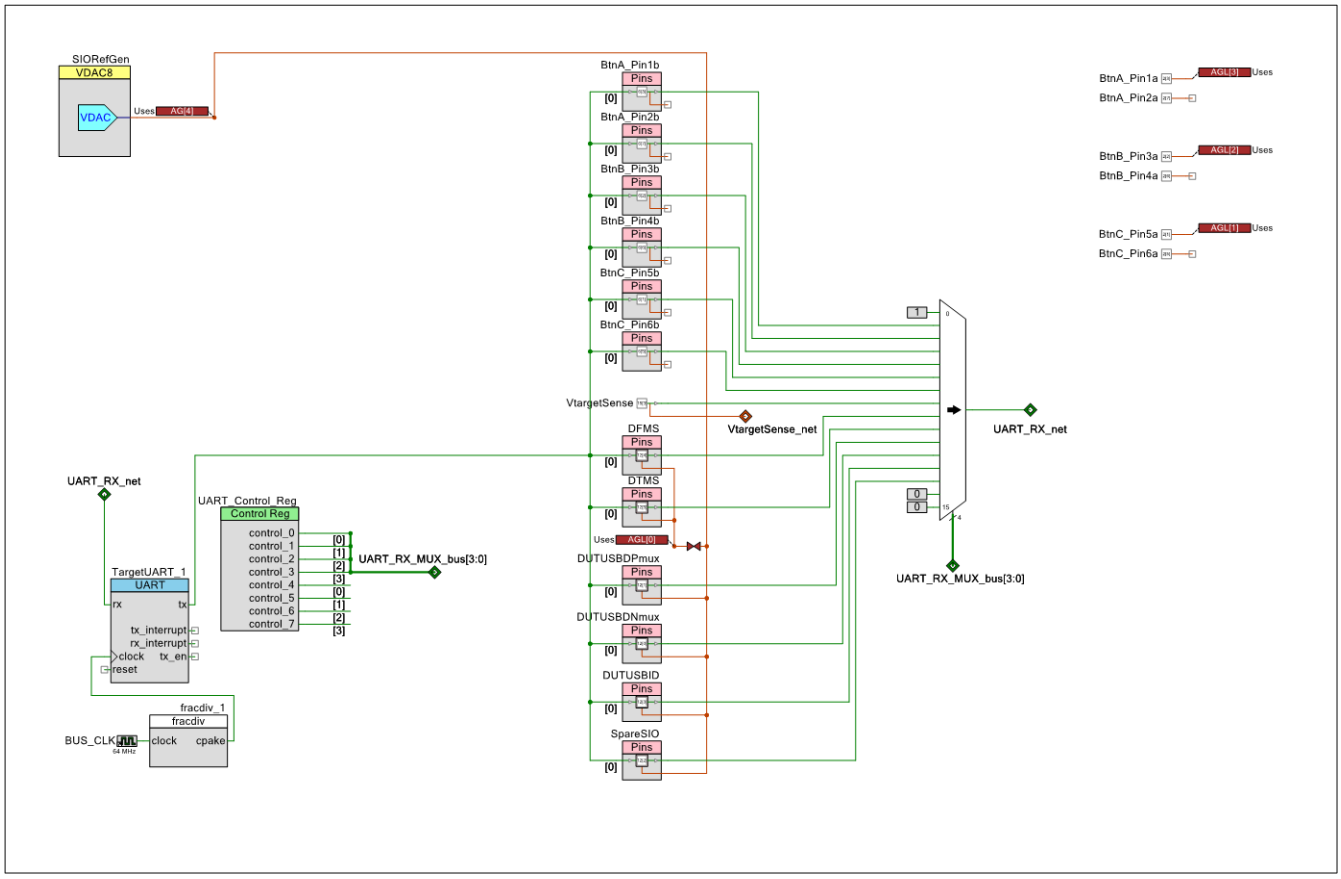
This schematic sheet contains the following component instances:

- Instance ADC_DelSig_1 (type: ADC_DelSig_v3_20)
- Instance ADC_SAR_1 (type: ADC_SAR_v3_0)
- Instance ADC_SAR_2 (type: ADC_SAR_v3_0)
- Instance AMux_1 (type: AMux_v1_80)
- Instance AMuxSeq_1 (type: AMuxSeq_v1_80)
- Instance Bootloadable_1 (type: Bootloadable_v1_40)
- Instance DieTemp_1 (type: DieTemp_v2_0)
- Instance DispSPI (type: SPI_Master_v2_50)
- Instance DitherPWM_1 (type: DitherPWM)
- Instance DummyLoadDriver (type: OpAmp_v1_90)
- Instance EEPROM_1 (type: EEPROM_v3_0)
- Instance IDAC8_1 (type: IDAC8_v2_0)
- Instance IDSwitcher (type: AMux_v1_80)
- Instance IntI2C (type: I2C_v3_50)
- Instance IOVoltBuffer (type: OpAmp_v1_90)
- Instance IOVoltGen (type: VDAC8_v1_90)
- Instance PGA_1 (type: PGA_v2_0)
- Instance PWM_SYNC (type: PWM_v3_30)
- Instance SenseRefGen (type: VDAC8_v1_90)

- Instance USBFS_1 (type: USBFS_v2_80)

8.2 Schematic Sheet: Page 2

Figure 7. Schematic Sheet: Page 2



This schematic sheet contains the following component instances:

- Instance fracdiv_1 (type: fracdiv)
- Instance SIORefGen (type: VDAC8_v1_90)
- Instance TargetUART_1 (type: UART_v2_50)
- Instance UART_Control_Reg (type: CyControlReg_v1_80)

9 Components

9.1 Component type: ADC_DelSig [v3.20]

9.1.1 Instance ADC_DelSig_1

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.20]
Datasheet: online component datasheet for ADC_DelSig

Table 15. Component Parameters for ADC_DelSig_1

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	0.0 to 2*Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Bypassed on P0.3	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	16	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits

Parameter Name	Value	Description
ADC_Resolution_Config4	16	ADC Resolution in bits
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	2 - Continuous	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Bypass Buffer	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.024	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	2000	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz

Parameter Name	Value	Description
Sample_Rate_Config4	10000	Sample Rate in Hz
Start_of_Conversion	Software	Continuous conversions or hardware controlled

9.2 Component type: ADC_SAR [v3.0]

9.2.1 Instance ADC_SAR_1

Description: Successive approximation ADC
Instance type: ADC_SAR [v3.0]
Datasheet: online component datasheet for ADC_SAR

Table 16. Component Parameters for ADC_SAR_1

Parameter Name	Value	Description
ADC_Clock	Internal	Selects either the internal or external clock source.
ADC_Input_Range	Vssa to VDAC*2 (Single Ended)	Parameter used to choose the input operating mode that best supports the range of the signals being measured.
ADC_Power	High Power	This parameter sets the power level of the ADC.
ADC_Reference	Internal Vref, bypassed	Selects the voltage reference source and configuration.
ADC_Resolution	12	Sets the resolution of the ADC in bits.
ADC_SampleMode	Free Running	Selects the mode that the ADC operates in. This can be either free-running or triggered mode.
Enable_next_out	false	This parameter enables the End Of Sampling (eos) output terminal.
Ref_Voltage	2.496	Sets the reference voltage in volts.
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	55556	Specifies the sample rate in Hz.

9.2.2 Instance ADC_SAR_2

Description: Successive approximation ADC
Instance type: ADC_SAR [v3.0]
Datasheet: online component datasheet for ADC_SAR

Table 17. Component Parameters for ADC_SAR_2

Parameter Name	Value	Description
ADC_Clock	Internal	Selects either the internal or external clock source.
ADC_Input_Range	0.0 to 2.048V (Single Ended) 0 to Vref*2	Parameter used to choose the input operating mode that best supports the range of the signals being measured.
ADC_Power	High Power	This parameter sets the power level of the ADC.

Parameter Name	Value	Description
ADC_Reference	Internal Vref, bypassed	Selects the voltage reference source and configuration.
ADC_Resolution	12	Sets the resolution of the ADC in bits.
ADC_SampleMode	Free Running	Selects the mode that the ADC operates in. This can be either free-running or triggered mode.
Enable_next_out	false	This parameter enables the End Of Sampling (eos) output terminal.
Ref_Voltage	1.024	Sets the reference voltage in volts.
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	55556	Specifies the sample rate in Hz.

9.3 Component type: AMux [v1.80]

9.3.1 Instance AMux_1

Description: Multiplexer used to route analog signals.
Instance type: AMux [v1.80]
Datasheet: online component datasheet for AMux

Table 18. Component Parameters for AMux_1

Parameter Name	Value	Description
AtMostOneActive	true	Limit to at most one active channel.
Channels	2	Channel count.
Isolation	Medium	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.

9.3.2 Instance IDSwitcher

Description: Multiplexer used to route analog signals.
Instance type: AMux [v1.80]
Datasheet: online component datasheet for AMux

Table 19. Component Parameters for IDSwitcher

Parameter Name	Value	Description
AtMostOneActive	false	Limit to at most one active channel.
Channels	5	Channel count.
Isolation	Minimum	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.

9.4 Component type: AMuxSeq [v1.80]

9.4.1 Instance AMuxSeq_1

Description: Multiplexer used to route analog signals.
Instance type: AMuxSeq [v1.80]
Datasheet: online component datasheet for AMuxSeq

Table 20. Component Parameters for AMuxSeq_1

Parameter Name	Value	Description
Channels	3	Channel count.
Isolation	Medium	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.

9.5 Component type: Bootloadable [v1.40]

9.5.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.
Instance type: Bootloadable [v1.40]
Datasheet: online component datasheet for Bootloadable

Table 21. Component Parameters for Bootloadable_1

Parameter Name	Value	Description
appCustomID	1128546867	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	52659	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	32787	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	false	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of checksum exclude section
elfFilePath	..\Bootloader.cydsn\-CortexM3\ARM_GCC_-493\Debug\Bootloader.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\Bootloader.cydsn\-CortexM3\ARM_GCC_-493\Debug\Bootloader.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.

Parameter Name	Value	Description
placementAddress	16384	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.

9.6 Component type: CyControlReg [v1.80]

9.6.1 Instance UART_Control_Reg

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 22. Component Parameters for UART_Control_Reg

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	8	Defines the number of outputs needed (1-8)

9.7 Component type: DieTemp [v2.0]

9.7.1 Instance DieTemp_1

Description: This component provides an API to aquire the temperature of the DIE.
Instance type: DieTemp [v2.0]
Datasheet: online component datasheet for DieTemp

9.8 Component type: DitherPWM [v0.0]

9.8.1 Instance DitherPWM_1

Description: (custom component)
Instance type: DitherPWM [v0.0]
Datasheet: (not available)

9.9 Component type: EEPROM [v3.0]

9.9.1 Instance EEPROM_1

Description: Provides an API to Erase and Write EEPROM.
Instance type: EEPROM [v3.0]

Datasheet: online component datasheet for EEPROM

9.10 Component type: fracdiv [v0.0]

9.10.1 Instance fracdiv_1

Description: (custom component)
Instance type: fracdiv [v0.0]
Datasheet: (not available)

9.11 Component type: I2C [v3.50]

9.11.1 Instance IntI2C

Description: Standard I2C communication interface
Instance type: I2C [v3.50]
Datasheet: online component datasheet for I2C

Table 23. Component Parameters for IntI2C

Parameter Name	Value	Description
Address_Decode	Hardware	Determines either hardware or software address match logic.
BusSpeed_kHz	400	I2C Data Rate in kbps. Standard settings are 50, 100, 400 or 1000. The value must be between 1 and 1000.
EnableWakeup	false	Determines if I2C is selected as wakeup source.
ExternalBuffer	false	Exposes scl and sda in and out terminals outside the component.
Externi2cIntrHandler	false	Allows I2C interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
ExternTmoutIntrHandler	false	Allows I2C timeout interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
Hex	false	Indicates that address has been input in hexadecimal format.
I2C_Mode	Master	Determines I2C mode (Slave/Master/Multi-Master/Multi-Master-Slave).
I2cBusPort	Any	Determines which I2C pins have been selected. Select I2C0/I2C1 and connect to corresponding pins to be able use I2C as wakeup source.
Implementation	FixedFunction	Determines either I2C implementation Fixed Function or UDB.
NotSlaveClockMinusTolerance	25	Internal component clock negative tolerance value in Master, Multi-Master or Multi-Master-Slave mode.

Parameter Name	Value	Description
NotSlaveClockPlusTolerance	5	Internal component clock positive tolerance value in Master, Multi-Master or Multi-Master-Slave mode.
PrescalerEnabled	false	Enables prescaler (7-bit counter) to expand timeout timer range.
PrescalerPeriod	3	Prescaler period of timeout timer.
SclTimeoutEnabled	false	Enables low time monitoring of scl line.
SdaTimeoutEnabled	false	Enables low time monitoring of sda line.
Slave_Address	8	7-bits I2C slave address.
SlaveClockMinusTolerance	5	Internal component clock negative tolerance value in Slave mode.
SlaveClockPlusTolerance	50	Internal component clock positive tolerance value in Slave mode.
TimeoutImplementation	UDB	Determines either timeout timer feature implementation as UDB or Fixed Function. The Fixed Function implementation only available for PSoC5LP.
TimeOutms	25	Determines maximum time allowed for scl or sda to be low state (in mS). The timeout timer generates interrupt after timeout expires.
TimeoutPeriodff	39999	Period of timeout timer (Fixed Function).
TimeoutPeriodUdb	39999	Period of timeout timer (UDB).
UdbInternalClock	false	Determines either internal or external clock source for I2C UDB.
UdbSlaveFixedPlacementEnable	false	Enables fixed placement for I2C UDB. Only available in slave mode.

9.12 Component type: IDAC8 [v2.0]

9.12.1 Instance IDAC8_1

Description: 8-Bit current DAC
Instance type: IDAC8 [v2.0]
Datasheet: online component datasheet for IDAC8

Table 24. Component Parameters for IDAC8_1

Parameter Name	Value	Description
Current	0	To set the current value
Data_Source	CPU or DMA (Data Bus)	Selects how the data will be written to the iDAC.
Hardware_Enable	false	UDB control for current flow
IDAC_Range	0 - 2040uA (8uA/bit)	Selects full scale range of the iDAC.

Parameter Name	Value	Description
IDAC_Speed	Low Speed	Selects the iDAC settling speed. The Slow Speed selection consumes less power.
Initial_Value	0	Configures the initial iDAC output value. The initial current = value*(FullRange/255). This value is invalid if DAC Bus is used.
Polarity	Current Source	Selects the Sink or Source mode for the iDAC.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. An external data strobe signal is required for External. For Register Write the the data is strobed into the DAC on each CPU or DMA write.

9.13 Component type: OpAmp [v1.90]

9.13.1 Instance DummyLoadDriver

Description: Opamp
Instance type: OpAmp [v1.90]
Datasheet: online component datasheet for OpAmp

Table 25. Component Parameters for DummyLoadDriver

Parameter Name	Value	Description
Mode	OpAmp	Selects between uncommitted op-amp or follower mode.
Power	High Power	Selects the device power level.

9.13.2 Instance IOVoltBuffer

Description: Opamp
Instance type: OpAmp [v1.90]
Datasheet: online component datasheet for OpAmp

Table 26. Component Parameters for IOVoltBuffer

Parameter Name	Value	Description
Mode	Follower	Selects between uncommitted op-amp or follower mode.
Power	High Power	Selects the device power level.

9.14 Component type: PGA [v2.0]

9.14.1 Instance PGA_1

Description: Programmable Gain Amplifier
Instance type: PGA [v2.0]
Datasheet: online component datasheet for PGA

Table 27. Component Parameters for PGA_1

Parameter Name	Value	Description
Gain	32	Selects supported gain value.
Power	Low Power	Selects the device power.
Vref_Input	Internal Vss	Enables direct connection from the Analog ground (Agnd) to the inverting input.

9.15 Component type: PWM [v3.30]

9.15.1 Instance PWM_SYNC

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.30]
Datasheet: online component datasheet for PWM

Table 28. Component Parameters for PWM_SYNC

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Greater	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	255	Compares Output 1 to value
CompareValue2	128	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event

Parameter Name	Value	Description
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	255	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	8	Defines the bit width of the PWM (8 or 16 bits)
RunMode	One Shot with Multi Trigger	Defines the run mode options to be either continuous or one shot
TriggerMode	Falling Edge	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

9.16 Component type: SPI_Master [v2.50]

9.16.1 Instance DispSPI

Description: Serial Peripheral Interface Master
Instance type: SPI_Master [v2.50]
Datasheet: online component datasheet for SPI_Master

Table 29. Component Parameters for DispSPI

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	true	Allow use of the internal clock and desired bit rate or an external clock source
DesiredBitRate	8000000	Desired Bit Rate in bps
HighSpeedMode	false	Enables using of the High Speed Mode
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Full
InterruptOnRXNotEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Overrun
InterruptOnSPIDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnSPIIdle	false	Set Initial Interrupt Source to Enable Interrupt on SPI Idle
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty

Parameter Name	Value	Description
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Not Full
Mode	CPHA = 1, CPOL = 1	SPI mode defines the Clock Phase and Clock Polarity desired
NumberOfDataBits	8	Set the Number of Data bits 3-16
RxBufferSize	4	Defines the amount of RAM Set asside for the RX Buffer
ShiftDir	MSB First	Set the Shift Out Direction
TxBufferSize	4	Defines the amount of RAM Set asside for the TX Buffer
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

9.17 Component type: UART [v2.50]

9.17.1 Instance TargetUART_1

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 30. Component Parameters for TargetUART_1

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	57600	Sets the target baud rate.
BreakBitsRX	14	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	14	Specifies the break signal length for the TX channel.
BreakDetect	true	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	true	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	true	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.
InternalClock	false	Enables the internal clock. This parameter removes the clock input pin.

Parameter Name	Value	Description
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	true	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	true	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	256	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	256	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.

9.18 Component type: USBFS [v2.80]

9.18.1 Instance USBFS_1

Description: USB 2.0 Full Speed Device Framework
Instance type: USBFS [v2.80]
Datasheet: online component datasheet for USBFS

Table 31. Component Parameters for USBFS_1

Parameter Name	Value	Description
EnableCDCApi	false	Enables additional high level API's that allow the CDC device to be used similar to a UART device.
EnableMidiApi	false	Enables additional high level MIDI API's.
endpointMA	MA_Static	Endpoint memory allocation
endpointMM	EP_Manual	Endpoint memory management
epDMAautoOptimization	false	This parameter enables resource optimization for DMA with Automatic Memory Management mode. Set this parameter value to true only when a single IN endpoint is present in the device. Enabling this parameter in a multi IN endpoint device configuration causes undesired effects.
extern_cls	true	This parameter allows for user or other component to implement his own handler for Class requests. USBFS_-DispatchClassRqst() function should be implemented if this parameter enabled.
extern_vbus	false	This parameter enables external VBUSDET input.
extern_vnd	false	This parameter allows for user or other component to implement his own handler for Vendor specific requests. USBFS_HandleVendorRqst() function should be implemented if this parameter enabled.
extJackCount	0	Max number of External MIDI IN Jack or OUT Jack descriptors
max_interfaces_num	6	Defines maximum interfaces number
Mode	false	Specifies whether the implementation will create API for interfacing to UART component(s) for a corresponding set of external MIDI connections.

Parameter Name	Value	Description
mon_vbus	false	The mon_vbus parameter adds a single VBUS monitor pin to the design. This pin must be connected to VBUS and must be assigned in the pin editor.
out_sof	false	The out_sof parameter enables Start-of-Frame output.
Pid	CDB3	Product ID
Vid	16D0	Vendor ID

9.19 Component type: VDAC8 [v1.90]

9.19.1 Instance IOVoltGen

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 32. Component Parameters for IOVoltGen

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.
Initial_Value	255	Configures the initial vDAC output voltage. The output uses the following relation: Initial output voltage = value*(FullRange/255). This calculated output voltage value is invalid if DAC Bus is used.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 4.080V (16mV/bit)	Specifies the full voltage scale range of the vDAC
VDAC_Speed	Low Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	4080	This parameter sets the voltage value.

9.19.2 Instance SenseRefGen

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 33. Component Parameters for SenseRefGen

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.

Parameter Name	Value	Description
Initial_Value	156	Configures the initial vDAC output voltage. The output uses the following relation: Initial output voltage = value*(FullRange/255). This calculated output voltage value is invalid if DAC Bus is used.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 4.080V (16mV/bit)	Specifies the full voltage scale range of the vDAC
VDAC_Speed	Low Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	2496	This parameter sets the voltage value.

9.19.3 Instance SIORefGen

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 34. Component Parameters for SIORefGen

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.
Initial_Value	112	Configures the initial vDAC output voltage. The output uses the following relation: Initial output voltage = value*(FullRange/255). This calculated output voltage value is invalid if DAC Bus is used.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 4.080V (16mV/bit)	Specifies the full voltage scale range of the vDAC
VDAC_Speed	Low Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	1792	This parameter sets the voltage value.

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5 register map is covered in the PSoC 5 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5 Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine