Machine Problem 2- Report

MSI without BusUpgrade.

Experiment 1: Cache size

Cache associativity 8

Block size 64B

MSI

Cache Size	read misses	memory
512 KB	91395	118528
1 MB	67922	84119
2 MB	53071	65716
4 MB	46134	57067

MESI

Cache Size	read misses	memory
512 KB	91395	75698
1 MB	67922	44633
2 MB	53071	29265
4 MB	46134	21353

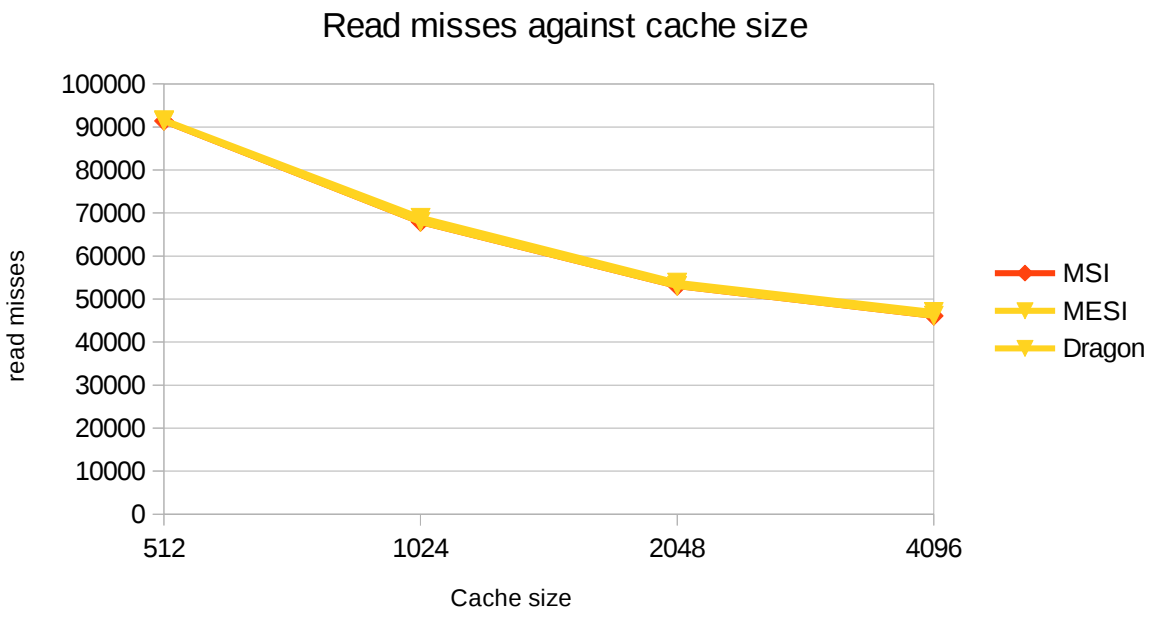
Dragon

Cache Size	read misses	memory
512 KB	91560	110713
1 MB	68912	78396
2 MB	53797	60134
4 MB	46993	52418

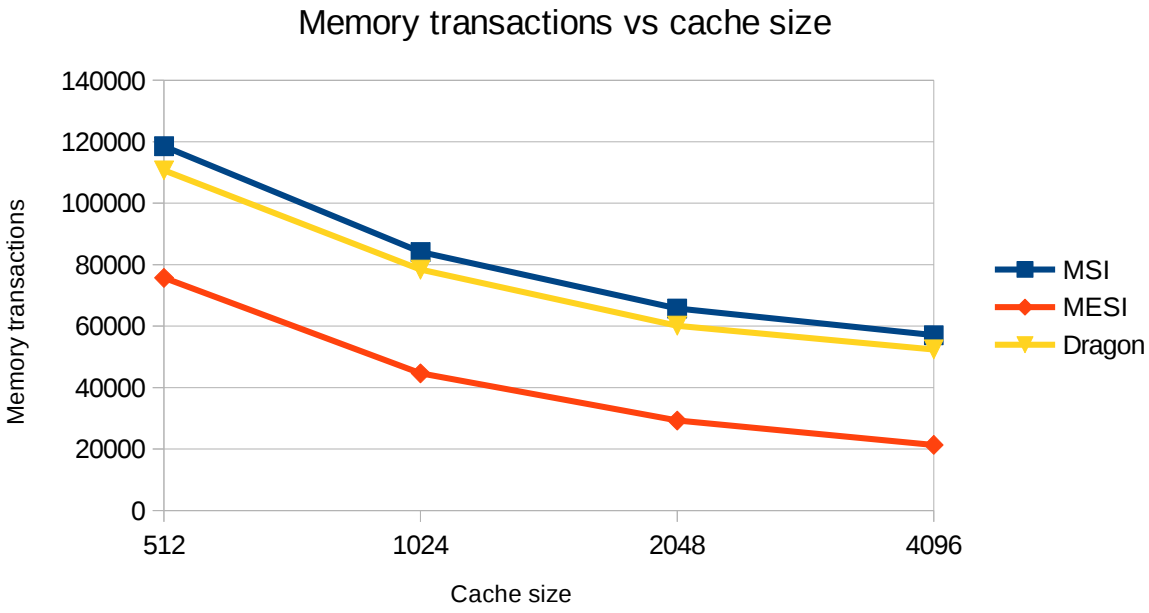
no. of sets*associativity*block size = cache size

Therefor some configurations such as cache size = 256 B, block size = 64B, associativity = 8 is not possible.

Compare read miss against cache size among the protocols



Compare memory transactions against cache size among the protocols



Observations:
As the cache size increases the read misses decreases since there is more space available now more cache blocks can be stores. This reduces read misses. The behavious is same for all protocols.
The read misses is same for MSI and MESI and very close for dragon protocol.
As the cache size increases the memory transactions decreases. With higher cache size more data is available in cache itself thus reducing memory transactions. This behaviour is also similar in all three protocols.
Also MESI has the lease number of memory transactions, followed by Dragon and then MSI.

Experiment 2: Varying cache associativity

Cache Size 1MB
Block size 64B

MSI

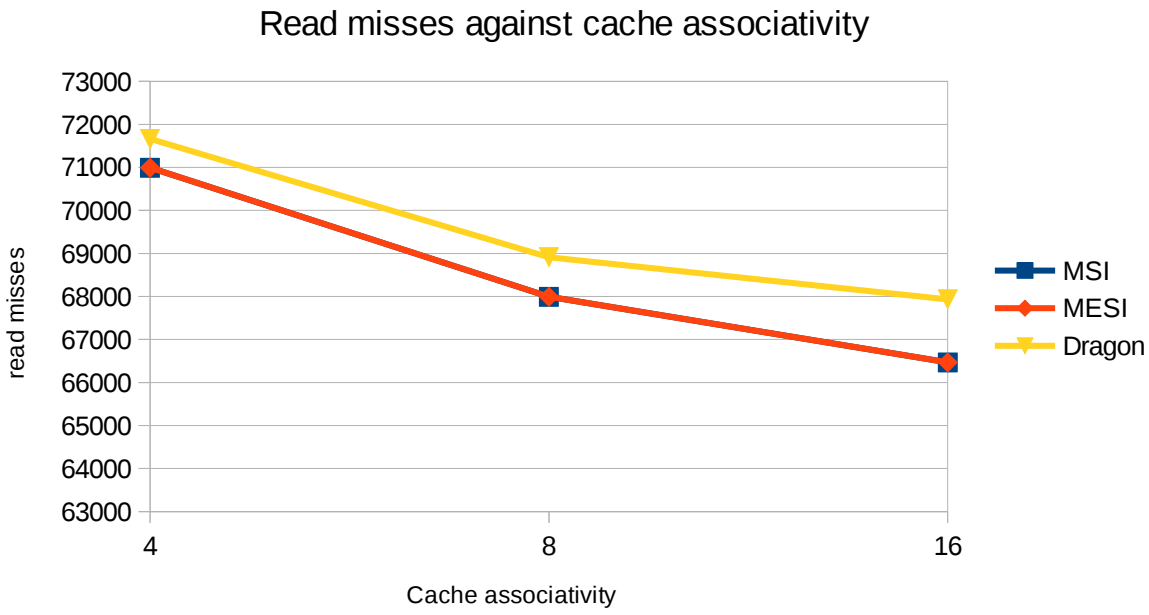
Cache associativity	read misses	memory
4	70991	87770
8	67992	84119
16	66467	82258

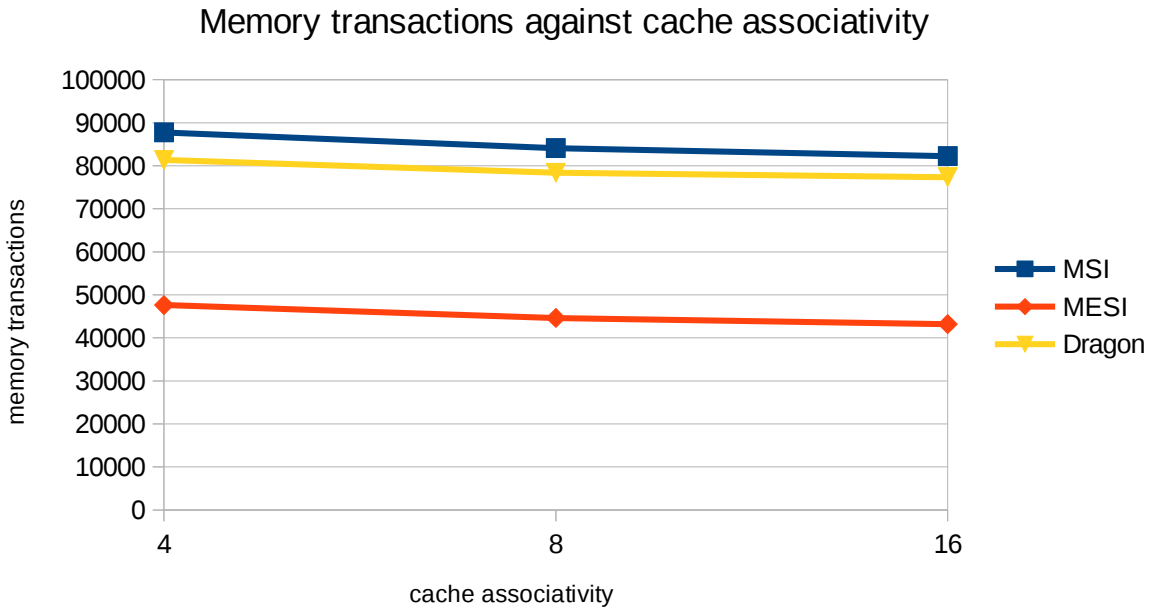
MESI

Cache associativity	read misses	memory
4	70991	47642
8	67992	44633
16	66467	43194

Dragon

Cache associativity	read misses	memory
4	71660	81352
8	68912	78396
16	67935	77354





Observations: Cache associativity has a great impact on read misses. Read misses decreases as cache associativity increases for all protocols. The read misses is same for the same set of data for MSI and MESI. Dragon protocol always has lesser number of read misses. The reduction in read misses can be explained by conflict misses. As the cache associativity increases the number of possible ways to put a block in cache increases, thus reducing conflict misses.

Cache associativity does not seem to have an effect on memory transactions. The memory transactions is slightly decreasing as the cache associativity is increases.

Experiment 3: Varying cache block size
Cache size 1MB
Cache associativity 8
MSI

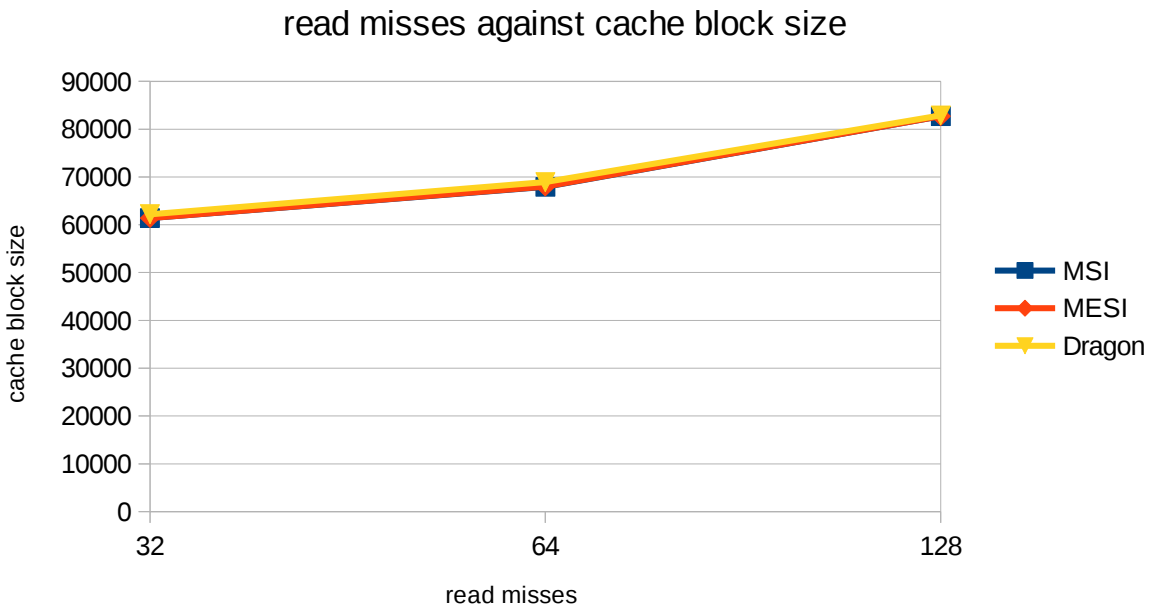
Cache block size in bytes	read misses	memory
32 B	61400	77327
64 B	67922	84119
128 B	82724	105170

MESI

Cache block size in bytes	read misses	memory
32 B	61400	37921
64 B	67922	44633
128 B	82724	63977

DRAGON

Cache block size in bytes	read misses	memory
32 B	62194	71323
64 B	68912	78396
128 B	82878	97778



Observations: Read misses increases as the cache block size increases.