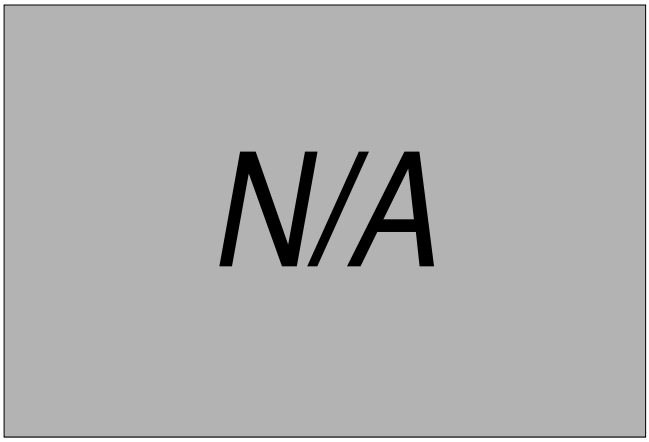
AND Displays



AND-TFT-8PA

480 x 468 Pixels
LCD Color Monitor

The AND-TFT-8PA is a compact full color TFT LCD module, whose driving board is capable of converting composite video signals to the proper interface of LCD panel and is suitable for security, car TV, portable DVD, GPS, multimedia applications and other AV system applications.

This device consists of a TFT-LCD module that has 480 x 468 pixels on a 8 inch diagonal screen which is normally white in the display mode.

Features

- Compatible with NTSC and PAL system
- Pixel in stripe configuration
- 8 inch diagonal screen
- High brightness
- Slim and compact
- Imager Reversion: Up/Down and Left/Right
- Anti-glare surface treatment
- Support multi-display mode (If you use this mode, you must use a specially made timing controller.)
- **RoHS compliant**

Mechanical Characteristics

Item	Specification	Unit
Screen Size	8 diagonal	inch
Outline Dimensions	172.4(W) x 132.0 (H) x 6.6 (D)(typ.)	mm
Active Area	161.28 (W) x 117.94 (H)	mm
Surface Treatment	Anti-glare	–
Weight	232 ± 15	g
Pixel Configuration	stripe	–
Pixel Pitch	0.112 (W) x 0.252 (H)	mm
Display Format	480 x 468	dot
Display Mode	Normally white	–

Absolute Maximum Rating (GND = 0V, Ta = 25°C)

Item		Symbol	Remarks	Absolute Maximum Rating		Unit
				Min.	Max.	
Supply Voltage for Source Driver		V_{DD2}		+9.0	+15	V
		V_{DD1}		-0.3	+7.0	
Supply Voltage for Gate Driver		V_{CC}		-0.3	+6.0	V
		V_{GH}- V_{EE}		-0.3	+40.0	
	H Level	V_{GH}		-0.3	+25.0	
	L Level	V_{EE}		-16	+0.3	
Analog Signal Input Level		V_{R+}, V_{G+}, V_{B+}	Note 1	+4	+13	V
		V_{R-}, V_{G-}, V_{B-}		0	5.5	V
Storage Temperature		–		-30	+80	°C
Operation Temperature		–	Note 2	-20	+70	°C

Note 1: V_R, V_G, V_B means analog input voltage.

Note 2: Optical characteristics are measured under Ta=+25ºC.

Power Consumption (Ta = 25°C)

Item		Symbol	Conditions	Specifications		Units	Remarks
				Typ.	Max.		
Supply Current for Gate Driver	Hi level	I_{GH}	V_{GH} = +20V	0.3814	0.4768	mA	
	Low level	I_{EE}	V_{EE} = -8V	0.4112	0.5141	mA	
Supply Current for Source Driver (Digital)		I_{DD1}	V_{DD1} = +3.3V	2.0245	2.5306	mA	
Supply Current for Source Driver (Analog)		I_{DD2}	V_{DD2} = +13V	5	6.24	mA	
Supply Current for Gate Driver (Digital)		I_{CC}	V_{CC} = +3.3V	0.1	0.2	mA	
LCD Panel Power Consumption (Note 1)		–	–	78.75	98.60	mW	Note 1
Backlight lamp Power Consumption (Note 2)		–	–	3.6	–	W	Note 2

Note 1: The power consumption for backlight is not included.
Note 2: Backlight lamp power consumption is calculated by I_L x V_L.

Recommended Driving Conditions for TFT-LCD Panel

Item		Symbol	Specifications			Unit	Remarks
			Min.	Typ.	Max.		
Supply Voltage for Source Driver	Analog	V_{DD2}	+12	+13	+14	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6		
Supply Voltage for Gate Driver	H Level	V_{GH}	+18	+20	+22	V	
	L Level	V_{EE}	-9	-8	-7		
	Logic	V_{CC}	+3.0	+3.3	+3.6		
Analog Signal Input Level	V_{R+}, V_{G+}, V_{B+} (Analog Video +)	$V_{+, AC}$	–	+4.0	–	O_{P-P}	
		$V_{+, HIGH}$	11.6	11.9	12.2	V	
	V_{R-}, V_{G-}, V_{B-} (Analog Video -)	$V_{-, AC}$	–	+4.0	–	O_{P-P}	
		$V_{-, LOW}$	1.6	1.9	2.2	V	
Digital Input Voltage	H Level	V_{IH}	0.7	–	V_{DD1}	V	
	L Level	V_{IL}	-0.3	–	0.3		
Digital Output Voltage	H Level	V_{OH}	0.7	–	V_{DD1}	V	
	L Level	V_{OL}	-0.3	–	0.3		
V_{COM}		$V_{COM\ DC}$	4.9	5.2	5.5	V	DC Component of V_{COM} Note 1

Note 1: Purdy strongly suggests that the $V_{COM\ DC}$ level shall be adjustable, and the adjustable level range is 5.2V ± 0.3V, every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

Backlight Driving (JST BHSR-02VS-1, Pin No.: 2)

Pin No.	Symbol	Description	Remarks
1	VL1	Input terminal (Hi voltage side)	Wire color: pink
2	VL2	Input terminal (Low voltage side)	Wire color: white Note 1
Note 1: Low voltage side of backllight inverter connects with Ground of inverter circuits.			

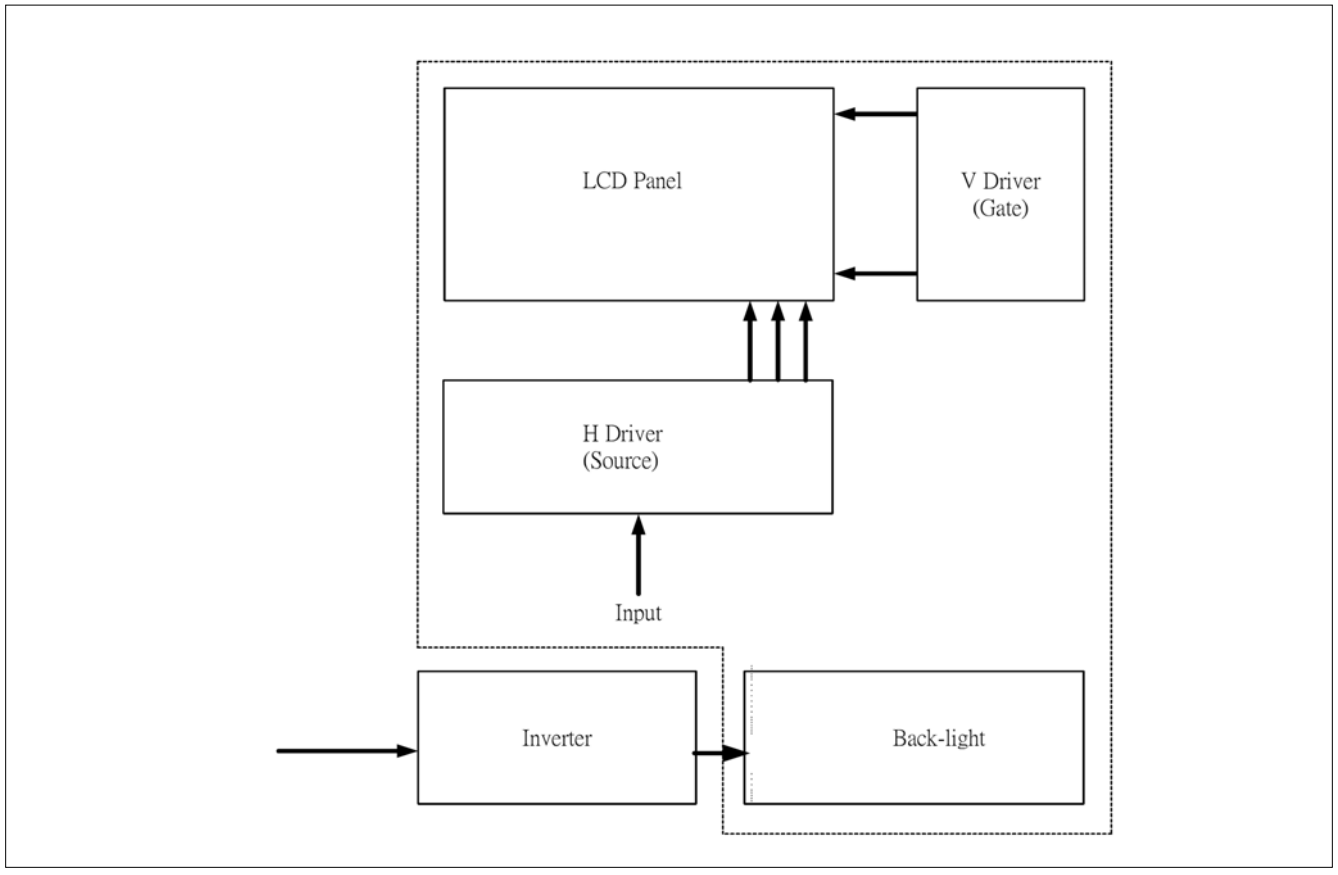
Optical Specifications (Ta = 25°C)

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Viewing Angle	Horizontal	θ = 21, θ = 22	CR ≥ 10	45	50	–	deg
	Vertical	θ = 12		10	15	–	
		θ = 11		30	35	–	
Contrast Ratio (Note 1)		CR	At optimized Viewing Angle	200	350	–	
Response Time	Rise	Tr	θ = 0	–	15	30	ms
	Fall	Tf		–	25	50	
Brightness (Note 2)		–	Center point	300	350	–	cd/m^2
Uniformity		U	–	70	75	–	%
White Chromaticity (Note 2)		x	θ = 0	0.270	0.300	0.330	–
		y		0.300	0.330	0.360	
Lamp Life Time +25 °C		–	-	–	30,000	–	hrs

Note 1: CR = Luminance when Testing point is White
Luminance when Testing point is Black
Contrast Ratio is measured in optimum common electrode voltage

Note 2: Topcon BM-7(fast) luminance meter 2° field of view is used in the testing (after 20~30 minutes operation). Lamp Current : 6mA; Inverter model: TDK-347

Block Diagram



Recommended Driving Conditions for Backlight Ta = 25°C

Item	Symbol	Remark	Specifications			Unit
			Min.	Typ.	Max.	
Lamp Voltage	V_L		540	600	660	Vrms
Lamp Current	I_L	Note1	4	6	8	mA
Lamp Frequency	P_L	Note 2	30	60	80	KHz
Starting Voltage (25 °C) (Reference Value)	V_S	Note 3	–	–	920	Vrms
Starting Voltage (0 °C) (Reference Value)	V_S	Note 3	–	–	1100	Vrms

Note 1: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L. Note 2: The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.' Note 3: The "Max of kick of voltage" means the minimum voltage of inverter to turn on the CCFL and it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

Interface Pin Assignment Connector:

Pin #.	Symbol	I/O	Function	Remark
1	STH2	I/O	Start pulse for source driver	Note 2
2	OEH	I	Output enable for source driver	
3	POL	I	Polarity control for column inversion	
4	MOD	I	Simultaneous/sequential mode select	
5	R/L	I	Left/Right Control for source driver	Note 2
6	V_{DD1}	–	Supply voltage of logic circuit for source driver	Note 7
7	CPH3	I	Sample and shift clock for source driver	
8	CPH2	I	Sample and shift clock for source driver	
9	CPH1	I	Sample and shift clock for source driver	
10	VSS1	–	Ground of logic circuit for source driver	Note 6
11	V_{DD2}	–	Supply voltage of analog circuit for source driver	
12	VB-	I	Video input B for negative polarity	
13	VG-	I	Video input G for negative polarity	
14	VR-	I	Video input R for negative polarity	
15	V_{SS2}	–	Ground for analog circuit for source driver	
16	VB+	I	Video input B for positive polarity	
17	VG+	I	Video input G for positive polarity	
18	VR+	I	Video input R for positive polarity	
19	V_{SS2}	–	Ground for analog circuit for source driver	
20	STH1	I/O	Start pulse for source driver	Note 2
21	VCOM	I	Voltage for common electrode	
22	OE1	I	Output enable for gate driver	
23	OE2	I	Output enable for gate driver	
24	OE3	I	Output enable for gate driver	
25	U/D	I	Up/Down Control for gate drive	Note 1
26	CKV	I	Shift clock for gate driver	
27	STVD	I/O	Vertical start pulse	Note 1
28	STVU	I/O	Vertical start pulse	Note 1
29	VCC	–	Power supply for gate driver circuit	Note 3
30	V_{EE}	–	Negative power gate driver	Note 4
31	V_{GH}	–	Positive power gate driver	Note 5
32	GND	–	Ground for gate driver	

Note 1

U/D	STVD	STVU	Scanning Direction
Vcc	Input	Output	Up to Down
GND	Output	Input	Down to Up

Note 2

R/L	STH1	STH2	Scanning Direction
Vcc	Input	Output	Left to Right
GND	Output	Input	Right to Left

Note 3: V_{CC} Typ. = +3.3V

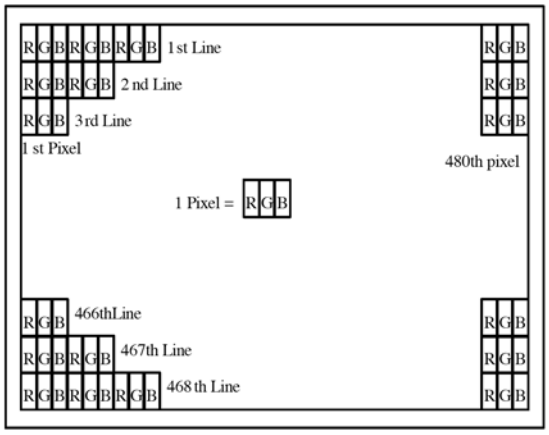
Note 4: V_{EE} Typ. = -8V

Note 5: V_{GH} Typ. = +20V

Note 6: V_{DD2} Typ. = +13V

Note 7: V_{DD1} Typ. = +3.3V

Pixel Arrangement and input connector pin no.



Timing Characteristics of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remarks
Rising Time	t_r	–	–	10	ns	
Falling Time	t_f	–	–	10	ns	
High and low level pulse width	t_{CPH}	9.2	9.6	10.0	MHz	CPH1 ~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1 ~ CPH3
STH setup time	t_{SUH}	20	–	–	ns	STH1, STH2
STH hold time	t_{HDH}	20	–	–	ns	STH1, STH2
STH pulse width	t_{STH}	–	1	–	t_{CPH}	STH1, STH2
STH period	t_H	61.5	63.5	65.5	µs	STH1, STH2
OEH pulse width	t_{OEH}	–	3.47	–	µs	OEH
Samplle and hold disable time	t_{DIS1}	–	7.43	–	µs	
OEV pulse width	t_{OEV}	–	52.3	–	µs	OEV
CKV pulse width	t_{CKV}	–	15.8	–	µs	CKV
Horizontal display start	t_{SH}	–	0	–	$t_{CPH}/3$	
Horizontal display timing range	t_{DH}	–	480	–	t_{CPH}	
STV pusle width	t_{STV}	–	1.5	–	t_H	STVD, STVU
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}	–	3	–	t_H	
Vertical display timing range	t_{DV}	–	234	–	t_H	
Distance from OEH to STVD (odd field)	t_{DIS2}	–	33.9	–	µs	
Distance from OEH to STVD (evenfield)	t_{DIS3}	–	2.2	–	µs	
OE (1, 2, 3) pulse width 1	Poev1	–	4.2	–	µs	
OE (1, 2, 3) pulse width 2	Poev2	–	81.6	–	µs	
Distance from CKV to OE1	T_{fa1}	–	14.9	–	µs	
Distance from OE1 to another OE2	T_{ra2}	–	18.1	–	µs	
DIstance from OE2 to another OE3	T_{ra3}	–	18.1	–	µs	
Distance2 from POL to STVD(u)	T_{pol}	–	2	–	t_H	

Dimensional Outline

General mechanical tolerance = 0.5mm