AND Displays

AND-TFT-7TN

800 x 480 Pixels
LCD Color Monitor

The AND-TFT-TN is a compact full color TFT LCD module, whose driving board is capable of converting composite video signals to the proper interface of LCD panel and is suitable for car TV, portable DVD and GPS, multimedia applications and other AV systems.

This device consists of amorphous silicon TFT liquid crystal display with B/L unit. The display has 800 x 480 pixels on a 7.0 inch diagonal screen. X and Y drivers, LSI controller, and a built-in CCFL backlight inverter (with optional board.)

Features

- Pixel in stripe configuration
- 7.0 inch (16 cm) diagonal screen
- High brightness CCFL backlight (400 Nits)
- Slim and compact
- Amorphous silicon TFT-LCD with B/L unit
- Imager Reversion: Up/Down and Left/Right
- Support multi display mode
- High performance, low power consumption
- **RoHS compliant**

Product specifications contained herein may be changed without prior notice. It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

Mechanical Characteristics

Item	Specification
Screen Size	7.0 inch (16.9 cm) diagonal
Driver Element	a-Si TFT active matrix
Resolution	800 x 3 (RGB) x 480
Display Mode	Normally white, Transmissive
Dot Pitch	0.0635 (W) x 0.1905 (H) mm
Active Area	152.4 (W) x 91.44 (H) mm
Module Size	165 (W) x 104 (H) x 5.5 (D) mm
Surface Treatment	Anti-Glare
Color Arrangement	RGB-stripe
Interface	Digital
Backlt Pwr Consumption	1.782 W (Typ.)
Panel Pwr Consumption	0.437 W (Typ.)
Weight	170 g (Typ.)

Absolute Maximum Rating NOTE: Do not exceed these ratings at any time.

Item	Symbol	Remark	Min.	Max.	Unit
Power Voltage	DV_{DD}		-0.5	5	V
	AV_{DD}		-0.5	13.5	V
	V_{GH}		-0.3	20.0	V
	V_{GL}		-13.0	0.3	V
	V_{GH} - V_{GL}		–	33.0	V
Input Signal Voltage AV_{DD} - 0.1 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ V6 ≥ V7, V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ V14 ≥ AV_{SS} +0.1	V1~V7		0.4 AV_{DD}	AV_{DD} + 0.3	V
Input Signal Voltage	V8~V14		-0.3	0.6 AV_{DD}	V
Operating Temperature	T_{OP}		-30	85	ºC
Storage Temperature	T_{ST}		-30	85	ºC
LED Reverse Voltage V_R conditions: Zener Diode 20 mA	V_R	Each LED	–	1.2	V
LED Forward Current	I_F	Each LED	–	25	mA

Optical Characteristics

Item	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Viewing Angle (CR ≥ 10)	θ_L	ϕ = 180º (9 o'clock)	60	70	–	deg
	θ_R	ϕ = 0º (3 o'clock)	60	70	–	deg
	θ_T	ϕ = 90º (12 o'clock)	40	50	–	deg
	θ_B	ϕ = 270º (6 o'clock)	60	70	–	deg
Contrast Ratio	CR	At optimized viewing angle	400	500	–	–
Response Time	T_{ON}	Normal $\theta = \phi = 0$	–	10	20	ms
	T_{OFF}		–	15	30	ms
Luminance Uniformity	Y_U		70	75	–	–
Luminance	L		360	450	–	cd/m^2
ColorChromaticity	Wx		0.26	0.31	0.36	–
	Wy		0.28	0.33	0.38	–

Test Conditions: DV_{DD} = 3.3V, I_L = 180 mA (Backlight current), the ambient temperature is 25 º C

Typical Operation Conditions (Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Voltage	DV_{DD}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	10.2	10.4	10.6	V	
	V_{GH}	15.3	16.0	16.7	V	
	V_{GL}	-7.7	-7.0	-6.3	V	
Input Signal Voltage	V_{COM}	–	4.1	–	V	(V1 + V14) /2 = 5.2V
	V1~V7	0.4 AV_{DD}	–	AV_{DD} -0.1	V	
	V8~V14	0.1	–	0.6 AV_{DD}	V	
Input Logic High Voltage	V_{IH}	0.7 DV_{DD}	–	DV_{DD}	V	Note 3
Input Logic Low Voltage	V_{IL}	0	–	0.3 DV_{DD}	V	

Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.

Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

Note 3: POL, STVD, OEV, CKV, STVU, EDGSL, U/D, STHL, REV, DCLK, STHR, LD, R/L.
R0~R5, G0~G5, B0~B5.

Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{GH}	–	0.2	0.5	mA	V_{GH} = 16.0V
	I_{GL}	–	0.2	1.0	mA	V_{GL} - -7.0V
	IDV_{DD}	–	5.0	10.0	mA	DV_{DD} = 3.3V
	IAV_{DD}	–	40.0	50.0	mA	AV_{DD} = 10.4 V

Pin Description: TFT LCD Panel Driving Section: P-TWO "AF 730L-A2G1T"

Pin #.	Symbol	I/O	Description
1	POL	I	Polarity selection
2	STVD	I/O	Vertical start pulse input when U/D = H (Note 1)
3	OEV	I	Output enable
4	CKV	I	Vertical clock
5	STVU	I/O	Vertical start pulse input when U/D = L (Note 1)
6	GND	P	Power Ground
7	EDGSL	I	Select rising edge or falling edge
8	DV_{DD}	P	Power Voltage for Digital Circuit
9	V9	I	Gamma Voltage Level 9
10	V_{GL}	P	Gate OFF Voltage
11	V2	I	Gamma Voltage Level 2
12	V_{GH}	P	Gate ON Voltage
13	V6	I	Gamma Voltage Level 6
14	U/D	I	Up/Down Selection (Note 1, 2)
15	V_{COM}	I	Common Voltage
16	GND	P	Power Ground
17	AV_{DD}	P	Power Voltage for Analog Circuit
18	V14	I	Gamma Voltage Level 14
19	V11	I	Gamma Voltage Level 11
20	V8	I	Gamma Voltage Level 8
21	V5	I	Gamma Voltage Level 5
22	V3	I	Gamma Voltage Level 3
23	GND	P	Power Ground
24	R5	I	Red Data (MSB)
25	R4	I	Red Data
26	R3	I	Red Data
27	R2	I	Red Data
28	R1	I	Red Data
29	R0	I	Red Data (LSB)
30	GND	P	Power Ground

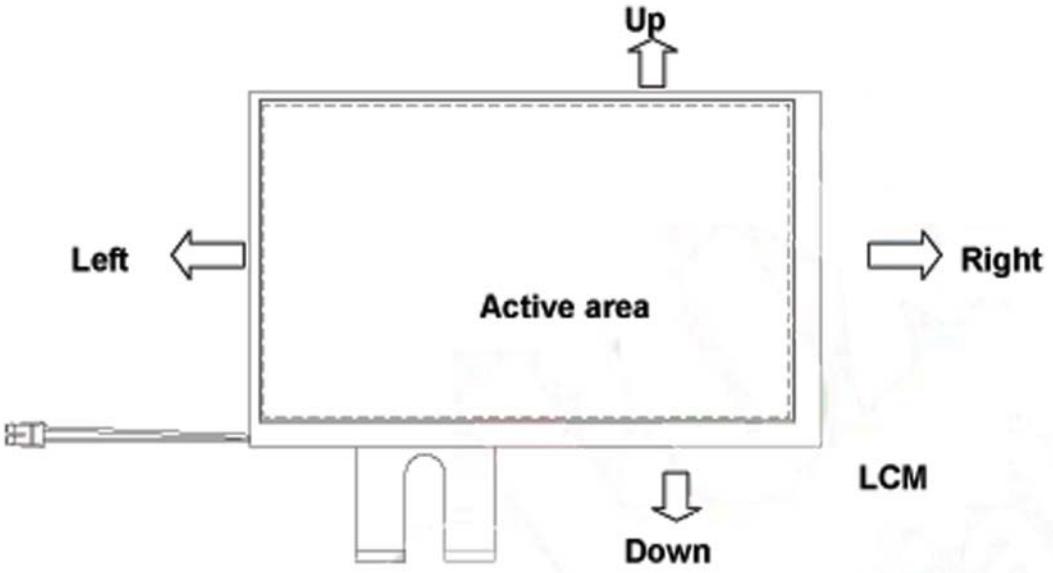
Pin #.	Symbol	I/O	Description
31	GND	P	Power Ground
32	G5	I	Green Data (MSB)
33	G4	I	Green Data
34	G3	I	Green Data
35	G2	I	Green Data
36	G1	I	Green Data
37	G0	I	Green Data (LSB)
38	STHL	I/O	Horizontal Start Pulse Input when R/L = L (Note 1)
39	REV	I	Control signal are inverted or not (Note 3)
40	GND	I	Power Ground
41	DCLK	I	Sample Clock
42	DV_{DD}	P	Power Voltage for Digital Circuit
43	STHR	I/O	Horizontal Start Pulse Input when R/L/ = H (Note 1)
44	LD	I	Latches the polarity of outputs and switches the new data to outputs
45	B5	I	Blue Data (MSB)
46	B4	I	Blue Data
47	B3	I	Blue Data
48	B2	I	Blue Data
49	B1	I	Blue Data
50	B0	I	Blue Data (LSB)
51	R/L	I	Right/Left Selection (Note 1, 2)
52	V1	I	Gamma Voltage Level 1
53	V4	I	Gamma Voltage Level 4
54	V7	I	Gamma Voltage Level 7
55	V10	I	Gamma Voltage Level 10
56	V12	I	Gamma Voltage Level 12
57	V13	I	Gamma Voltage Level 13
58	AV_{DD}	P	Power Voltage for Analog Circuit
59	GND	P	Power Ground
60	V_{COM}	I	Common Voltage

I: Input, O: output, P: Power

Note 1: Selection of scanning mode

Setting of Sacn control input		In/Out State for Start Pulse				Scanning Direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	DV_{DD}	O	I	I	O	Up to down, left to right
DV_{DD}	GND	I	O	O	I	Down to up, right to left
GND	GND	O	I	O	I	up to down, right to left
DV_{DD}	DV_{DD}	I	O	I	O	Down to up, left to right

Note 2: Definition of scanning direction. Refer tot he figure as below



Note 3: When REV = “L”, it’s under normal operation. When REV = “H”, these data will be inverted.

Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED Backlight	V_L	9.3	9.9	10.5	V	Note 1
Current for LED Backlight	I_L	170	180	200	mA	
LED Life Time	–	20,000	–	–	Hr	Note 2

Note 1: The Voltage for LED Backlight is defined at Ta = 25° C and I_L = 180 mA.

Note 2: The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at Ta = 25ºC and I_L - 180 mA. The LED lifetime could be decreased if operating I_L is larger than 180 mA.

Timing Conditions

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
DCLK frequency	Fdclk	–	40	45	MHz
DCLK cycle	Tcph	22	25	–	ns
DCLK pulse width	Tcw	8	–	–	ns
Data set-up time	Tsu	4	–	–	ns
Data hold time	Thd	2	–	–	ns
Time that the last data to LD	Tld	1	–	–	Tcph
Pulse width of LD	Twld	2	–	–	Tcph
Time that LD to STHL/R	Tlds	5	–	–	Tcph
POL set-up time	Tpsu	6	–	–	ns
POL hold time	Tphd	6	–	–	ns
CKV frequency	Fvclk	–	–	200	KHz
CKV rise time	Trck	–	–	100	ns
CKV falling time	Tfck	–	–	100	ns
CKV pulse time	PWCLK	500	–	–	ns
Horizontal display timing range	Tdh	–	800	–	Tcph
Horizontal timing range	Th	–	1056	–	Tcph
STVU/D setup time	Tsuv	200	–	–	ns
STVU/D hold time	Thdv	300	–	–	ns
STVU/D delay time	Tdt	–	–	500	ns
Driver output delay time	Tdo	–	–	900	ns
Output rise time	Ttih	–	500	1000	ns
Output falling time	Tthl	–	400	800	ns
OEV pulse width	Twcl	1	–	–	us
OEV to Driver output delay time	Toe	–	–	900	ns
Horizontal lines per field	Tv	512	525	610	Tdh
Vertical display timing range	Tvd	–	480	–	Tdh

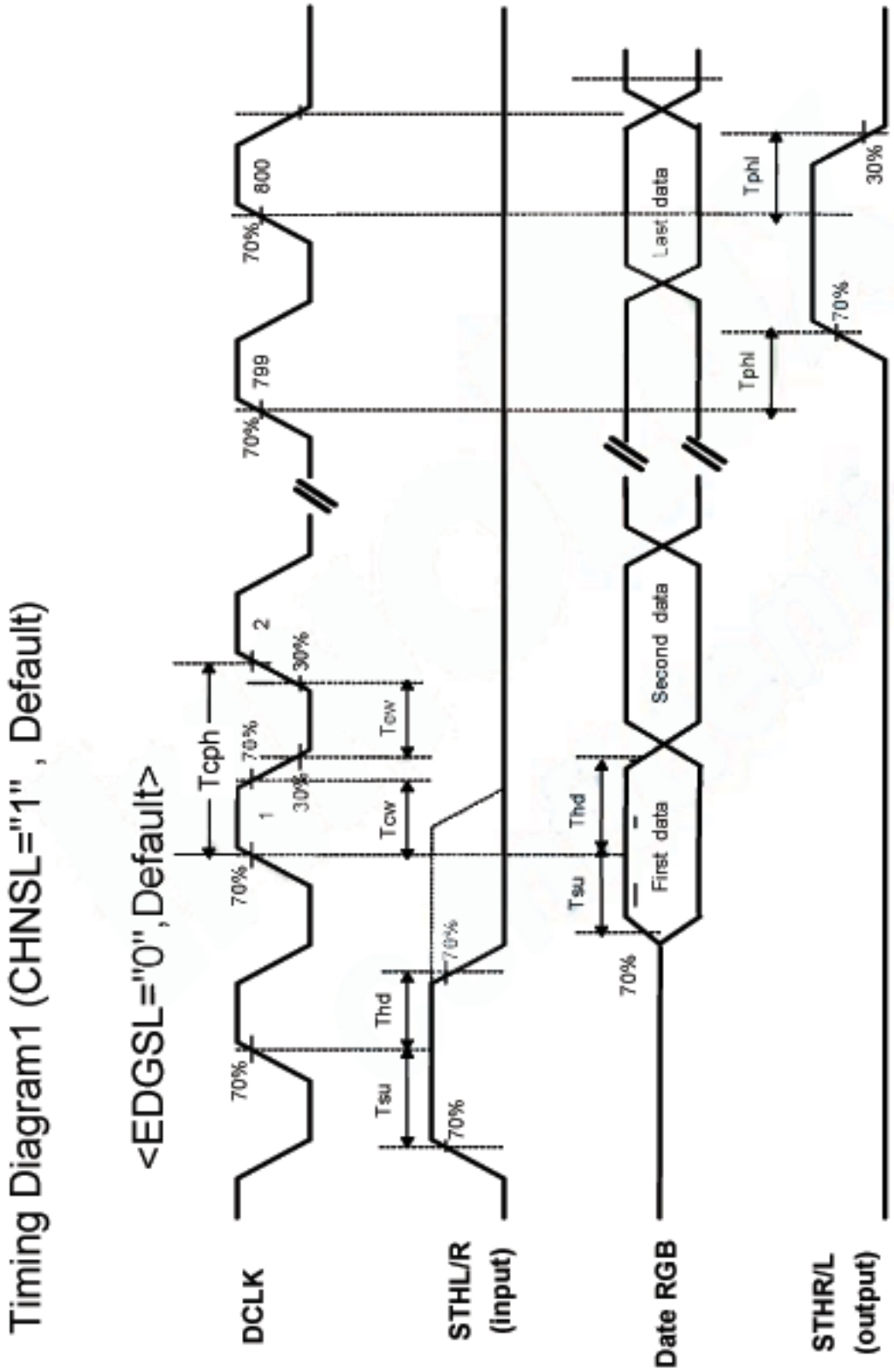


Fig.3-1 operation model 1

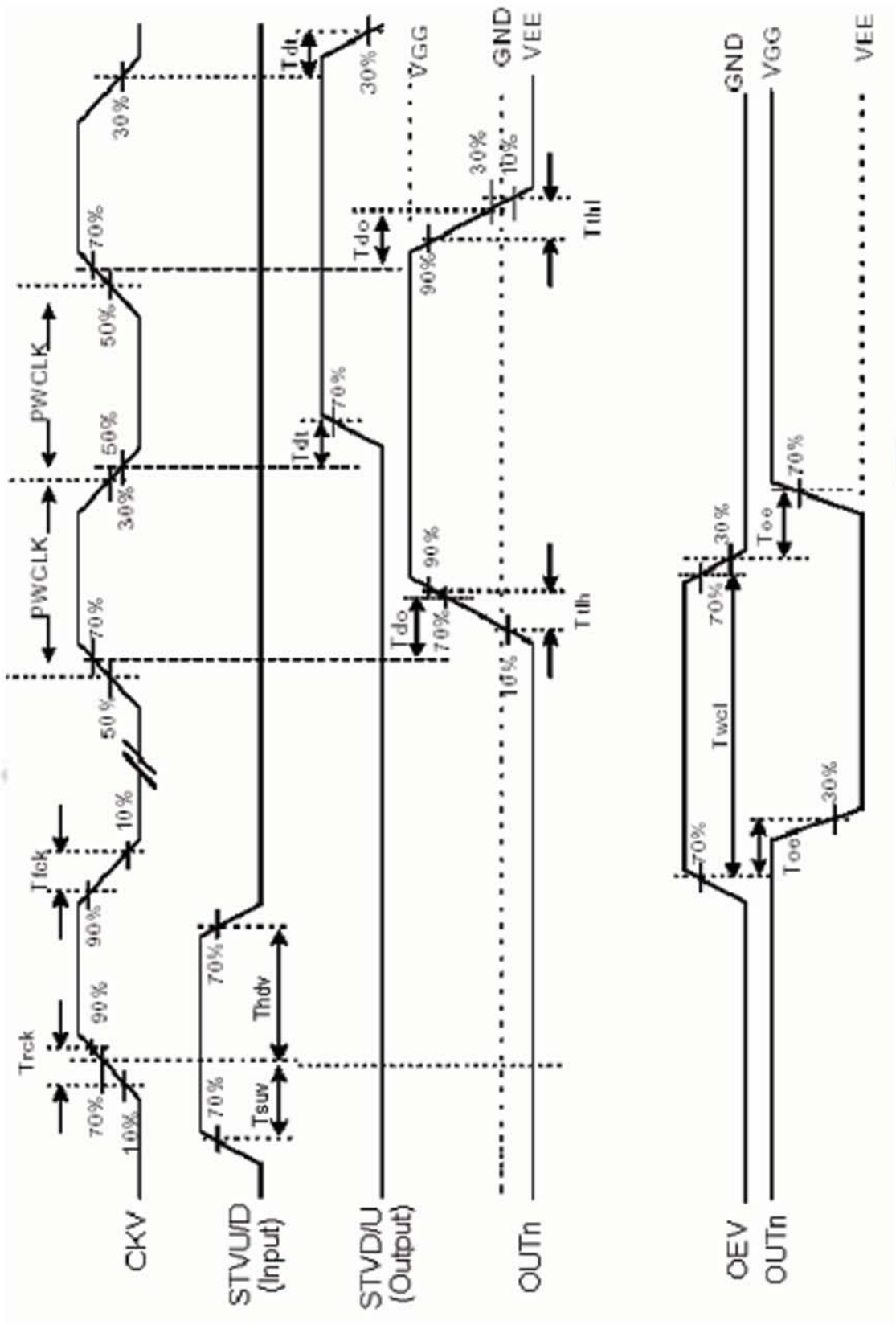


Fig.3-5 Vertical shift clock timing

Reliability Test Items (Note 3)

Item	Test Condition	Remark
High Temperature Storage	Ta = 85ºC 240 hrs	Note 1, Note 4
Low Temperature Storage	Ta = -30ºC 240 hrs	Note 1, Note 4
High Temperature Operation	Ts = 85 ºC 240 hrs	Note 2, Note 4
Low Temperature Operation	Ta = -30 º C 240 hrs	Note 1, Note 4
Operate at High Temperature & Humidity	+60ºC, 90% RH max. , 240 hrs	Note 4
Thermal Shock	-30ºC / 30 min ~ +85ºC / 30 min for a total of 100 cycles, start with cold temperature and end with high temperature	Note 4
Vibration Test	Frequency range: 10 ~ 55 Hz, Stroke: 1.5 mm; Sweep: 10Hz ~ 55 Hz ~ 10 Hz, 2 hours for each direction of X. Y. Z.; (6 hour for total)	
Mechanical Shock	100 G 6ms, ± X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	RandomVibration: 0.015G * G/Hz from 5-200 Hz, -6dB/Octave from 200-500 Hz; 2 hours for each direction of X.Y. Z.; (6 hours for total)	
Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100 pF /15000 Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Mechanical Drawing