



## AND-TFT-25PA-LED

### 480 x 234 Pixels LCD Color Monitor

The AND-TFT-25PA-LED is a compact full color TFT LCD module, that is suitable for applications such as a camcorder, digital camera applications and other electronic products which require high quality flat panel displays. This device consists of a twisted nematic (TN) liquid crystal cell, that incorporates a TFT-array that has 480 x 234 pixels on a 2.45 inch diagonal screen, X and Y drivers, an LSI controller, and a built-in LED backlight.

#### Features

- Long Life LED Backlight
- Controller IC is not necessary
- Compatible with NTSC or PAL system
- High Resolution: 112,320 dots
- High Brightness
- Optimum Viewing Direction: 6 o'clock
- Up/Down and Left/Right Image Reversion
- Accepts Analog RGB input

#### Mechanical Characteristics

Item	Specification	Unit
Screen Size	2.45 inch (6.4 cm) diagonal	inch
Surface Treatment	Anti-Glare	–
Display Format	480 x 234	dot
Active Area	49.68 (W) x 37.44 (H)	mm
Dot Pitch	0.1035 (W) x 0.160 (H)	mm
Pixel Configuration	Delta	–
Outline Dimension	60.6 (W) x 48.4 (H) x 3.45(D)	mm
Weight	20 ± 3	g

#### Absolute Maximum Rating (GND = 0V, Ta = 25°C)

Item			Symbol	Absolute Maximum Rating		Unit
				Min.	Max.	
Supply Voltage	for Source Driver	Analog	$AV_{DD}$	-0.3	+7.0	V
		Digital	$V_{DD}$	-0.3	+7.0	
	for Gate Driver	Positive	$V_{GH}$	-0.3	+45	
		Negative	$V_{GL}$	-23	+0.3	
			$V_{GH} - V_{GL}$	+15	+40	
Analog Input Voltage (Note1)			$V_{Video}$	-0.3	+7.3	V
Operating Temperature (Note 2)			Top	0	+60	°C
Storage Temperature			Tstg	-20	+70	°C

Note 1: Analog Input Voltage means  $V_R$ ,  $V_G$ ,  $V_B$

Note 2: Operating Temperature defines that contrast, response time, & other display optical characteristics are Ta=+25°C.

Product specifications contained herein may be changed without prior notice.

It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.



## Power Consumption

Item		Symbol	Remarks	Specifications			Units
				Min.	Typ.	Max.	
Power Consumption	for LCD Panel	—	Note 1	—	31.82	—	mW
	for Backlight Lamp	—	Note 2	—	0.34	—	W
	TOTAL	—	—	—	0.372	—	W

**Note 1:** The power consumption for backlight is not included. **Note 2:** Backlight power consumption is calculated by  $I_L \times V_L$ .

## Electrical Characteristics - Operating Conditions

Item		Symbol	Specifications			Unit	Remarks
			Min.	Typ.	Max.		
Supply Voltage	$V_{CC}$		+4.5	+5.0	+5.5	V	
	$V_{DD}$		+3.0	+3.3	+3.6		
	$AV_{DD}$		+4.5	+5.0	+5.5	V	
	$V_{GH}$		+14.5	+15.0	+15.5	V	
	$V_{EE}$		-15.5	-15.0	-14.5	V	
	$V_{GL\ AC}$		—	+6.0	—	$V_{P-P}$	AC Component of $V_{GL}$
	$V_{GL\ DC}$		-12.5	-11.0	-9.5	V	DC Component of $V_{GL}$
Video Signal ( $V_B, V_R, V_G$ )	$V_{i\ AC}$		—	+4.0	+4.2	$V_{P-P}$	AC Component, Note 2
	$V_{i\ DC}$		—	+2.5	—	V	DC Component
Vcom	$V_{COM\ AC}$		—	+6.0	—	$V_{P-P}$	AC Component of $V_{COM}$
	$V_{COM\ DC}$		+0.9	+1.0	+1.1	V	DC Component of $V_{COM}$
H Level	$V_{IH}$		+0.7 $V_{DD}$	—	—	V	Note 1
	$V_{IL}$		—	—	+0.3 $V_{DD}$	V	

Note 1: STH1, STH2, CPH1, CPH2, CPH3, Q2H, INH, CPV, XOE, DIO1, DIO2

Note 1: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.

## Optical Specifications

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Viewing Angle	Horizontal	$\theta$		$\pm 45$	$\pm 50$	–	deg
	Vertical	$\theta$ (to 12 o'clock)	CR $\geq 10$	10	15	–	
		$\theta$ (to 6 o'clock)		30	35	–	
Contrast Ratio (Note 1)		CR	At optimized viewing angle	200	350	–	
Response Time	Rise	Tr	$\theta = 0^\circ$	–	15	30	ms
	Fall	Tf		–	25	50	
Transmission	Ratio	T	–	7.3	7.8	8.3	%
Uniformity		U	–	65	70	–	–
Brightness (Note 2)		LUM	–	200	250	–	cd/m <sup>2</sup>
White Chromaticity (Note 2)		X	$\theta = 0^\circ$	0.280	0.310	0.340	–
		Y		0.300	0.330	0.360	
LED Life Time + 25°C		–	–	1,000	5,000	–	hrs

Note 1:  $CR = \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.

Note 2: Topcon BM-7 (fast) luminance meter 1.0° field of view is used in the testing (after 10 minutes operation.)

**Current Consumption (GND = AV<sub>SS</sub> = 0V, Ta=25°C)**

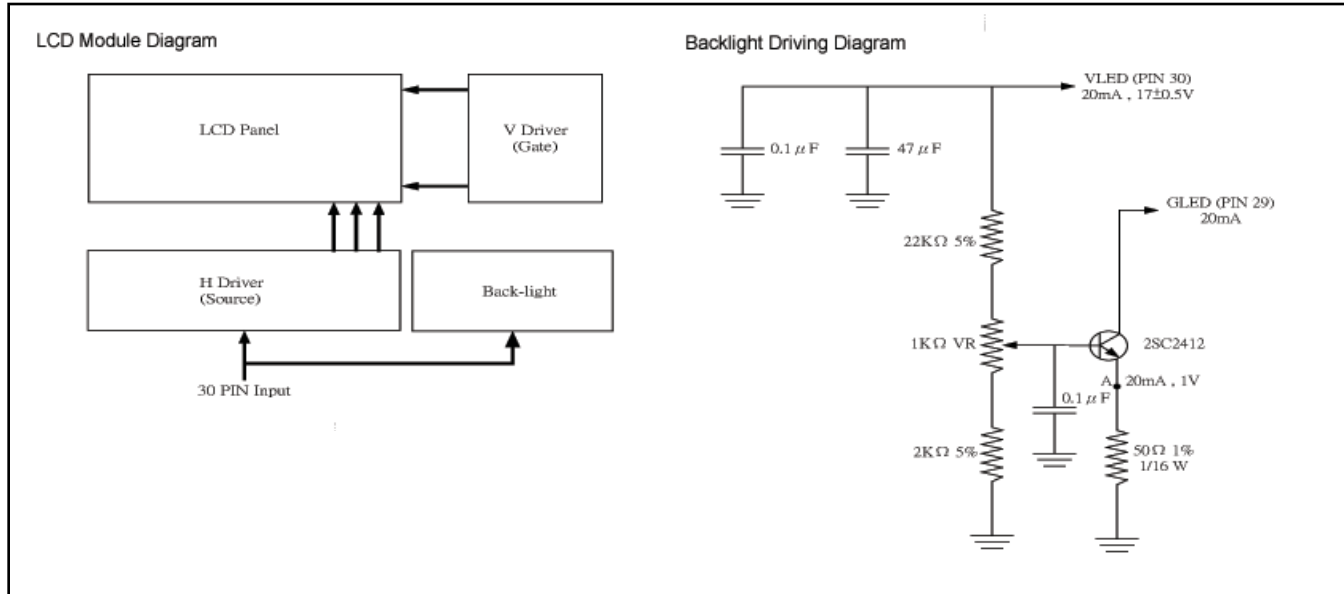
Parameter	Symbol	Condition	Specifications			Unit	Remark
			Min.	Typ.	Max.		
Current for Driver	I <sub>GH</sub>	V <sub>GH</sub> = +15V	–	0.1	0.2	mA	V <sub>GL</sub> center voltage
	I <sub>GL</sub>	V <sub>GL</sub> = -12V	–	0.36	0.9		
	I <sub>CC</sub>	V <sub>CC</sub> = +5V	–	0.2	0.4		
	AI <sub>DD</sub>	AV <sub>DD</sub> = +5V	–	3.5	5.0		
	I <sub>DD</sub>	V <sub>DD</sub> = +5V	–	0.6	1.5		
	I <sub>EE</sub>	V <sub>EE</sub> = -15V	–	0.3	0.6		

**Backlight Driving for Power Consumption**

Pin No.	Symbol	Description	Remarks
29	GLD	Supply current for LED	I <sub>L</sub>
30	VLED	Supply voltage for LED	V <sub>L</sub> , Note 1

**Note 1: Supply voltage for LED would depend on supply current.**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V <sub>L</sub>	–	17	–	V	I <sub>L</sub> =20mA Ta=25° C
Supply current	I <sub>L</sub>	–	20	–	mA	Ta=25° C

**Block Diagrams**



## Input/Output Terminals

Pin No.	Symbol	Function	Input/Output	Remarks
1	STH1	Start pulse for source driver	I/O	Note 1
2	AV <sub>SS</sub>	Analog GND for source driver	I	–
3	AV <sub>DD</sub>	Analog power input for source driver	I	Note 2
4	V <sub>S</sub>	Video Input B	I	Note 4
5	V <sub>G</sub>	Video Input G	I	
6	V <sub>R</sub>	Video Input R	I	
7	V <sub>SS</sub>	Digital GND	I	–
8	V <sub>DD</sub>	Digital power input	I	Note 3
9	CPH1	Sampling and shift clock for source driver	I	–
10	CPH2	Sampling and shift clock for source driver	I	–
11	CPH3	Sampling and shift clock for source driver	I	–
12	STH2	Start pulse for source driver	I/O	Note 1
13	Q2H	Video input rotation control	I	–
14	INH	Output enable for source driver	I	–
15	R/L	Left/Right Control for source driver	I	Note 1
16	V <sub>COM</sub>	Common electrode voltage	I	Note 4
17	XOE	Output enable for gate driver	I	–
18	CPV	Clock input for gate driver	I	–
19	U/D	Up/Down Control for gate driver	I	–
20	DIO2	Vertical start pulse	I/O	Note 5
21	DIO1	Vertical start pulse	I/O	
22	V <sub>GL</sub>	Gate off voltage (alternative every 1-H0	I	Note 4
23	V <sub>EE</sub>	Gate driver negative voltage	I	Note 6
24	V <sub>SS</sub>	GND	I	–
25	V <sub>CC</sub>	Logic power for gate driver	I	Note 3
26	V <sub>GH</sub>	Gate on voltage	I	Note 7
27	NC	No connection	–	–
28	NC	No connection	–	–
29	GLD	Supply current for LED	–	Note 8
30	VLED	Supply voltage for LED	–	Note 9

## Note 1: R/L, STH1 and STH2 mode

R/L	STH1	STH2	Remarks
High (V <sub>DD</sub> )	Input	Output	Left to Right
Low (0 Volt.)	Output	Input	Right to Left

Note 2: AV<sub>DD</sub> = +5V (Typ.)Note 3: V<sub>DD</sub>, V<sub>CC</sub> = +5V (Typ.)Note 4: V<sub>COM</sub> = 6V<sub>PP</sub>

## Note 5: DIO1, DIO2 and U/D mode

U/D	DIO1	DIO2	Remarks
High (V <sub>DD</sub> )	Input	Output	Down to Up
Low (0 Volt.)	Output	Input	Up to Down



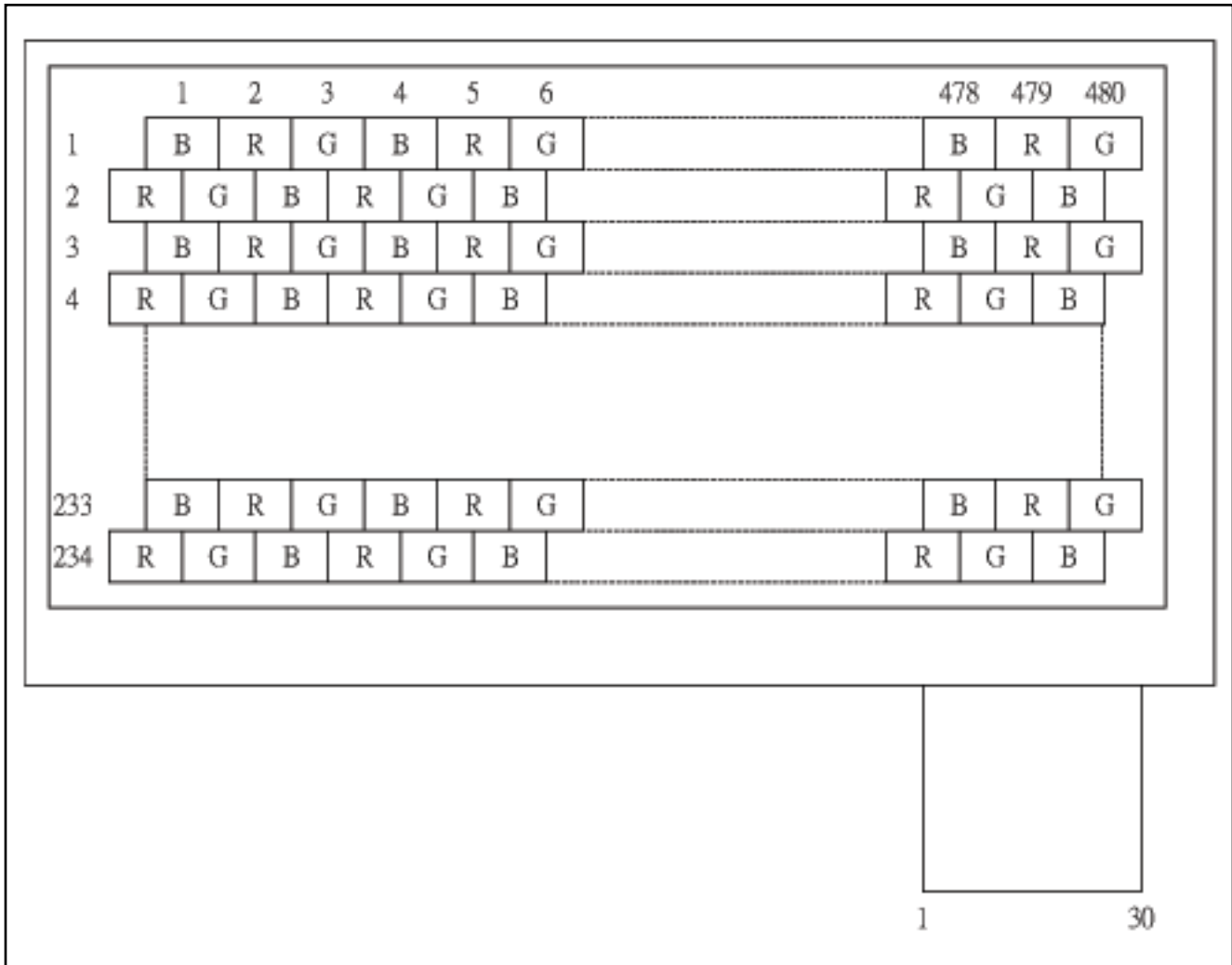
**Note 6:**  $V_{EE} = -15V$  (Typ.)

**Note 7:**  $V_{GH} = +15V$  (Typ.)

**Note 8:**  $G_{LED} = 20\text{ mA}$  (Typ.)

**Note 9:**  $V_{LED} = +17V$  (Typ.)

**Pixel Arrangement and input connector pin NO.**



**Input / Output Connector**

LCD Module Connector, FFC Down Connector, 30 pins, Pitch: 0.5 mm

**Timing Characteristics of Input Signals**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remarks
1 Field Scanning Period	t1V	–	262.5	–	H	
1 Line Scanning Period	t1H	–	63.5	–	μs	
Source Driver Operating Frequency	fhc	1.0	3.14	5.0	MHz	
Signal Sampling Pulse Width	tch <sub>w</sub>	200	317.7	1000	ns	
Signal Sampling Pulse Delay	tch <sub>d</sub>	95.3	105.9	116.5	ns	tch <sub>d</sub> 12, 23
Signal Sampling Pulse Width (H)	tch <sub>wh</sub>	142.9	158.8	174.7	ns	
Signal Sampling Pulse Delay (L)	tch <sub>wl</sub>	142.9	158.8	174.7	ns	
Source Start Signal Pulse Width	tsh <sub>w</sub>	90	317.7	630*	ns	*tsh <sub>set</sub> = tsh <sub>hld</sub>
Source Start Signal Setup Time	tsh <sub>set</sub>	20	158.8	–	ns	
Source Start Signal Hold Time	tsh <sub>hld</sub>	20	158.8	–	ns	
Source Output Enable Pulse Width	to <sub>hw</sub>	1.0	2.0	–	μs	
Source Start Signal Rising Time	tss	–	9.8	–	μs	
Video Input Signal Start Point	tvs	–	10.0	–	μs	
Phase Difference Between OE <sub>H</sub> & CPV	to <sub>c</sub>	1.5	2.3	–	μs	
Gate Clock Period	tc <sub>vw</sub>	10	63.5	–	μs	
Gate Clock Pulse Width (H)	tc <sub>vwh</sub>	10	31.7	48	μs	
Gate Clock Pulse Width (L)	tc <sub>vwl</sub>	10	31.7	48	μs	
Gate Start Signal Pulse Width	ts <sub>vw</sub>	5	63.5	126**	μs	**ts <sub>vset</sub> = ts <sub>vld</sub>
Gate Start Signal Setup Time	ts <sub>vset</sub>	5	53.2	–	μs	
Gate Start Signal Hold Time	ts <sub>vld</sub>	5	10.3	–	μs	
Phase Difference Between OE <sub>H</sub> & STH	to <sub>sp</sub>	–	4	–	μs	
Phase Difference Between SYNC & OE <sub>H</sub>	to <sub>hs</sub>	–	1.4	–	μs	
Gate Output Enable Pulse Width	to <sub>ev</sub>	–	2.5	–	μs	
V <sub>COM</sub> Delay Time	t <sub>DCOM</sub>	–	–	3	μs	
RGB Delay Time	t <sub>DRGB</sub>	–	–	2	μs	
Vertical Display Start	ts <sub>v</sub>	–	3	–	tH	



Dimensional Outline

