AND-TFT-62PA

1440 x 234 Pixels
LCD Color Monitor

The AND-TFT-62PA is a compact full color TFT LCD module, that is suitable for applications such as a car TV, portable DCD, GPS, multimedia applications and other AV equipment. This device consists of a twisted nematic (TN) liquid crystal cell, that incorporates a TFT-array that has 1440 x 234 pixels on a 6.2 inch diagonal screen, X and Y drivers, an LSI controller, and a built-in CCFL backlight and inverter (with optional board.)

Features

- 6.2 inch (16:9 diagonal)
- Compatible with NTSC & PAL system
- Accepts VGA Input (Analog RGB)
- High brightness CCFL backlight (350 Nits)
- Slim and compact
- Operating temperature range 0 to 60° C
- Storage temperature range -20 to 70° C
- High brightness

Mechanical Characteristics

Item	Specification	Unit
Screen Size	6.2 inch (16:9 diagonal)	inch
Surface Treatment	Anti-Glare	–
Display Format	1440 (W) x 234 (H)	dot
Active Area	137.52 (W) x 77.22(H)	mm
Dot Pitch	0.114 (W) x 0.33 (H)	mm
Pixel Configuration	Stripe	–
Outline Dimensions	154.4 typ. (W) x 92.6 (H) x 5.9 typ (D)	mm
Weight	140 ± 5	g

Absolute Maximum Rating

Item		Symbol	Absolute Maximum Rating		Unit
			Min.	Max.	
Supply Voltage for Source Driver		V_{DD2}	-0.3	+5.8	V
		V_{DD1}	-0.3	+7.0	V
Supply Voltage for Gate Driver		V_{CC}	-0.3	+6.0	V
		V_{GH}-V_{EE}	-0.3	+40.0	V
	H Level	V_{GH}	-0.3	+25.0	V
	L Level	V_{EE}	-16	+0.3	V
Analog Signal Input Level		V_R,V_G,V_B	-0.3	V_{DD1}+0.2	V
Storage Temperature		–	-20	+70	°C
Operation Temperature (defines that contrast, response time & other display optical characteristics are Ta=+25.)		–	0	+60	°C

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Product specifications contained herein may be changed without prior notice.
It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

Electrical Specification

Item		Symbol	Specifications			Units	Remark
			Min.	Typ.	Max.		
Supply Voltage For Source Driver	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H Level	V_{GH}	+15	+17	+19	V	
	L Level	$V_{EE\ DC}$	-13.0	-12	-10.5	V	DC Component of V_{EE}
	–	$V_{EE\ AC}$	–	+6.0	–	V_{P-P}	AC Component of V_{EE}
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	
Analog Signal Inut Level	V_{iAC}	–	–	+4.0	+4.2	V	AC Component
	V_{iDC}	–	–	2.5	–	V	DC Component
Digital Input Voltage	H Level	V_{IH}	0.7 V_{DD1}	–	V_{DD1}	V	
	H Level	V_{IL}	-0.3	–	0.3 V_{DD1}	V	
Digital Output Voltage	L Level	V_{OH}	0.7 V_{DD1}	–	V_{DD1}	V	
	L Level	V_{OL}	-0.3	–	0.3 V_{DD1}	V	
V_{COM}		$V_{C\ AC}$	–	+6.0	–	V_{P-P}	AC Component of V_{COM}
		$V_{C\ DC}$	–	1.5	–	V	DC Component of V_{COM}

Recommended Driving Condition for Back Light

Lam Voltage	V_L	500	550	600	Vrms	I_L=6mA
Lamp Current	I_L	3	6	8	MA	Note 1
Lamp Frequency	P_L	30	43	80	KHz	Note 2
Kick-off Voltage (25ºC) (Reference Value)	V_S	–	720	830	Vrms	Note 3

Note 1: In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.
Note 2 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.
Note 3 : The Kick-off times ≥1sec.

Back Light Driving

Pin Number	Symbol	Description	Remark
1	VL1	Input Terminal (Hi Voltage Side)	
2	VL2	Input Terminal (Low Voltage Side)	Note 1

Note 1: Low voltage side of back light inverter connects with Ground of inverter circuits.

Power Consumption

Parameter	Symbol	Conditions	Typ.	Max.	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	I_{GH} = +17V	0.60	0.90	mA	
Supply current for Gate Driver (Low level)	I_{EE}	I_{EE} = -12V	1.50	1.90	mA	V_{EE} center voltage
Supply current for Source Driver(Digital)	I_{DD1}	I_{DD1} = +3.3V	1.10	1.35	mA	
Supply current for Source Driver(Analog)	I_{DD2}	I_{DD2} = +5V	14.0	18.5	mA	
Supply current for Gate Driver (Digital)	I_{CC}	I_{CC} = +3.3V	0.05	0.09	mA	
LCD Panel Power Consumption	–	–	102.0	135.4	mW	Note 1
Back Light Lamp Power Consumption	–	–	3.30	–	W	Note 2

Note 1: The power consumption for back light is not included

Note 2: Back light lamp power consumption is calculated by I_LxV_L

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Optical Specifications

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Viewing Angle	Horizontal	θ 21, θ 22,	CR≥10	45	50	–	deg
	Vertical	θ 12		10	15	–	deg
		θ 11		30	35	–	deg
Contrast Ratio		CR	at optimized viewing angle*	200	350	–	–
Response Time	Rise	Tr	θ = 0°	–	15	30	ms
	Fall	Tf		–	25	50	ms
Transmission Ratio		T	θ = 0°	8.5	9.2	–	%
Uniformity ***		U	–	60	75	–	%
Brightness **		L	θ = 0°	300	350	–	cd/m^2
White Chromaticity **		x	θ = 0°	0.280	0.310	0.340	–
		y		0.300	0.330	0.360	–
Lamp Life Time	+25°C	–	–	20,000	30,000	–	hr

* Note: Contrast Ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance when Testing Point is White}}{\text{Luminance when Testing Point is Black}}$$

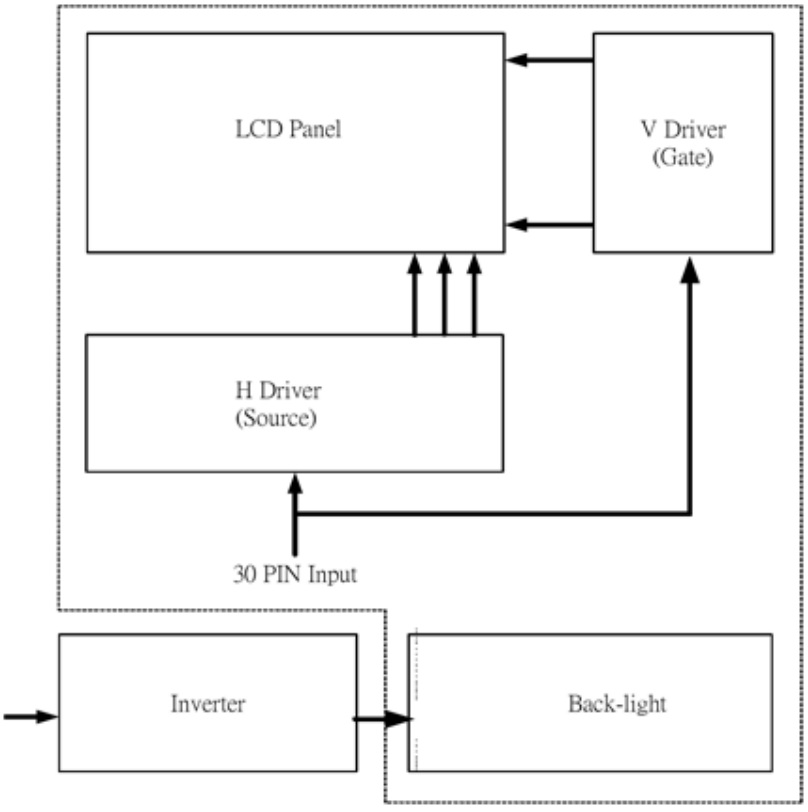
*** The uniformity of LCD is defined as:

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

** 1. Topcon BM-7 (fast) luminance meter 2º field of view is used in the testing (after 20~30 minutes operation.)
2. Lamp Current: 6mA
3. Inverter model: TDK-347.

Luminance meter: BM-5A or MB-7 fast (TOPCON)
Measurement distance: 500mm +/- 50 mm
Ambient illumination: < 1 Lux
Measurement direction: Perpendicular to the surface of module.
The test pattern is white (Gray Level 63.)

Block Diagram



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Inut/Output Terminals LCD Module Connector FC Down Connect, 30 pins, Pitch: 0.5 mm

Pin No.	Symbol	I/O	Description
1	GND	–	Ground for logic circuit
2	V_{CC}	I	Supply voltage of logic control circuit for gate driver
3	NC	–	No connection
4	V_{EE}	I	Negative power for gate driver
5	NC	–	No connection
6	V_{GH}	I	Positive power for gate driver
7	NC	–	No connection
8	STVD	I/O	Vertical start pulse ***Note 1
9	STVU	I/O	Vertical start pulse ***Note 1
10	CKV	I	Shift clock for gate driver
11	U/D	I	Up / Down Control for gate driver ***Note 1
12	OE3	I	Output enable for gate driver
13*	OE2	I	Output enable for gate driver
14	OE1	I	Output enable for gate driver
15	V_{COM}	I	Common electrode voltage
16	STHL	I/O	Start pulse for source driver ***Note 2
17	V_{SS2}	–	Ground for analog circuit
18	V_R	I	Video Input R
19	V_G	I	Video Input G
20	V_B	I	Video Input B
21	V_{SS1}	–	Ground for digital circuit
22	V_{DD2}	I	Supply power for analog circuit
23	CPH1	I	Sampling and shift clock for source driver
24	CPH2	I	Sampling and shift clock for source driver
25	CPH3	I	Sampling and shift clock for source driver
26	V_{DD1}	I	Supply power for digital circuit
27	R/L	I	Left / Right Control for source driver ***Note 2
28	NC	I	No Connection
29	OEH	I	Output enable for source driver
30	STHR	I/O	Start pulse for source driver ***Note 2

Note 1:

U/D	STVD	STVU	Scanning Direction
V_{CC}	Input	Output	Down to Up
GND	Output	Input	Up to Down

Note 2:

R/L	STHL	STHR	Scanning Direction
V_{CC}	Output	Input	Left to Right
GND	Input	Output	Right to Left

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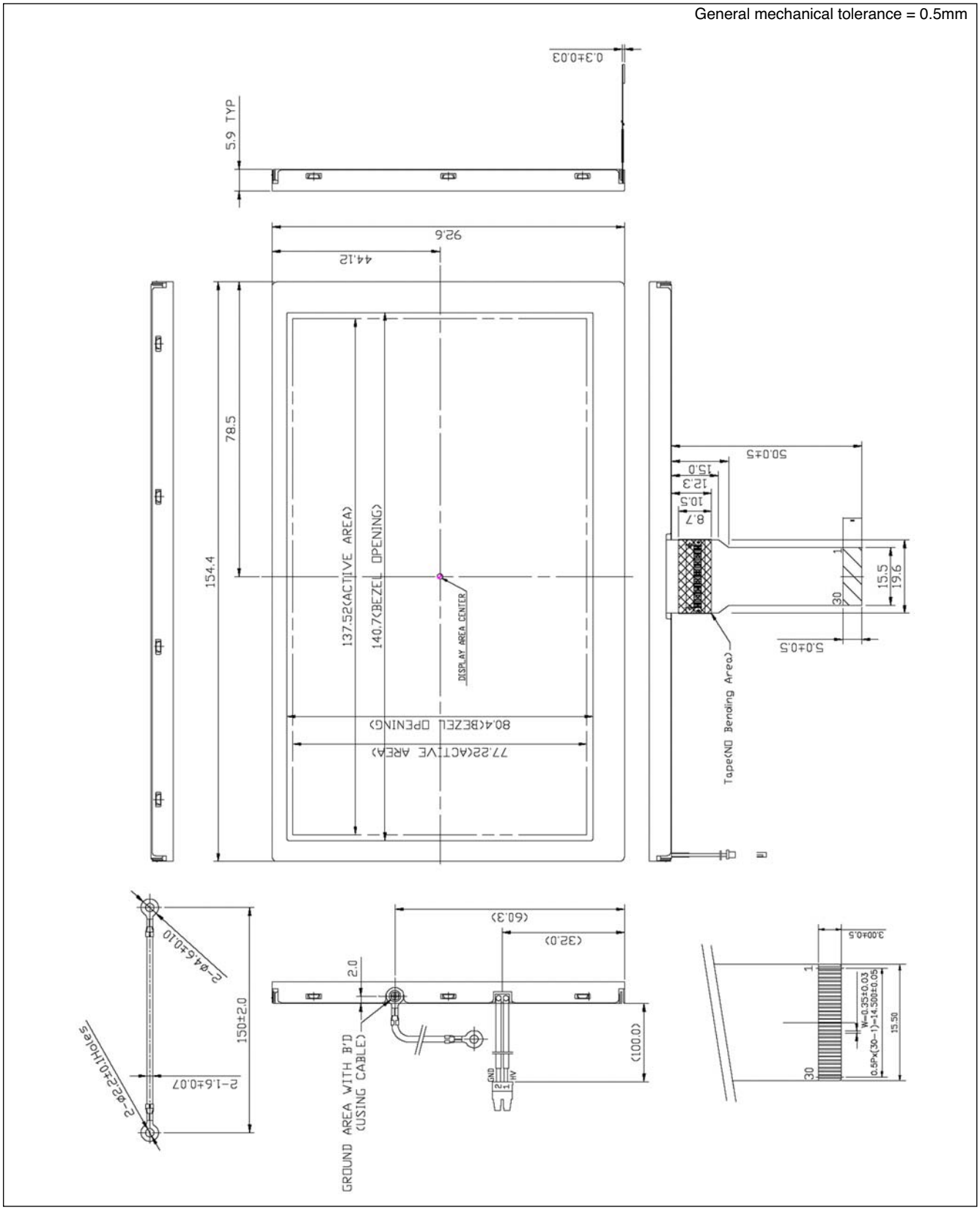
Dimensional Outline

General mechanical tolerance = 0.5mm



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