

Features

- p-Si construction with drivers on glass
- High luminance
- Digital and Analog Interface
- NTSC and PAL format compatible
- 16 Million/Full Color
- Slim (2.53 mm) and lightweight design
- Transmissive type. Fixed current LED backlight
- RoHS Compliant

Mechanical Characteristics

| Item | Specification | Unit |
|-------------------------|--------------------------------|------|
| Display Size (diag.) | 2.0 | inch |
| Display Type | Transmissive | – |
| Active Area | 40.672 (H) x 30.48 (V) | mm |
| Number of Dots | 640 (H) x RGB x 240 (V) | dot |
| Dot Pitch | 0.0635 (H) x 0.127 (V) | mm |
| Color Arrangement | RGB Delta | – |
| Color Numbers | 16 Million/Full Color | – |
| Outline Dimensions | 46.1(H) x 40.96(V) x 2.53* (D) | mm |
| Weight | 8.5 | g |
| Panel surface treatment | Hard Coating (3H) | – |

* Exclude FPC and protrusions.

Absolute Maximum Ratings (GND=0V)

| Item | Symbol | Min. | Max. | Unit |
|---|-----------|------|------|------|
| Logic Power Supply Voltage | V_{CC} | -0.5 | 4.5 | V |
| Input Signal Voltage VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRETB | V_{IN1} | 0 | VCC | V |
| Backlight Forward current | I_F | – | 25 | mA |

ANDpSi020TG-LED

2.0" Active color TFT LCD Module with Digital/Analog Interface

The ANDpSi020TG-LED is an 640 x 240 active matrix color TFT LCD Module with Digital and Analog Interface that utilizes new low temperature poly-silicon (p-Si) technology to provide brighter, thinner and lighter display with high resolution. Both of horizontal and vertical scan are reversible and controlled by the serial interface commands. The product is designed for the requirement of the green product, and the specification complies with Toppoly's "Green Product Chemical Substance Specification Standard Hand Book". All these features making it ideal for portable applications including personal digital assistants (PDAs), medical instruments and test & measurements instruments.

Absolute Maximum Ratings (Cont.) (GND=0V)

| Item | Symbol | Min. | Max. | Unit |
|-----------------|--------|------|------|------|
| Operating Temp. | Topr | -10 | +60 | °C |
| Storage Temp. | Tstg | -30 | +80 | °C |

Electrical Characteristics (GND=0V, Ta = 25°C) Driving TFT LCD Panel

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--|-----------|----------|------------------|------------|------|
| Power Supply for H/V Driver | V_{CC} | 2.85 | 3.0 | 3.6 | V |
| Input Driver Voltage VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRETB | Low | V_{IL} | GND | – | V |
| | High | V_{IH} | 0.8 x V_{CC}^* | V_{CC}^* | |
| PWM Output Voltage | V_{PWM} | 0 | – | V_{CC}^* | V |
| Feedback Voltage | V_{FB} | 0.55 | 0.6 | 0.65 | V |
| Panel Power Consumption | W_p | – | 50 | 60 | mW |

$V_{CC}^* = V_{CC}(\text{TYP})$

Note 1: The V_{CC} power is provided for overall panel module supply voltage.

Note 2: DC/DC feedback control voltage.

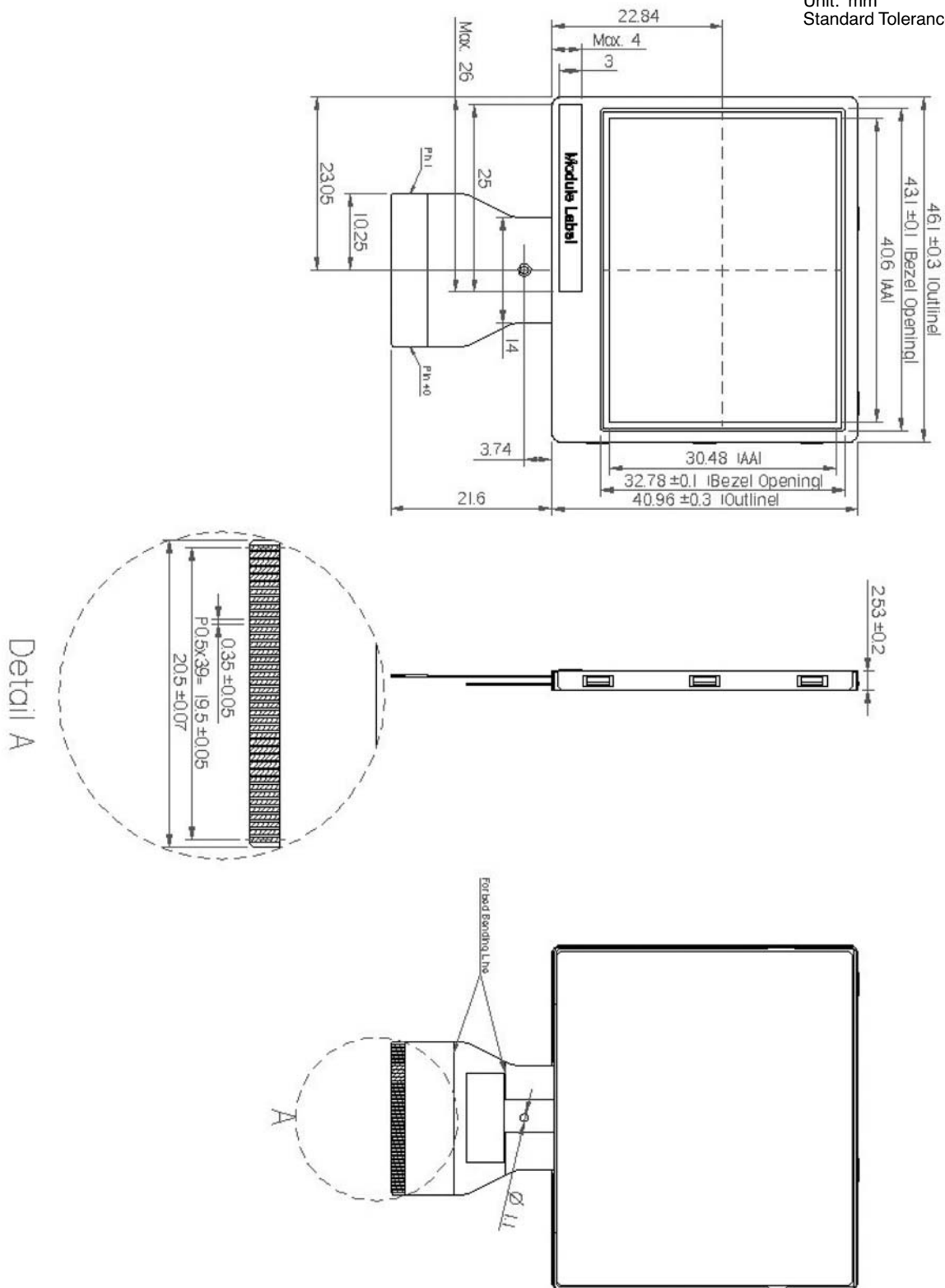
Driving Backlight in Standard Mode (Ta = 25°C)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|----------|------|------|------|------|
| Forward Current | I_F | – | 23 | 25 | mA |
| Forward Current Volt. | V_F | – | 3.4 | 3.6 | V |
| Backlight Power Consumption* | W_{BL} | – | 78.2 | 90 | mW |

* Backlight driving circuit is recommended as the fix current circuit

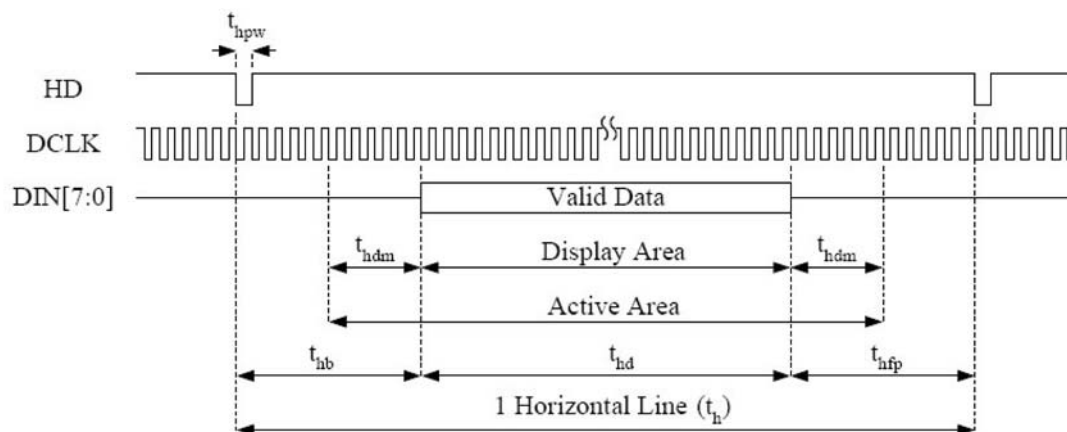
Dimensional Outline

Unit: mm
Standard Tolerance: 0.5mm



Timing Chart
YUV Mode: ITUR601-NTSC

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------|--------------|------|------|------|------|
| Dot Clock Frequency | DCLK | – | 27 | – | MHz |
| Horizontal Display Active | Display Area | – | 1440 | – | DCLK |
| Horizontal Line | t_h | – | 1716 | – | DCLK |
| HSYNC PULse Width | t_{hpw} | 1 | 1 | – | DCLK |
| Horizontal Back Porch | t_{hb} | – | 240 | – | DCLK |
| Horizontal Front Porch | t_{hfp} | – | 36 | – | DCLK |
| Horizontal Dummy Time | t_{hdm} | – | 4 | – | DCLK |

Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Horizontal

YUV Mode: ITUR601-PAL

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------|--------------|------|------|------|------|
| Dot Clock Frequency | DCLK | – | 27 | – | MHz |
| Horizontal Display Active | Display Area | – | 1440 | – | DCLK |
| Horizontal Line | t_h | – | 1728 | – | DCLK |
| HSYNC PULse Width | t_{hpw} | 1 | 1 | – | DCLK |
| Horizontal Back Porch | t_{hb} | – | 240 | – | DCLK |
| Horizontal Front Porch | t_{hfp} | – | 48 | – | DCLK |
| Horizontal Dummy Time | t_{hdm} | – | 4 | – | DCLK |

Timing Chart With Analog Interface

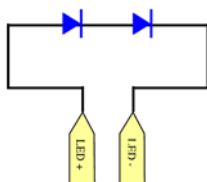
| Item | | Symbol | Min | Typ | Max | Unit |
|---------------------------|------|--------------|-----|-------|-----|------|
| Dot Clock Frequency | QVGA | DCLK | – | 25 | – | MHz |
| | NTSC | | – | 24.54 | – | |
| | PAL | | – | 24.38 | – | |
| Horizontal Display Active | | Display Area | – | 1280 | – | DCLK |
| Horizontal Line | | t_h | – | 1560 | – | DCLK |
| HSYNC PULse Width | | t_{hpw} | – | 1 | – | DCLK |
| Horizontal Back Porch | | t_{hb} | – | 240 | – | DCLK |
| Horizontal Front Porch | | t_{hfp} | – | 40 | – | DCLK |
| Horizontal Dummy Time | | t_{hdm} | – | 4 | – | DCLK |

Optical Specification Ta=25°C

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------|------------|---------------|--------------------|------|------|------|-------------------|
| Viewing Angle | | θ_{11} | $CR \geq 10$ | 30 | 40 | – | degree |
| | | θ_{12} | | 30 | 40 | – | |
| | | θ_{21} | | 15 | 20 | – | |
| | | θ_{22} | | 40 | 50 | – | |
| Contrast Ratio | | CR | $\theta = 0^\circ$ | 200 | 300 | – | – |
| Response Time | Rising | Tr | | – | 13 | 20 | ms |
| | Falling | Tf | | – | 22 | 30 | |
| Luminance | $I_F=23mA$ | L | | 200 | 250 | – | cd/m ² |
| Chromaticity | White | x_w | | 0.26 | 0.31 | 0.36 | – |
| | | y_w | | 0.29 | 0.34 | 0.39 | |

Input/Output Terminals
TFT LCD Panel - Recommended connector Molex 51374-4073

| Pin | Symbol | Input/Output | Description |
|-----|--------|--------------|---|
| 1 | CP3 | C | Capacitor for power setting |
| 2 | CP4 | C | Capacitor for power setting |
| 3 | CP5 | C | Capacitor for charge pump |
| 4 | CP6 | C | Capacitor for charge pump |
| 5 | CP7 | C | Capacitor for charge pump |
| 6 | CP8 | C | Capacitor for charge pump |
| 7 | DUMMY | – | Dummy |
| 8 | DUMMY | – | Dummy |
| 9 | PCD | C | Capacitor for pre-charge data signal high |
| 10 | VCOML | C | Capacitor for VCOM low |
| 11 | VCOMH | C | Capacitor for VCOM high |
| 12 | AGND | – | Analog ground |
| 13 | DUMMY | – | Dummy |
| 14 | AVDD | C | Regulation capacitor for analog voltage |
| 15 | CP1 | C | Capacitor for charge pump |
| 16 | CP2 | C | Capacitor for charge pump |
| 17 | PWM | O | Power transistor gate signal for the boost converter |
| 18 | FB | I | Main boost regulator feedback input |
| 19 | LED- | – | LED power: cathode; Note 1 below |
| 20 | DUMMY | – | Dummy |
| 21 | DUMMY | – | Dummy |
| 22 | LED+ | – | LED power: anode; Note 1 below |
| 23 | GND | – | Ground |
| 24 | VCC | – | Power supply for digital circuit and charge pump circuit |
| 25 | VSYNC | I | Vertical sync input. Negative polarity |
| 26 | HSYNC | I | Horizontal syn input. Negative polarity |
| 27 | DCLK | I | Clock signal, latch data onto line latches at the rising edge |
| 28 | DIN0 | I | Data input |
| 29 | DIN1 | I | Data input |
| 30 | DIN2 | I | Data input |
| 31 | DIN3 | I | Data input |
| 32 | DIN4 | I | Data input |
| 33 | DIN5 | I | Data input |
| 34 | DIN6 | I | Data input |
| 35 | DIN7 | I | Data input |
| 36 | SDA | I/O | Serial interface data line |
| 37 | SCL | I | Serial interface clock line |
| 38 | SCEN | I | Serial interface chip enable line |
| 39 | SHDB | I | Shutdown input |
| 40 | GREST | I | System reset pin |



Note 1: The figure to the left shows the connection of backlight LED.