CMPE222 HW2

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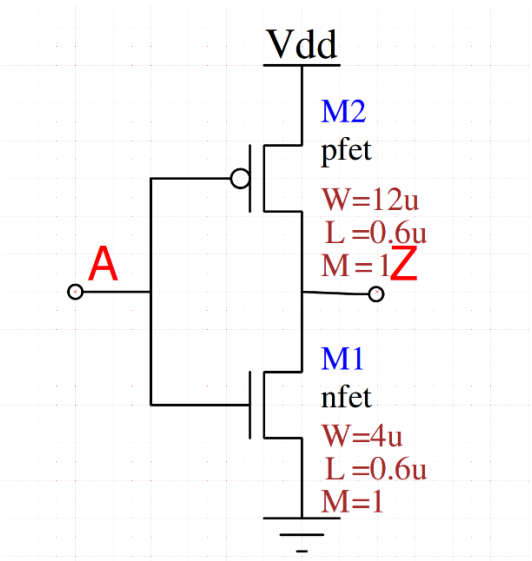
Assume all the MOSFET in this homework has a Minimum transistor length of 0.6um

Assume all the standard analysis is performed under temperature of 20C

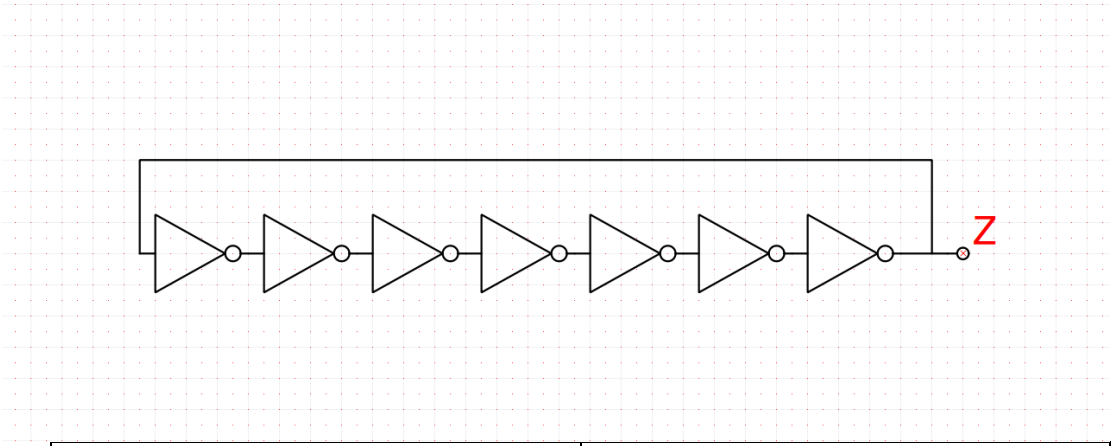
Q1: Ring Oscillator frequency analysis:

1. Single inverter:

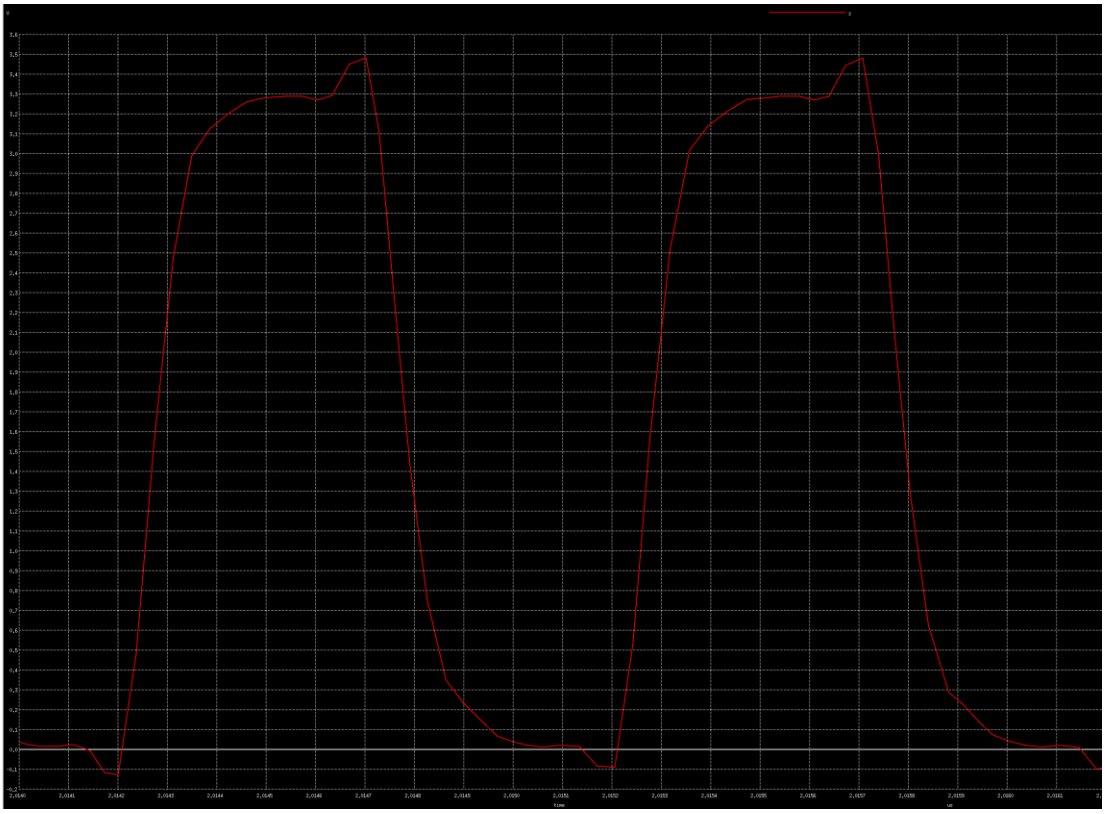


T_p = 7.927187e-11s

2. Ring Oscillator (7 inverter in series):



Theoretical frequency	Experimental frequency
$f = \frac{1}{2*t_p*n} = \frac{1}{7.927*10^{-11}*2*7} = 901.07\text{MHZ}$	$f = \frac{1}{2*t_p*n} = \frac{1}{1.00358*10^{-9}} = 996.64\text{MHZ}$



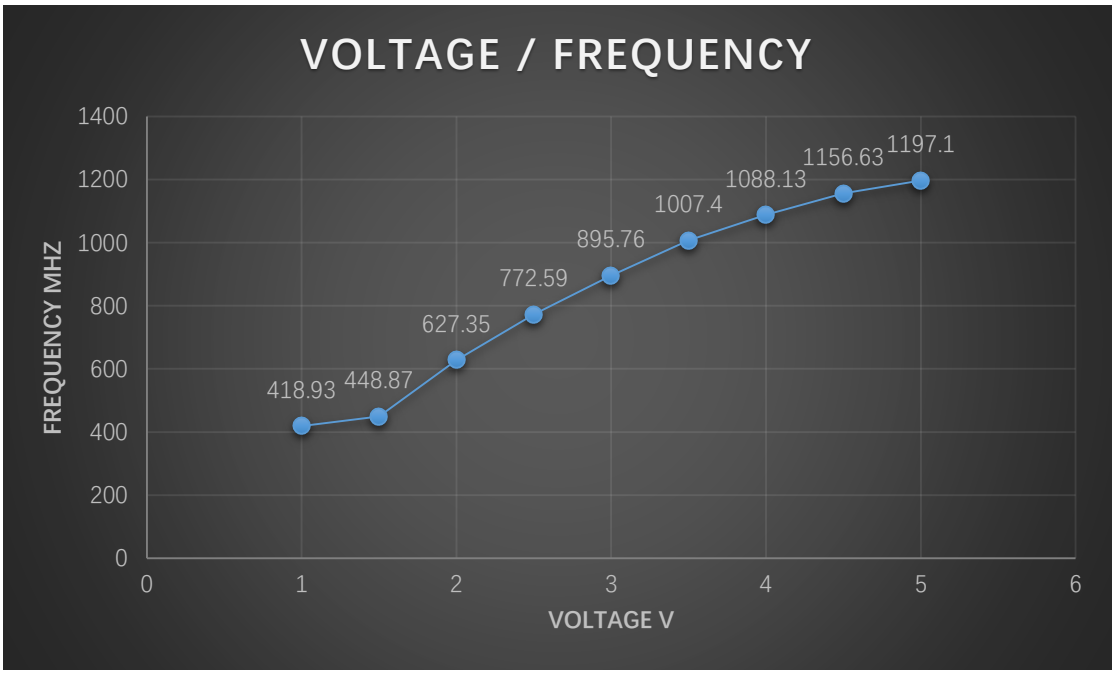
Q2: How does Ring Oscillator frequency Vary with supply voltage? :

In my spice simulation file, I intentionally create an exponentially incremental suuply voltage form 1V to 5v in approximately 5us

Since the voltage rise-time is very slow compare to the desired frequency, so we can assume that the ring oscillator is stable at every moment;

I take sample point at supply voltage reach 1v 1.5v 2v 2.5v 3v 3.5 4v 4.5 5v

Supply voltage	frequency
1.0V	418.93MHZ
1.5V	448.87MHZ
2.0V	627.35MHZ
2.5V	772.59MHZ
3.0V	895.76MHZ
3.5V	1007.4MHZ
4.0V	1088.13MHZ
4.5V	1156.63MHZ
5.0V	1197.10MHZ

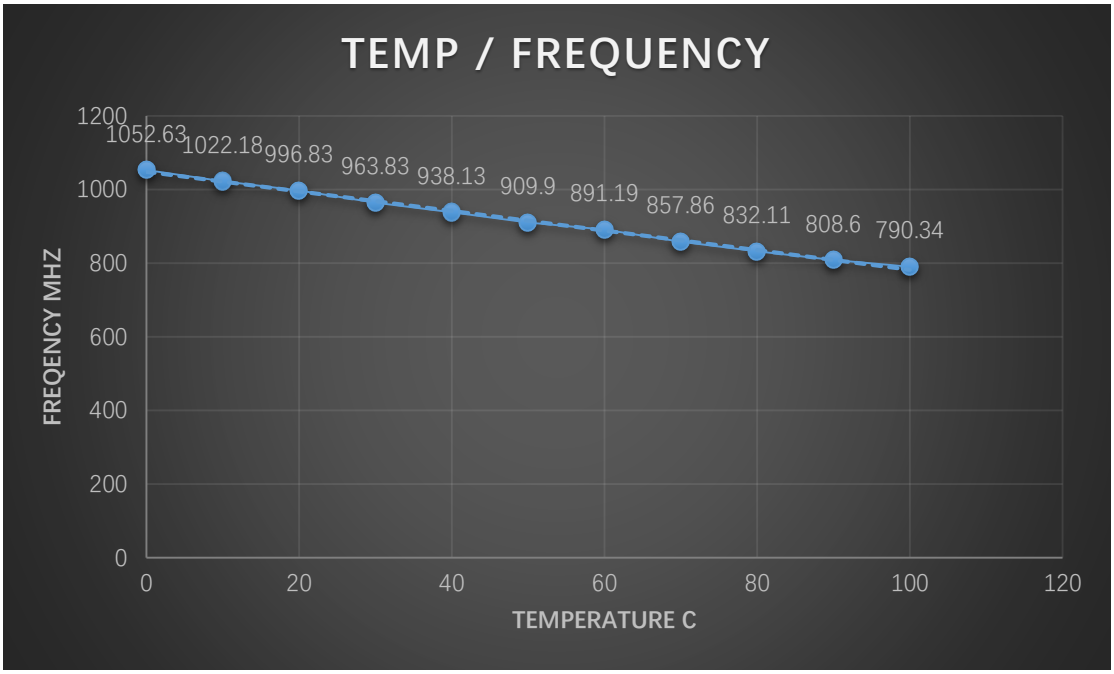


Q3 HOW should Ring Oscillator frequency vary with temperature from 0-100c?

The following table is temperature versus frequency

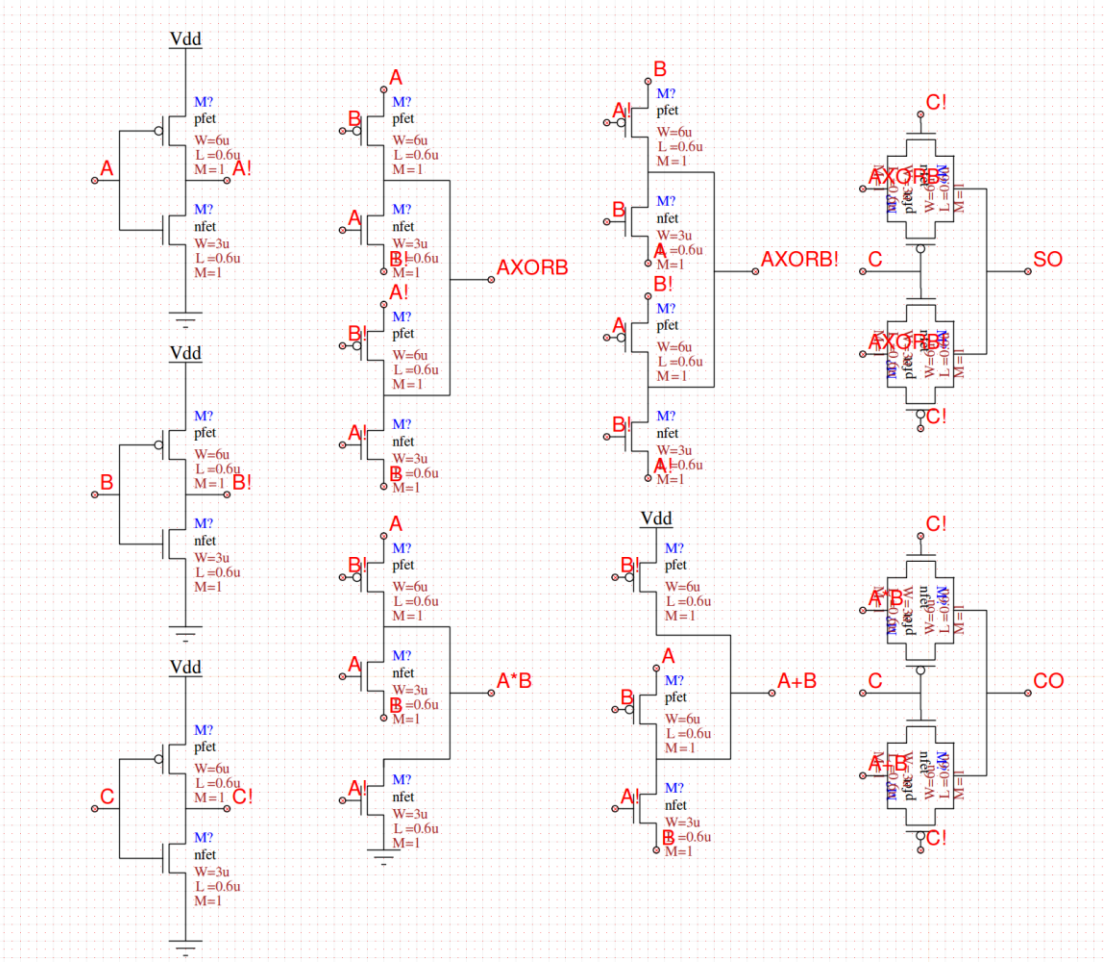
Temperature	Experimental frequency
0C	1052.63MHZ
10C	1022.18MHZ
20C	996.64MHZ
30C	963.83MHZ
40C	938.13MHZ
50C	909.90MHZ
60C	891.19MHZ
70C	857.86MHZ
80C	832.11MHZ
90C	808.60MHZ
100C	790.38MHZ

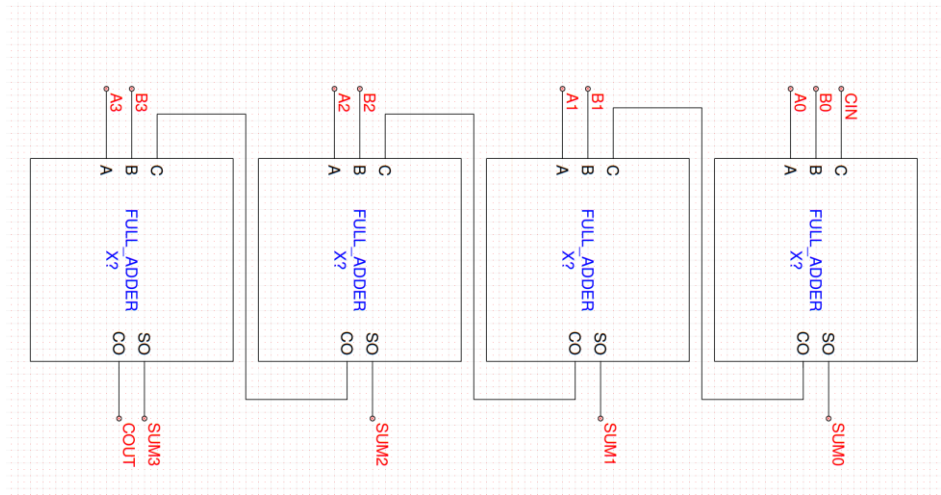
As the temperature increase, the frequency of the ring oscillator decreases



Q4: 4-bit Full adder

I use custom designed DPL-logic-style 4bit Full adder

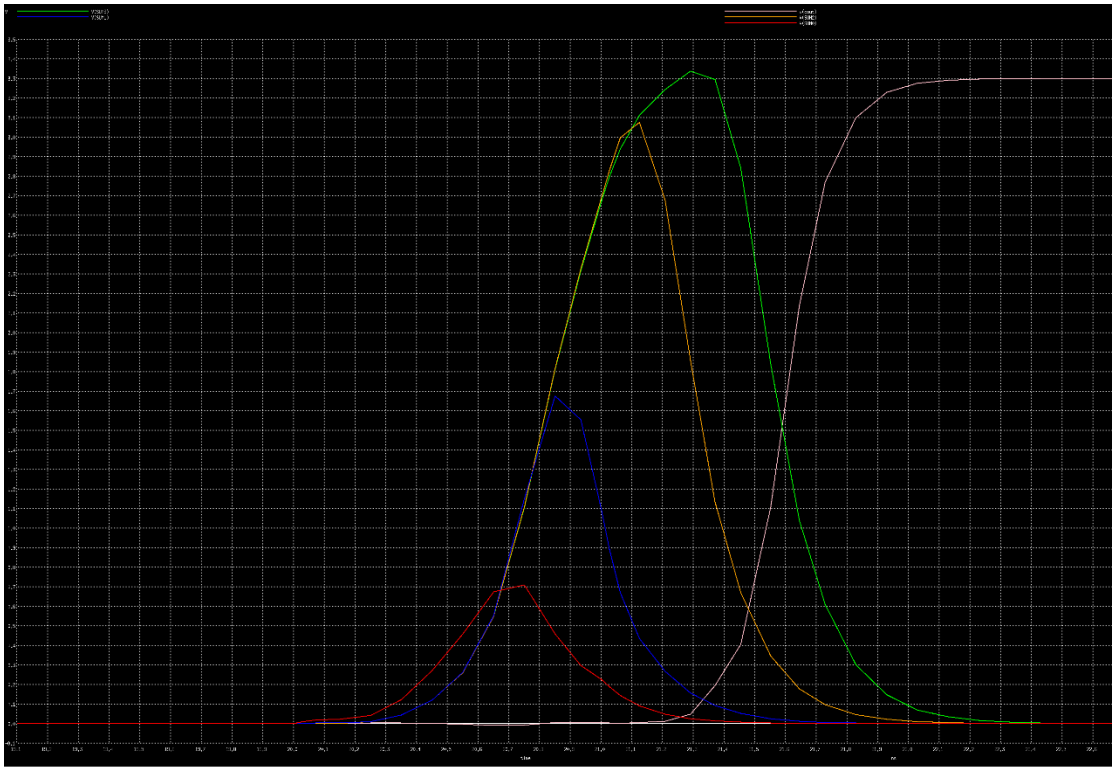




The worst case delay for ripple carry adder is determined by the carry chain:
Say A[3:0]=1111; B[3:0] = 0000; Carry = 1;
The COUT has the slowest output delay:
My spice file analyzes the worst case carry chain delay;
Initially A[3:0] = 4b1111; B[3:0] = 4b0000; CIN = 0;
At 20ns CIN = 1;
At 40ns CIN = 0;

0~20ns, COUT is 0;
20~40ns; COUT is 1;
40~100ns COUT is 0;

This input can analyze the worst case delay of carry chain of the four bit adder, since the carry chain signal shall propagate through the entire path of the adder, which makes it a critical path of the design;



Note: Pink line is the COUT
We can see that COUT has the slowest delay compare to SUM0 SUM1 SUM2 SUM3
carry_chain_worst_rise_delay= 1.10005×10^{-9}s = 1.10ns
carry_chain_worst_fall_delay= 1.027993×10^{-9}s = 1.02ns
4bit adder power consumption: 2.37945×10^{-9}watt