

Radio Frequency Integrated Circuits (RFIC)

Part I

Fonctions analogiques intégrées pour les radiofréquences

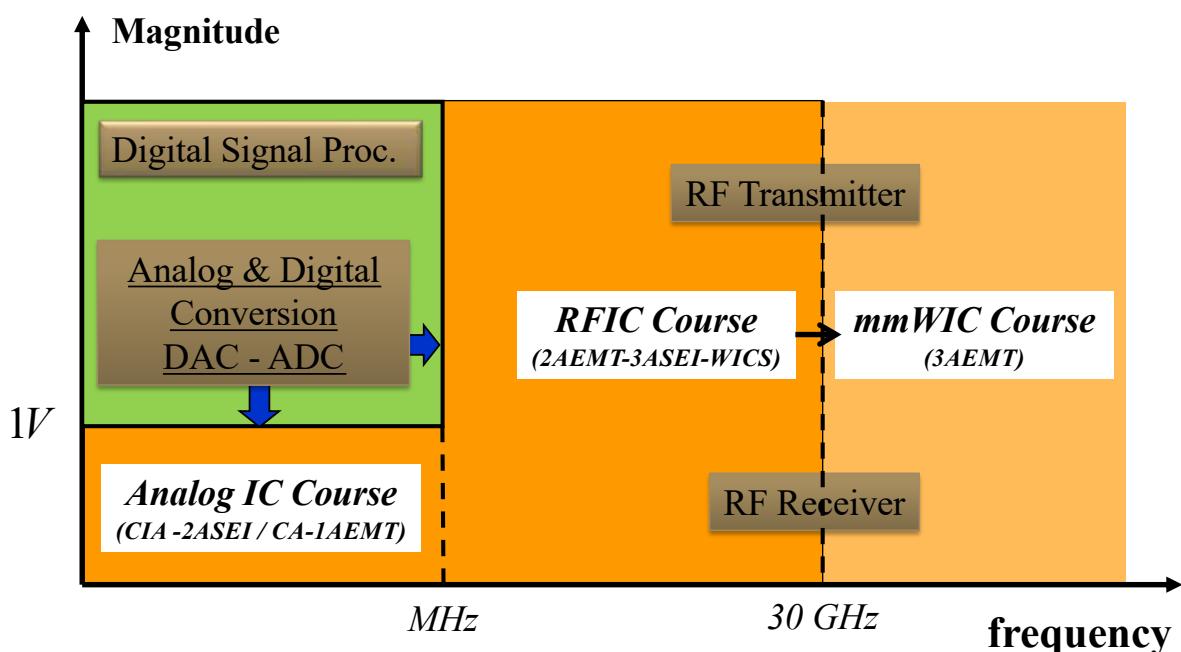
Sylvain BOURDEL

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Analog & Digital sharing in Integrated Circuits



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Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

➤ Packaging

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➤ Introduction to ITC

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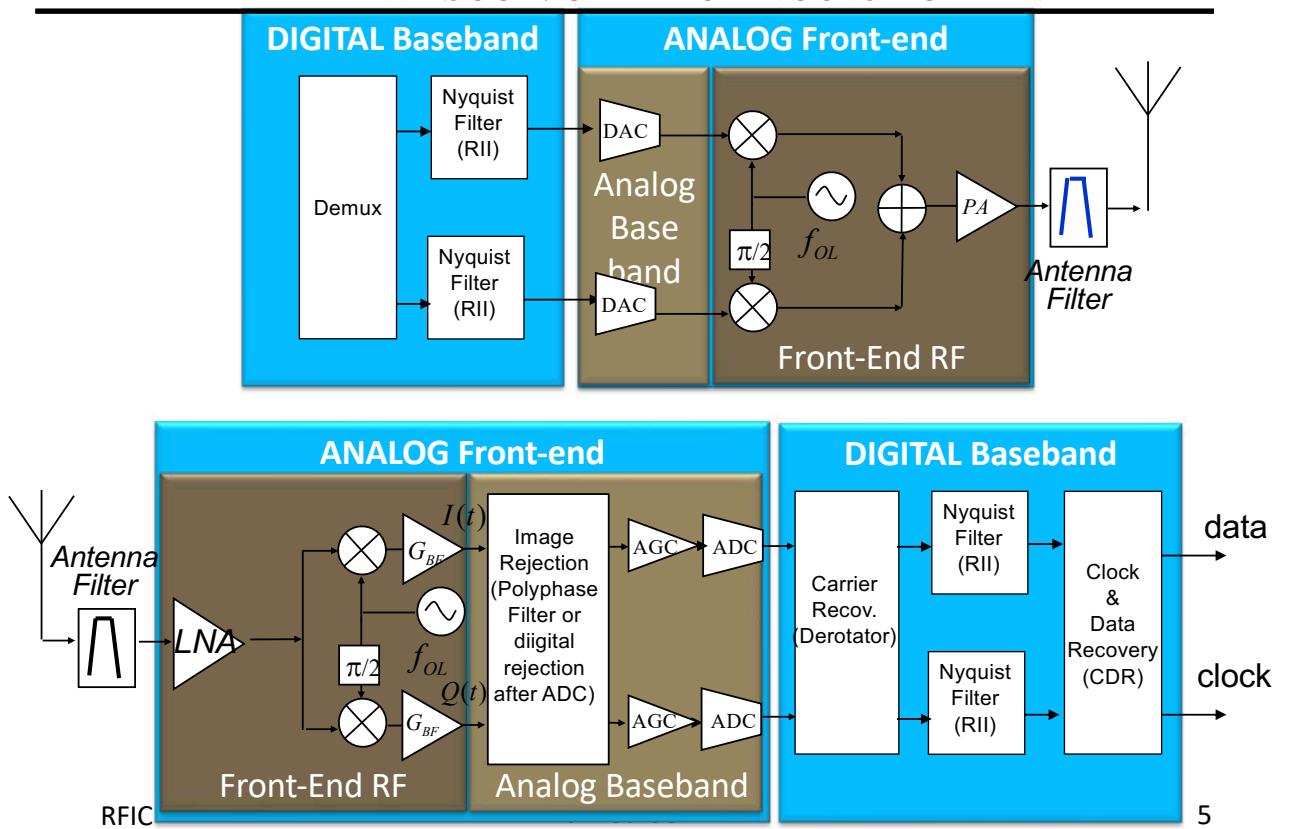
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Digital Modulation : Transceiver Architecture

➤ Analog RF signal processing basis



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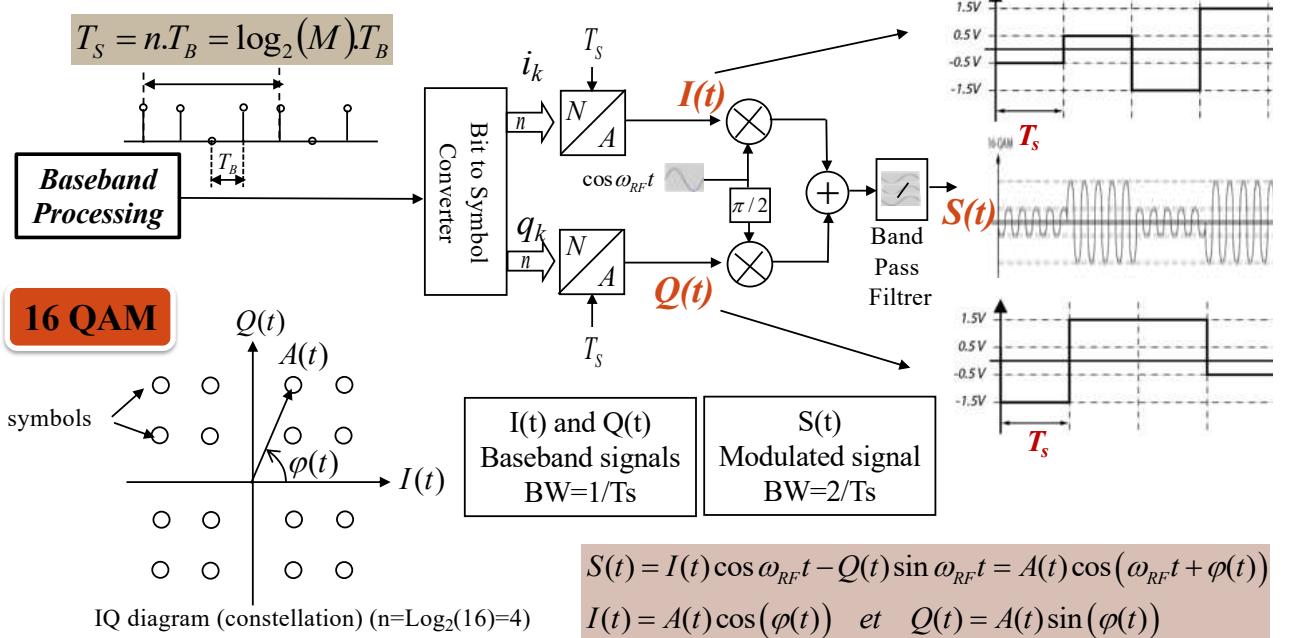
Digital Modulation : Basis

➤ Analog RF signal processing basis

Quadrature Amplitude Modulation (QAM) Principle

$S(t)$

Amplitude and phase modulation of a carrier (f_0) clocked at the symbol time (T_s)

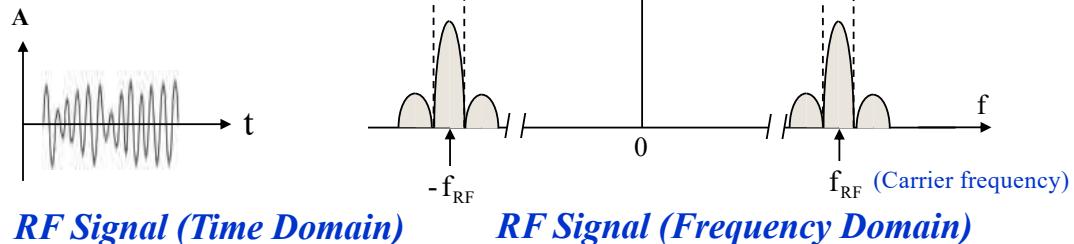


Digital Modulation : Frequency Spectrum

➤ Analog RF signal processing basis

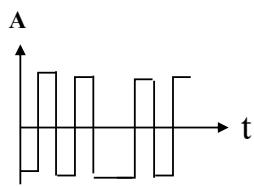
Band Pass Signal

Narrow bandpass signal:
 $BW/f_{RF} < 0,1\%$



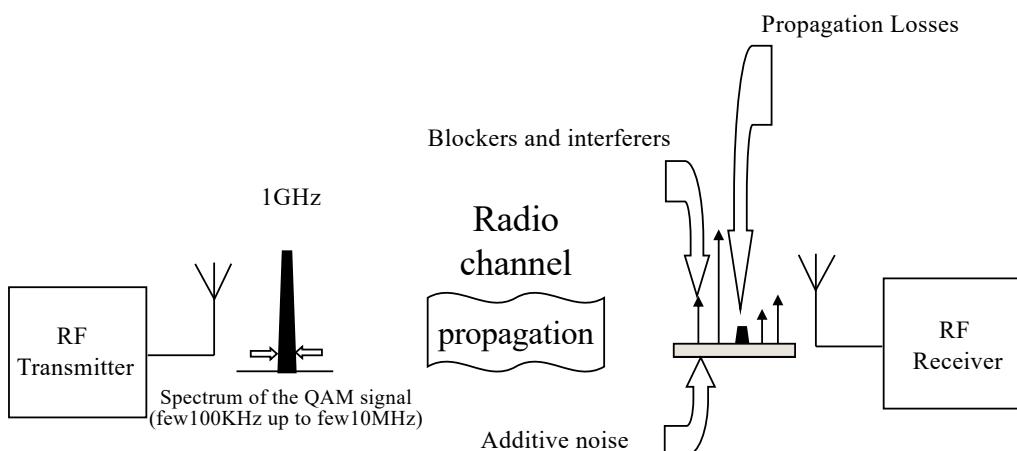
Base Band Signal

$BW = B_{BP}/2$



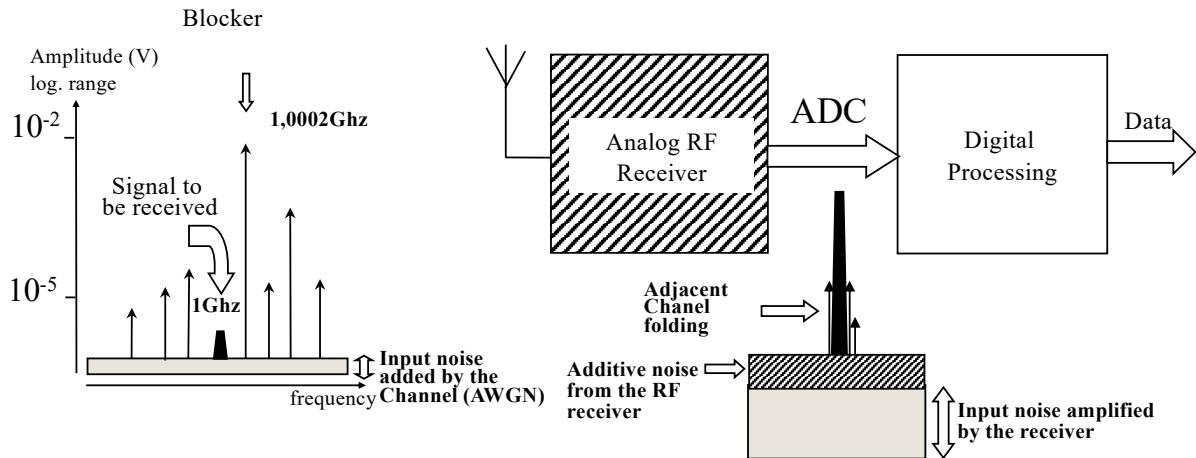
Behaviour of a narrowband RF signal (from transmitter to receiver)

➤ Analog RF signal processing basis



+ impact of the radio channel inside the signal bandwidth (filtering effect) => Wireless Communications lecture

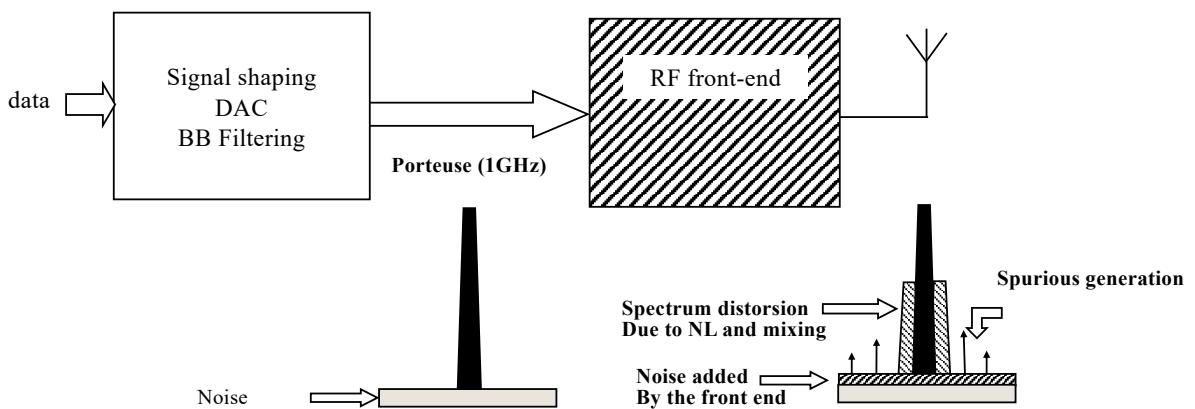
Issues of the analog RF signal processing (Receiver side)



The RF receiver must :

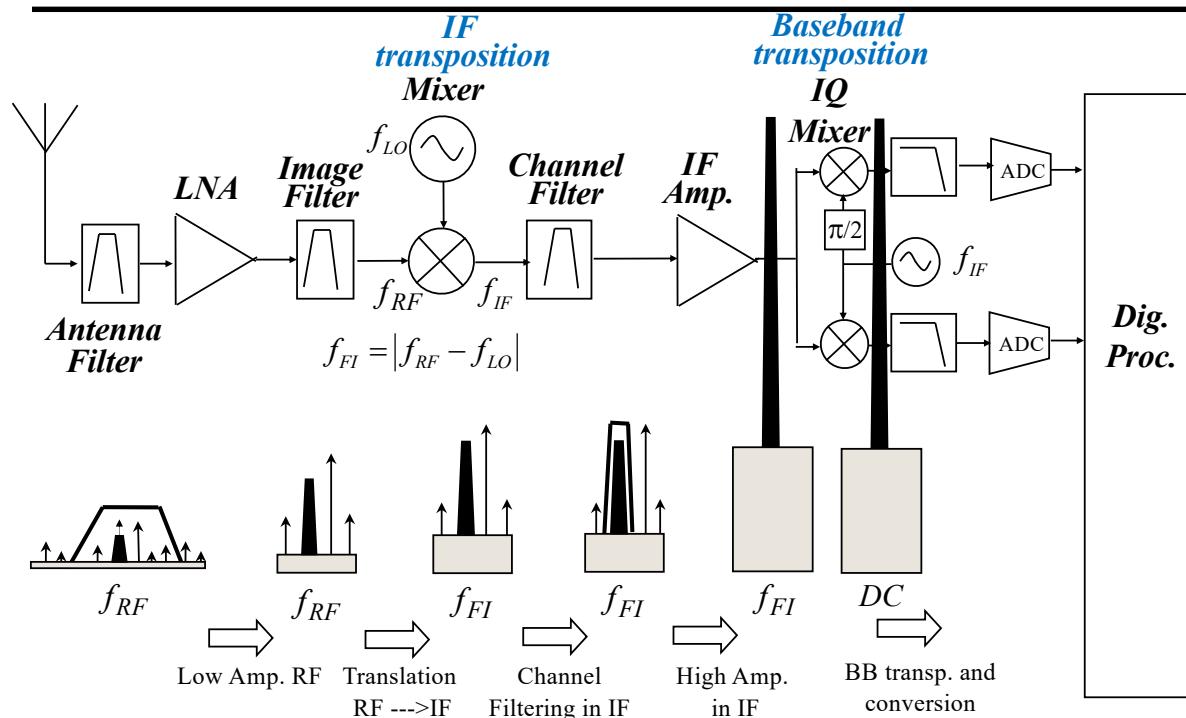
- amplify the input signal, filter out-of-band noise and blockers and transpose the input signal at lower frequency to be processed in digital domain for better convenience and performances :
 - with a minimum additive noise (**F**)
 - with low distortion due to non-linearities (**IIP3**)
 - with a good rejection of blocker, image, and adjacent channel (**IIP3/SFDR**)

Issues of the analog RF signal processing (Transmitter side)



The RF transmitter must :

- amplify the modulated signal at the power level required by the standard :
 - with a minimum additive noise
 - with low distortion
 - with low spurious



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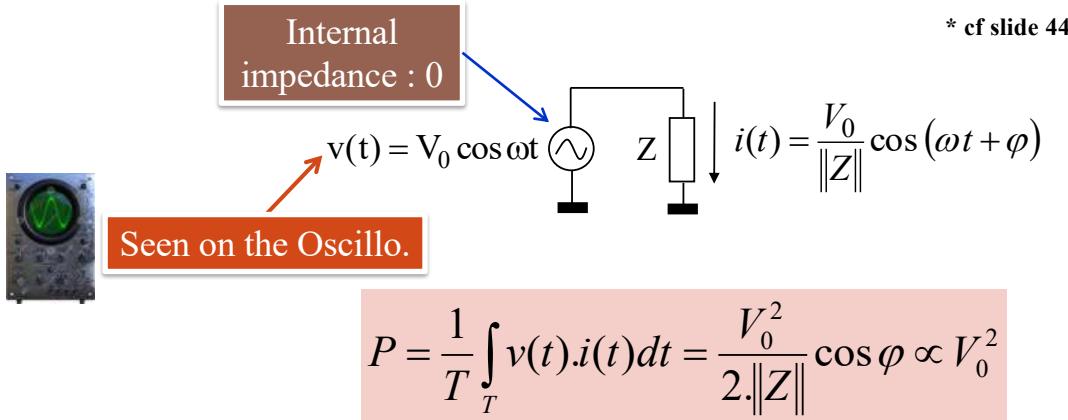
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Power for a sine signal

A – Mean Power delivered to an impedance Z in AC (Power Signal*)



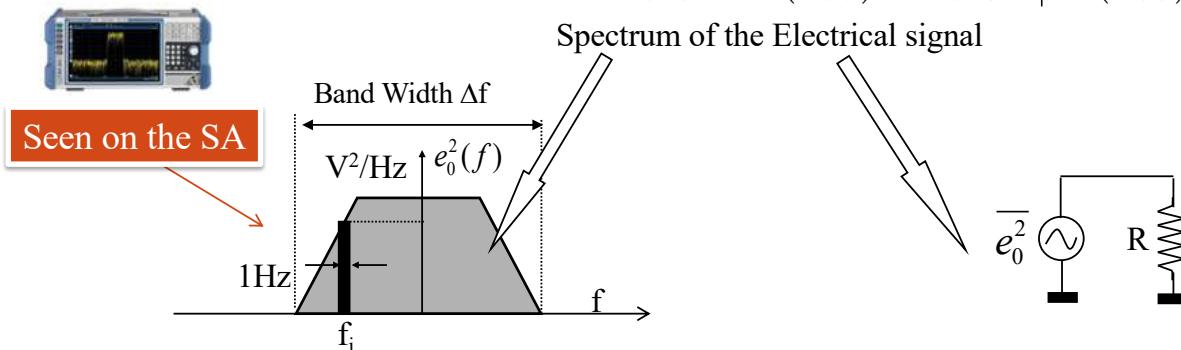
$$P = \frac{V_0^2}{2.R} = \frac{V_{RMS}^2}{R} \text{ if } Z = R$$

Power for a real signal (Power signal*)

* Finite mean power signal

B – Mean Power of a Power signal (sine, random sequence, white noise, ...) in a resistor R is given by the integration of the **Power Spectral Density (PSD)** $e^2(f)$ (en V^2/Hz).

for deterministic signals : $e(f) = TF(e(t))$ $e^2(f) = |TF(e(t))|^2$

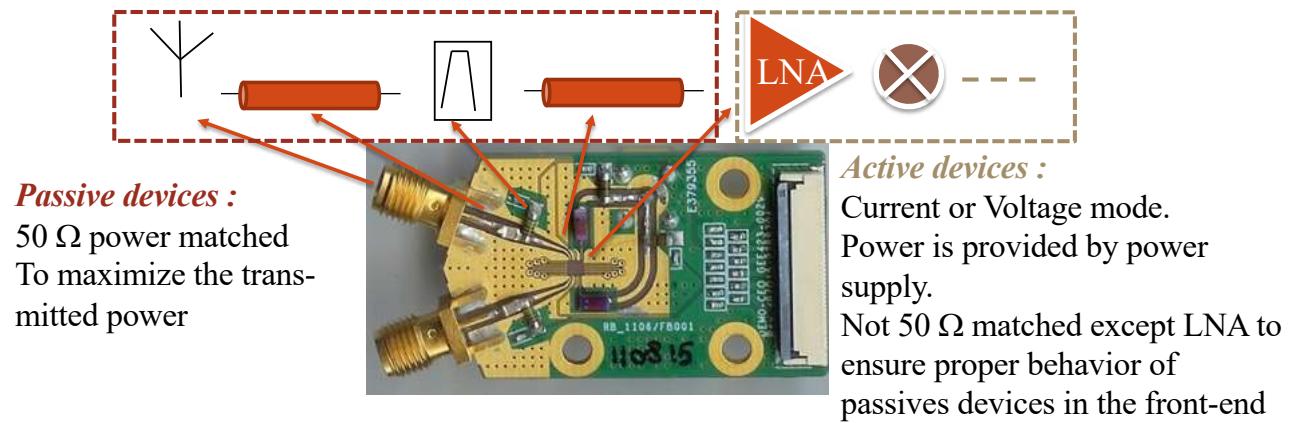
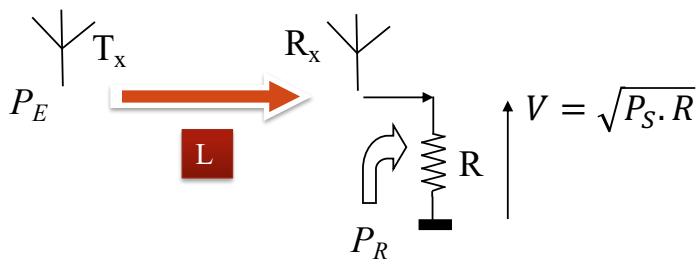


$$P = \frac{1}{R} \int_{\Delta f} e^2(f) df$$

If $e^2(f)$ is a constant over Δf $P = \frac{\bar{e}_0^2 \cdot \Delta f}{R} = \frac{V_{RMS}^2}{R}$

with $V_{RMS}^2 = \bar{e}_0^2 \cdot \Delta f$

Power delivered by an antenna



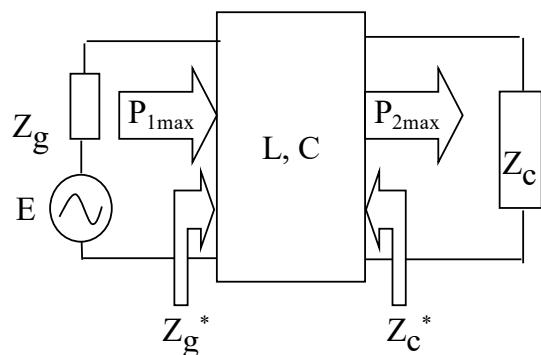
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Power matching

The power matching (maximal power delivered to a load Z_c which is also named **available power**) is achieved with a LC network which synthesizes conjugate impedance of the generator (Z_g^*) and of the load (Z_c^*) on each side of the network



For a lossless network (L and C are ideal)
 $\Rightarrow P_1 = P_2$

Available Power :

$$P_{av} = P_1 = P_2 = \frac{E^2}{4 \operatorname{Re}(Z_g)}$$

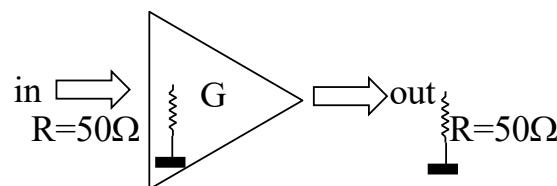
- power matching is achieved at only one frequency (narrowband network)
- when power matching is performed, the voltage across the Z_c load is maximum

Power matching

-Power matching is achieved only at the IC access to ensure full connection with external functions whose impedances are often set at 50Ω . Especially, the matching is mandatory

- in case of connections with transmission lines to avoid reflections and control the voltage levels at the lines access.
- in case of external filters for which 50Ω matching is necessary to fit the filter frequency specification.
- At RF frequency power matching is not achieved between stages inside the IC because propagation effects are negligible.
- At the circuit inputs, converting power into voltage is performed through impedance matching (not necessary on 50Ω).

Power gain and voltage gain



$$\begin{aligned} V_i &= 1V_{\text{RMS}} \\ \rightarrow 20\log(V_i) &= 0 \text{dBv} \end{aligned}$$

$$\begin{aligned} G_v &= V_o/V_i = 10 \\ \rightarrow 20\log(G_v) &= 20 \text{dB} \end{aligned}$$

$$\begin{aligned} V_o &= 10V_{\text{RMS}} \\ \rightarrow 20\log(V_o) &= 20 \text{dBv} \end{aligned}$$

$$\begin{aligned} P_i &= V_i^2/R = 0.02 \text{W} \\ \rightarrow 10\log(P_i \cdot 10^3) &= 13 \text{dBm} \end{aligned}$$

$$\begin{aligned} G_p &= P_o/P_i = (V_o/V_i)^2 = 100 \\ \rightarrow 10\log(P_o/P_i) &= 10\log(V_o/V_i)^2 \\ &= 20\log(V_o/V_i) \\ &= 20 \text{dB} \end{aligned}$$

$$\begin{aligned} P_o &= V_o^2/R = 2 \text{W} \\ \rightarrow 10\log(P_o \cdot 10^3) &= 33 \text{dBm} \end{aligned}$$

Measurement Metrics

A – Relative measurement in dB (decibel) (Gain)

$$\text{Power: } \left(\frac{P_1}{P_2} \right)_{\text{dB}} = 10 \log \frac{P_1}{P_2} \quad \text{Voltage: } \left(\frac{V_1}{V_2} \right)_{\text{dB}} = 20 \log \frac{V_1}{V_2}$$

B – Power measurement in dBm « dBmilliwatt »

$$P_{\text{dBm}} = 10 \log \frac{P_W}{10^{-3}} \quad \triangle! \quad P_{1_{\text{dBm}}} - P_{2_{\text{dBm}}} = 10 \log \frac{P_{1W}}{P_{2W}} = \left(\frac{P_{1W}}{P_{2W}} \right)_{\text{dB}}$$

Gain

C – Relation between peak voltage and power in dBm (in AC)

$$P_{\text{dBm}} = 10 \log \frac{P_W}{10^{-3}} = 10 \log \frac{V_{\text{peak}}^2}{2R \cdot 10^{-3}} \Rightarrow R = 50\Omega : P_{\text{dBm}} = 10 \log \frac{P_W}{10^{-3}} = 10 \log 10 V_{\text{peak}}^2$$

D - dBc « dBcarrier »: ratio between a blocker P_b and the carrier P_c

$$P_{b_{\text{dBc}}} = 10 \log \frac{P_b}{P_c}$$

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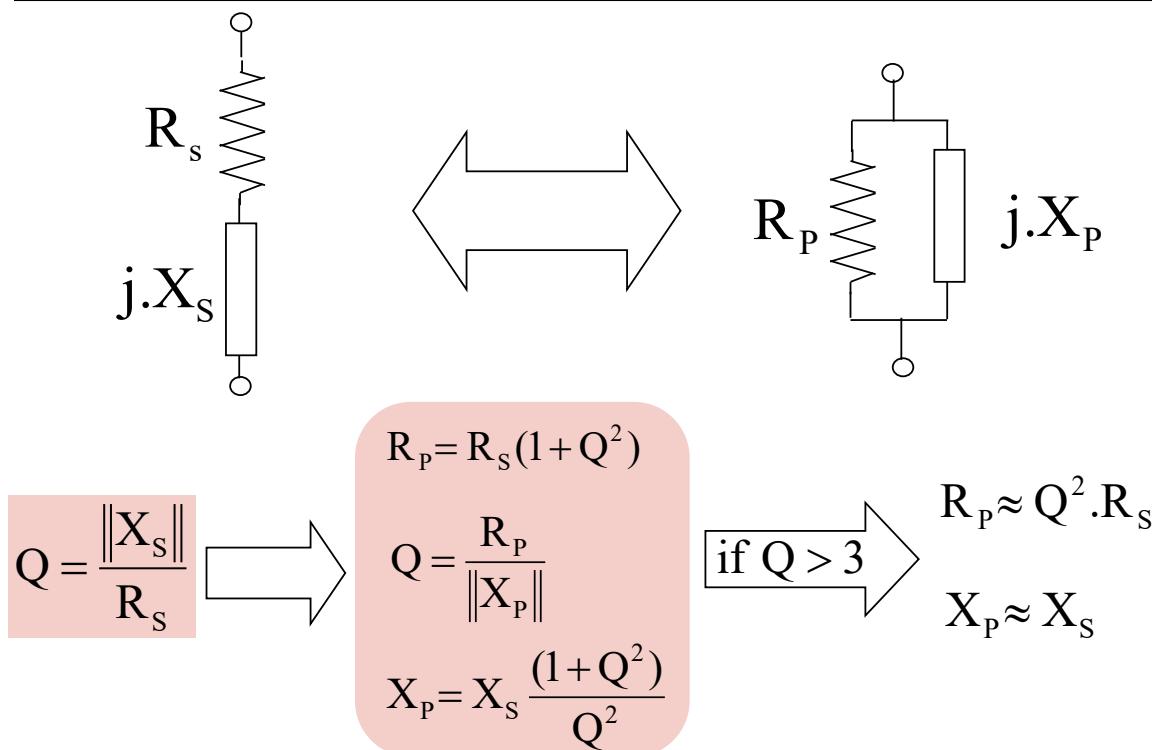
➤ Packaging

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S/P impedance transformation at f_0

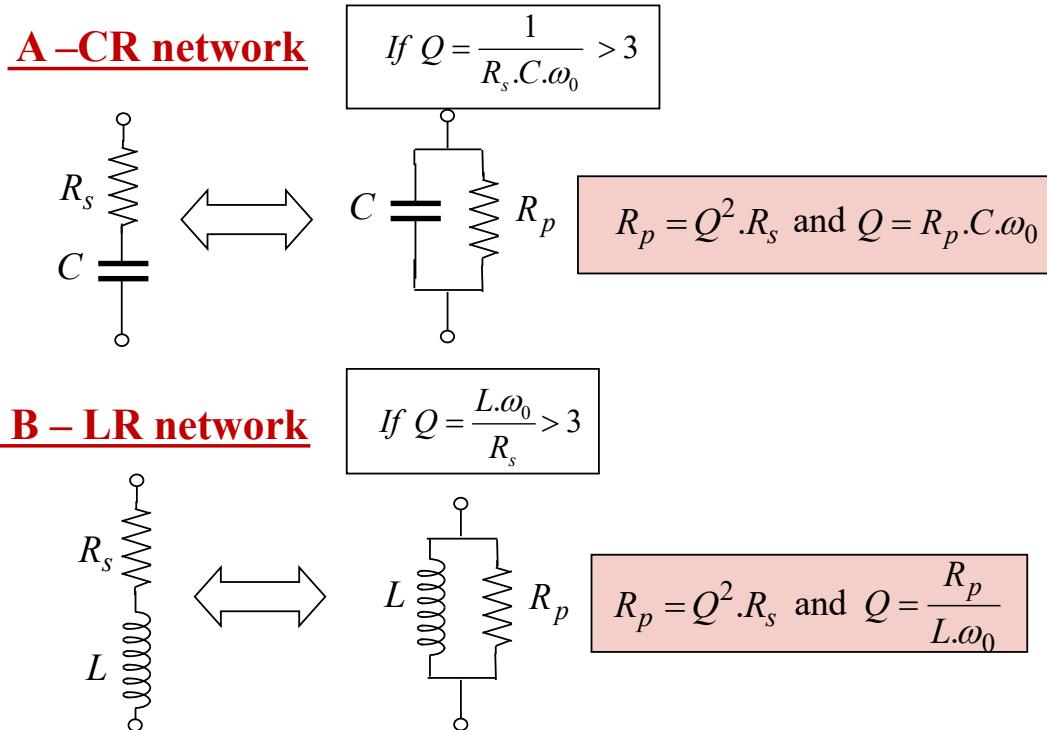


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S/P impedance transformation at f_0

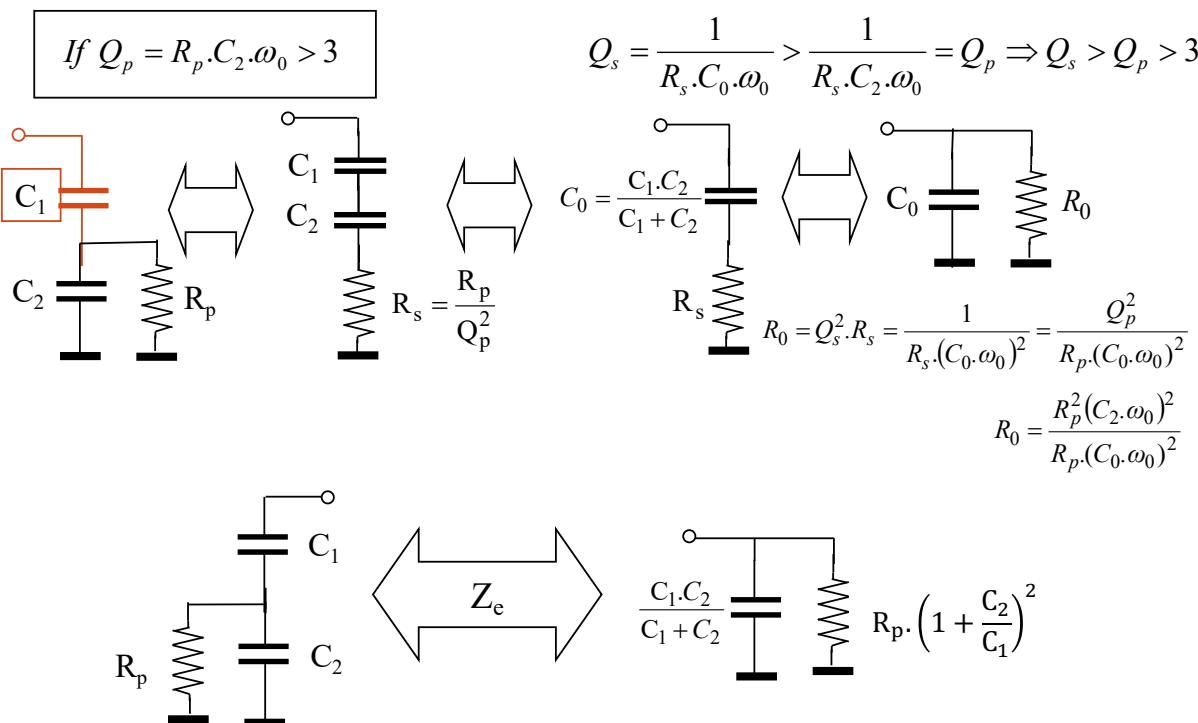


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S/P impedance transformation at f_0



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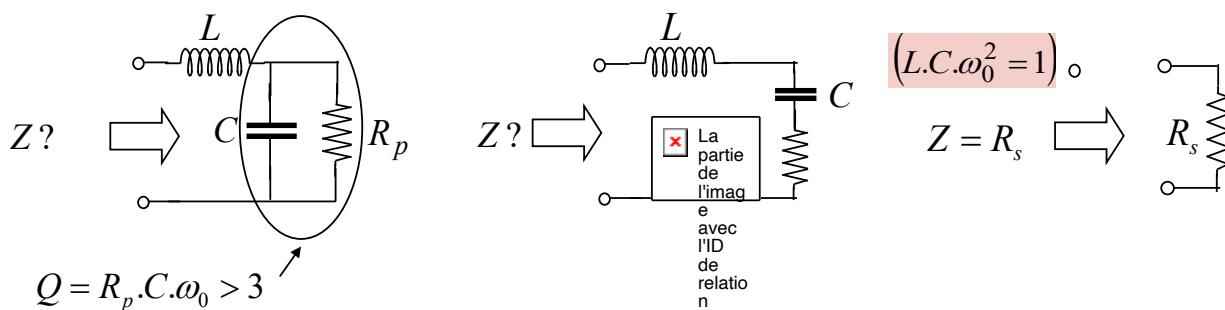
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S/P impedance transformation at f_0

C - RLC network at resonant frequency

Exemple :



This kind of network lower the value of a resistive (real) load :

$$R_p \Rightarrow R_s = \frac{R_p}{Q^2}$$

é dans le fichier

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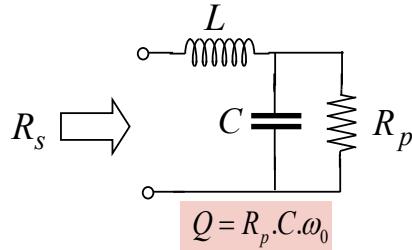
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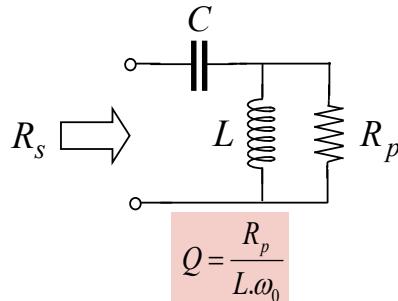
S/P impedance transformation at f_0

D - Application : Transformation of a resistive load

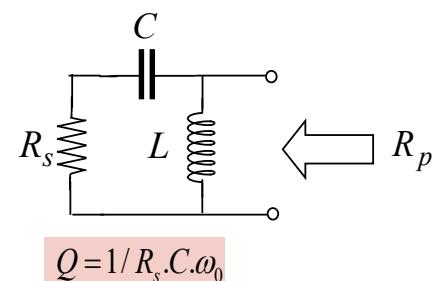
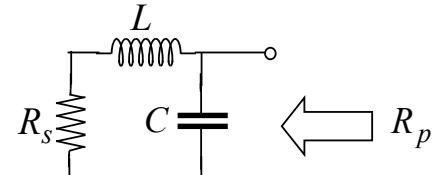
- Step-down network



$$\begin{aligned} L \cdot C \cdot \omega_0^2 &= 1 \\ \text{and} \\ R_s &= R_p / Q^2 \end{aligned}$$



- Step-up network

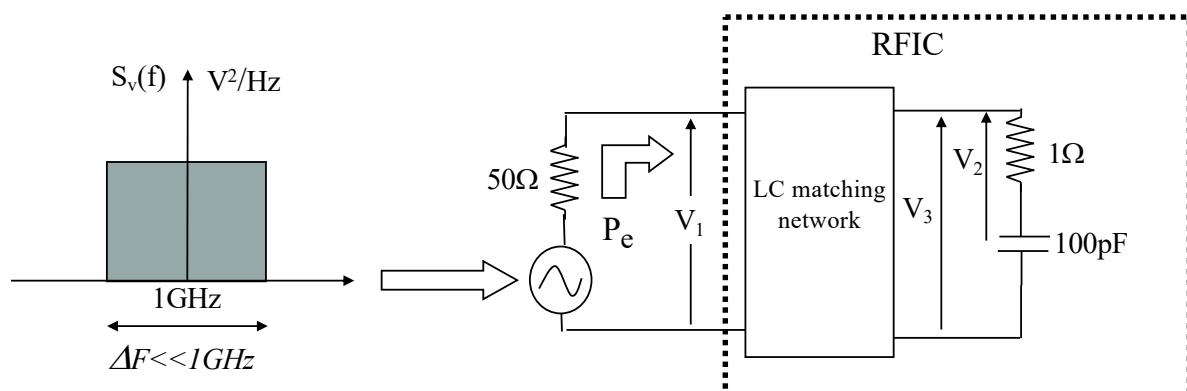


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S/P impedance transformation at f_0



Exercise

- Calculate the necessary LC network to perform power matching at the input of the IC at 1GHz.
- Give the mean voltages V_1 , V_2 and V_3 (in Volt and in dB V) for $P_e = 0dBm$

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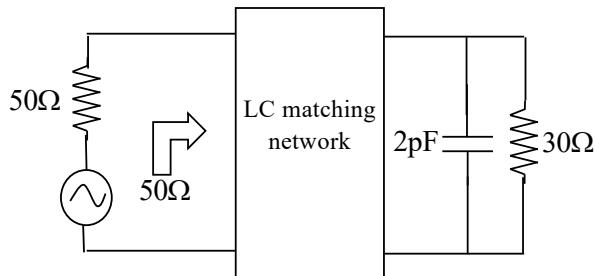
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S/P impedance transformation at f_0

Important Notes:

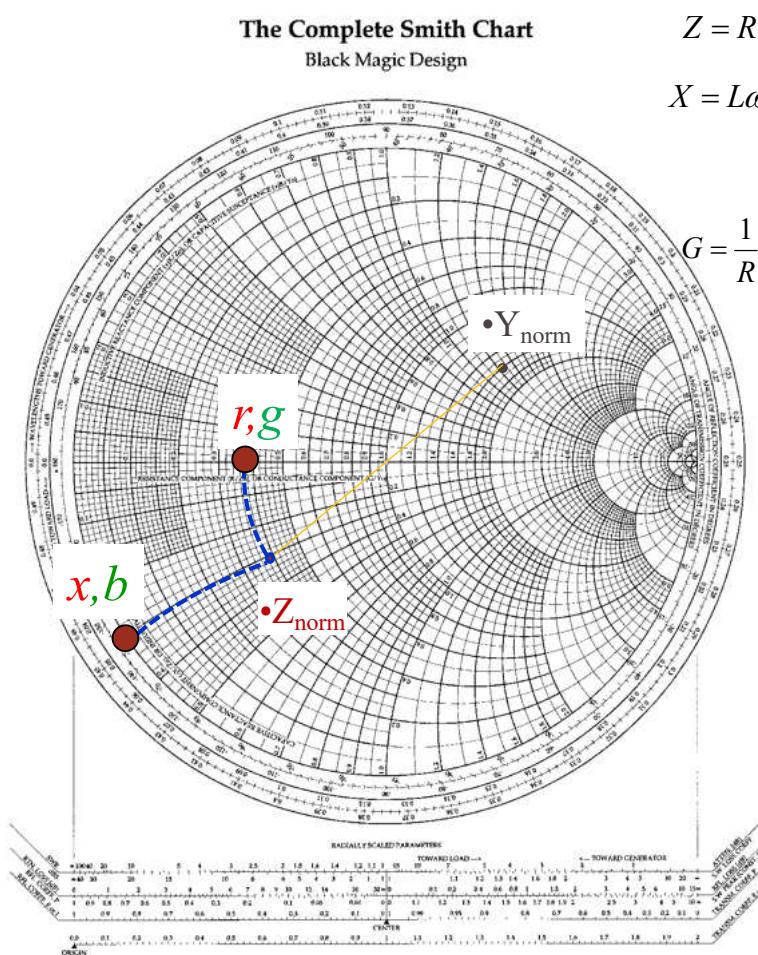
If the Quality Factors are lower than 3, the approximated transformation is not possible. Use the complete formulas (T22).

Impedance matching network can be calculated with the smith chart.



Exercise

- Calculate the LC network to perform power matching at the input of the IC at 2GHz. (First check that $Q < 3$ and use the Smith)



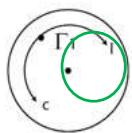
$$Z = R + jX = Z_0r + jZ_0x$$

$$X = L\omega = Z_0x \quad ou \quad X = -1/C\omega = Z_0x$$

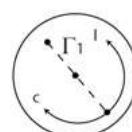
$$Y = G + jB = \frac{1}{Z} = \frac{g}{Z_0} + j \frac{b}{Z_0}$$

$$G = \frac{1}{R} = \frac{g}{Z_0} \quad ; \quad B = \frac{1}{L\omega} = \frac{b}{Z_0} \quad ou \quad B = C\omega = \frac{b}{Z_0}$$

Serial components
($R=cte$ circles)

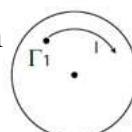


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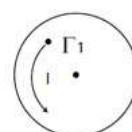


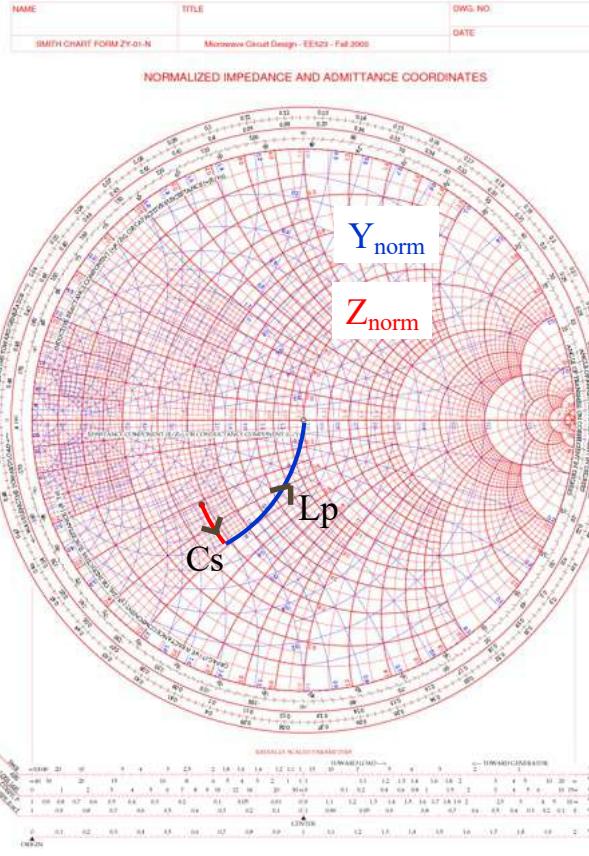
Serial quarter length TL

(constant circle with origine at the Smith chart center - toward generator)



quarter length stub
(constant circle with origine at the Smith chart center)





$$Y_{\text{norm}} = g + jb = (Z_0/R) + j(Z_0\omega C) = 1.66 + j1.25$$

$$Z_{\text{norm}} = r + jx = 0.38 - j0.29 \quad \Leftrightarrow$$

Chart or Calculus

Zsmith

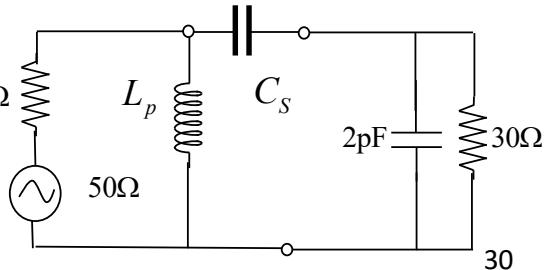
$$x_c = -0.3 - (-0.5) = 0.2$$

$$\frac{1}{C_s \omega} = Z_0 x_c \rightarrow C_s = \frac{1}{50.0, 2.2\pi \cdot 2.10^9} = 7.9 \text{ pF}$$

Ysmith

$$b_L = 1.3$$

$$\frac{1}{L_p \omega} = \frac{b_L}{Z_0} \rightarrow L_p = \frac{50}{b_L * \omega} = 3.1 \text{ nH}$$



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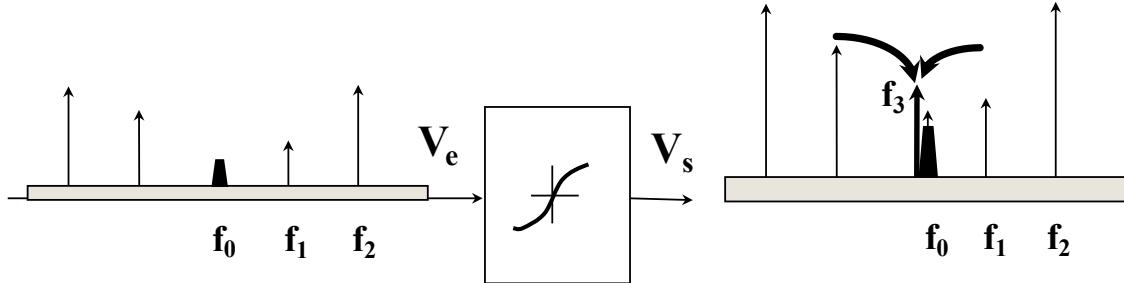
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➤ Packaging RFIC

Non-Linearity Effects

A first issue

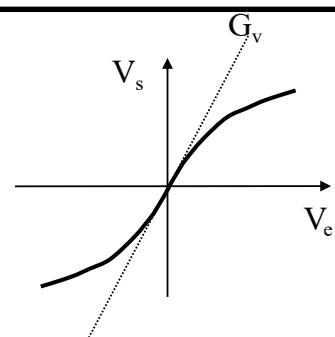
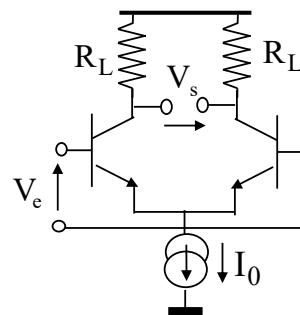


Blockers (adjacent channels, spurious, other stds, ...) generate harmonic frequencies which fall , after linear combination, in the received channel. This effect is called **Jamming**.

In the figure, f_3 is given by : $f_3 = 2.f_1 - f_2$

Non-Linearity Effects

Exemple of a differential amplifier



Non-linear odd transfert function

$$V_s = f(V_e) = 2R_L I_0 \cdot \operatorname{arctg} \left(\frac{V_e}{2V_T} \right) \xrightarrow{\text{Small } V_e} V_s \cong G_v V_e + \alpha_3 V_e^3 + \dots$$

$$V_T = \frac{kT}{q} = 25mV \text{ à } 27^\circ C$$

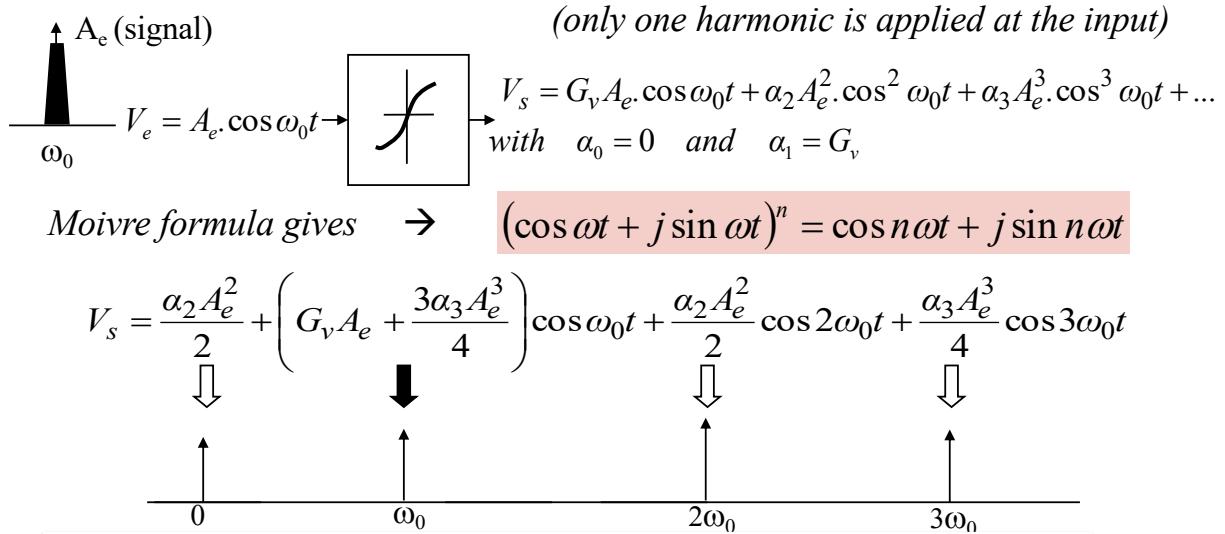
$$\operatorname{Arctg}(x)_{x \rightarrow 0} \approx x - \frac{x^3}{3} + \frac{x^5}{5}$$

$$\text{Hence : } \begin{cases} G_v = \frac{R_L I_0}{V_T} & \text{Small signal AC gain} \\ \alpha_3 = -\frac{1}{3} \frac{2R_L I_0}{(2V_T)^3} = -\frac{1}{12} \frac{R_L I_0}{V_T^3} & \end{cases}$$

Non-Linearity Effects

General case : $V_s = f(V_e) = \underbrace{\alpha_0}_{\text{DC}} + \underbrace{\alpha_1 V_e}_{\text{AC (Gv - small signal)}} + \alpha_2 V_e^2 + \alpha_3 V_e^3 + \dots$ Limited to the 3rd order

A – Harmonic distortion and Gain compression



⇒ Effect 1 : Generation of harmonics which can easily be filtered

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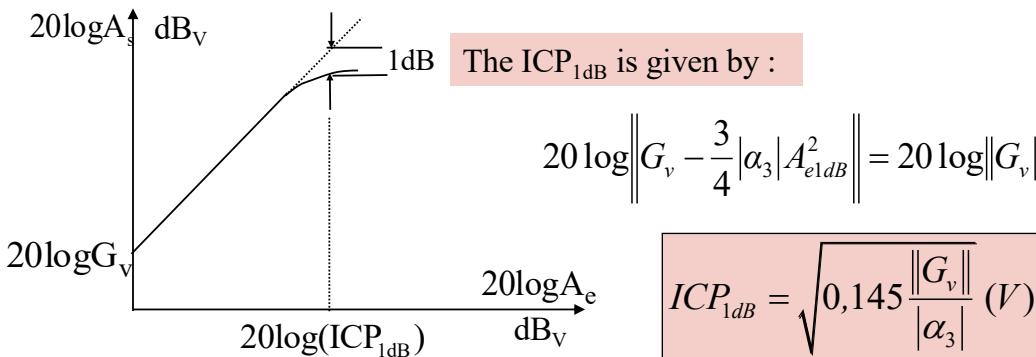
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Non-Linearity Effects

⇒ Effect 2 : Gain Compression (1dB Input Compression Point ICP_{1dB})

The magnitude (A_s) of the fundamental harmonic at the output is a non-linear function of the input signal amplitude A_e : The ICP_{1dB} is the value of A_e for which the gain is reduced of 1dB.

$$A_s = G_v A_e + \frac{3\alpha_3 A_e^3}{4} \quad \text{with } \alpha_3 < 0 \text{ (most cases)} \Rightarrow \text{the gain is reduced: } G_v \rightarrow G_v - \frac{3}{4} |\alpha_3| A_e^2$$



Exercise : Calculate the magnitude ICP_{1dB} at the input of the differential pair

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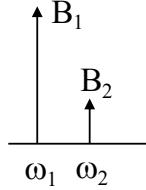
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Non-Linearity Effects

B – Intermodulation distortion

(2 harmonic frequencies are applied at the input of the NL device)



$$V_e = B_2 \cos \omega_2 t + B_1 \cos \omega_1 t \rightarrow \boxed{\text{NL Device}} \rightarrow V_s = f(V_e) = \alpha_0 + \alpha_1 V_e + \alpha_2 V_e^2 + \alpha_3 V_e^3 + \dots$$

DC

$$V_s = \alpha_0 + \frac{1}{2} \alpha_2 (B_2^2 + B_1^2)$$

Fond.

$$+ \left(G_v B_2 + \frac{3}{4} \alpha_3 B_2^3 + \frac{3}{2} \alpha_3 B_2 B_1^2 \right) \cos \omega_2 t + \left(G_v B_1 + \frac{3}{4} \alpha_3 B_1^3 + \frac{3}{2} \alpha_3 B_2^2 B_1 \right) \cos \omega_1 t$$

Hn

$$+ \frac{1}{2} \alpha_2 B_2^2 \cos 2\omega_2 t + \frac{1}{2} \alpha_2 B_1^2 \cos 2\omega_1 t + \frac{1}{4} \alpha_3 B_2^3 \cos 3\omega_2 t + \frac{1}{4} \alpha_3 B_1^3 \cos 3\omega_1 t + \dots$$

IM2

$$+ \alpha_2 B_2 B_1 \cos(\omega_2 t \pm \omega_1 t)$$

IM3

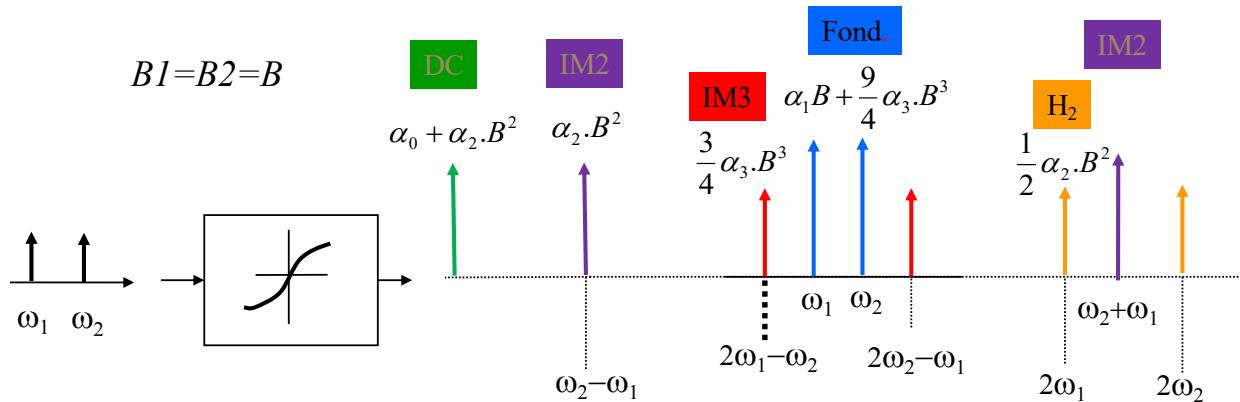
$$+ \frac{3}{4} \alpha_3 B_2^2 B_1 \cos(2\omega_2 t \pm \omega_1 t) + \frac{3}{4} \alpha_3 B_2 B_1^2 \cos(\omega_2 t \pm 2\omega_1 t)$$

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Non-Linearity Effects

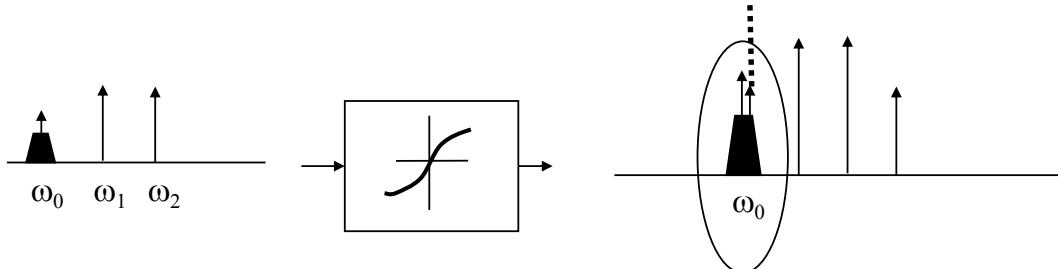


- The IMn occurs at frequencies: $n=p+m$ with $(m.\omega_1 +/- p.\omega_2) !!!$
- The IM3 can not be filtered because they fallback into the signal spectrum

Non-Linearity Effects

⇒ Effect 1 - Blocking due to interferer

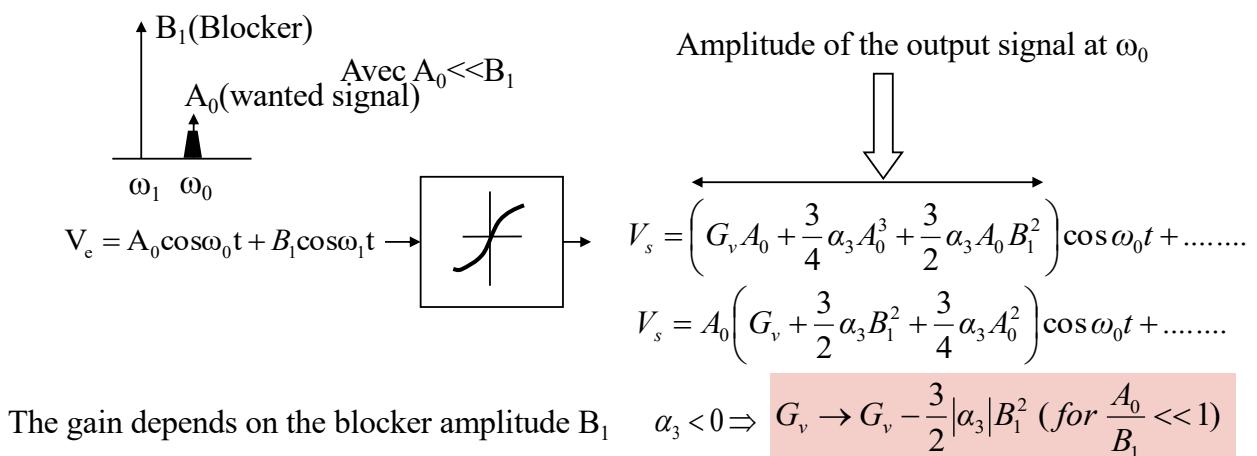
ω_2 and ω_1 are interferers (blockers) closed to the wanted signal (ω_0)



If $(2\omega_2 - \omega_1)$ fall into the spectrum of the wanted signal, a blocking occurs due to the intermodulation $(2\omega_1 - \omega_2)$ of the two blockers

Non-Linearity Effects

⇒ Effet 2 – Desensitization of the gain

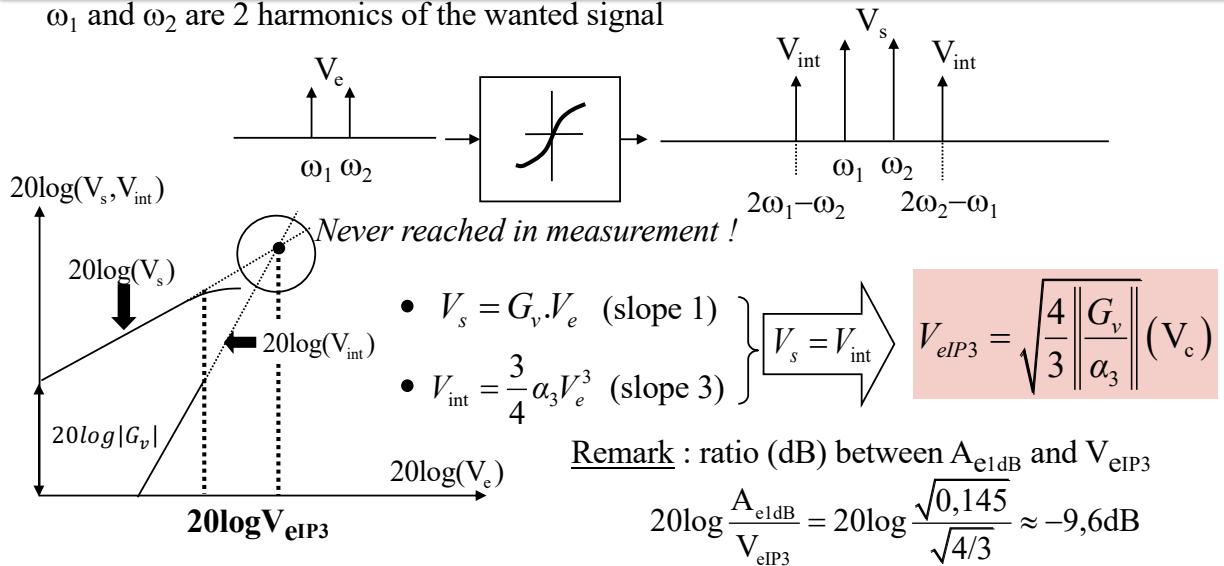


The gain decreases when B_1 increases.
The gain is blocked by the interferer (blocker) B_1

Non-Linearity Effects

⇒ Effet 3 – Intermodulation, B_{eIP3} ($IIP3 \ll 3rd\ order\ Input\ Interception\ Point$) »

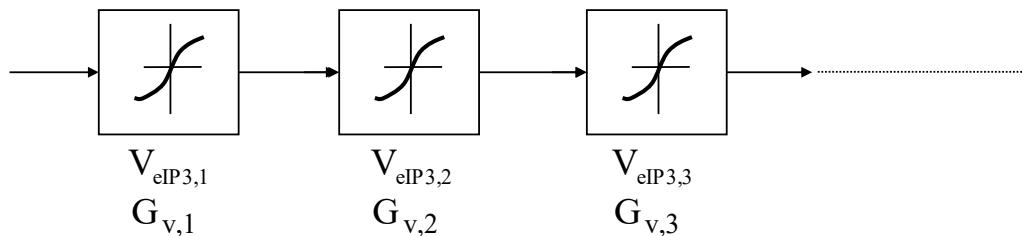
ω_1 and ω_2 are 2 harmonics of the wanted signal



The IIP3 (V_{eIP3}) is the input signal level for which the output IM3 is equaling the fundamental harmonic (V_s) extrapolated from small signal (AC).

Non-Linearity Effects

C - IIP3 of a chained devices (G_v =loaded voltage gain and V_{eIP3} =IIP3 (V)) :



It is demonstrated that :

$$\frac{1}{V_{eIP3}^2} = \frac{1}{V_{eIP3,1}^2} + \frac{G_{v,1}^2}{V_{eIP3,2}^2} + \frac{G_{v,1}^2 \cdot G_{v,2}^2}{V_{eIP3,3}^2} + \dots$$

If all the stages have $G_v > 1$, then the IIP3 of the last stage before digital conversion is the most critical

Non-Linearity Effects

Exercise : calculate the output signal to in band blocker ratio (after IM) for a signal of $1\mu V$ level and 2 blockers having an amplitude of $60dBc$ at the input of an amplifier having $IIP3 = B_{eIP3} = 70mV$?

$$S_o = G_v \cdot S_i$$

$$B_o = \frac{3}{4} a_3 \cdot B_i^3 = \frac{3}{4} a_3 \cdot (10^3 S_i)^3$$

$$\frac{S_o}{B_o} = \frac{4 \cdot G_v \cdot S_i}{3 \cdot a_3 \cdot (10^3 S_i)^3} = \frac{IIP_3^2}{10^9 \cdot S_i^2} = \frac{(70 \cdot 10^{-3})^2}{10^9 \cdot 10^{-12}} = 4,9 = 20 \log(4,9) dB = 13 dB$$

Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

Noise – Basis on signal theory

- Different class of signal :
 - Deterministic / Random
 - Continuous (analog) / Discret (digital)
 - Power / Energy

$$E = \int_{-\infty}^{+\infty} |x(t)|^2 dt \quad P = \lim_{T \rightarrow \infty} \frac{1}{2T} \int_{-T}^{+T} |x(t)|^2 dt$$

Energy signal ($0 < E < \infty$):
(burst, square, ...)

$$e(t) \xleftrightarrow{\text{TF}} e(f)$$

$$ESD = |e(f)|^2 (V^2 / \sqrt{\text{Hz}})$$

$$E = \int |e(f)|^2 df (J)$$

RFIC

Power signal ($0 < P < \infty$):
(sine, noise, bit sequence ...)

$$e(t) \xleftrightarrow{\text{TF}} e(f)$$

$$PSD = |e(f)|^2 (V^2 / \text{Hz})$$

$$P = \int |e(f)|^2 df (V^2; W|_{\Omega})$$

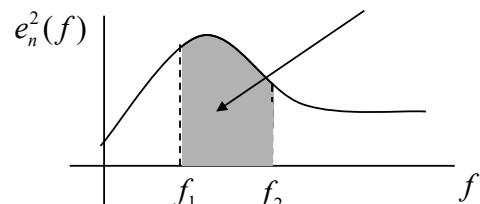
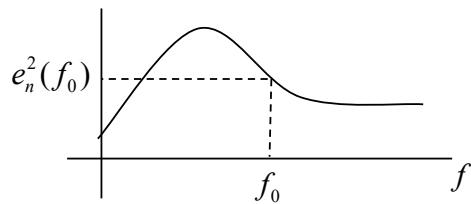
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Noise – Basis on noise in electronics

Noise is a continuous power random signal:

- Undefined in time domain
- Defined in frequency domain by the spectral density $e_n^2(f)$ in V²/Hz



~~$$V_n = \lim_{T \rightarrow \infty} \sqrt{\frac{1}{2T} \int_{-T}^{+T} e^2(t) dt}$$~~

The RMS voltage of the noise is given for $\Delta f = f_2 - f_1$ by :

$$V_n = \sqrt{\int_{f_1}^{f_2} e_n^2(f) df} \quad (\text{in Volt})$$

The power delivered to a resistive load (R) by a noise source of V_n RMS voltage is :

$$P_n = \frac{V_n^2}{R} = \frac{1}{R} \int_{f_1}^{f_2} e_n^2(f) df \quad (\text{in Watt})$$

RFIC

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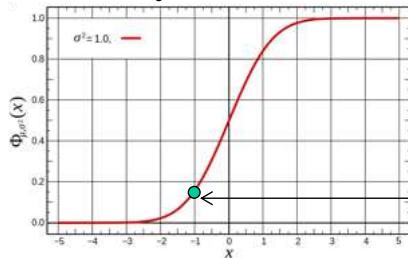
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Noise – Statistics on noise in electronics

Gaussian noise (white noise)

Cumulative Density Function

$$F_n(a) = \int f_n(a) = p(n < a)$$



$$p(n < -a) = p(n > a)$$

$$p(n > a) = Q(a) = 1 - Q(-a) = \frac{1}{\sqrt{2\pi}} \int_a^\infty \exp\left(-\frac{a^2}{2}\right) da$$

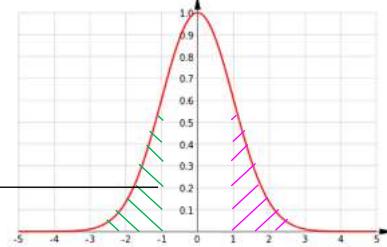
Mean Value:

$$\mu = \bar{\varepsilon}_q = E[x] = \int_{-\infty}^{+\infty} a \cdot f_x(a) da$$

Système RF Intégré

Density Function

$$f_n(a) = d \frac{F_n(a)}{da} \approx p(n = a)$$



RMS Value:

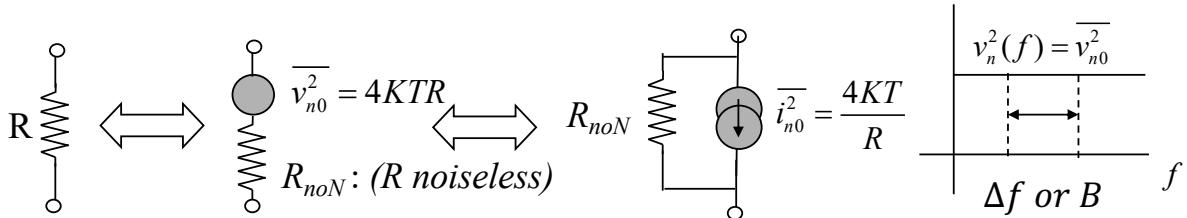
$$\sigma^2 = \bar{\varepsilon}_x^2 = E[x^2] = \int_{-\infty}^{+\infty} a^2 \cdot f_x(a) da$$

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Noise – Basis on noise in electronics

• Noise in resistors (white noise)



$$V_{nR}(\Delta f) = \sqrt{\int_{\Delta f} v_n^2(f) df} = \sqrt{v_n^2₀ \cdot \Delta f} = \sqrt{4KTR \cdot \Delta f}$$

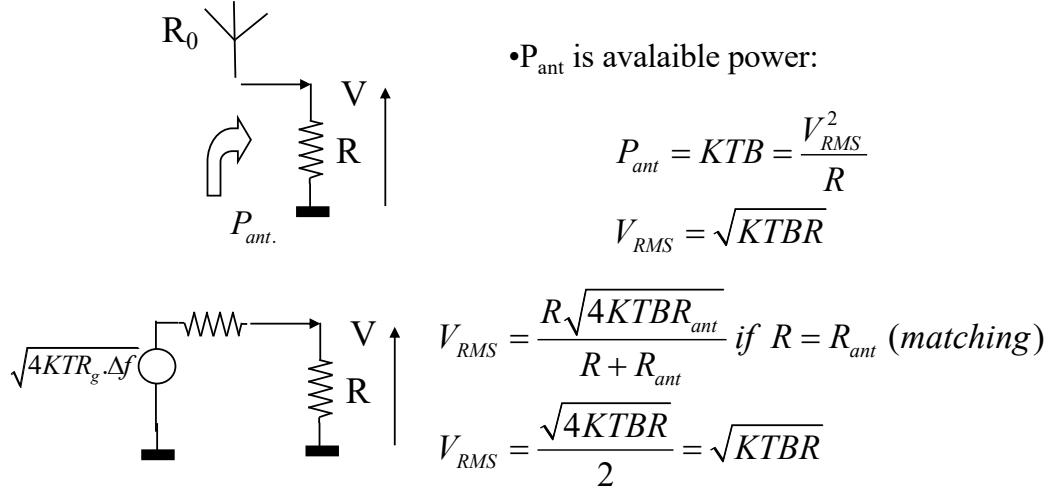
with $4KT=1,65 \cdot 10^{-20} \text{ J}$ à 27°C

Note 1 : Active devices have also noise sources

Note 2 : The available noise power of an antenna is KTB with $T=290,5^\circ\text{K}$

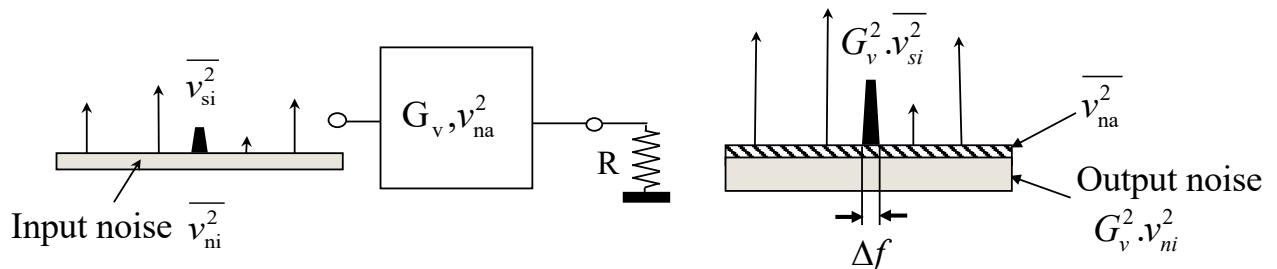
Bruit – Sensibilité & Dynamique

- Exercise : show that the available noise power of an antenna is equal to the noise of a resistor heated at 290,5°K)



Noise – Added noise by a stage

Note: Since the noise is defined by its Power Spectral Density (PSD), we consider the PSD of the noise $v_{ni}^2(f)$ and the PSD of the signal $v_{si}^2(f)$. The study is done on a spectral domain of Δf which is signal bandwidth.



The stage adds its own noise $\overline{v_{na}^2}$: the signal to noise ratio is reduced : $S/N = \frac{P_{Signal}}{P_{Noise}}$

$$(S/N)_{o,\Delta f} = \frac{G_v^2 \cdot \frac{1}{R} \cdot \int_{\Delta f} v_{si}^2(f) df}{G_v^2 \cdot \frac{1}{R} \int_{\Delta f} v_{ni}^2(f) df + \frac{1}{R} \int_{\Delta f} v_{na}^2(f) df} = \frac{\overline{v_{si}^2}}{\overline{v_{ni}^2} + \frac{\overline{v_{na}^2}}{G_v^2}} < (S/N)_{i,\Delta f} = \frac{\overline{v_{si}^2}_{RMS}}{\overline{v_{ni}^2}_{RMS}} = \frac{V_{si_RMS}^2}{V_{ni_RMS}^2}$$

Noise – Noise Figure (F)

F is the signal to noise ratio dégradation (Eq. 1).

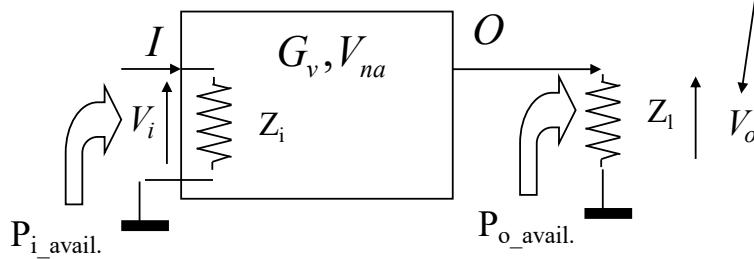
$$F = \frac{(S/N)_i}{(S/N)_o} \quad (1)$$

Note : The Noise Figure (NF) is the Noise Factor expressed in dB

F is evaluated on the basis of available power:

$$F = \frac{P_{si}}{P_{ni}} \cdot \frac{P_{no}}{P_{so}} = \frac{V_{si}^2}{Z_i} \frac{Z_i}{V_{ni}^2} \frac{V_{no}^2}{Z_l} \frac{Z_l}{V_{so}^2}$$

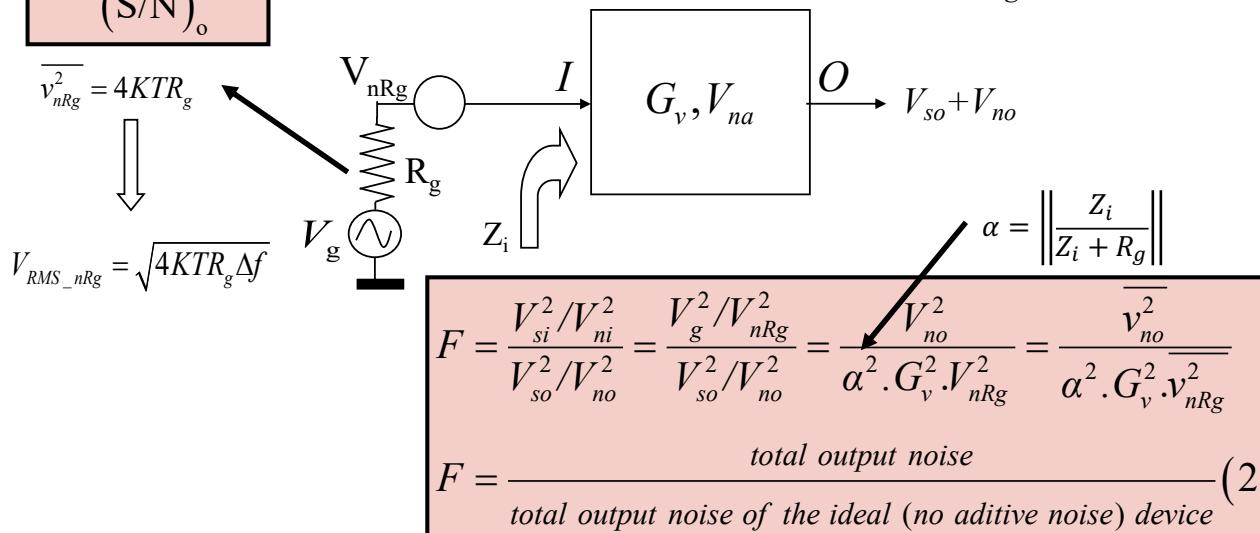
RMS values or magnitude can be considered



Noise – Noise Figure (F)

$$F = \frac{(S/N)_i}{(S/N)_o} \quad (1)$$

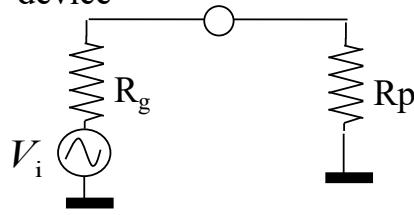
NF also express the quantity of noise added by the stage regarding the noise delivered by the source (R_g) on Δf . (Eq. 2)



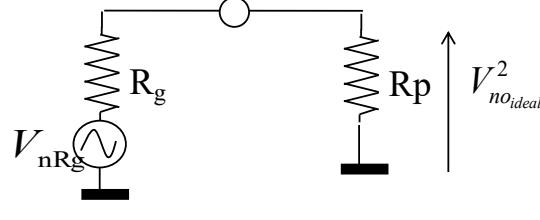
Exercises :

- 1- Give the F of a resistive divider R_g/R_P
- 2- Give $(S/B)_o$ when the BW of the device is $>$ the BW Δf of the signal
- 3- Establish (2) based upon (1)

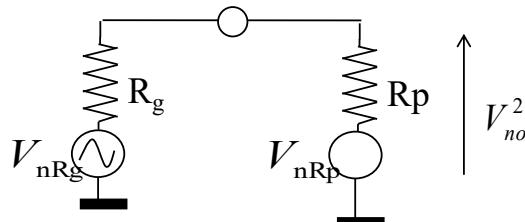
F of a resistive divider R_g/R_p



•Idéal device



•Non-ideal device



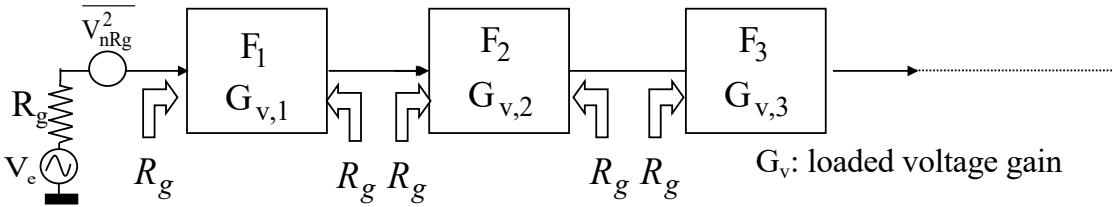
$$F = \frac{V_{no}^2}{V_{no_{ideal}}^2} = \frac{\left(\frac{R_p}{R_p + R_g} \right)^2 V_{nRg}^2 + \left(\frac{R_g}{R_p + R_g} \right)^2 V_{nRp}^2}{\left(\frac{R_p}{R_p + R_g} \right)^2 V_{nRg}^2} = 1 + \left(\frac{R_g}{R_p} \right)^2 \frac{V_{nRp}^2}{V_{nRg}^2} = 2 \quad (\text{if } R_p = R_g)$$

2- $(S/B)_S$ when the BW of the device is > the BW Δf of the signal

$$(S/N)_{o,\Delta f} = \frac{G_v^2 \frac{1}{R} \int_{\Delta f} e_{si}^2 \cdot df}{G_v^2 \frac{1}{R} \int_{\Delta f} e_{ni}^2 \cdot df + \frac{1}{R} \int_{\Delta f} e_{na}^2 \cdot df} = \frac{e_{si}^2}{e_{ni}^2 + \frac{e_{na}^2}{G_v^2}}$$

$$(S/N)_{o,B_{dev}} = \frac{G_v^2 \frac{1}{R} \int_{\Delta f} e_{si}^2 \cdot df}{G_v^2 \frac{1}{R} \int_{B_{dev}} e_{ni}^2 \cdot df + \frac{1}{R} \int_{B_{dev}} e_{na}^2 \cdot df} = \frac{\frac{e_{si}^2 \cdot \Delta f}{e_{ni}^2 \cdot B_{dev} + \frac{e_{na}^2 \cdot B_{dev}}{G_v^2}}}{\frac{e_{si}^2 \cdot \Delta f}{B_{dev}}} = \frac{\Delta f}{B_{dev}} (S/N)_{o,\Delta f}$$

Noise – Friss Formula



$$F = F_1 + \frac{(F_2 - 1)}{G_{v,1}^2} + \frac{(F_3 - 1)}{G_{v,1}^2 \cdot G_{v,2}^2} + \dots$$

This formula is valid only for real impedances
and in case of power matching:
($Z_s = Z_e = R_g$)

In RFIC, impedances are complex and never equal. This formula cannot be used as is.
However, the following statements remain valid in RFIC.

The gain of the first stages reduces the NF of the following ones.

- => The receiver chain must start by amplifiers
- => The NF of the first stage must be as low as possible

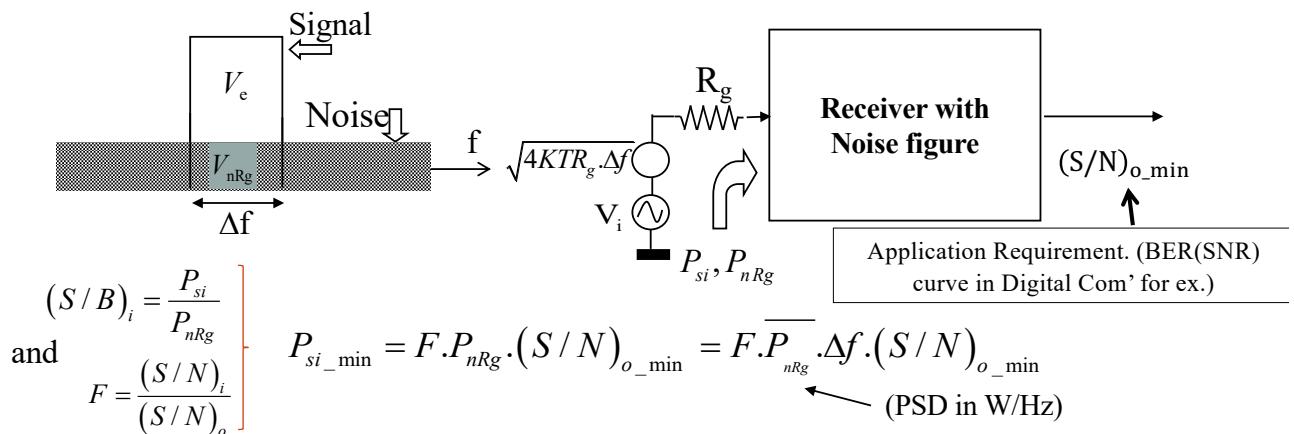


LNA

Note that lossy stages ($G_v < 1$) increase the NF, especially when they are in front of the receiver chain (antenna filter, image rejection filter, antenna switch).

Noise – Sensitivity & Dynamic

A- Receiver Sensitivity: minimum input power (P_{si_min}) which can be detected by the receiver for a given output signal to noise ratio (S/N)_{o_min})



or $P_{si_min} = F(dB) + PSD_{NRG}(dBm) + 10\log(\Delta_f) + (S/N)_{o_min} \text{ (dB)}$

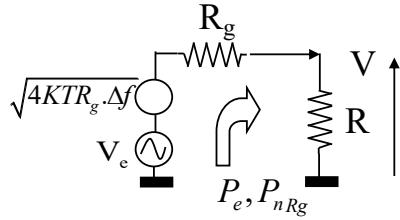
Input Noise Floor: $P_{NFi} = P_{no}/G_p$

Exercise : Give the expression of P_{nRg} in the case of input matching

Exercise : demonstrate : $P_{NFi} = F + PSD_{nRg} + 10\log(\Delta f)$

Bruit – Sensibilité & Dynamique

Exercise : Give the expression of P_{nRg} in the case of input matching



• P_e and P_{nRg} are available power:

$$\begin{aligned} P_{nRg} &= \frac{V_{RMS}^2}{R} = \frac{1}{R} \left(\frac{R\sqrt{4.K.T.Rg.\Delta f}}{R_g + R} \right)^2 \\ &= K.T.\Delta f(W) = N_0 B \quad \text{si } R_g = R \text{ (matching)} \\ &= 10.\log(K.T.10^3)(dBm) + 10\log(\Delta f) \\ &= -174dBm + 10\log(\Delta f) \end{aligned}$$

Exercise : demonstrate :

$$P_{NFi} = F + D S P_{nRg} + 10\log(\Delta f)$$

$$P_{NFe} = \frac{P_{Ns}}{G_p} = \frac{G_p P_{Ne} + P_{Na}}{G_p} = P_{Ne} + \frac{P_{Na}}{G_p}$$

$$F = \frac{P_{Se}}{P_{Ne}} \cdot \frac{P_{Ns}}{P_{Ss}} = \frac{P_{Se}}{P_{Ne}} \frac{G_p P_{Ne} + P_{Na}}{G_p P_{Se}} = 1 + \frac{P_{Na}}{P_{Ne} G_p}$$

$$P_{Ne} \cdot F = P_{Ne} \cdot \left(1 + \frac{P_{Na}}{P_{Ne} G_p} \right) = P_{NFe}$$

RFIC

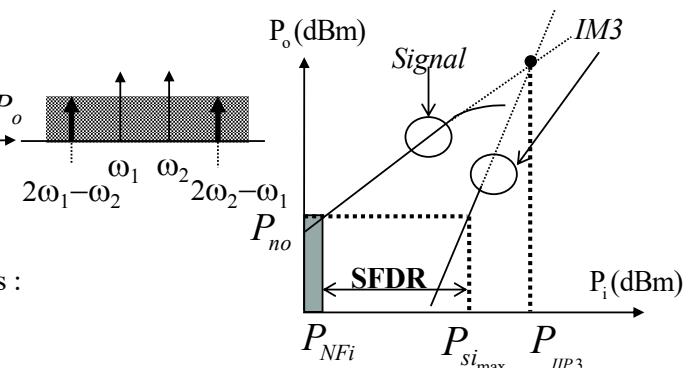
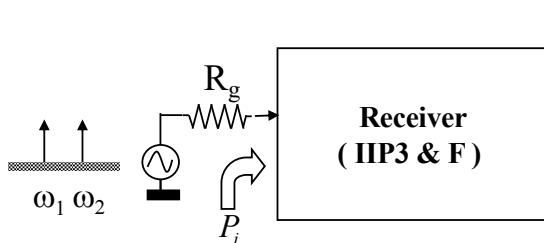
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Noise – Sensitivity & Dynamic

B –Dynamic and SFDR :

$$Dyn = P_{si_{max}} / P_{si_{min}}$$

$P_{si_{max}}$ is the power of two blockers which give by 3rd order intermodulation an output IM3 equal to the output noise floor (P_{no}).



Due to relative slope (1 and 3) of the two curves :

$$P_{si_{max}}(dBm) = \frac{2P_{IIP3}(dBm) + P_{NFi}(dBm)}{3}$$

$$\begin{aligned} Dyn(dB) &= P_{si_{max}}(dBm) - P_{si_{min}}(dBm) = 2 \frac{P_{IIP3}(dBm) - P_{NFi}(dBm)}{3} - (S/N)_0 (dB) \\ SFDR &= P_{si_{max}}(dBm) - P_{NFi}(dBm) \end{aligned}$$

Exercice : Calculate Dyn for $P_{eIIP3} = -15dBm$, $F = 9dB$, $(S/B)o = 12dB$ et $BW = 200kHz$
in the case of input power matching

RFIC

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Outline

➤ Analog RF signal processing basis

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- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

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- Passive devices (resistors, capacitors, inductors)

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- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

➤ Packaging

RFIC

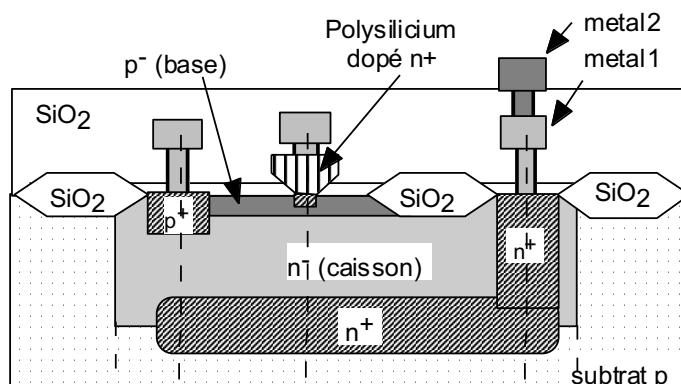
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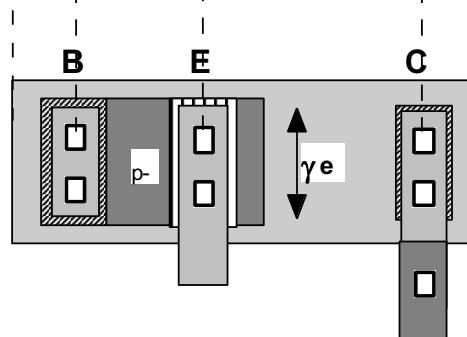
Technology

Active devices: BIPOLAR

Technological
Cutting



Layout

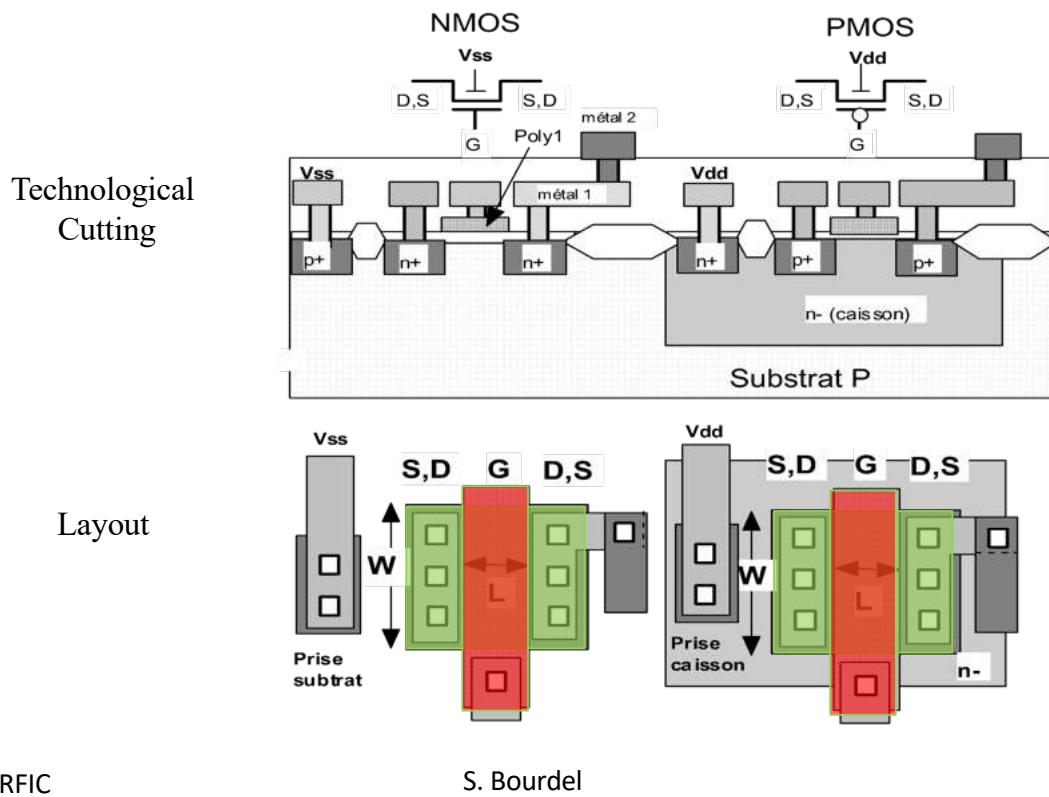


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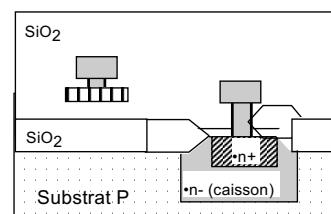
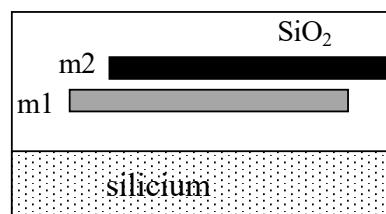
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Active devices: MOSFET



Passive devices: CAPACITOR

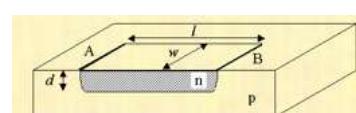
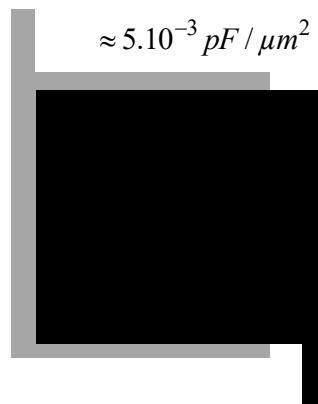
Technological
Cutting



MIM Capacitor

$$\approx 5.10^{-3} \text{ pF} / \mu\text{m}^2$$

Layout

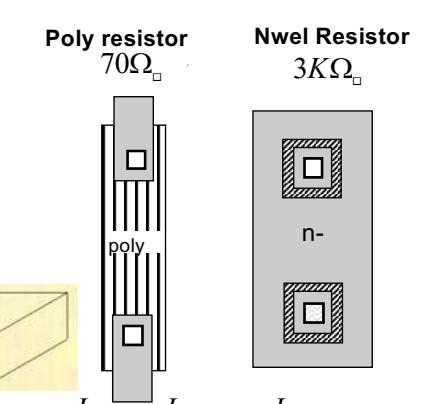


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Poly resistor $70\Omega_{\square}$

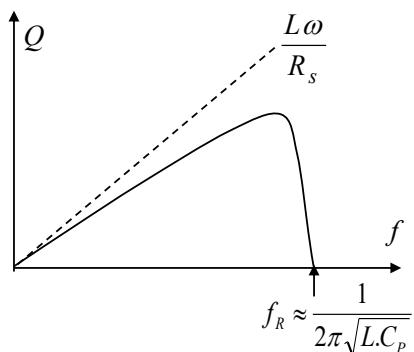
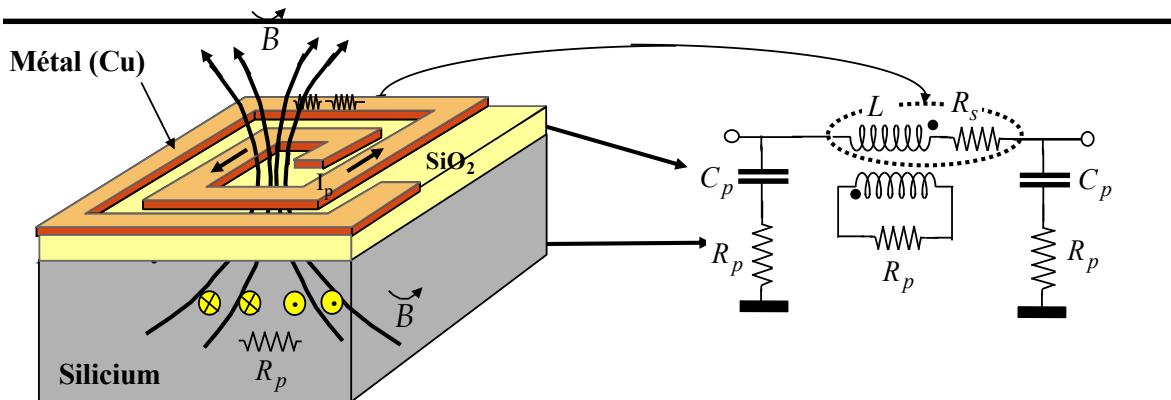
Nwell Resistor $3K\Omega_{\square}$



$$R_{AB} = \rho \frac{L}{S} = \rho \frac{L}{W.d} = R_{\square} \cdot \frac{L}{W}$$

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Passive devices: INDUCTORS



RFIC

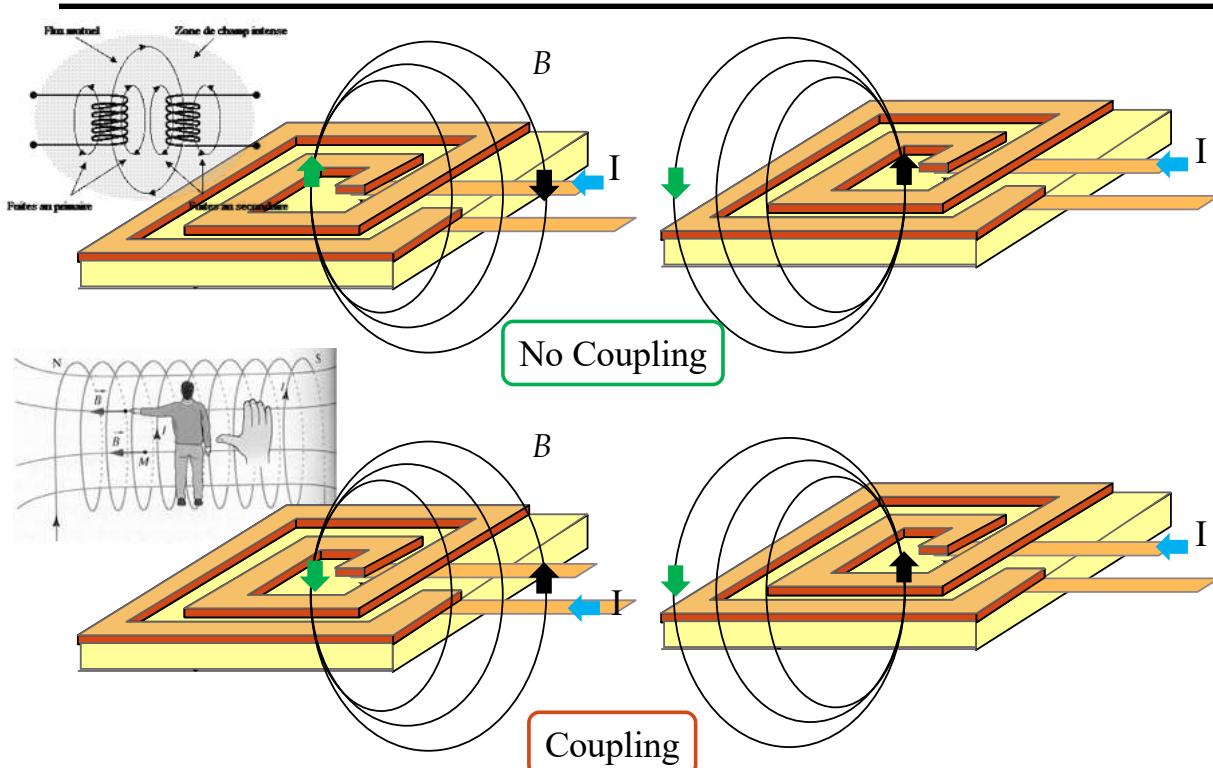
Budget Losses

- Joule effect : Losses due to serial resistance R_s .
- Losses in R_p due to induced current in the substrate by the magnetic field which lower the Q factor.
- Losses due to R_p by coupling across C_p . These losses increase with f and lower the Q factor.

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Passive devices: INDUCTORS

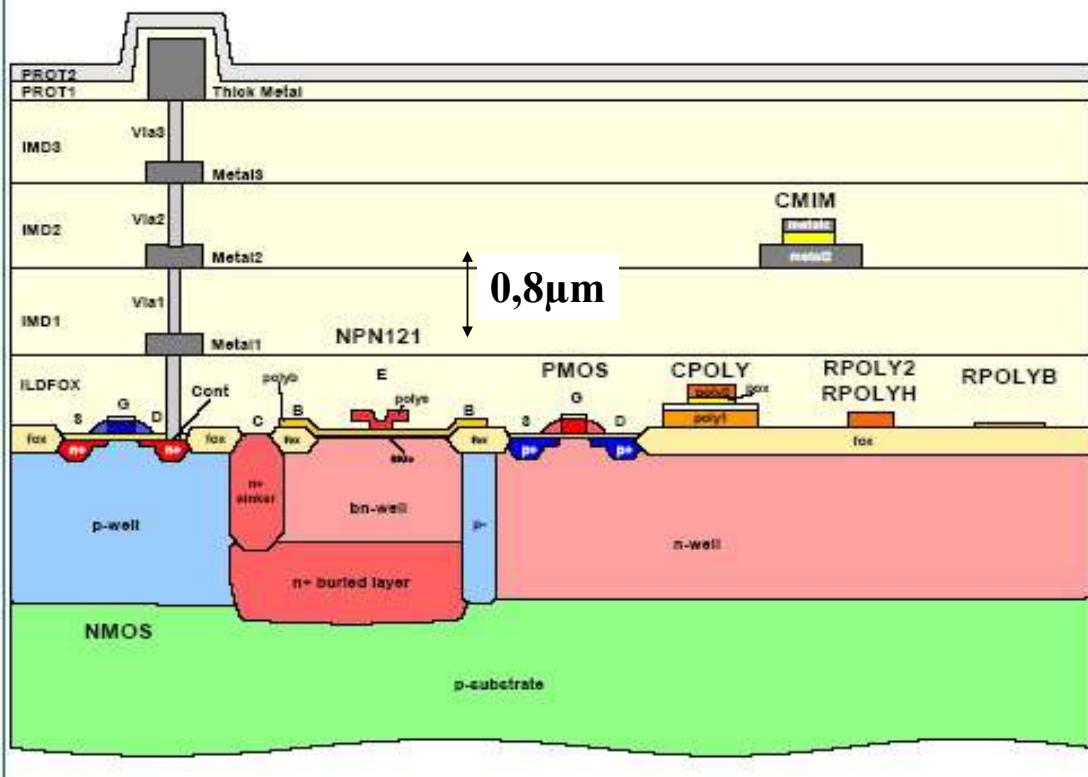


RFIC

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AMS BiCMOS(SiGe) 0,35µm Technology



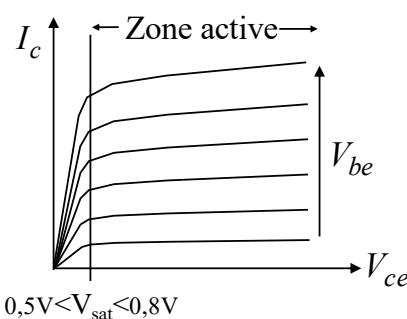
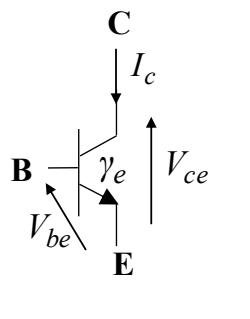
RFIC

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Active devices: BIPOLEAR

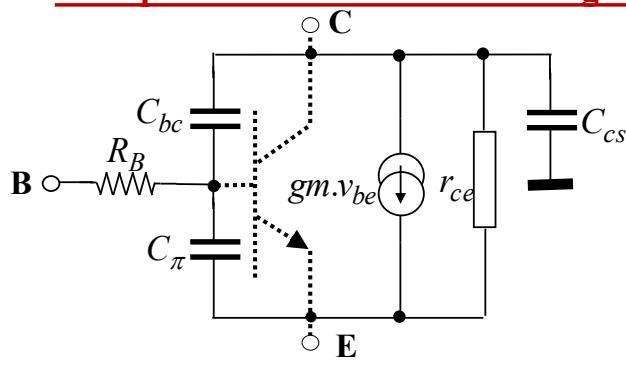
A – Static current in active region (saturation)



$$I_c = I_s \exp \frac{V_{be}}{V_T} \left(1 + \frac{V_{ce}}{V_A} \right)$$

avec : $I_s \propto \gamma_e$

B – Equivalent Scheme in active region (RF model)



$$\begin{aligned} C_{bc}, C_{cs}, C_{be} &\propto \gamma_e \text{ et } R_B \propto \frac{1}{\gamma_e} \\ C_\pi &= gm \cdot \tau_F + C_{be} \\ gm &= \frac{I_c}{V_T} = 40I_c (\text{à } 27^\circ\text{C}) \text{ et } r_{ce} = \frac{V_A}{I_c} \end{aligned}$$

$$f_T \equiv \frac{gm}{2\pi C_\pi} \quad (\text{for optimal } \gamma_e)$$

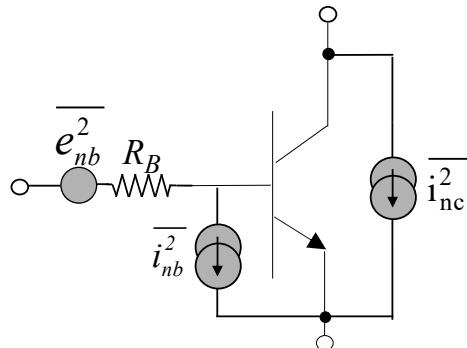
RFIC

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Active devices: BIOPOLAR

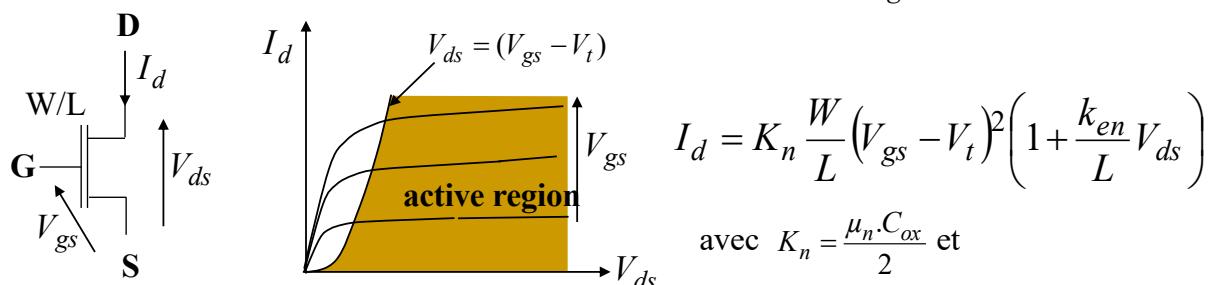
C – Noise sources



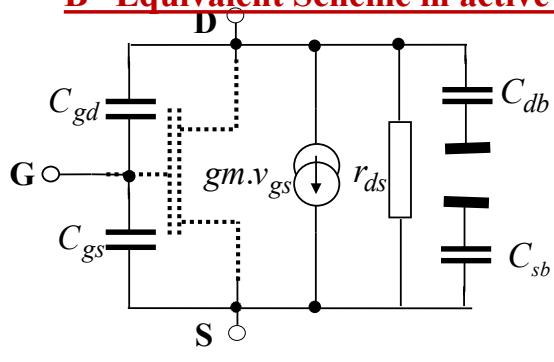
- Shotky Noise due to current in the collector (A^2/Hz) $\Rightarrow i_{nc}^2 = 2KTgm$
- Shotky Noise due to current in the base (A^2/Hz) $\Rightarrow i_{nb}^2 = 2KT \frac{gm}{\beta_0}$
- Thermal Noise due the base resistor (V^2/Hz) $\Rightarrow e_{nb}^2 = 4KTR_B$

Active devices: MOSFET

A – Static current in active region (saturation) $V_{ds} \geq (V_{gs} - V_t)$



B – Equivalent Scheme in active region (RF model)



$$C_{gd}, C_{gs}, C_{sb}, C_{db} \propto W$$

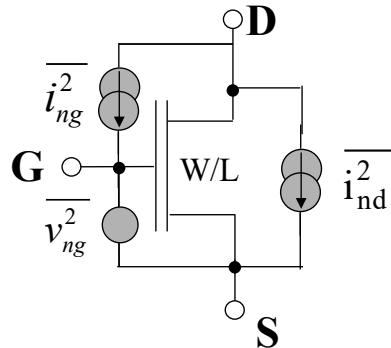
$$C_{gs} = \frac{2}{3} C_{ox} W L$$

$$gm = \frac{2I_d}{V_{gs} - V_t} = 2\sqrt{K_n \frac{W}{L} I_d} \text{ et } r_{ds} = \frac{L}{k_{en} \cdot I_d}$$

$$f_T \approx \frac{gm}{2\pi C_{gs}}$$

Active devices: MOSFET

C – Noise source in active region

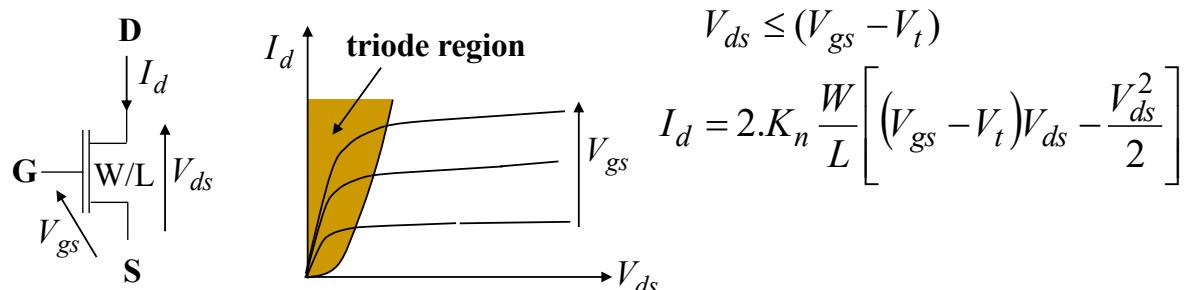


• K_f is a technological parameter
(can vary inside the process)

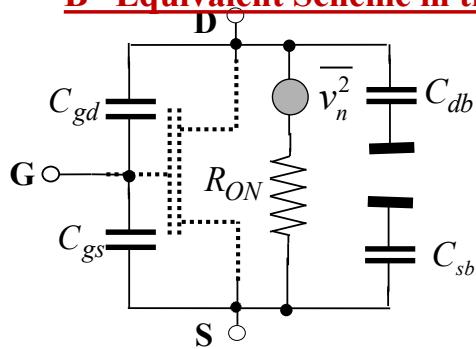
- Channel noise (A^2/Hz) $\Rightarrow \overline{i_{nd}^2} = 4KT\gamma g_m$ $(L > 1\mu\text{m}) \frac{2}{3} < \gamma < 2 (L \ll 1\mu\text{m})$
- 1/f Noise (V^2/Hz) $\Rightarrow \overline{v_{ng}^2} = \frac{K_f}{W.L.C_{ox}} \cdot \frac{1}{f}$ $(\downarrow \text{avec } W.L \text{ et PMOS})$
- Noise induced by the gate (A^2/Hz) $\Rightarrow \overline{i_{ng}^2} = \delta.4KT \frac{\omega^2 C_{gs}^2}{5.g_m} (L > 1\mu\text{m}) \frac{2}{3} < \delta < 2 (L \ll 1\mu\text{m})$

Active devices: MOSFET

A – Static current in triode region



B – Equivalent Scheme in triode region (RF model)



$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} W \cdot L$$

$$R_{ON} = \frac{1}{2K_n \frac{W}{L} (V_{gs} - V_t)} \quad \text{for low } V_{ds}$$

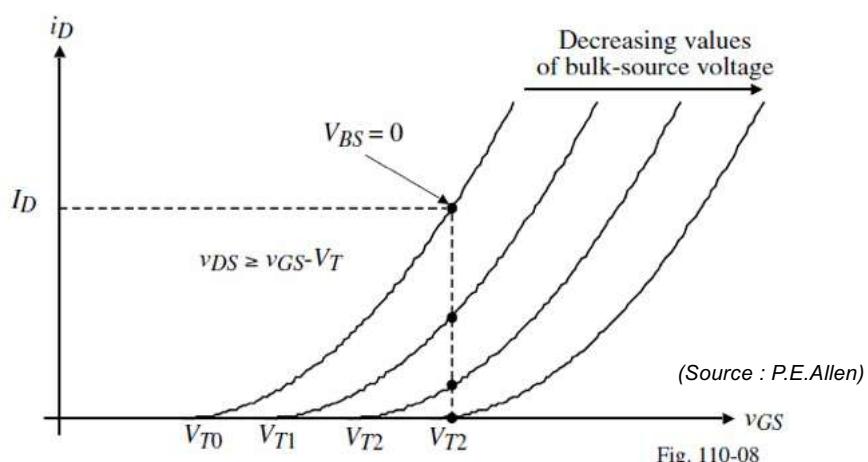
• Thermal noise of R_{ON} (V^2/Hz): $\overline{v_n^2} = 4KTR_{ON}$

Paramètres de la technologie C35 d'AMS (AustriaMicroSystems)

NMOS	PMOS
$K_N = \mu_n C_{OX} / 2 = 80 \mu\text{A/V}^2$	$K_P = \mu_p C_{OX} / 2 = 55 \mu\text{A/V}^2$
$K_{en} = 0,03 \mu\text{m/V}$ (avec $\lambda_n = k_{en}/L$)	$K_{ep} = 0,06 \mu\text{m/V}$ (avec $\lambda_p = k_{ep}/L$)
$V_{Tn0} = 0,57\text{V}$	$V_{Tp0} = -0,73\text{V}$

- $L_{min} = 0,35 \mu\text{m}$
- $\Delta L = 0,05 \mu\text{m}$
- $C_{OX} = 5,5 \text{ fF}/\mu\text{m}^2$
- $C_{DB} = C_{SB} = 1 \text{ fF}$ pour $W = 1 \mu\text{m}$

Si $V_{BS} \neq 0$: Effet substrat



$$V_{tn,p} = V_{tn,p0} + \gamma \sqrt{2|\phi_F| + |V_{BS}|} - \gamma \sqrt{2|\phi_F|} \quad \text{avec} \quad |\phi_F| = \left| \frac{kT}{q} \ln \left(\frac{N_{A,D}}{n_i} \right) \right|$$

En pratique on prendra : $V_{tn,p} \approx V_{tn,p0} + 0,2 V_{sb}$

Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

➤ Packaging

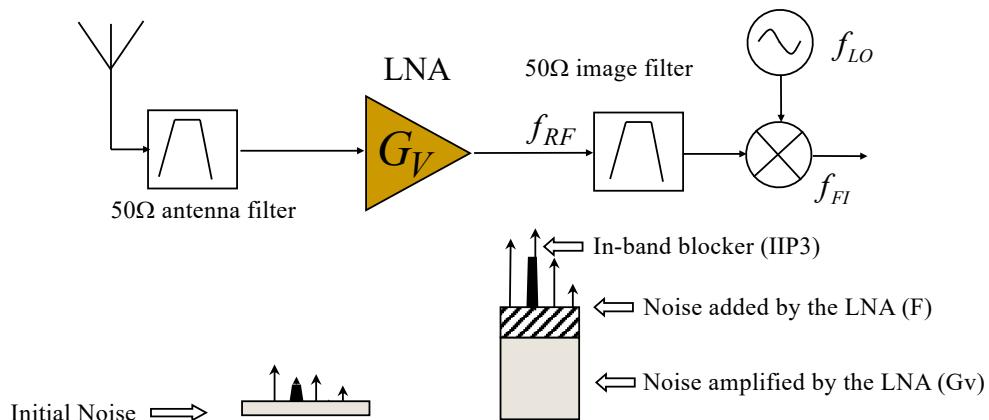
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Low Noise Amplifier

Requirements

LNA



Main issues for LNA design (heterodyne receiver):

- Low Noise Factor: first stage of the receiver chain (Friis formula)
- High IIP3 (high blocker at the receiver input)
- **Tradeoff for the gain:**
 - High gain to reduce the impact of the mixer NF and the losses in the image filter (Friss)
 - Low gain to lower the blockers at the mixer input
- Input and output impedance closed to 50 Ohm

Requirements

$NF_{dB} = 10 \log(F)$	< 2dB
IIP3 (dBm)	-10dBm
Direct Gain (S_{21})	15dB
Input and (output) impedance	50Ω
Reverse Gain	< -30dB
Stability :	$\Re(Z_e) \text{ et } \Re(Z_s) > 0 \quad \forall f$

Typical performances of LNA in a heterodyne receiver

How to find the best suited structures to achieve the best trade-off:

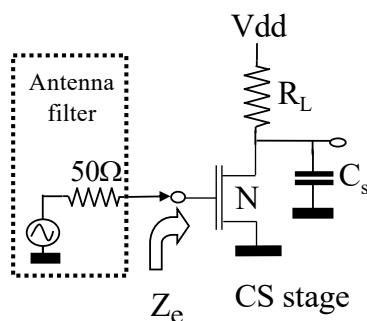
- Real impedances for power matching
- Low NF
- High linearity
- Low reverse gain (good output to input isolation)
- High direct gain (limited by NL in the mixer)
- Stability

Two main topologies: CS or CG based amplifier

(source follower ($G_v < 1$, $Z_e \gg$ and $Z_s \ll$) is used for matching inside the IC)

Low Noise Amplifier

Trade-off between input matching and Noise Factor



$$G_v = -\frac{g_m \cdot R_L}{1 + j \cdot f / f_c} \text{ with } f_c = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_s}$$

$$Z_{in} = \frac{-1}{C_{gs} \omega}$$

$$Z_{in} \neq Z_{ant}^* = 50\Omega$$

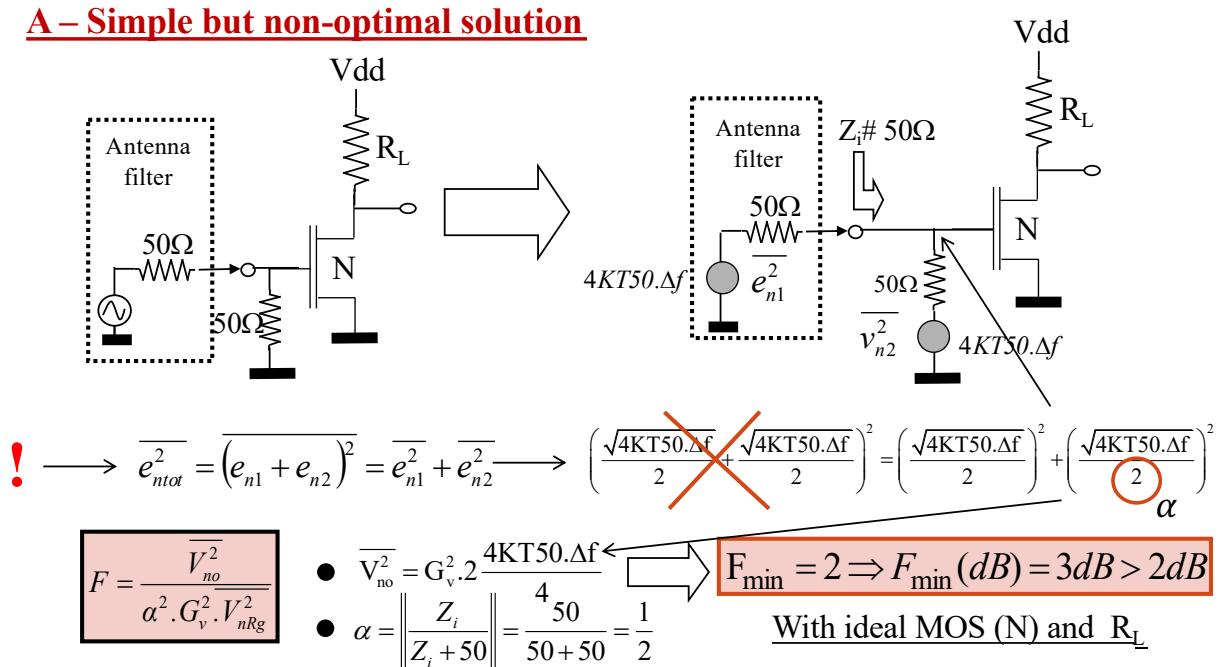
Input impedance Z_{in} is mainly capacitive and closed to $C_{gs}(N)$

Question : How can we synthesize a real impedance equal to 50Ω in parallel with the input capacitance C_e without adding noise ?

Low Noise Amplifier

Trade-off between input matching and Noise Factor

A – Simple but non-optimal solution

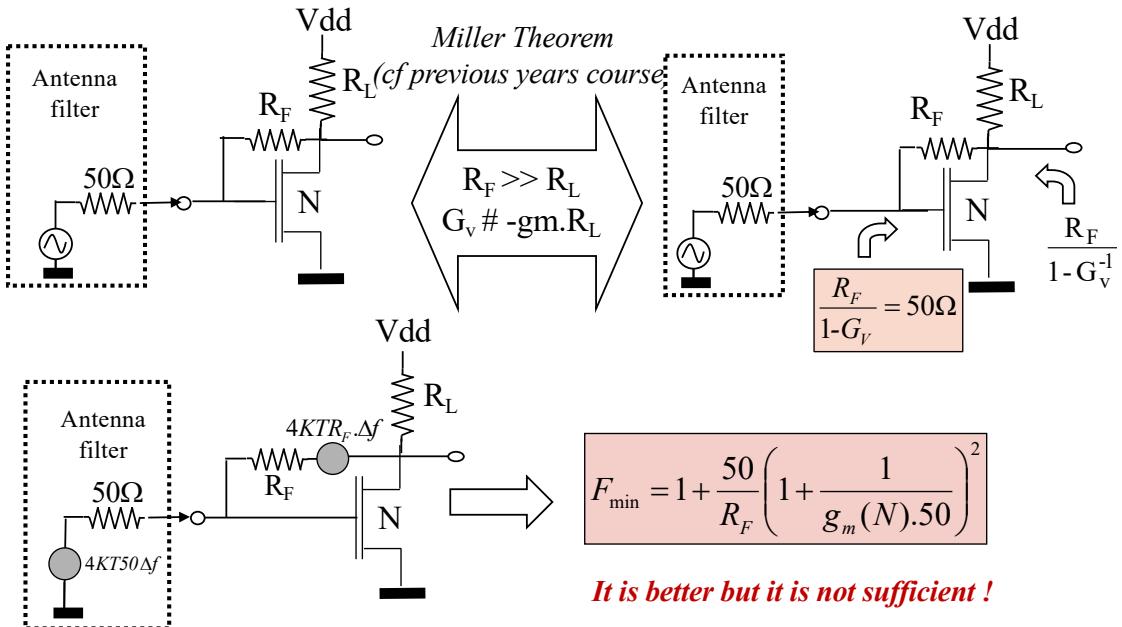


Requirements are not achieved even with ideal devices !!

Low Noise Amplifier

Trade-off between input matching and Noise Factor

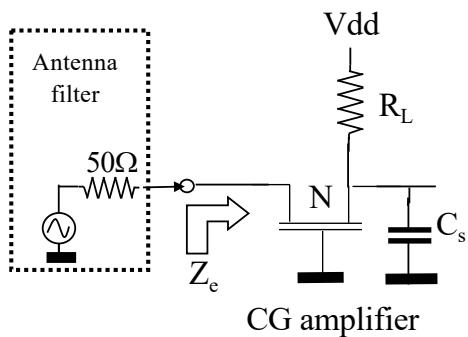
B – RF feedback topology



Low Noise Amplifier

Trade-off between input matching and Noise Factor

C – Amplifier based on Common Gate topology



$$G_v = + \frac{g_m \cdot R_L}{1 + j \cdot f / f_c} \text{ with } f_c = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_s}$$

$$Z_e \# \frac{1}{gm} \quad (\text{if } r_{ds} \gg R_L)$$

Cf CIA course

The transconductance must be sized such as $(1/g_m) = 50\Omega$

$$\overline{V_{ns}^2} = G_v^2 \overline{V_{nRg}^2} \cdot \alpha^2 \rightarrow F_{min} \approx 1$$

- Pros :** the real 50Ω impedance is not synthesized with a resistor (no thermal noise is added)
Cons : Due to Common Gate topology it is not possible to independently tune the gain and the consumption since gm is fixed to reach a given value (20ms).

Low Noise Amplifier

Trade-off between input matching and Noise Factor

Note

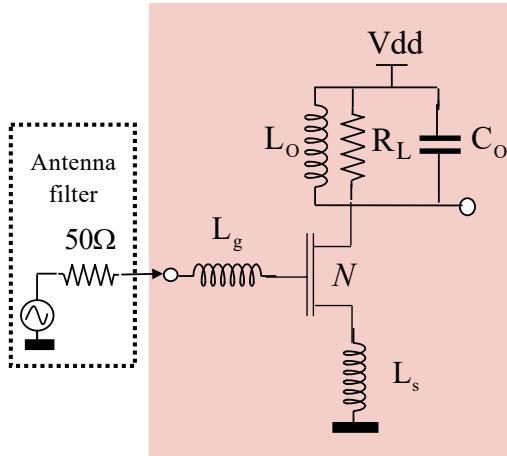
- ⇒ Previous solutions are wide band ($0 < f < f_c$)
- ⇒ Most of RF standards (GSM, Wifi, BT, ...) are narrowband ($\Delta f/f_0 < 10^{-3}$). Then, impedances R_L , Z_i , Z_o can be synthesized with LC network operating at resonant frequency f_0 .



CS based topologies with L placed in the source (emitter) and in the load are used

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load



A – Interest for RLC (band-pass filter)

The load (L_o, R_L, C_o) achieves at $\omega_o = \frac{1}{\sqrt{L_o \cdot C_o}}$ a real impedance equal to R_L

In DC mode, the load is null (*well suited to low Vdd*)

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

B – Input power matching

Source is degenerated by L_s

$$Z_i = Z + \frac{1}{C_{gs} \cdot p} (1 + g m_N \cdot Z)$$

See previous course

$$Z_i = \left(L_s p + \frac{1}{C_{gs} p} \right) + \left(\frac{g m_N \cdot L_s}{C_{gs}} \right)$$

$\Re m$ $\Re e$

Real part

$$Z_i = (L_g + L_s)p + \frac{1}{C_{gs} \cdot p} + L_s \cdot \omega_T \quad \text{with } \omega_T = \frac{g m_N}{C_{gs}}$$

$(L_g + L_s)p$ is sized to null $(1/C_{gs} \cdot p)$ at ω_0 :

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s) \cdot C_{gs}}} \quad (1)$$

L_s is sized so as :

$$L_s \cdot \omega_T = 50\Omega \quad (2)$$

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

C - Interest of inductive degeneration (L_s)

*The real impedance of 50Ω is not achieved with a resistor :
No thermal noise added to the device :*

$$F_{\min} \approx 1$$

With ideal MOS (N) : best trade-off

D – Miller Effect, use of a cascode stage (Cf previous course) :

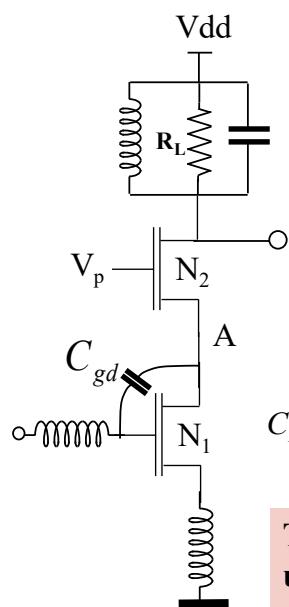
The previous derivation of Z_i neglect the Miller effect due to the C_{GD} capacitor. For high frequency this effect cannot be neglected. At the resonant frequency this effect can achieve a frequency dependent input impedance (Z_i). **Such impedance can have a negative real part and instabilities can occur.**

The Miller effect is highly reduced by a cascode topology.

Exercise : for a frequency $f < f_0$, the impedance of the RLC load is inductive and closed to de L_o . Shows that the Miller effect produces a negative real input impedance.

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load



The isolation stage (CG) N_2 achieves at node A a real impedance of low value (# $1/gm_2$) (cf previous course).

The gain between input and node A is equal to : $G_V = -\frac{g_{m1}}{g_{m2}}$

The Miller effect on C_{gd} synthesizes an input capacitance C_M in parallel with Z_e :

$$\left(Z_{miller} = \frac{Z_{Feedback}}{1 - G_V} \right)$$

$C_M = C_{gd} \left(1 + \frac{g_{m1}}{g_{m2}} \right) \approx 2C_{gd} \ll C_{gs}$ which has finally quite low influence on Z_e

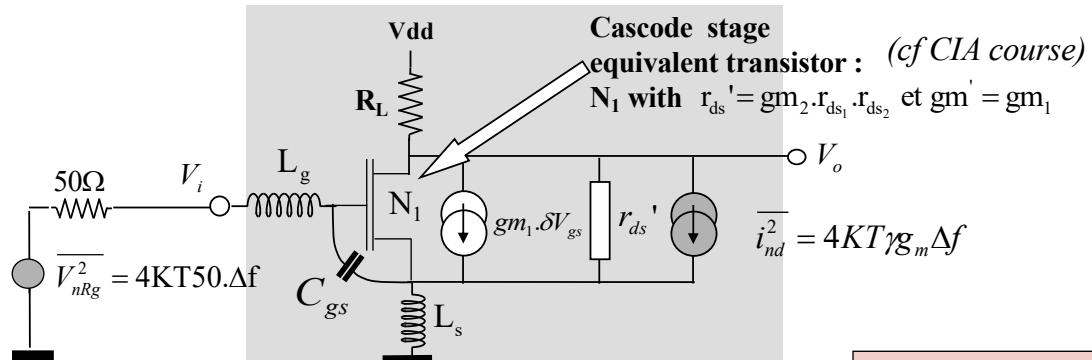
This topology is one of the best suited for the integration of an LNA under low voltage supply. It achieves the best trade-off between matching, stability and noise factor.

Low Noise Amplifier

Inductive degenerated CS or CE topology with RLC load

E – Noise Factor calculation

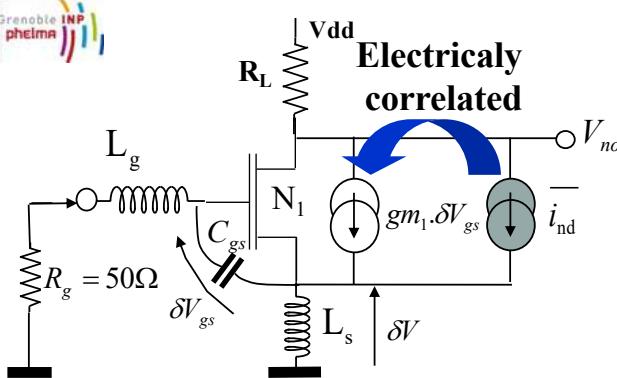
Only noise in the channel is considered



$$F = \frac{\overline{V_{no}^2}}{\alpha^2 \cdot G_v^2 \cdot V_{nRg}^2} \quad \left\{ \begin{array}{l} \bullet \quad \overline{V_{no}^2} \approx \alpha^2 \cdot G_v^2 \cdot 4KT50.\Delta f + R_L^2 \frac{i_{nd}^2}{4} \quad (1) \\ \bullet \quad \alpha = \left\| \frac{Z_i}{Z_i + 50} \right\| = \frac{50}{50+50} = \frac{1}{2} \\ \bullet \quad G_v = \frac{\delta V_s}{\delta V_{gs}} \approx -gm_1 \cdot R_L \cdot \frac{1}{50 \cdot C_{gs} \cdot \omega_0} = -gm_1 \cdot R_L \cdot Q_i \end{array} \right.$$

$F = 1 + \frac{\gamma}{50 \cdot gm_1} \frac{1}{Q_i^2}$
$F = 1 + \frac{1}{2.50 \cdot gm_1} \frac{1}{Q_i^2}$

Exercice : Shows that (1) is verified if $\omega_0 \ll \omega_T$



$$\delta V = (jL_s \omega_0) (\overline{i_{nd}} + gm_1 \delta V_{gs}) \quad (1)$$

$$\delta V_{gs} = -\delta V \left(\frac{(1/jC_{gs}\omega_0)}{(1/jC_{gs}\omega_0) + R_g + jL_s \omega_0} \right) \quad (2)$$

$$\overline{V_{no}}(\text{MOS}) = R_L (\overline{i_{nd}} + gm_1 \delta V_{gs}) \quad (3)$$

$$(1) + (2) \Rightarrow \delta V_{gs} \left[(1/C_{gs}\omega_0) + R_g + L_s \omega_0 \right] = -\frac{L_s}{C_{gs}} (gm_1 \delta V_{gs} + \overline{i_{nd}})$$

$$L_s \omega_T = R_g$$

$$\omega_T = \frac{gm_1}{C_{gs}}$$

$$(1/jC_{gs}\omega_0) + jL_s \omega_0 = -jL_s \omega_0$$

$$\delta V_{gs} \left[R_g - jL_s \omega_0 \right] = - \left[R_g \delta V_{gs} + \frac{R_g}{gm_1} \overline{i_{nd}} \right] \quad \text{or} \quad \omega_0 \ll \omega_T \Rightarrow L_s \omega_T = R_g \gg L_s \omega_0$$

$$\delta V_{gs} \cdot R_g = - \left[R_g \cdot \delta V_{gs} + \frac{R_g}{gm_1} \overline{i_{nd}} \right] \Rightarrow \delta V_{gs} = -\frac{1}{2gm_1} \overline{i_{nd}}$$

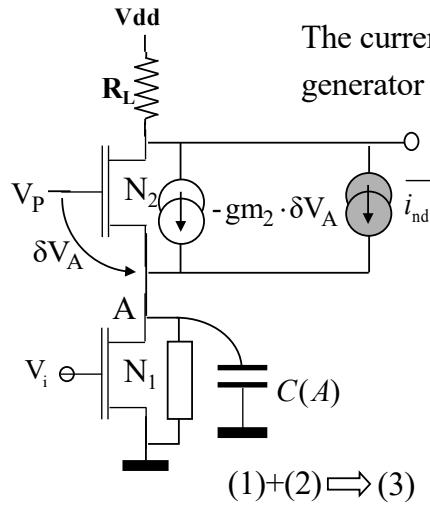
$$(3) \Rightarrow \overline{V_{no}}(\text{MOS}) = R_L \left[\overline{i_{nd}} - \frac{\overline{i_{nd}}}{2} \right] = R_L \frac{\overline{i_{nd}}}{2}$$

hence : $\overline{V_{ns}^2} = R_L^2 \frac{\overline{i_{nd}}^2}{4}$

Low Noise Amplifier

Inductive degenerated CS or CE topology with RLC load

F – Contribution of the cascode transistor (N2) on the noise



The current generator $-gm_2 \cdot \delta V_A$ is correlated in phase with the current generator $\sqrt{i_{nd}^2} = \sqrt{4KT\gamma gm \Delta f}$ by the voltage variation δV_A

$$\text{Then we have : } \delta V_A \approx \frac{1}{j.C(A) \cdot \omega_0} [i_{nd} - gm_2 \cdot \delta V_A] \quad (1)$$

The noise added by N2 to the load is then:

$$\overline{V_{no}^2}(\text{casc}) = R_L^2 [i_{nd} - gm_2 \cdot \delta V_A]^2 \quad (2)$$

$$\overline{V_{no}^2}(\text{casc}) = R_L^2 \cdot i_{nd}^2 \left[\frac{\omega_0^2}{\omega_0^2 + \omega_A^2} \right], \text{ with } \omega_A = \frac{gm_2}{C(A)} \quad (3)$$

Conclusion : To minimise the contribution of N2 to the Noise Factor, C(A) must be minimised. And the circuit must be sized so as $\omega_A \gg \omega_0$

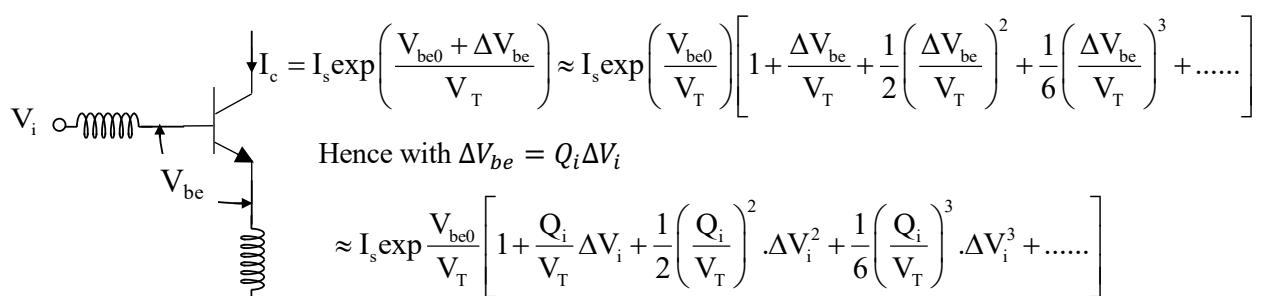
Exercise : Show the relationship (3)

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

H- Non Linearities: Bipolar Transistor example

The distortion on V_o is due to the non linear variation of the current I_c in function of V_{be} .



From slide 39 :

$$V_{elP3} = \sqrt{\frac{4}{3} \left| \frac{G_v}{\alpha_3} \right|} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} \quad V_{elP3} = \sqrt{\frac{4}{3} \left| \frac{\left(\frac{Q_i}{V_T} \right)}{\frac{1}{6} \left(\frac{Q_i}{V_T} \right)^3} \right|} = 2\sqrt{2} \cdot V_T \frac{1}{Q_i} (V_C) \Rightarrow \boxed{V_{elP3} \propto 2\sqrt{2} \cdot V_T \frac{1}{Q_i} (\text{Volt})}$$

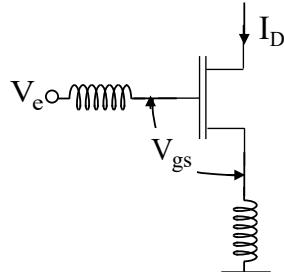
Trade-off with F

Exercise : Calculate the IIP3 in dBm on 50Ω input impedance with $Q_i=1$. Verify that requirement (slide 58) are satisfied.

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

H- Non-linearities : MOS transistor example



In short channel transistor ($< 0,2\mu m$) the current (I_D) is no more quadratic. The relationship between I_D and V_{gs} introduces 3rd order non-linearities and the IIP3 has a finite value
We can show that :

$$V_{eIP3} \propto \sqrt{V_{gs} - V_t} \frac{1}{Q_i} (\text{Volt})$$

Trade-off with F

For a given Q_i , the IIP3 is not constant as it is in the Bipolar Transistor and it can be optimized by tuning V_{gs} . This introduces an additional degree of freedom to achieve better trade-off between F and IIP3

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

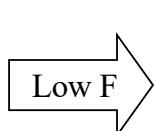
G- Trade-off between NF, IIP3 and Power consumption

$$(L > 1\mu m) \frac{2}{3} < \gamma < 2 \quad (L \ll 1\mu m)$$

MOS : $F = 1 + \frac{\gamma}{50.gm_1} \frac{1}{Q_i^2}$ $V_{eIP3} \propto \sqrt{V_{gs} - V_t} \frac{1}{Q_i} (\text{en Volt})$

Bip : $F = 1 + \frac{1}{2.50.gm_1} \frac{1}{Q_i^2}$ $V_{eIP3} \propto 2\sqrt{2}.V_T \frac{1}{Q_i} (\text{Volt})$

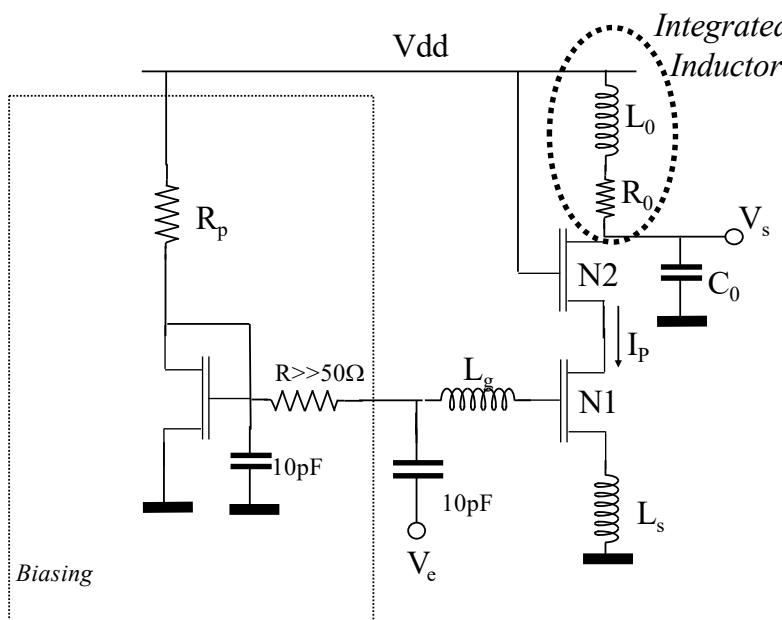
*Only channel noise
is considered*



- Q_i : high but degrades linearity
- gm_1 : high but degrades the power consumption

Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load



$$\text{At : } \omega_0 = \frac{1}{\sqrt{L_0 \cdot C_0}}$$

The LRC network is equivalent to a resistor $R_L = Q_0^2 \cdot R_0$

with Q_0 the Q factor of the integrated L_0

$$Q_0 = \frac{L_0 \cdot \omega_0}{R_0}$$

In the cascode stage :

- The N2 MOS achieves a good isolation.
- The N1 MOS gives a good trade-off F-IIP3.
- The resistor $R >> 50\Omega$ isolates RF path from DC.
- $C=10\text{pF}$ filters the noise from DC

Exemple of the implementation of a LNA

RFIC

S. Bourdel

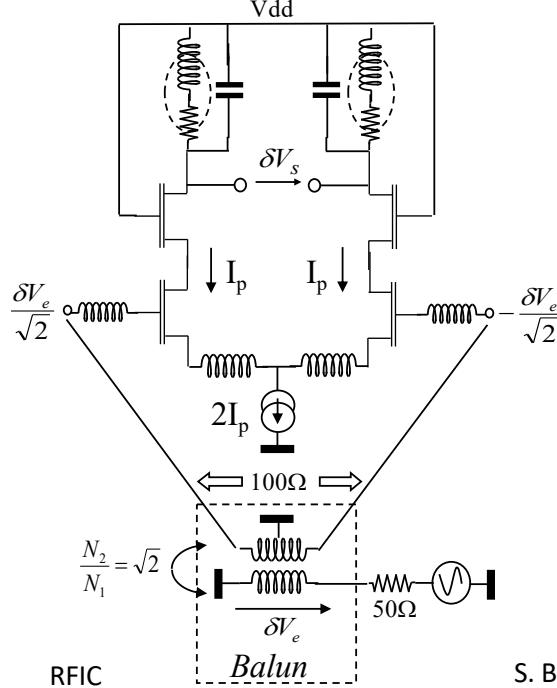
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Low Noise Amplifier

Inductively degenerated CS or CE topology with RLC load

Differential Structure

Lower the effects of common mode noise coupled via substrate



Single (VS) Differential

Single

$$\text{Cons.} = V_{dd} \cdot I_p$$

$$G_V = g_m \cdot R_L$$

$$\alpha^2 = \frac{1}{4}$$

$$F = 1 + \frac{V_{ns}^2(\text{MOS})}{\alpha^2 \cdot G_V^2 \cdot V_{nRg}^2}$$

Differential

$$\text{Cons.} = 2 \cdot V_{dd} \cdot I_p$$

$$G_V = \sqrt{2} g_m \cdot R_L$$

$$\alpha^2 = \frac{1}{4}$$

$$F = 1 + \frac{2V_{ns}^2(\text{MOS})}{\alpha^2 \cdot G_V^2 \cdot V_{nRg}^2}$$

For differential LNA, noise due to amplifier is twice but the G_V is increased thanks to the balun transformation ratio ($\sqrt{2}$), so F is unchanged.

RFIC

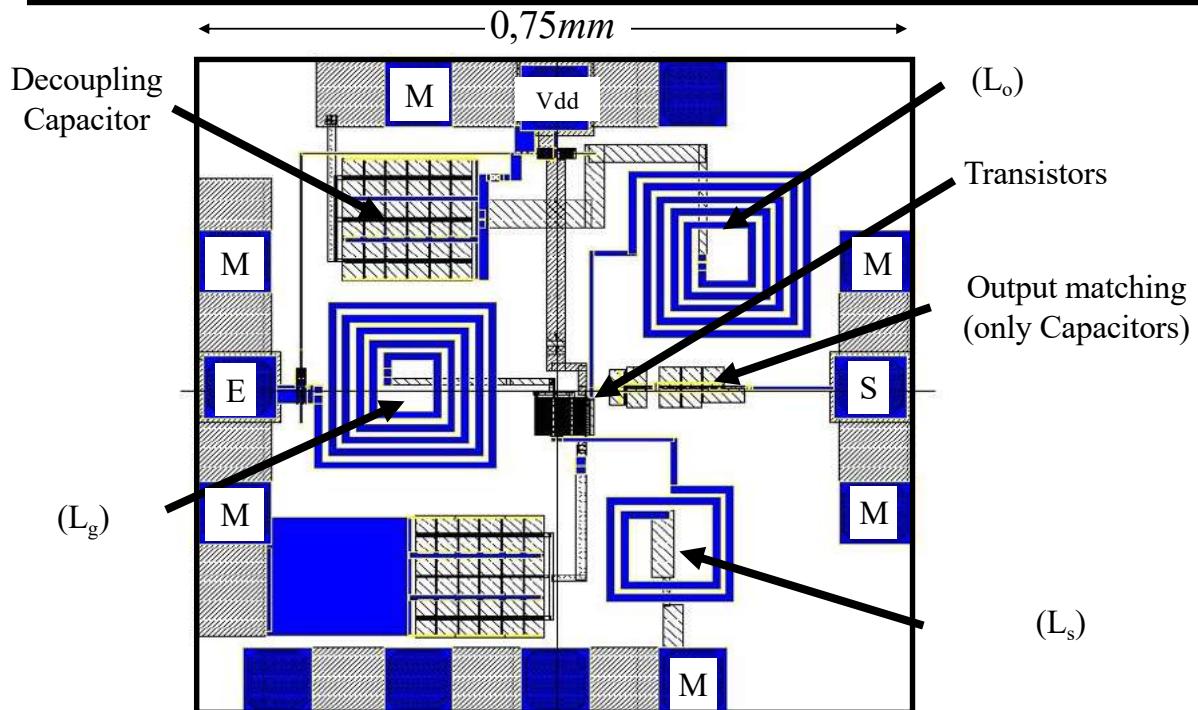
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Low Noise Amplifier

Layout exemple

LNA



Layout of L degenerated MOS cascode LNA

RFIC

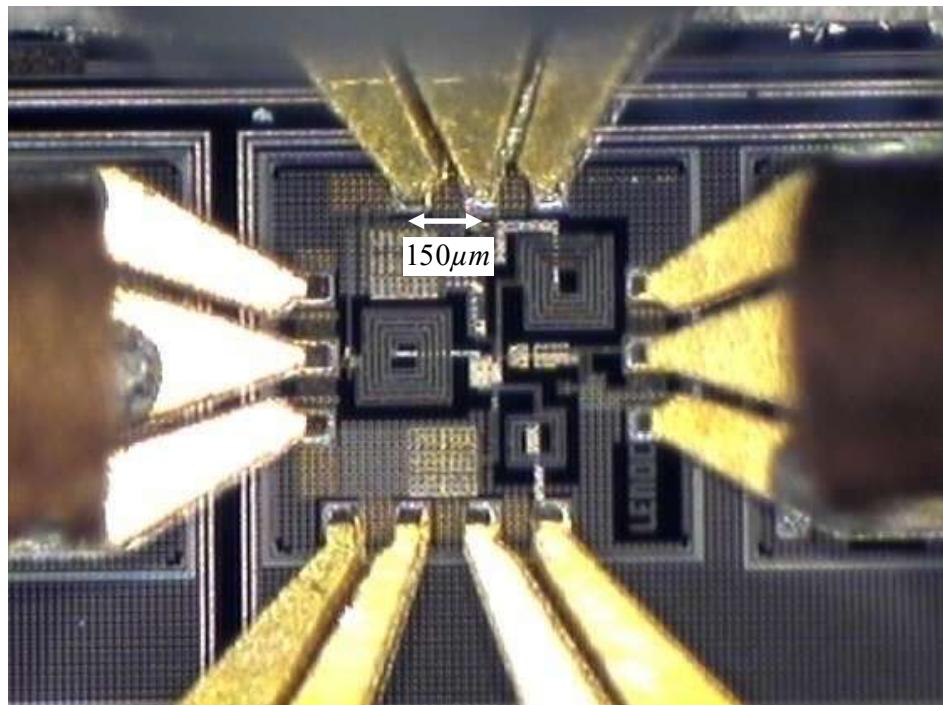
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Low Noise Amplifier

Die Photograph

LNA



LNA Measurement with prober

RFIC

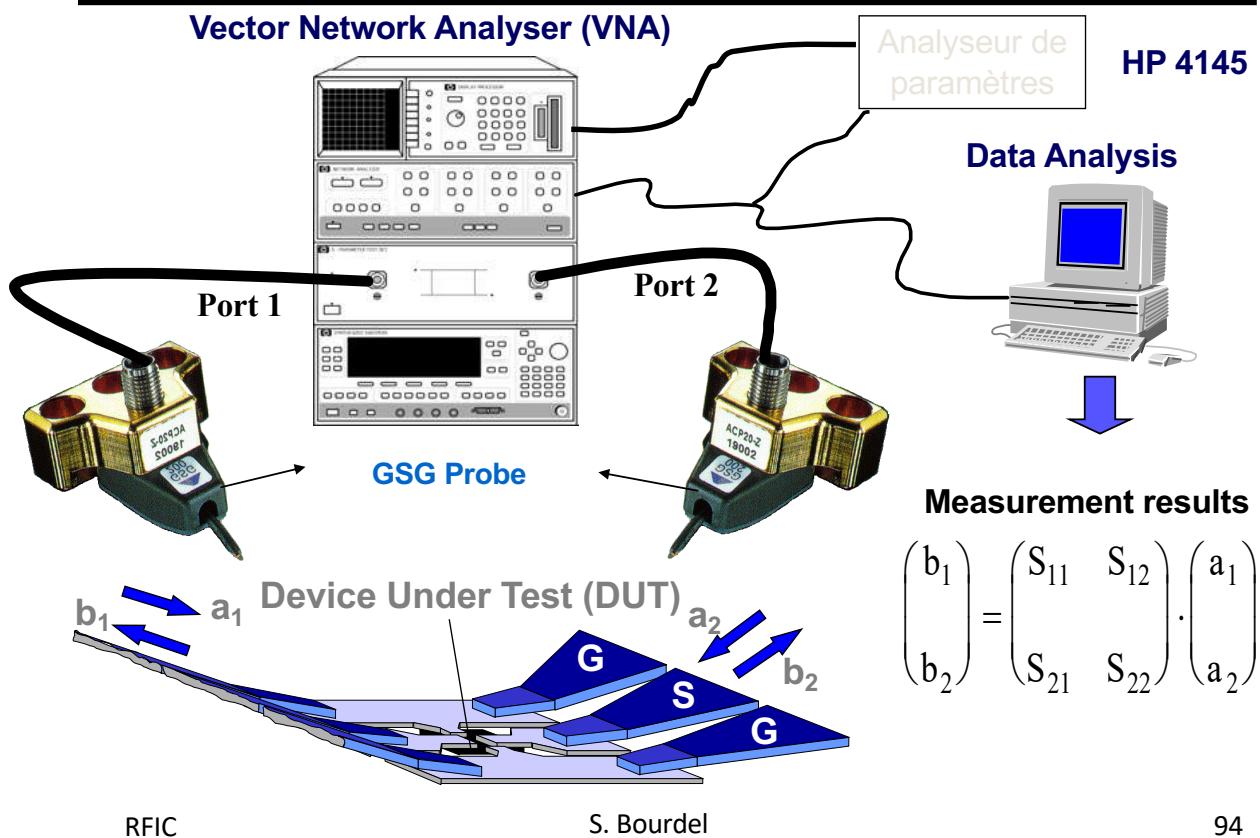
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Low Noise Amplifier

Test Bench for a LNA

LNA



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Version : 2020

Radio Frequency Integrated Circuits (RFIC)

Part II

Fonctions analogiques intégrées pour les radiofréquences

Sylvain BOURDEL

Outline

➤ Analog RF signal processing basis

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➤ Packaging

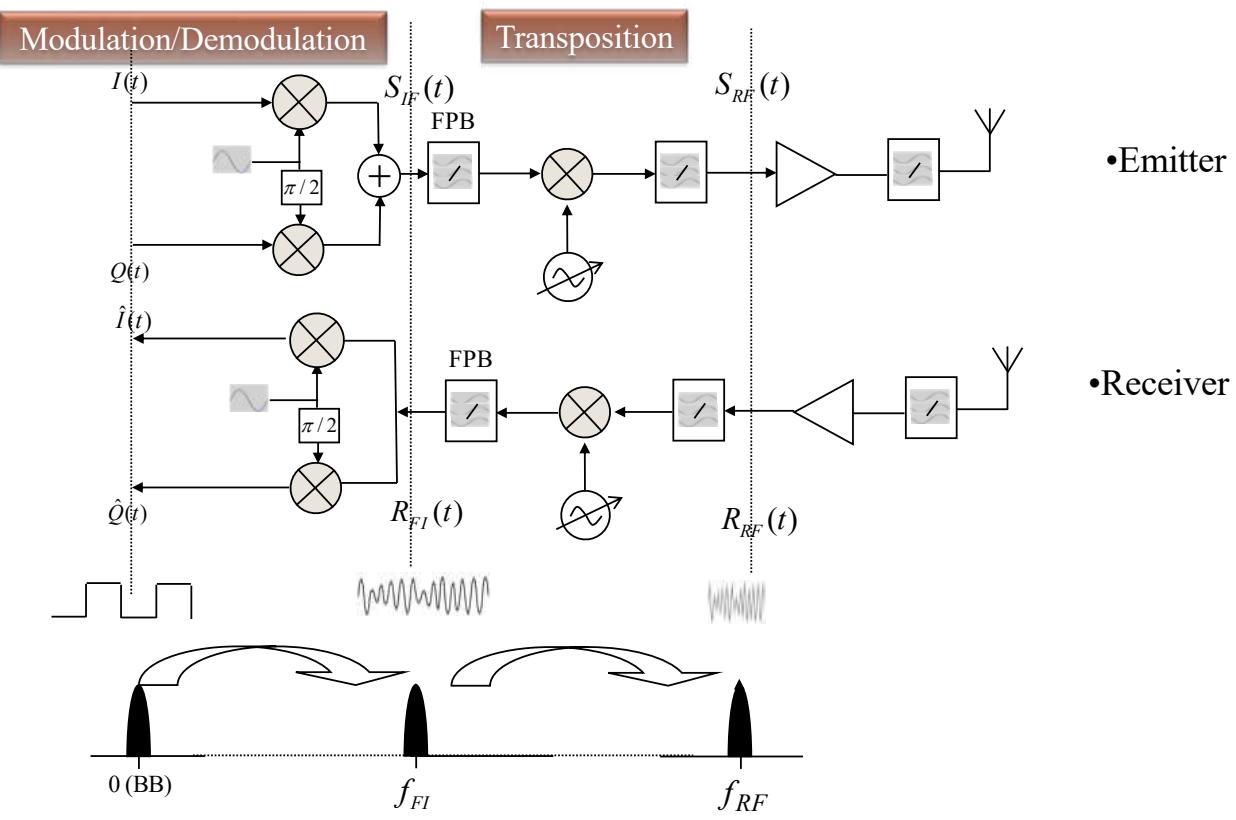
RFIC

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Mixer : Purpose

Mixer



RFIC

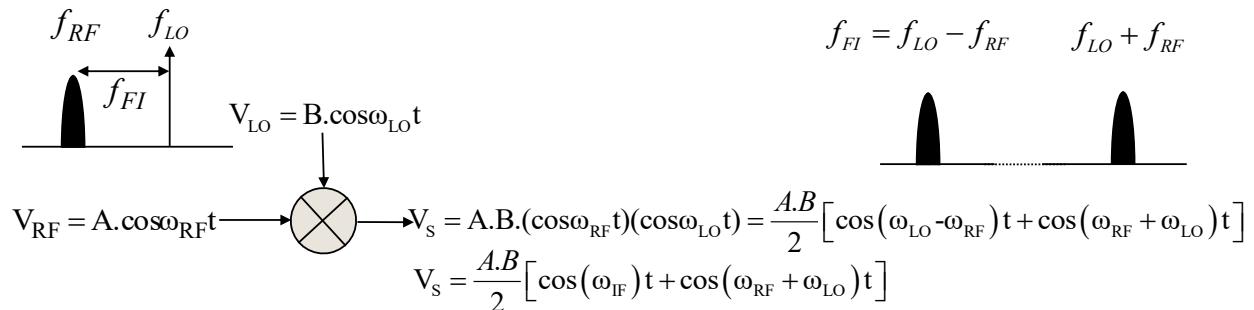
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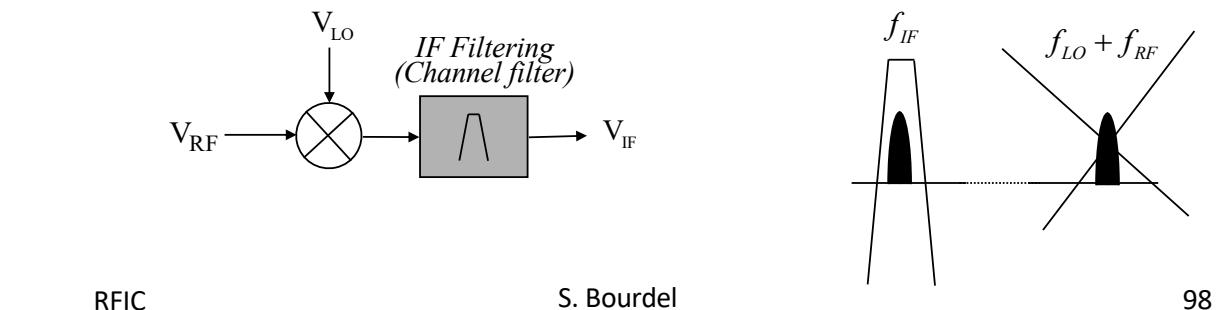
Mixers

Frequency transposition principle

A - Multiplication of RF signal with LO signal



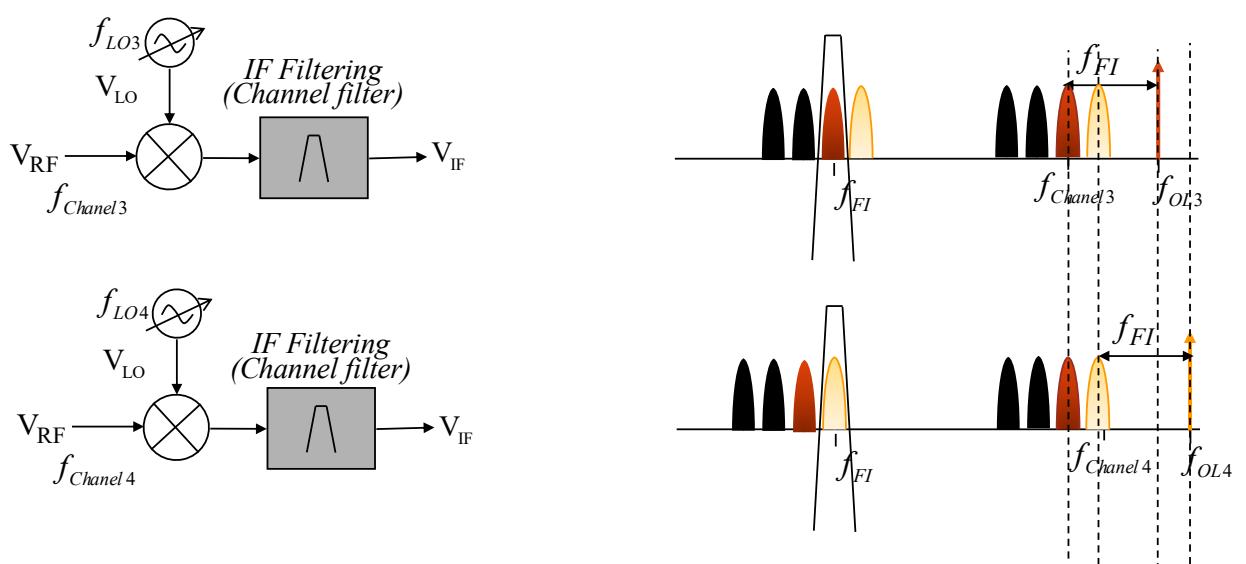
B- Band Pass Filtering of the output signal: only the IF signal is kept



Mixers

Frequency transposition principle

C- Channel selection during transposition :

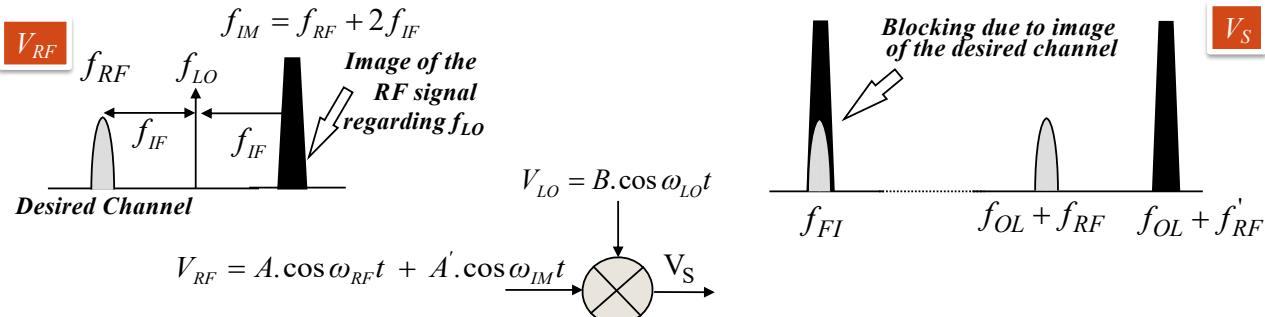


- A unique IF to simplify baseband processing
- A stated filter and a tunable LO (easier than the other way round)

Mixers

Frequency transposition principle

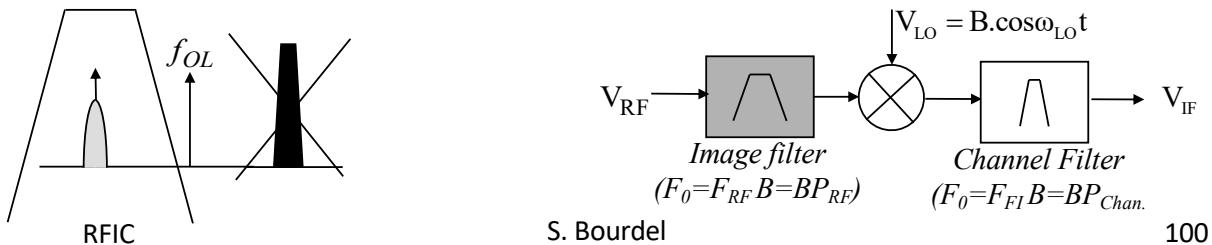
D – Image Frequency Issue (heterodyne structure)



$$V_S = (A \cdot B / 2) [\cos(\omega_{LO} - \omega_{RF})t + \cos(\omega_{RF} + \omega_{LO})t] + (A' \cdot B / 2) [\cos(\omega_{LO} - \omega_{IM})t + \cos(\omega_{IM} + \omega_{LO})t]$$

$$= (A \cdot B / 2) [\cos(\omega_{IF})t + \cos(\omega_{RF} + \omega_{LO})t] + (A' \cdot B / 2) [\cos(-\omega_{IF})t + \cos(\omega_{IM} + \omega_{LO})t]$$

E- solution : Image filtering before mixing with an image filter (band pass)

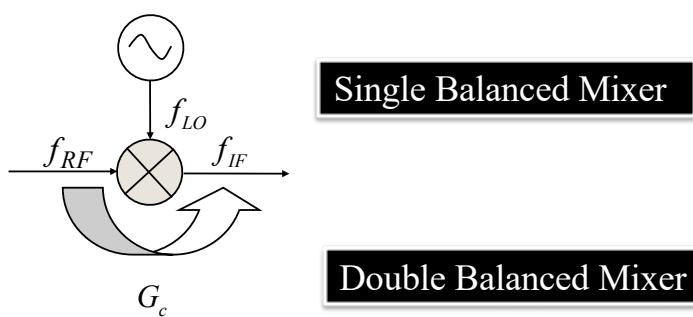


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Mixers

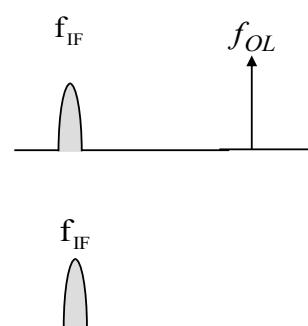
Major concepts

- Mixers are not Multipliers: $A_{IF} \neq A_{RF} \times A_{LO}$
- Only few mixers (regarding their topology) are multipliers
- The conversion gain (G_c) is defined as: $G_c = \frac{A_{IF}}{A_{RF}}$
- A mixer has : one **high level signal** input and one **low level signal** input
- LO signal is generally applied to the high level signal input
- Signal to be transposed (IF or RF) is generally applied to the low level signal input
- Some mixers let the LO signal going through out the output (as Single Balanced Mixer) and other not (as Double Balanced Mixer)

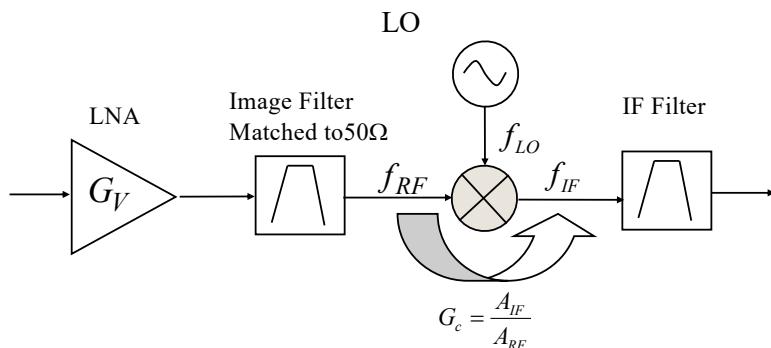


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Main requirement of a mixer in heterodyne receiver:

- Medium Noise Factor (Single Side Band) – (Second stage)
- High IIP3 > LNA IIP3 (Blockers have been amplified by the LNA)
- Medium Conversion Gain (RF---->IF) G_c (reduced by IIP3)
- Leakage: LO---->RF, LO--->IF and RF---->IF as low as possible
- Matched to input and output circuits (LNA or filters)

Typical values for an heterodyne receiver :

$F_{SSB} = 10\log F$	10dB
IIP3 (in dBm over 50Ω)	+5dBm
Conversion Gain G_c	10dB
Input Impedance	50Ω (Heterodyne)
Leakage (port to port)	< -20dB

Mixers

Sampling design methodology

Fourier Series of a periodic function $F(t)$ with $\omega = 2\pi/T$ pulsation

$$F(t) = a_0 + a_1 \cos\left(\frac{2\pi}{T}t\right) + b_1 \sin\left(\frac{2\pi}{T}t\right) + \dots + a_n \cos\left(n\frac{2\pi}{T}t\right) + b_n \sin\left(n\frac{2\pi}{T}t\right) + \dots$$

with : $a_0 = \frac{1}{T} \int_{-T/2}^{+T/2} F(t) \cdot dt$ $a_n = \frac{2}{T} \int_{-T/2}^{+T/2} F(t) \cdot \cos\left(n\frac{2\pi}{T}t\right) \cdot dt$

$$b_n = \frac{2}{T} \int_{-T/2}^{+T/2} F(t) \cdot \sin\left(n\frac{2\pi}{T}t\right) \cdot dt$$

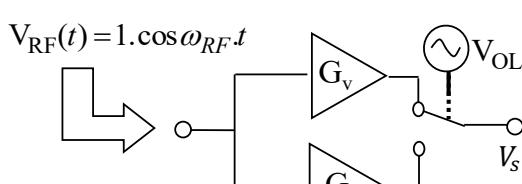
=> Square Signal

$$V_{OL}(t) = \text{sgn}(\sin(\omega_{OL}t)) = \frac{4}{\pi} \left\{ \sin\omega_{OL}t - \frac{1}{3}\sin 3\omega_{OL}t + \frac{1}{5}\sin 5\omega_{OL}t - \dots \right\}$$

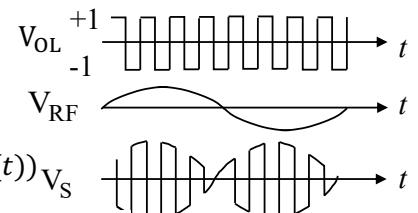
Mixers

Sampling design methodology

A – Sampling of amplified RF with LO (most often used technique) => Mixing



$$\text{sgn}(V_{OL}(t)) = \frac{4}{\pi} \left(\sin(\omega_{LO}t) - \frac{1}{3}\sin(3\omega_{LO}t) + \frac{1}{5}\sin(5\omega_{LO}t) \dots \right)$$



$$V_s(t) = G_V \cdot V_{RF}(t) \cdot V_{LO}(t) = \frac{2}{\pi} \cdot G_V \cdot \left\{ \begin{array}{l} \sin(\omega_{LO} + \omega_{RF})t + \sin(\omega_{LO} - \omega_{RF})t \\ -\frac{1}{3}\sin(3\omega_{LO} + \omega_{RF})t + \frac{1}{3}\sin(3\omega_{LO} - \omega_{RF})t \\ +\frac{1}{5}\sin(5\omega_{LO} + \omega_{RF})t + \frac{1}{5}\sin(5\omega_{LO} - \omega_{RF})t + \dots \end{array} \right\}$$

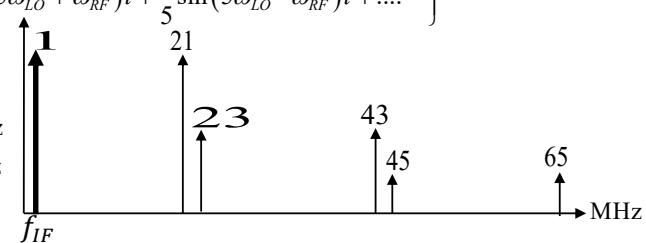
Conversion Gain $G_c = G_v \cdot 2/\pi$

No LO nor RF components at the output

Example:

$$f_{RF} = 10 \text{ MHz}$$

$$f_{LO} = 11 \text{ MHz}$$

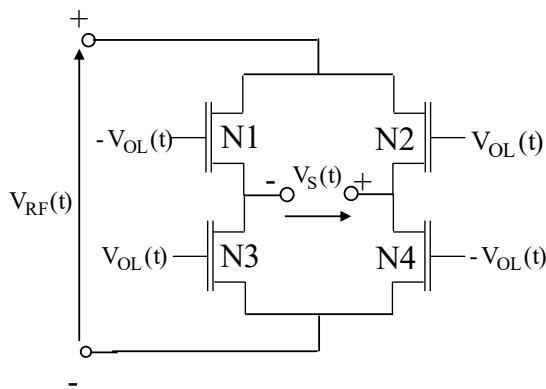


Exercise : Derive G_c and the output signal spectrum in the case of a simple switch ($V_{LO} [0-1]$)

Mixers

Sampling design methodology

B- Passive mixer ($G_c < 1$) based on differential CMOS ring (like diode mixer)



Principle : The MOS are ON or OFF when $V_{OL}(t)$ is at High or Low level, respectively.

$$V_{OL}(t) = 1 : V_S = V_{RF} \quad V_{OL}(t) = -1 : V_S = -V_{RF}$$

The output differential voltage $V_S(t)$ is :

$$V_S(t) = [\text{sgn}(V_{OL}(t))].V_{RF}(t)$$

Same spectrum than previously with $G_c = 2/\pi < 1$

Pros :

- No DC Bias (low power consumption and low voltage)
- High linearity (High IIP) because the gain is constant on a high dynamic range
- High Bandwidth

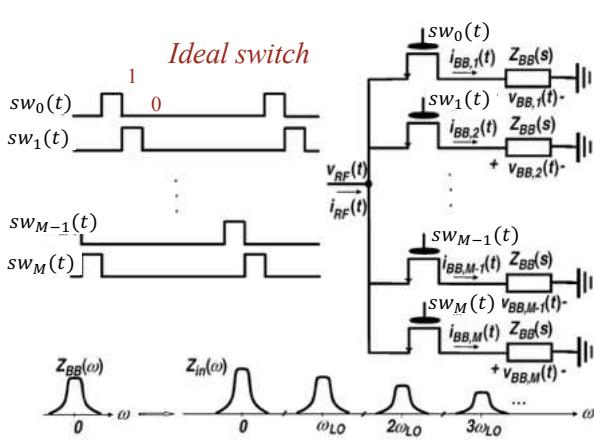
Cons. :

- Low conversion gain $G_c < 1$ (degrades the NF of the receiver – FRISS)

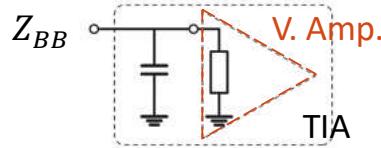
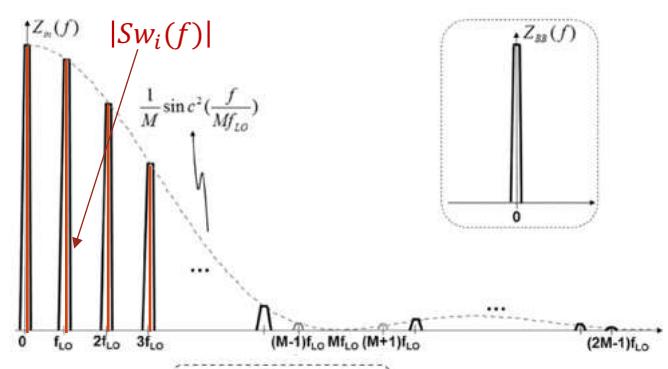
Mixers

Sampling design methodology

B- Passive mixer (N-Path Mixer)



$$Z_{in}(\omega) \cong R_{SW} + \frac{M}{\pi^2} \sin^2 \left(\frac{\pi}{M} \right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})]$$



Pros :

- $Z_{BB}(f)$ is transposed at f_{LO} .
- $Q_{eff} = \frac{2BW_{BB}}{f_{LO}}$
- Passive
- Almost digital

Cons. :

- $v_{BB,i}(t) = i_{RF}(t).sw_i(t) * z_{BB,i}(t)$
- $V_{BB,i}(f) = I_{RF}(f) * SW_i(f).Z_{BB,i}(f)$
- All the RF signals at $n.f_{LO}$ are folded back

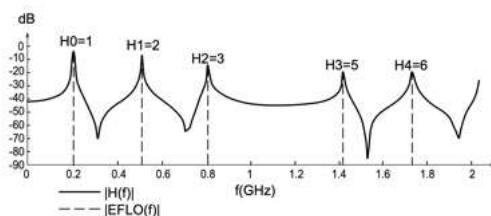
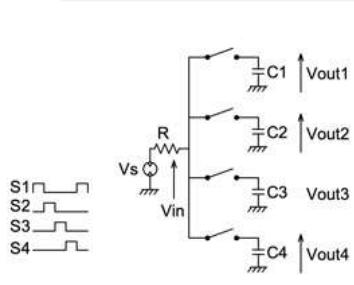
Mixers

Sampling design methodology

B- Passive mixer (N-Path Mixer) – Harmonic rejection issues

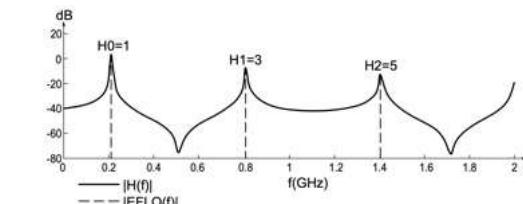
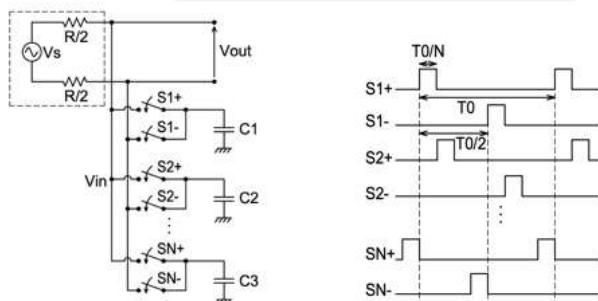
Generally Z_{bb} is synthesized with R_{on_switch} and a capacitor

4PM – Single Mode



RFIC

4PM – Differential Mode



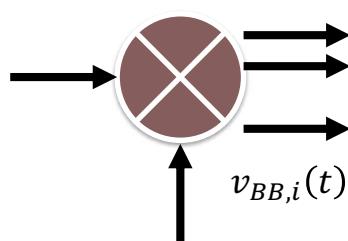
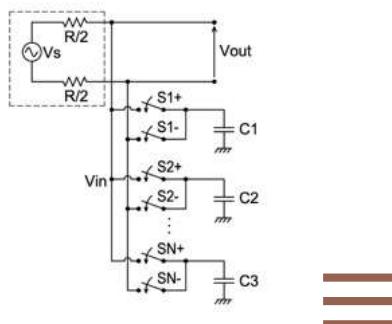
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Mixers

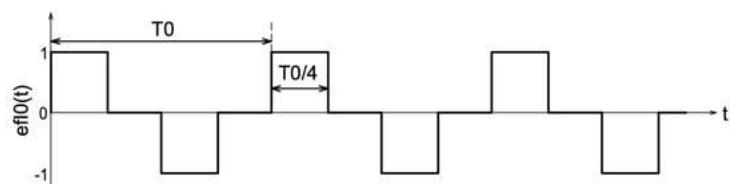
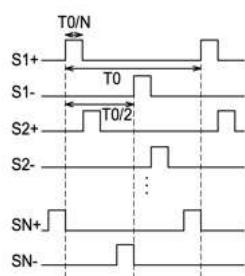
Sampling design methodology

B- Passive mixer (N-Path Mixer) – Harmonic rejection issues



$$v_{BB,i}(t) = i_{RF}(t) \cdot eflo_i(t) * z_{BB,i}(t)$$

$$\text{with } eflo_i(t) = s_{i+}(t) + s_{i-}(t)$$



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Sampling design methodology

B- Passive mixer (N-Path Mixer) – Harmonic rejection issues

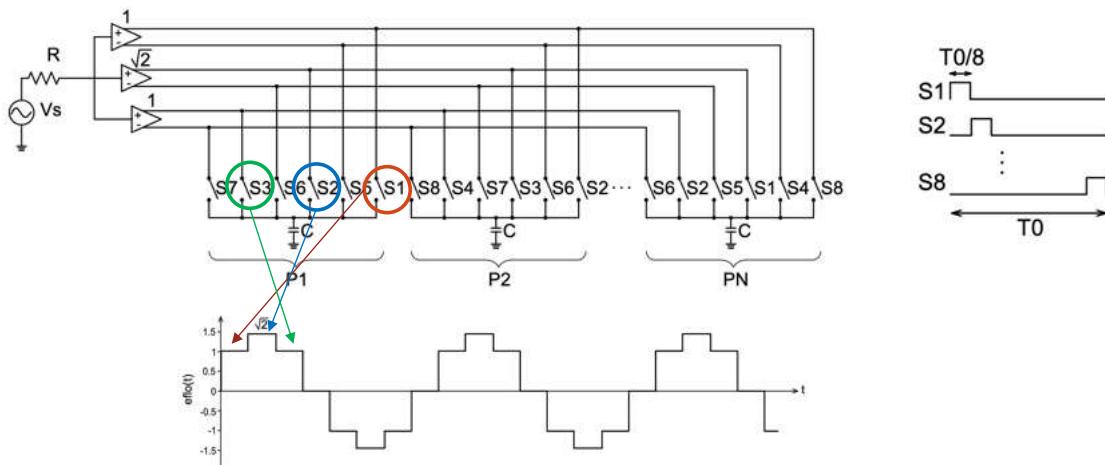
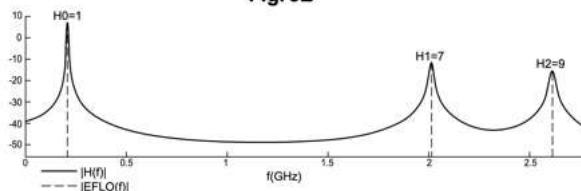


Fig. 3E



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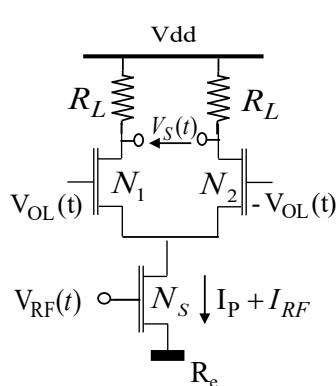
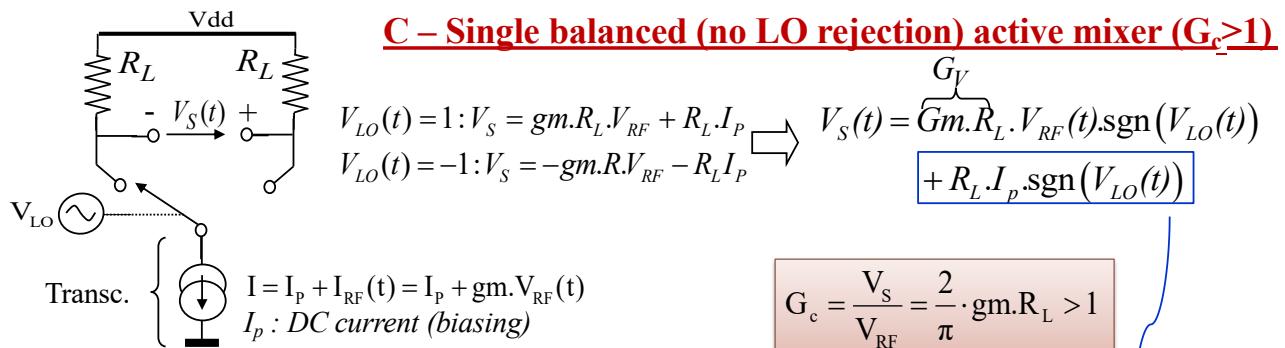
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Mixers

Sampling design methodology

C – Single balanced (no LO rejection) active mixer ($G_c \geq 1$)



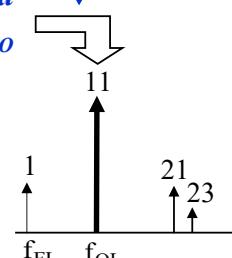
The modulation of the DC current produces a high signal component at f_{LO}

Pros. :

- Gain > 1 good for receiver NF

Cons. :

- DC power consumption
- The f_{LO} component at the output can saturate the following stage
- The LO noise is coupled at the output



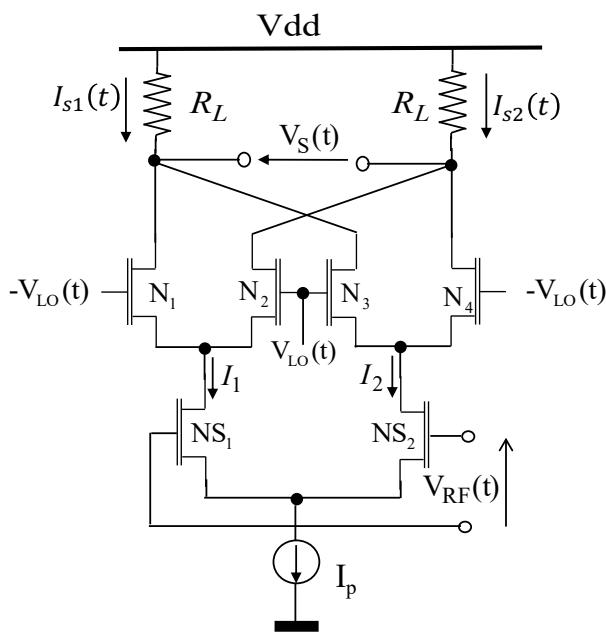
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Sampling design methodology

D – Double Balanced Active Mixer (Gilbert Cell)



$$\text{if } V_{RF}(t) \neq 0 \Rightarrow I_1 \neq I_2$$

- $V_{OL} > 0$, N_3 and N_2 ON,
 $\rightarrow V_S = R_L \cdot (I_2 - I_1) = R_L \cdot [g_m V_{RF}/2 + I_P - gm(-V_{RF}/2) - I_P] = R_L g_m V_{RF}$

- $V_{OL} < 0$, N_1 and N_4 ON,
 $\rightarrow V_S = R_L \cdot (I_1 - I_2) = R_L (g_m (-V_{RF}/2) - g_m V_{RF}/2) = -R_L g_m V_{RF}$

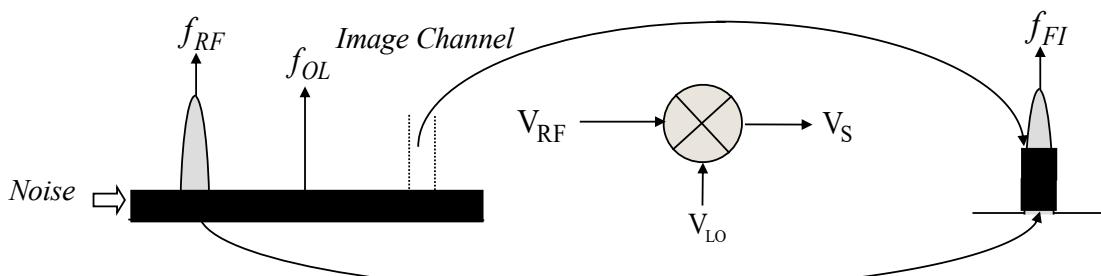
$$\Rightarrow V_S = R_L g_m \cdot \text{sgn}(V_{OL}) V_{RF}$$

$$G_e = \frac{V_S}{V_{RF}} = \frac{2}{\pi} \cdot g_m \cdot R_L > 1$$

No output component at f_{LO}
(rejection of CM noise and LO noise)
But higher consumption, more noise
and a larger V_{dd} is needed

Single Side Band Noise Factor (F_{SSB})

Heterodyne Receiver ($f_{FI} \neq 0$) : Noise Factor F_{SSB}

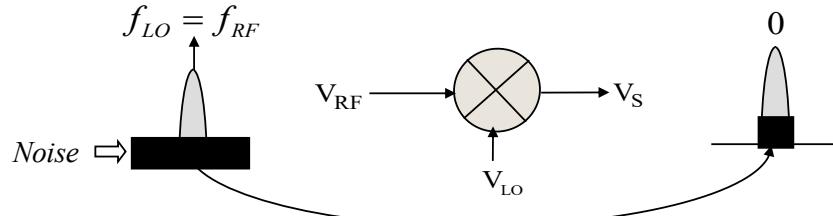


For heterodyne receiver ($f_{FI} \neq 0$) the noise from the image channel is transposed at f_{IF} and is added to the noise in the channel to be received

And for an homodyne receiver ($f_{FI} = 0$) ?

Double Side Band Noise Factor (F_{DSB})

Homodyne receiver ($f_{LO} = f_{RF} \rightarrow f_{FI} = 0$) : Noise Factor $F_{(DSB)}$



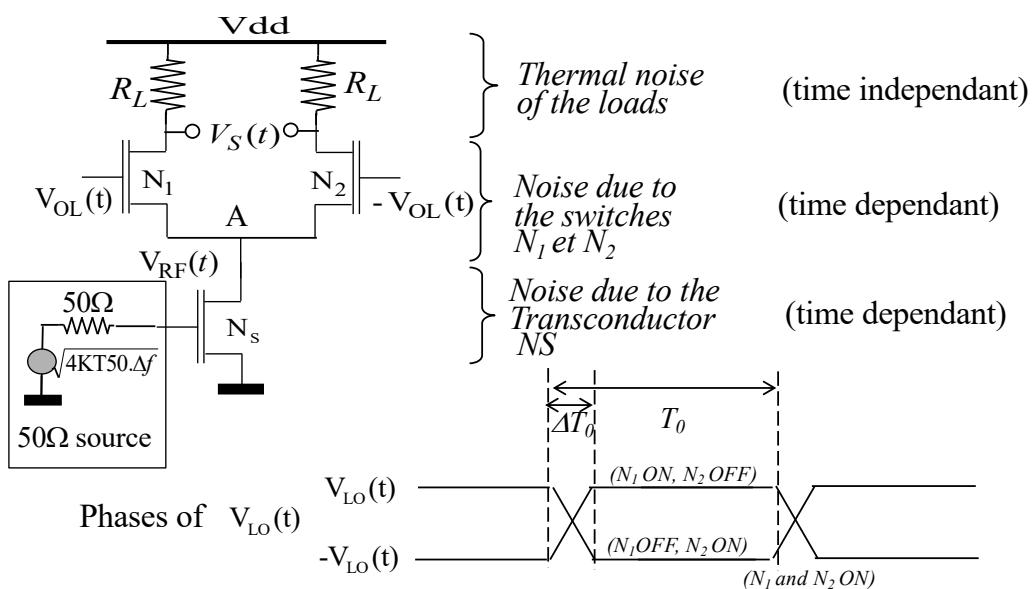
For homodyne receiver ($f_{FI} = 0$) image signal of the channel is the channel itself
There is no noise added by the channel

In heterodyne configuration the noise factor $F_{(SSB)}$ is 3dB higher than the one obtained in double side band topology $F_{(DSB)}$

$$F_{(SSB)}_{dB} = F_{(DSB)}_{dB} + 3dB$$

- Generally the mixer is characterised by : $F_{(SSB)}$

Noise in Single Balanced Active Mixers



The output noise depends on the states of N_1 and N_2 . 2 states must be considered :

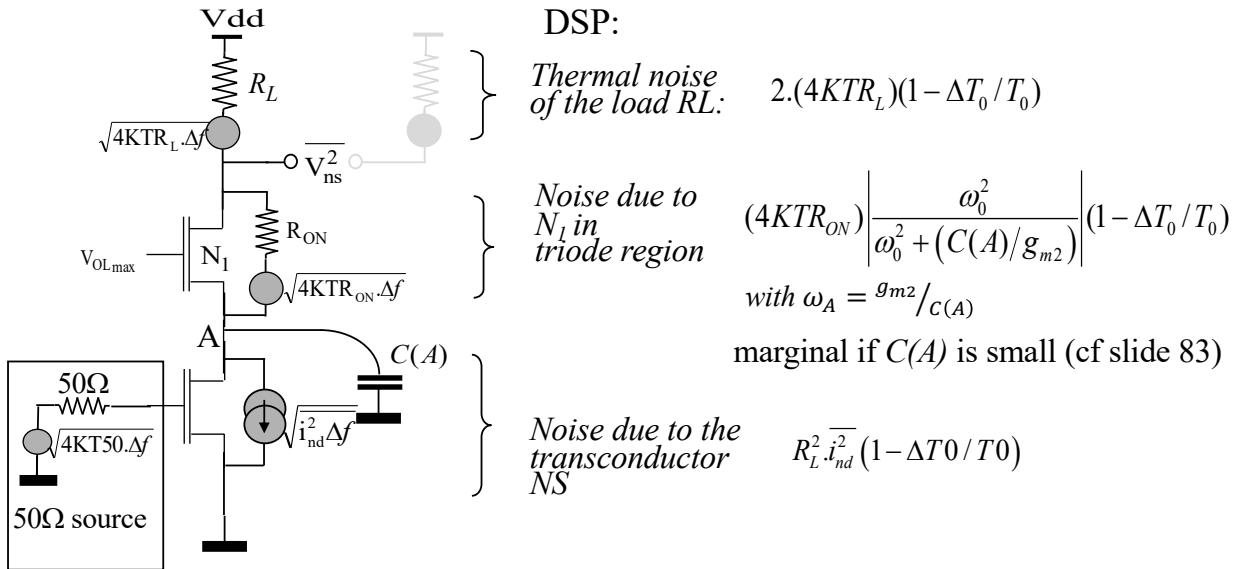
- N_1 ON and N_2 OFF for example
- N_1 and N_2 ON at the same time : overlapping of the two phases of $V_{LO}(t)$

Noise contribution of the source is time independant and is considered through the conversion gain



Noise in Active Mixers

• State : N_1 ON and N_2 OFF



Exercise : - Calculate $\overline{V_{ns}^2}$ when $C(A)$ can not be neglected (cf. slide 81)

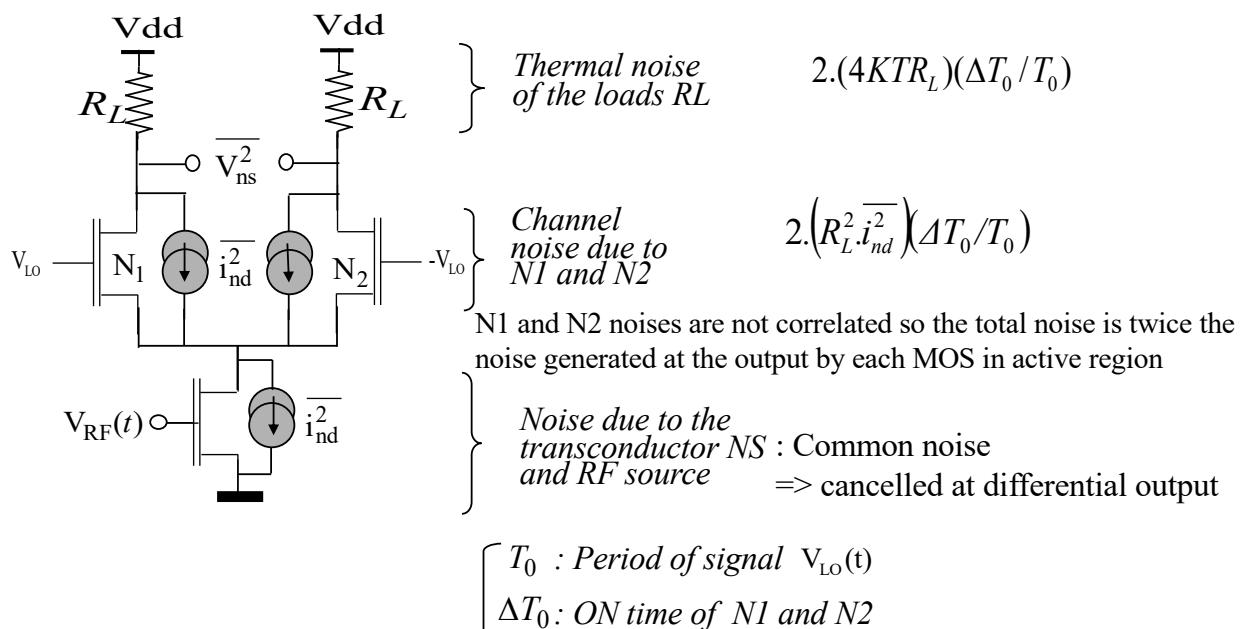
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Noise in Active Mixers

• State : N_1 and N_2 ON :



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Noise in Active Mixers

- Approximation of the total noise (considering $C(A)$ small)**

$$\overline{e_{no_v}^2} = \underbrace{G_c^2 4KTR_0}_{\text{Source}} + \underbrace{R_L^2 \overline{I_{nd}^2(N_s)} (1 - \Delta T / T_0)}_{\text{Transconductor}} + \underbrace{8KTR_L + 2R_L^2 \overline{I_{nd}^2(N_{1,2})} (\Delta T / T_0)}_{\text{Loads}} + \underbrace{\overline{R_L^2 I_{nd}^2(N_{1,2})} (\Delta T / T_0)}_{\text{Switches during commutation}}$$

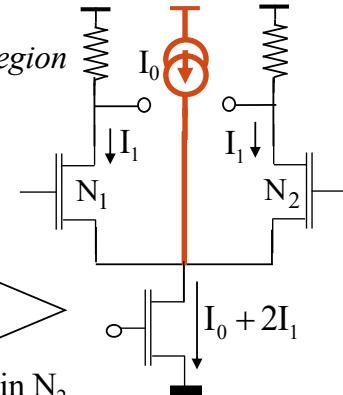
added noise ($V_{n_a}^2$)

$$F = 1 + \frac{R_L^2 \overline{I_{nd}^2(N_s)} (1 - \Delta T / T_0) + 8KTR_L + 2R_L^2 \overline{I_{nd}^2(N_{1,2})} (\Delta T / T_0)}{G_c^2 4KTR_0}$$

Optimisation rules:

- lower $C(A)$ (low sizes of N_1 and N_2)
 - lower transient time ΔT_0 (*High LO signal*)
 - Lower the current I_1 in N_1 and N_2 to lower the noise
- $$\overline{i_{nd}^2(N_{1,2})} = 4KT \cdot \gamma \cdot g_m$$

Switches in triode region



Exemple of solution :

- I_0 increases $g_m(N_s)$
- but does not increase the current in N_1 nor in N_2

Non-linearities in active mixers

- Two Main Origins:**

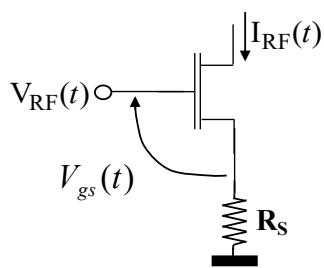
- distortion due to the non linear I-V curve of the transconductor (like in LNA)
- distortion due to sampling time since it depends on the V_{RF} signal

- Limitation of the distortion due to the non linear I-V curve of the transconductor
 - A resistor in the source R_S reduces the magnitude of $V_{gs}(t)$

$$V_{gs}(t) = V_{RF}(t) - R_S \cdot I_{RF}(t) = V_{RF}(t) - R_S \cdot gm(NS) \cdot V_{gs}(t) \Rightarrow V_{gs}(t) = \frac{V_{RF}(t)}{1 + gm \cdot R_S}$$

then (slide 85) :

$$IIP3 \propto \sqrt{V_{gs0} - V_t} \cdot \frac{1}{Q_i} \cdot (1 + gmR_S)$$

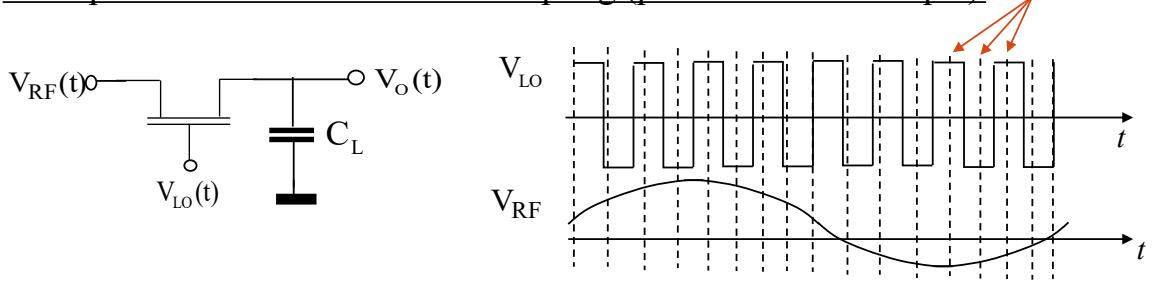


*Be careful however!
Resistor R_S adds noise and gain G_c is lower: NF increases*

What about distortion due to sampling ?



- Principle of the distortion due to sampling (passive mixer example)



➤ The sampling times (from OFF to ON state and reversely) are modeled as follows:

$$V_{gs}(t) = V_{LO}(t) - V_{RF}(t) = V_t \quad ; \quad \text{with } V_t \text{ the voltage threshold of the MOS}$$

Switching when : $V_{LO}(t) > V_t + V_{RF}(t)$

➤ The delay between two sampling times varies with $V_{RF}(t)$. This induces 3rd order distortion.

This distortion mainly occurs in passive mixers: take high LO voltage.

Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

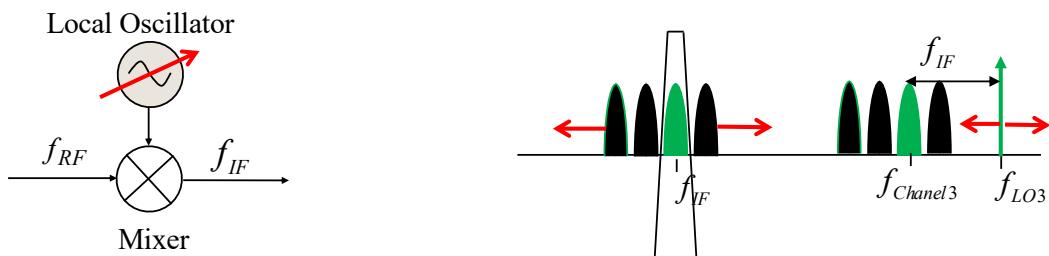
- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO)
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver



Local Oscillator Purpose: Generating an harmonic frequency f_{LO} so that:

$$f_{LO} = f_{RF} \pm f_{IF}$$

↑ ↑
 Variable Frequency Fixed Frequency
(depends on the channel frequency to be demodulated)

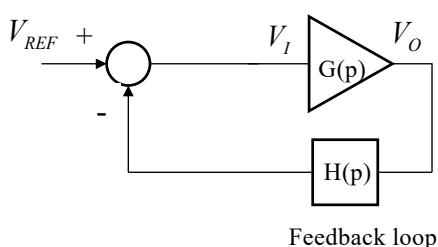
The oscillator frequency f_{LO} must be tunable with a step equal to the channel spacing, within a range equal to the RF bandwidth.

The local oscillator must be a VCO (Voltage Control Oscillator)

2 kinds of feedback : positive or negative feedback

A- Negative feedback: $G(p)H(p) < 0$

Direct path



$$\frac{V_o(p)}{V_{REF}(p)} = \frac{G(p)}{1 + G(p).H(p)}$$

with $p = j\omega$

Oscillation occurs if « V_o exists when $V_{REF} = 0$ »

$$\frac{V_o(p)_{=cte}}{V_{REF}(p)_{=0}} \rightarrow \infty \Rightarrow \frac{G(p)}{1 + G(p).H(p)} \rightarrow \infty$$

Barkausen Criteria

$$1 + G(j\omega_0).H(j\omega_0) = 0$$

Theoretically

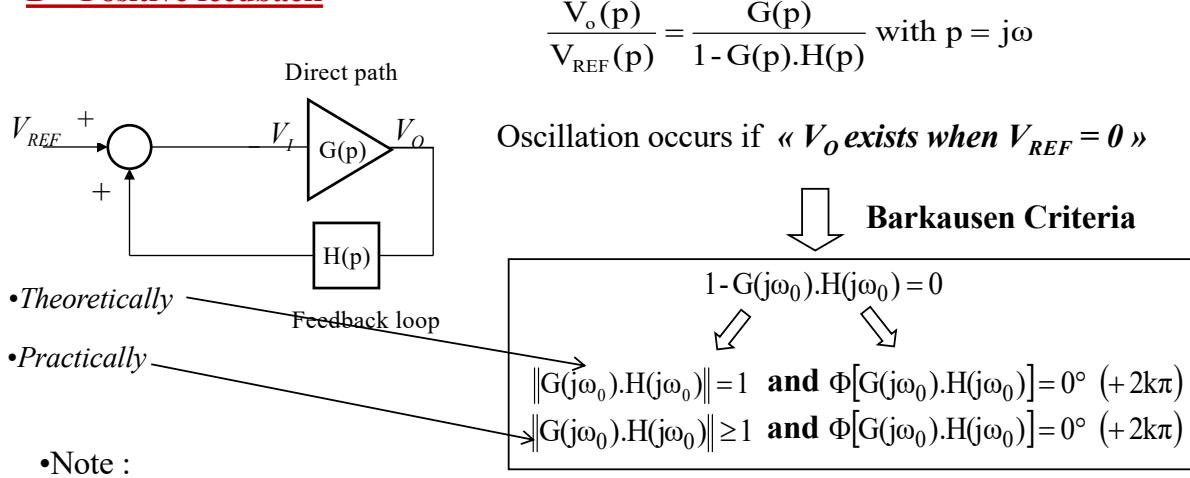
Practically, when the system starts, G goes from 0 to a steady state value and will pass through a value = to $1/H$. Then the LO can start.

$$\begin{aligned} & \|G(j\omega_0).H(j\omega_0)\| = 1 \quad \text{and} \quad \Phi[G(j\omega_0).H(j\omega_0)] = 180^\circ (+2k\pi) \\ & \|G(j\omega_0).H(j\omega_0)\| \geq 1 \quad \text{and} \quad \Phi[G(j\omega_0).H(j\omega_0)] = 180^\circ (+2k\pi) \end{aligned}$$

The Barkausen criteria gives :

- Condition on the modulus of the open loop gain $G(j\omega_0).H(j\omega_0)$ to ensure oscillations
- The value of ω_0 from the condition on the phase : $\Phi[G(j\omega_0).H(j\omega_0)] = 180^\circ$

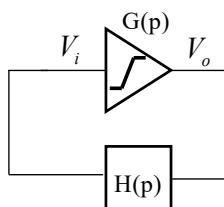
B – Positive feedback



The Barkausen criteria does not give the magnitude of oscillations

$$[1 \pm G(p).H(p)] \rightarrow 0 \longrightarrow \frac{V_o(p)}{V_{REF}(p)} = \frac{G(p)}{1 - G(p).H(p)} \rightarrow \frac{G(p)}{0} \dots ?$$

The NL of the amplifier limits the magnitude of the output signal :



Assumption 1 : The NL transfer function of the amplifier is given as follows: $V_o = f(V_i) = G_v V_i + \alpha_3 V_i^3$

Assumption 2 : The feedback loop is a filter at ω_0 (resonator).

Assumption 3: Input signal $V_i(t)$ is a sine: $V_i(t) = V_{i0} \sin \omega_0 t$

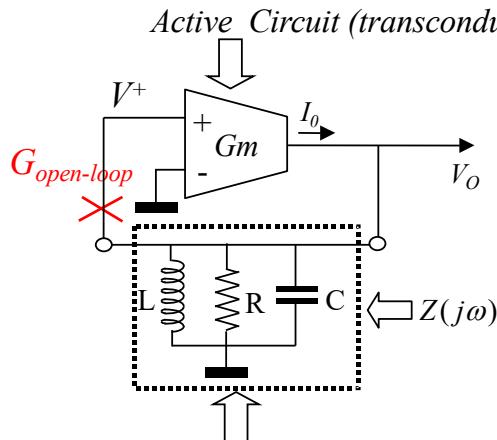
- After starting up, the amplifier compresses and the magnitude of the fundamental harmonic (ω_0) at the output of the amplifier is given by: (cf slide 34)

$$V_{o0} = \left[G_v V_{i0} + \frac{3\alpha_3 V_{i0}^3}{4} \right] \quad (1) \quad \text{where } G_v \text{ and } \alpha_3 \text{ have opposite signs}$$

- The feedback loop transfert function gives for ω_0 : $V_{i0} = \|H(j\omega_0)\| \cdot V_{o0}$ (2)

$$(1) + (2) \longrightarrow V_{o0} = \left[G_v V_{o0} + \frac{3\alpha_3 V_{o0}^3}{4} \right] \cdot \|H(j\omega_0)\| \quad \text{Magnitude } V_{o0} \text{ is solution of this equation.}$$

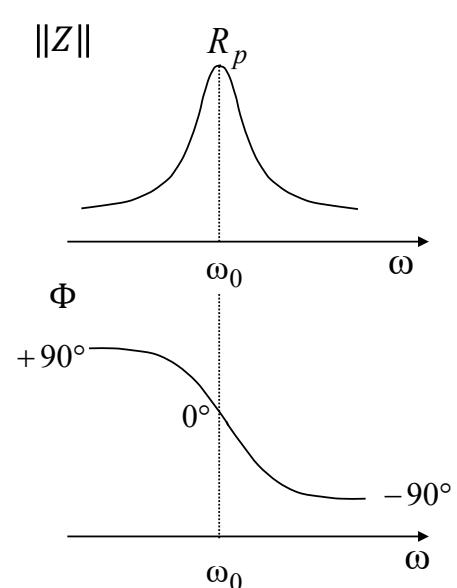
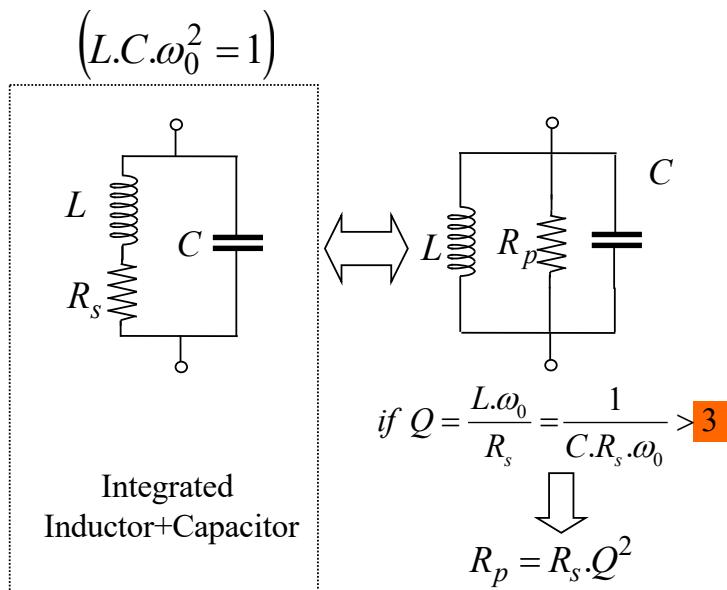
Topology of integrated LC Local Oscillators



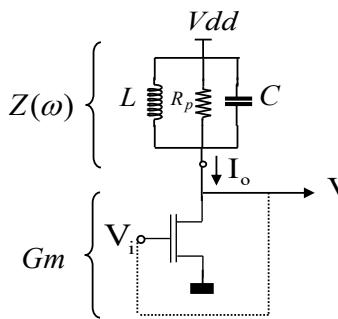
Interest for LC network (resonator)

- Good rejection of the supply noise (Vdd). Phase noise is due to only one stage.
- Low power consumption
- Low spurious responses on V_o (as I_o is filtered by the LC network) : no harmonic distortion

RLC network at resonant frequency



Electrical topology of a LC oscillator

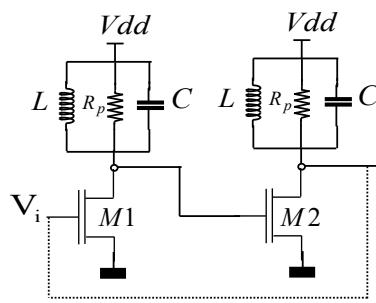


- One looped CS stage (CE)

$$\Delta\Phi\left(\frac{V_o}{V_i}\right) = \Delta\Phi_{Gm}\left(\frac{I_o}{V_i}\right) + \Delta\Phi_Z\left(\frac{V_o}{I_o}\right) = 180^\circ + / - 90^\circ$$

$$180^\circ - 90^\circ < \Delta\Phi\left(\frac{V_o}{V_i}\right) < 180^\circ + 90^\circ$$

Never equal to $0^\circ + 2k\pi$ → No Oscillation !



- Two looped cascaded CS stages (CE)

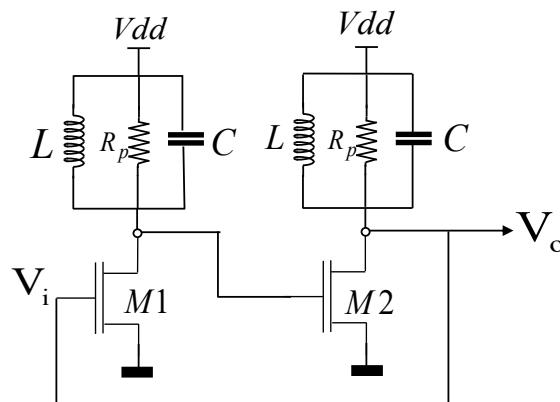
$$\Delta\Phi\left(\frac{V_o}{V_i}\right) = 2\Delta\Phi_{Gm}\left(\frac{I_o}{V_i}\right) + 2\Delta\Phi_Z\left(\frac{V_o}{I_o}\right)$$

$$360^\circ - 180^\circ < \Delta\Phi\left(\frac{V_o}{V_i}\right) < 360^\circ + 180^\circ$$

Equal to $0^\circ + 2k\pi$ at $\omega_0 = \frac{1}{\sqrt{LC}}$ → Oscillation occurs

- Start-up conditions?

Electrical topology of a LC oscillator

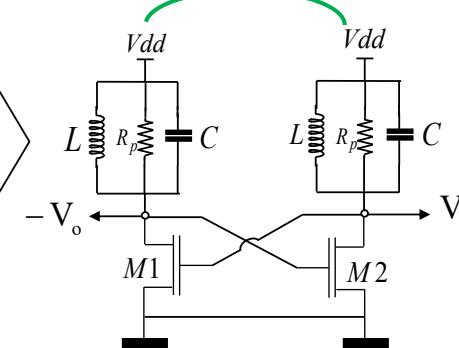
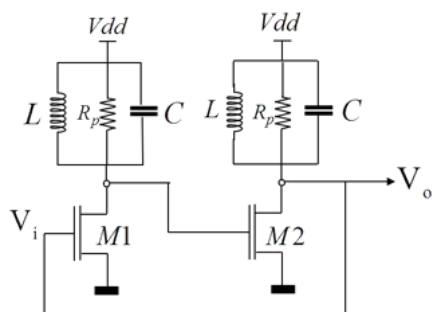


Start up Condition

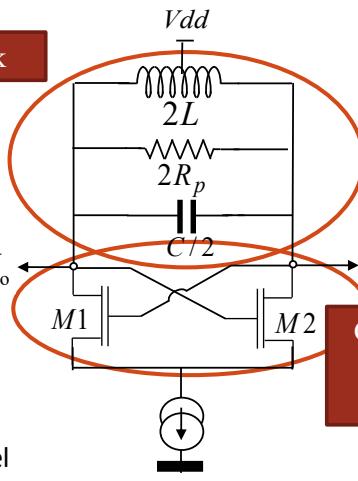
$$\|G_{open-loop}\|^2 = \|Gm \cdot Z(j\omega_0)\|^2 = (GmR_p)^2 \rightarrow \boxed{Gm \cdot R_p > 1}$$

Another way to consider this LO

Electrical topology of a LC oscillator



LC Tank



Cross Coupled Pair (CCP) or negative resistor

Differential outputs:

well suited for driving mixer inputs.

It is a **widespread topology**. The current source allows the control of the power consumption independently of the DC supply.

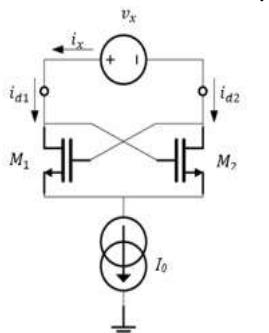
RFIC

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Electrical topology of a LC oscillator

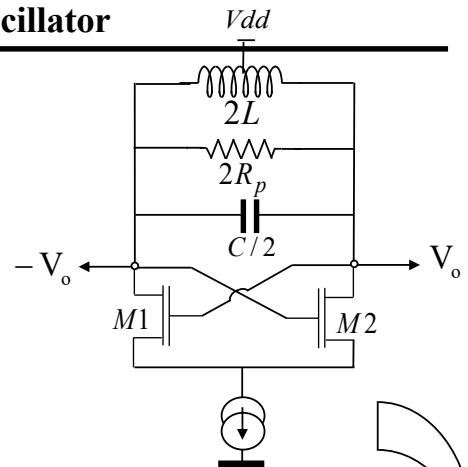
Note: The cross coupled pair (CCP) is a negative resistor



$$i_x = i_{d1} = g_m V_{gs1} = -i_{d2} = -g_m V_{gs2}$$

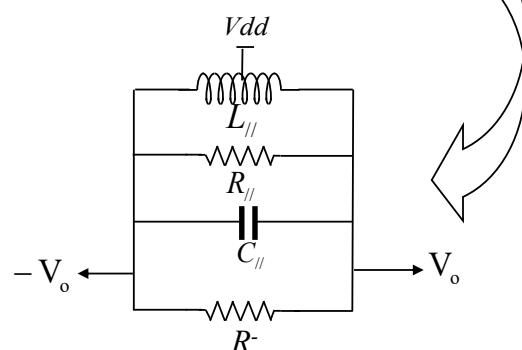
$$v_x = V_{gs2} - V_{gs1} = \frac{-i_x}{g_m} - \frac{i_x}{g_m}$$

$$R^- = \frac{v_x}{i_x} = \frac{-2}{g_m}$$



The oscillator can be seen as a lossless resonator
It will oscillate if R_{tot} is negative

$$R_{tot} = R_{\parallel} \parallel R^- < 0 \text{ if } |R^-| < R_{\parallel} \text{ if } g_m > \frac{2}{R_{\parallel}} = \frac{1}{R_p}$$

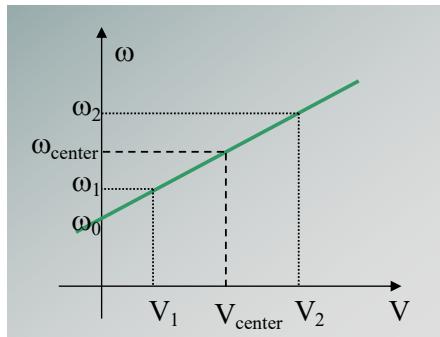


RFIC

S. Bourdel

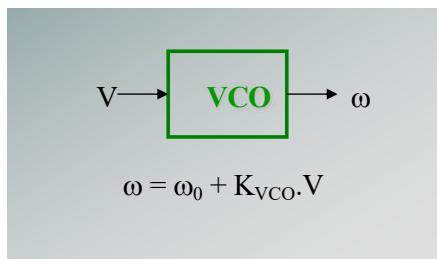
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VCO : LO + frequency tuning



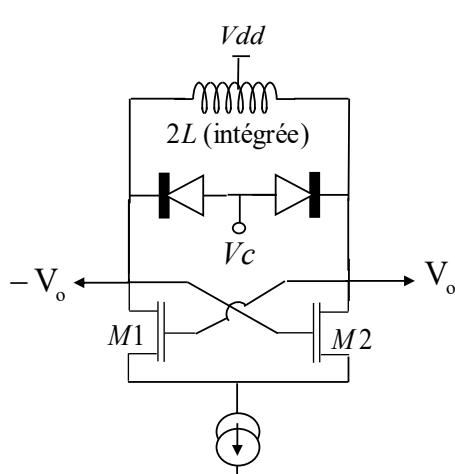
Performance

- Center frequency: @ $(V_1+V_2)/2$
- Tuning range:
 - Center frequency (temperature and process)
 - Gain : $K_{VCO} = (\omega_2 - \omega_1)/(V_2 - V_1)$
 - Center frequency must be calibrated
- Output dynamic: to be maximized (noise is reduced)
- Linear control
- Power cons. (1 to 10mW)
- Rejection of DC supply and common mode
- Spectral purity (phase noise and spurs)

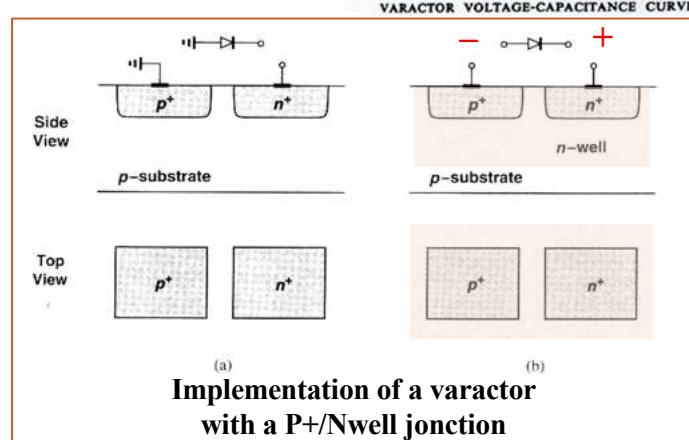
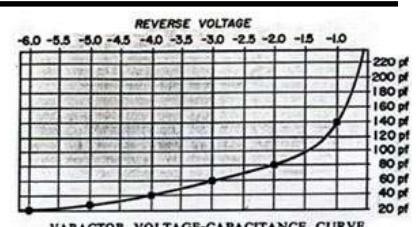


VCO

LC VCO with varactor

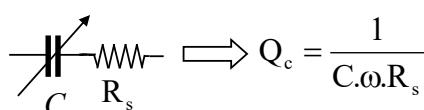
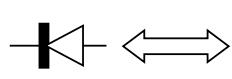


The capacitance of a reverse biased diode varies a lot with voltage



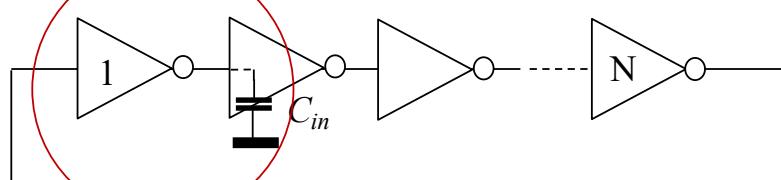
$$C_j(V_c) = C_j(0) / (1 + V_c/V_t)^{1/2}$$

Varactor model:



Rs limits the Q factor of the LC tank

1 pole



$$G_{open-loop} = G(p) \cdot H(p) = G(p) = \left(\frac{G_0}{1 + p/\omega_0} \right)^N \text{ with } G_0 < 0$$

Start up condition:

- Positive Feedback
- $N > 2$ $\Phi[G(j\infty)] = 180^\circ (+2k\pi)$

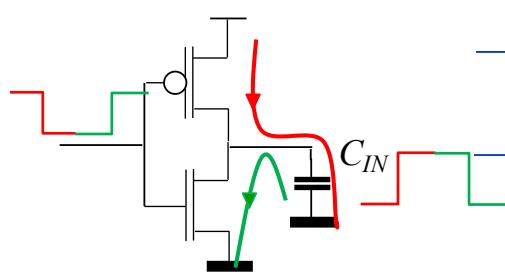
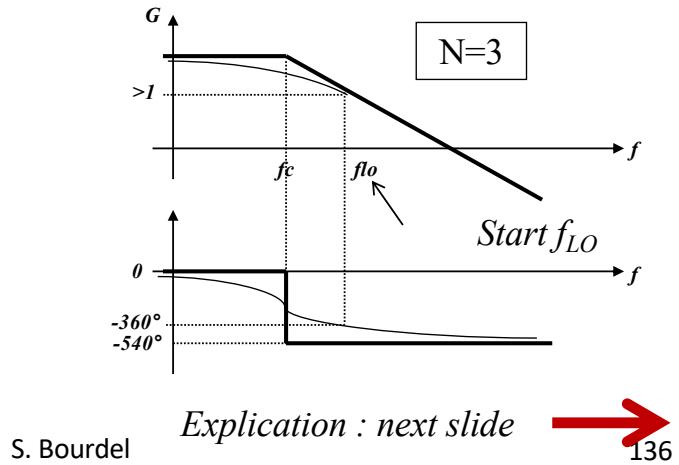
Steady state (N odd) :

$$f_{OL} = \frac{1}{N \cdot T_d}$$

Inverter delay

$$T_d = \text{rise time} + \text{fall time} = t_r + t_f$$

RFIC



$$\frac{dV_{rise}}{dt} = \frac{I_{DPmax}}{C_{IN}}, \text{ and } \frac{dV_{fall}}{dt} = \frac{I_{DNmax}}{C_{IN}}$$

$$I_{DN_{max}} = \frac{K_{PN}}{2} \frac{W}{L} (V_{DD} - V_{THN})^2$$

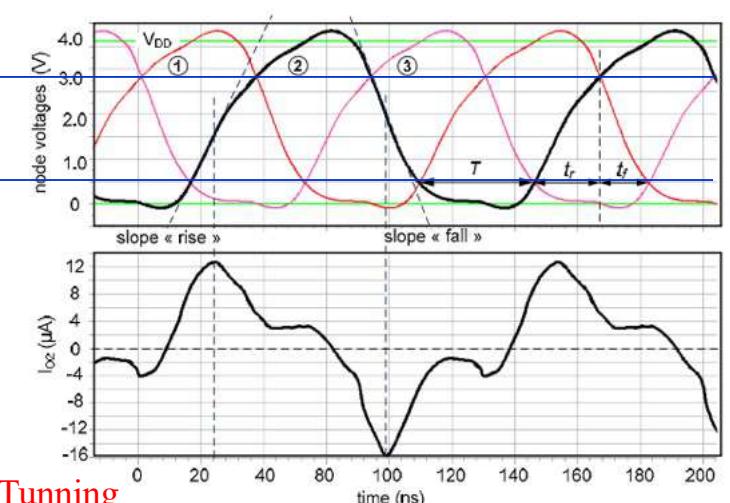
$$I_{DP_{max}} = k \frac{K_{PP}}{2} \frac{W}{L} (V_{DD} - |V_{THP}|)^2 \quad t_r = \frac{\Delta V}{I_{DP_{max}} / C_{IN}} = \frac{2C_{ox}L^2(k+1)[V_{DD} - (V_{THN} + |V_{THP}|)]}{kK_{PP}(V_{DD} - |V_{THP}|)^2}$$

$$C_{IN} = C_{ox}W \cdot L(k+1)$$

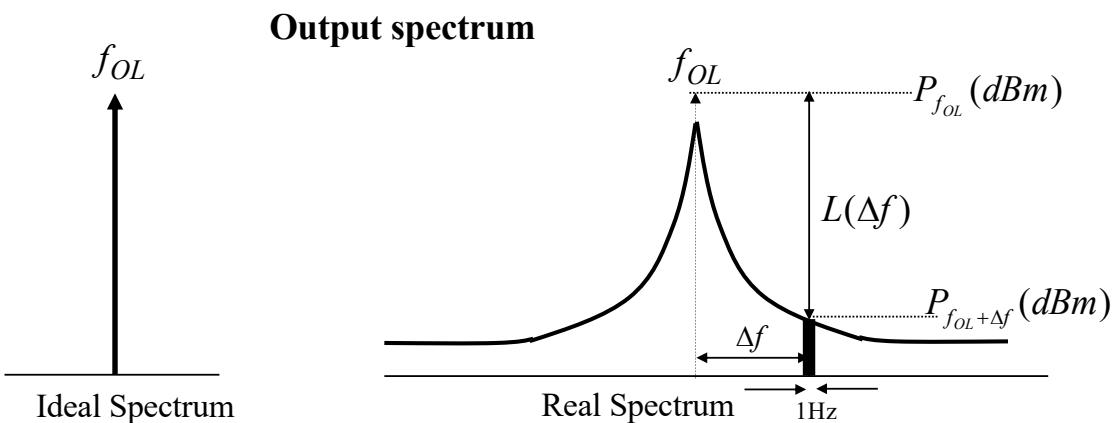
$$t_f = \frac{\Delta V}{I_{DN_{max}} / C_{IN}} = \frac{2C_{ox}L^2(k+1)[V_{DD} - (V_{THN} + |V_{THP}|)]}{K_{PN}(V_{DD} - V_{THN})^2}$$

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Tunning

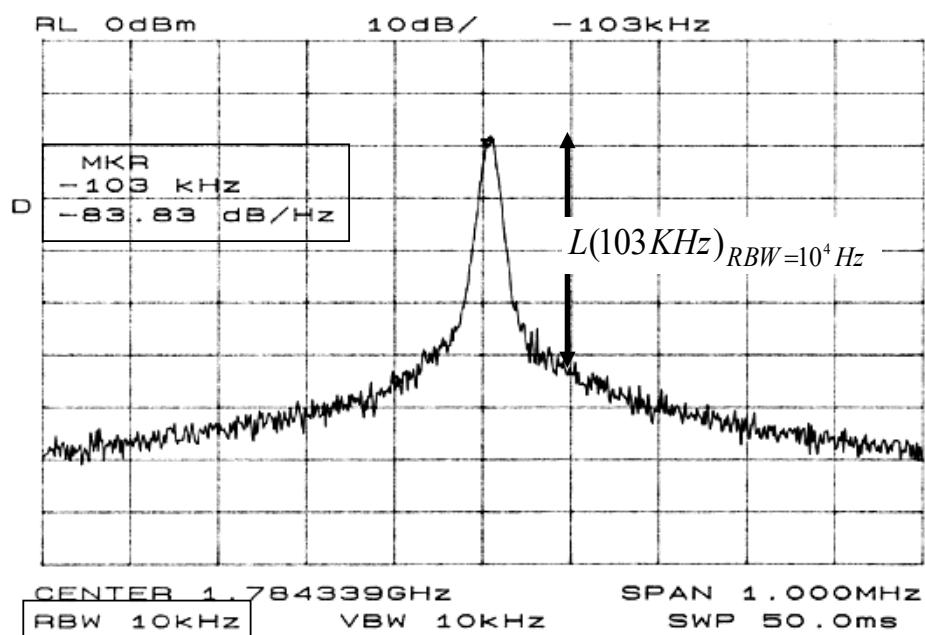


The spectrum is enlarged due to phase noise created by the VCO components

The phase noise is measured relatively to the power of the carrier in a 1Hz bandwidth and at a distance of Δf from F_{LO} .

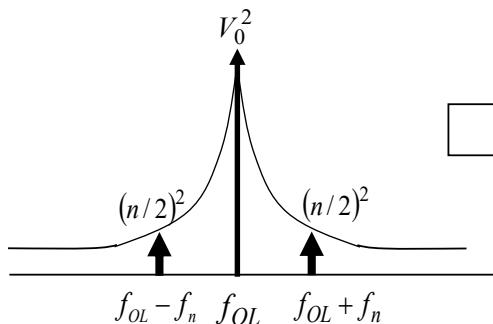
$$L(\Delta f)_{dBc} = 10 \log \left(\frac{P_{f_{LO} \pm \Delta f}(W)}{P_{f_{LO}}(W)} \right) = P_{f_{LO} \pm \Delta f} \text{ (dBm)} - P_{f_{LO}} \text{ (dBm)}$$

Exemple of a phase noise measurement

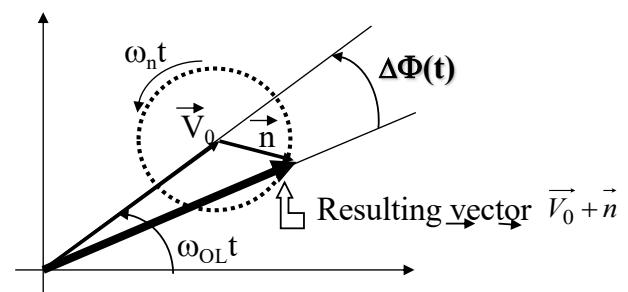


$$L(\Delta f)_{RBW=1Hz} = L(\Delta f)_{RBW=10^4} - 10 \log(RBW) = -43dB - 40dB = -83dBc$$

Time domain representation of the phase noise generated by $V_o(t)$

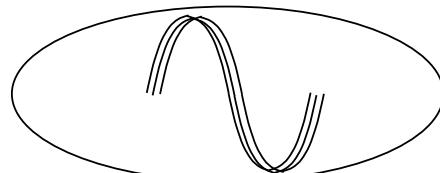


Frequency representation



Fresnel diagram representation

$$V_o(t) = (V_0) \cos(\omega_{OL})t + \frac{n}{2} [\cos(\omega_{OL} + \omega_n)t + \Psi_1] + \frac{n}{2} [\cos(\omega_{OL} - \omega_n)t + \Psi_2] \approx V_0(1 + a(t)) \cos[\omega_{OL}t + \Delta\Phi(t)]$$

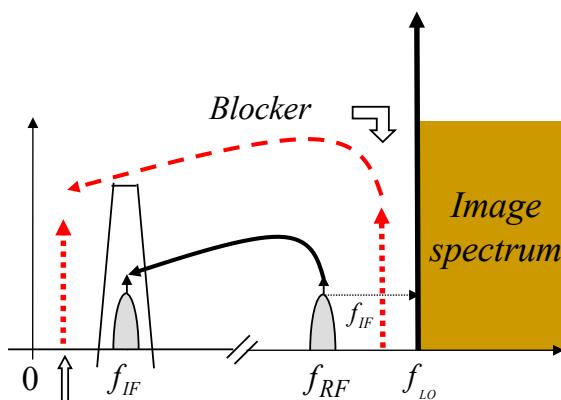


$$\Delta\Phi_{\max} \propto n/V_0$$

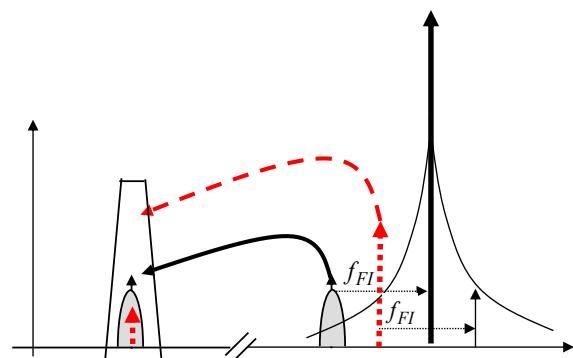
Time representation of the output signal $V_o(t)$ with phase jitter

$\Delta\Phi(t)$ is a random process.

Effect of the phase noise on the blocker behavior in the frequency transposition process



The blocker is filtered
by the IF filter

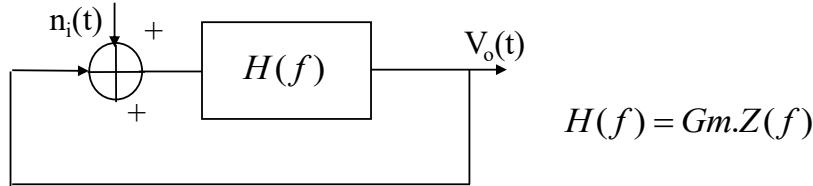


The blocker is transposed
by a phase noise harmonic
which is at $f_{blk} + f_{IF}$

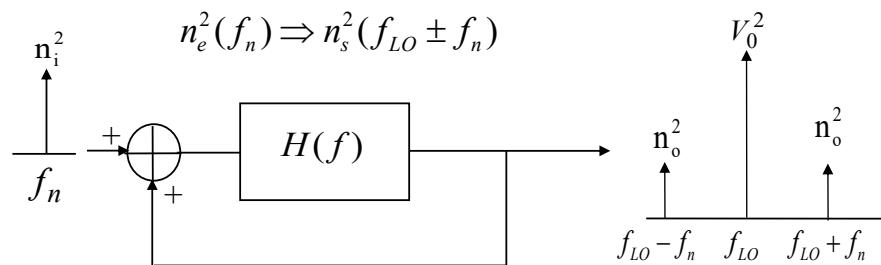
Phase noise must be as low as possible

1st order approximation

- Noise generated in the signal path



1st step: The noise is transposed around the f_{LO} by the amplifier NL :



2nd step : The noise is shaped by $H(f)$: $n_o^2(f) = n_i^2(f) \cdot \left| \frac{H(f)}{1+H(f)} \right|^2$

- by using the Mean value theorem $\left(\frac{dH}{df} \right)_{f_{OL}} = \frac{H(f_{OL} + f_n) - H(f_{OL})}{(f_{OL} + f_n) - (f_{OL})}$

$$\left| \frac{n_o(f_{LO} + f_n)}{n_i(f_{LO} + f_n)} \right|^2 = \frac{|H(f_{LO} + f_n)|^2}{|1 + H(f_{LO} + f_n)|^2} \approx_{f_n \ll f_{LO}} \frac{\left| H(f_{LO}) + f_n \frac{dH(f)}{df} \Big|_{f_{LO}} \right|^2}{\left| 1 + H(f_{LO}) + f_n \frac{dH(f)}{df} \Big|_{f_{LO}} \right|^2}$$

- by considering $H(f_{OL}) = -1$ (start-up conditions), and $f_n \left(\frac{dH}{df} \right)_{f_{OL}} \ll 1$ then we have:

$$\left| \frac{n_o(f_{LO} + f_n)}{n_i(f_{LO} + f_n)} \right|^2 \approx \frac{1}{f_n^2 \left| \frac{dH(f)}{df} \Big|_{f_{LO}} \right|^2} \quad \text{which gives with } H(f) = |H(f)| \exp[j\Phi(f)]:$$

$$\left| \frac{n_o(f_{LO} + f_n)}{n_i(f_{LO} + f_n)} \right|^2 \approx \frac{1}{f_n^2 \left[\left(\frac{d|H(f)|}{df} \Big|_{f_{LO}} \right)^2 + \left(\frac{d\Phi}{df} \Big|_{f_{LO}} \right)^2 \right]} \approx \frac{1}{f_n^2 \left(\frac{d\Phi}{df} \Big|_{f_{LO}} \right)^2} \quad \begin{aligned} &\text{because in a LC network (cf slide 120)} \\ &\text{we have: } \left(\frac{d|H(f)|}{df} \right)_{f_{OL}} \ll \left(\frac{d\Phi}{df} \right)_{f_{OL}} \end{aligned}$$

- which gives with $Q = -\frac{f_{OL}}{2} \left(\frac{d\Phi}{df} \right)_{f_{OL}}$ for a LC network $\rightarrow \left| \frac{n_o(f_{LO} + f_n)}{n_i(f_{LO} + f_n)} \right|^2 \approx \frac{1}{4Q^2} \left(\frac{f_{LO}}{f_n} \right)^2$

VCO

Phase Noise Origin

VCO

Elements for demonstration: $H(f) = |H(f)| \exp(j\Phi(f))$

$$\left| \frac{dH(f)}{df} \right|_{f_{LO}}^2 = \left| \frac{d(|H(f)| \exp(j\Phi(f)))}{df} \right|_{f_{LO}}^2$$

$$\left| \frac{dH(f)}{df} \right|_{f_{LO}}^2 = \left| \frac{d|H(f)|}{df} \right|_{f_{LO}} \exp(j\Phi(f_{LO})) + j|H(f_{LO})| \exp(j\Phi(f_{LO})) \frac{d\Phi}{df} \Big|_{f_{LO}}^2$$

We have: $H(f_{LO}) = -1$ which means $|H(f_{LO})| = 1$ and $\exp(j\Phi(f_{LO})) = -1$

$$\left| \frac{dH(f)}{df} \right|_{f_{LO}}^2 = \left| -\frac{d|H(f)|}{df} \Big|_{f_{LO}} - j \frac{d\Phi}{df} \Big|_{f_{LO}} \right|^2 = \left(\frac{d|H(f)|}{df} \Big|_{f_{LO}} \right)^2 + \left(\frac{d\Phi}{df} \Big|_{f_{LO}} \right)^2$$

As: $\frac{d|H(f)|}{df} \Big|_{f_{LO}} \ll \frac{d\Phi}{df} \Big|_{f_{LO}}$ (see Bode diagram)

$$\left| \frac{dH(f)}{df} \right|_{f_{LO}}^2 = \left(\frac{d\Phi}{df} \Big|_{f_{LO}} \right)^2$$

RLC //, we have : $Y(\omega) = \frac{1}{Z(\omega)} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C$

For $\Delta\omega = \omega - \omega_{LO} \ll \omega_{LO}$: $Y(\omega = \omega_{LO} + \Delta\omega) = \frac{1}{R} + 2j\Delta\omega C$

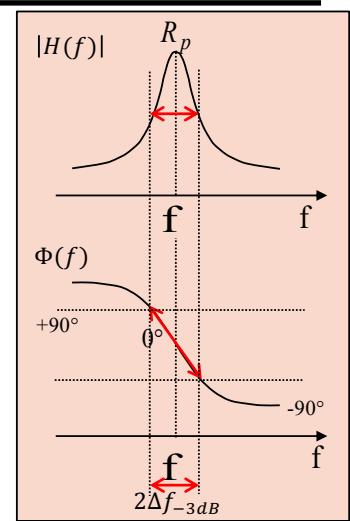
Phase: $\Phi_Z(\omega) = -\Phi_Y(\omega) = -\text{atan}(2\Delta\omega RC) = -2\Delta\omega RC$

$$\Rightarrow \frac{d\Phi}{d\omega} \Big|_{\omega_{LO}} = \frac{\Phi_Z(\omega_{LO} + \Delta\omega) - \Phi_Z(\omega_{LO} - \Delta\omega)}{(\omega_{LO} + \Delta\omega) - (\omega_{LO} - \Delta\omega)} = \frac{-2\Delta\omega RC - (-2(-\Delta\omega) RC)}{2\Delta\omega} = -2RC$$

As $Q = RC\omega_0$, we get $Q = -\frac{1}{2} \frac{d\Phi}{d\omega} \Big|_{\omega_{LO}} \omega_{LO} = -\frac{1}{2} \frac{d\Phi}{df} \Big|_{f_{LO}} f_{LO}$,

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RFIC



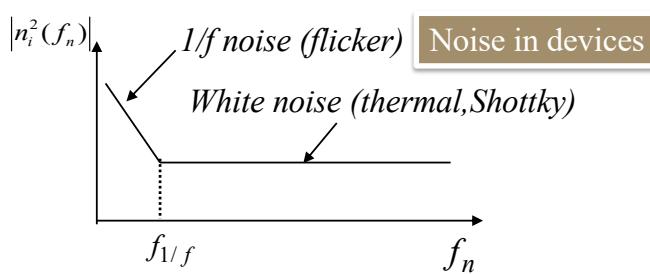
VCO

Phase Noise Origin

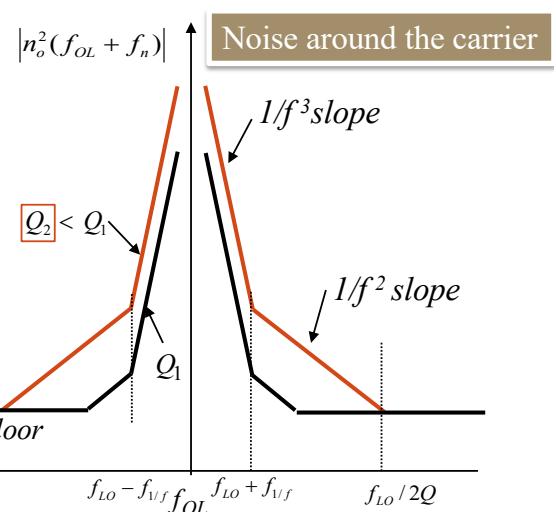
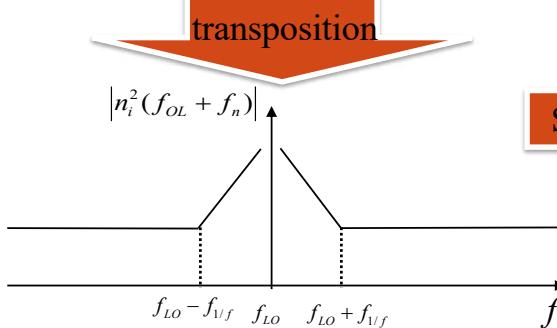
VCO

$$\left| \frac{n_o(f_{LO} + f_n)}{n_i(f_{LO} + f_n)} \right|^2 \approx \frac{1}{4Q^2} \left(\frac{f_{LO}}{f_n} \right)^2$$

The Q factor must be as high as possible
(low loss integrated inductors and capacitors are needed.
Big issue !!!)



- 1/f noise produces 1/f³ phase noise
- white noise produces 1/f² phase noise



RFIC

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Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO)
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

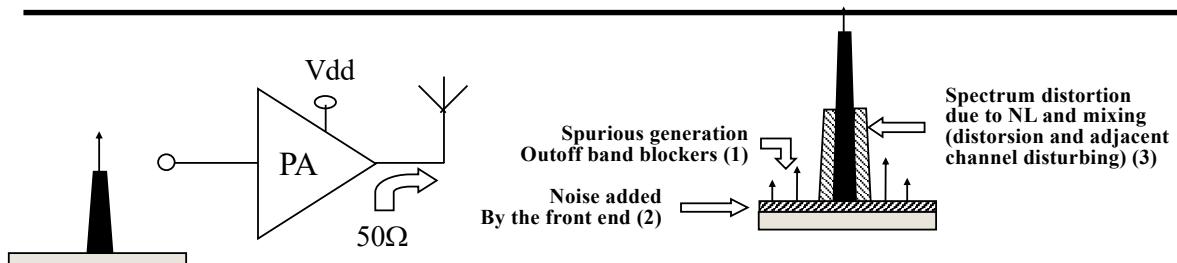
➤ Packaging

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Power Amplifier Requirements

PA



General Requirement

- IC : high power with low DC supply Vdd (high current must be dissipated)
- PA => 80% of the power consumption : **dissipating power** as low as possible
=> (high efficiency η)
- Generate low out off band noise (2) and spurs (1) (standards gives requirements)

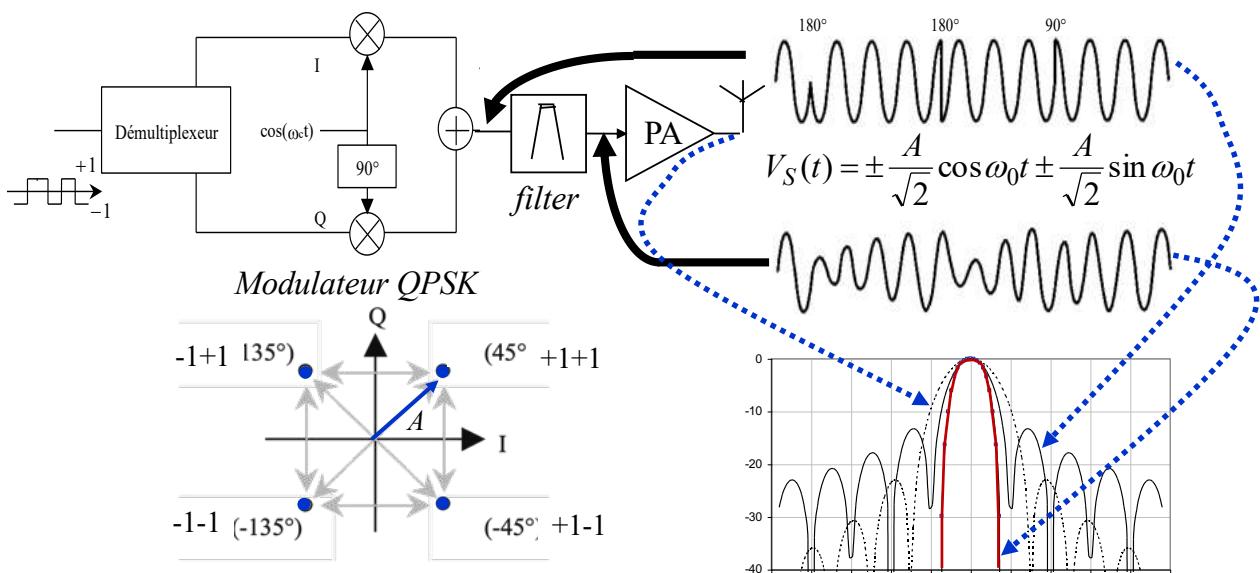
Non-linearity is a big issue, especially for M-QAM having high M (due to amplitude variation of the RF signal) (3)

- The gain must be highly linear (AM/AM distortion)
- The output phase should not depend on the input magnitude (AM/PM distortion)

Power Amplifier

PA

QAM modulation : magnitude variation in time domain



Signal magnitude and phase (constellation)

Spectrum of the signal before and after filtering

For QAM modulations (QPSK, M-QAM), the signal at the input does not have a constant envelope shaping. FSK modulations are preferred to alleviate non-linearity constraints

RFIC

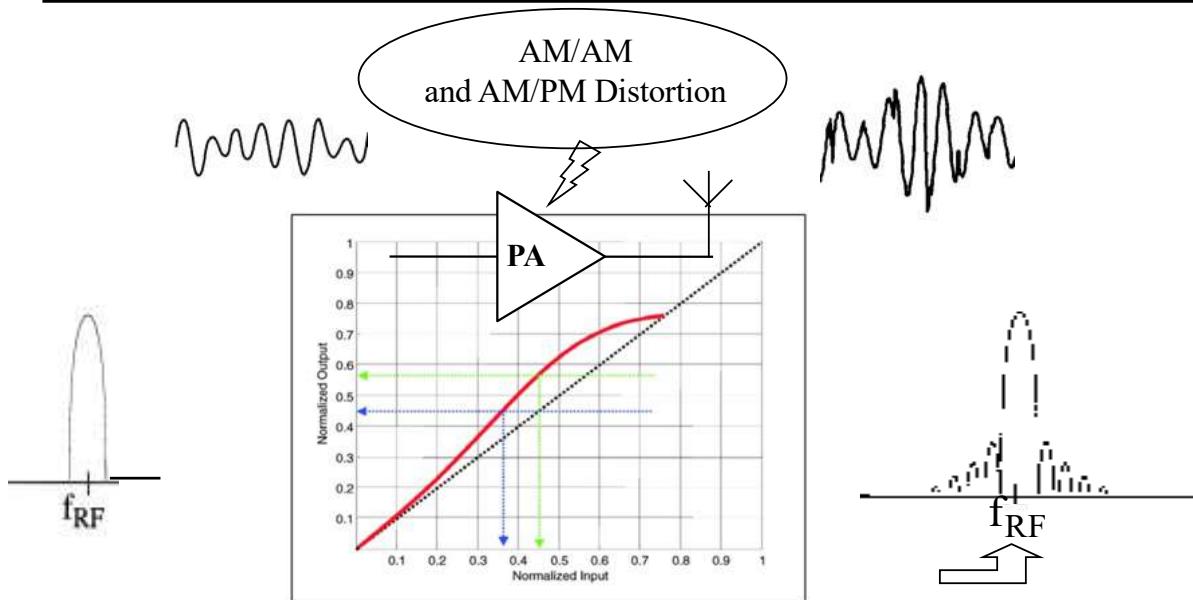
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Power Amplifier

PA

Non-Linearity effects on non-constant envelope signal



Output spectrum is enlarged : this will disturb the adjacent channel

Non-linearity compensation in PA for high M M-QAM modulation is an active research area

RFIC

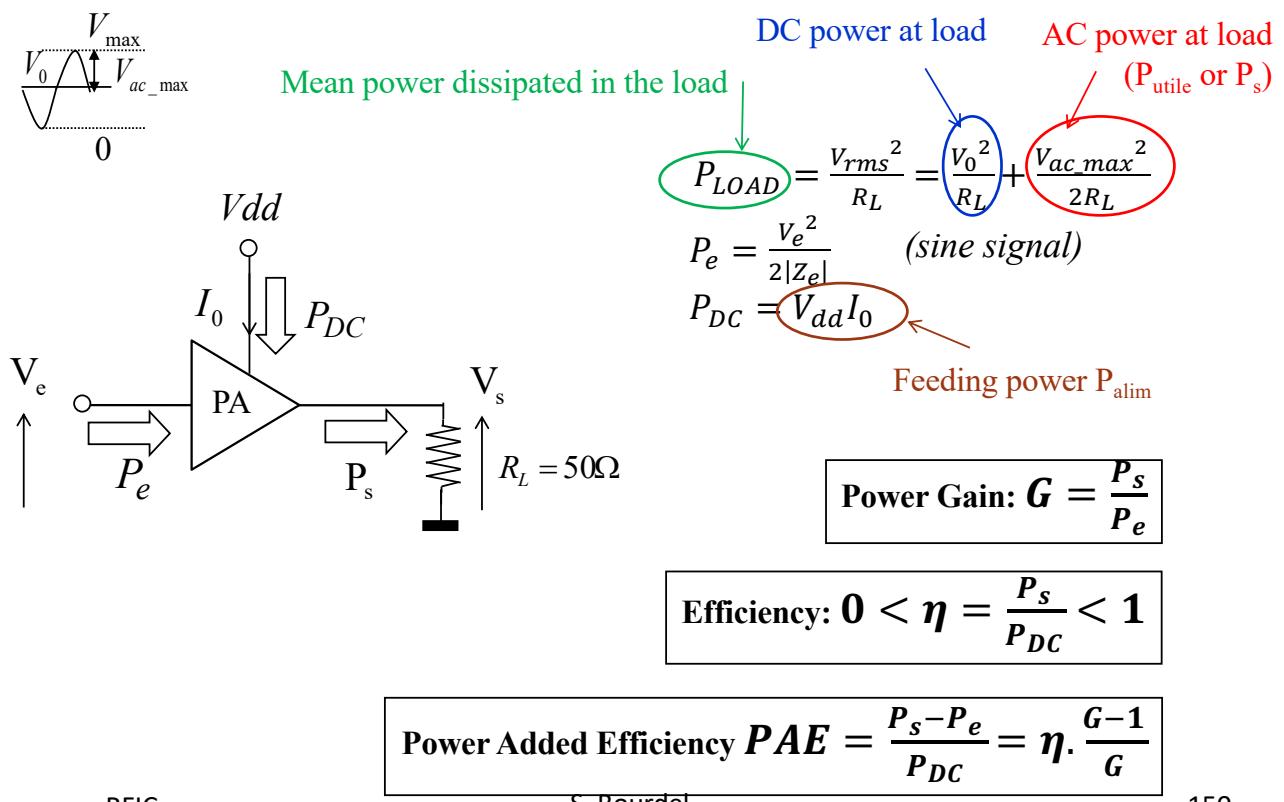
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Power Amplifier

PA

Power Efficiency



RFIC

S. Bourdel

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Power Amplifier

PA

Main Issue

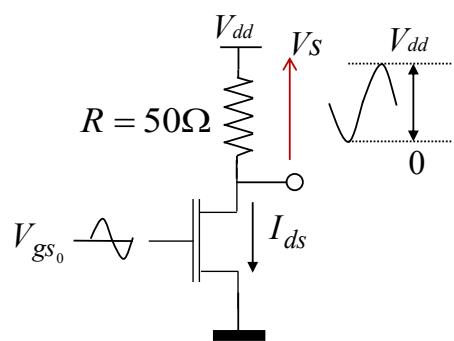


How to deliver a large amount of power (1W)
to a 50Ω impedance (antenna) with a low V_{dd} ?



The CS topology is the best regarding power gain and input-output isolation

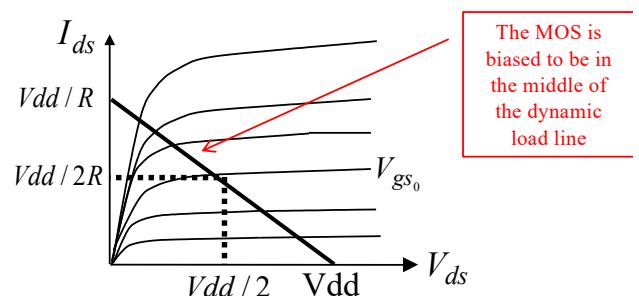
A- 1st solution : with the load R in the drain. V_{gs0} is set so as $I_{ds0} = V_{dd}/2.R$ (A class)



$$P_s = \frac{V_{rms}^2}{R} = \frac{(V_{peak}/\sqrt{2})^2}{R}$$

$$P_s = \frac{(V_{dd}/2)^2}{2.50} = 1W$$

RFIC



- The load must be connected to the supply
 - High V_{dd} is needed. Big issue in IC !!!!
 - The MOS is highly stressed
- S. Bourdel

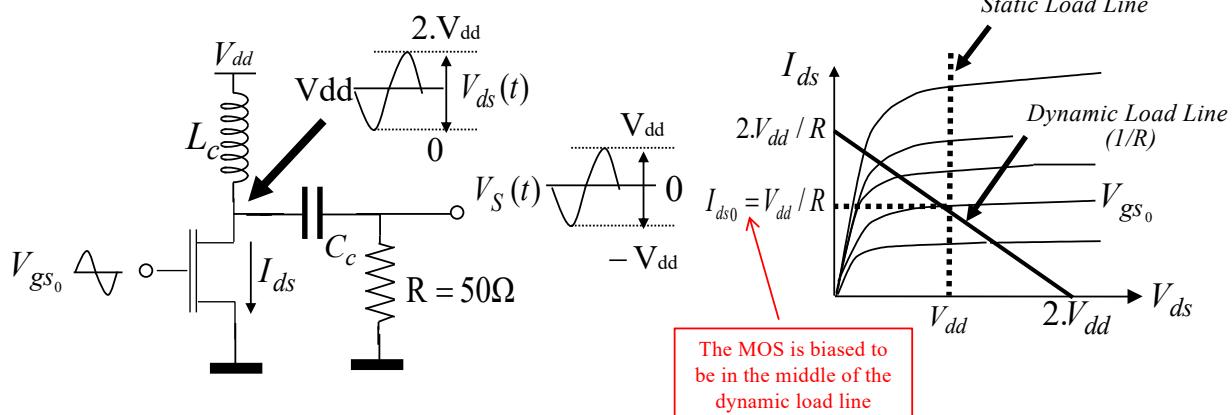
151

Power Amplifier

Main Issue

B – 2nd solution: High pass filtering L_C-C_c (V_{gs0} is set so as I_{ds0}=V_{dd}/R)

The choke inductor L_c can be seen as the current generator having the ability of providing a constant current while the voltage polarity changes at its terms. The C_c removes the DC component => V_s is around 0V



$$P_S = \frac{V_{dd}^2}{2.50} = 1W \quad \boxed{V_{dd} \geq 10V} \quad \left\{ \begin{array}{l} \text{• The load can be connected to the ground} \\ \text{• } V_{dd} \text{ can be divided by 2 as compared to the resistive load on drain} \\ \text{• The MOS is highly stressed.} \end{array} \right.$$

RFIC

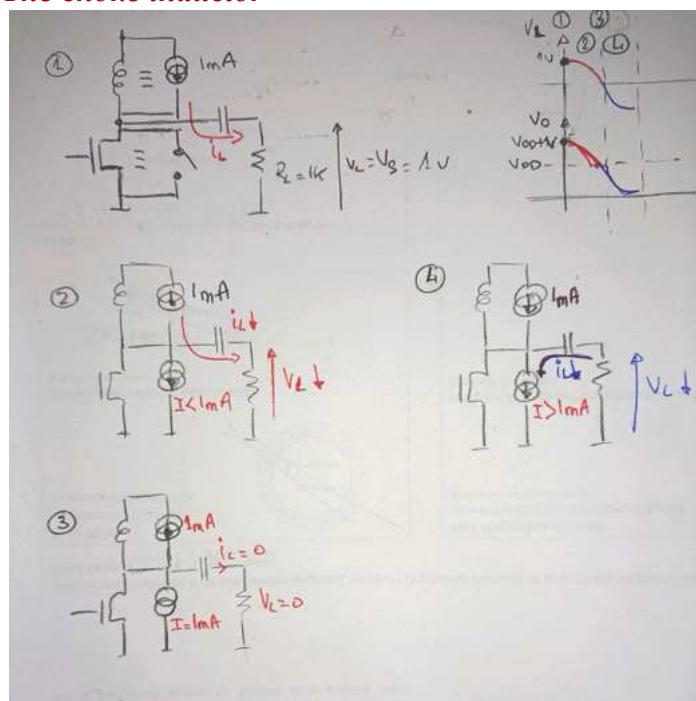
S. Bourdel

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Power Amplifier

Main Issue

B – 2nd solution: High pass filtering L_C-C_c (V_{gs0} is set so as I_{ds0}=V_{dd}/R) The choke inductor



RFIC

The choke inductor L_c can be seen as the current generator having the ability of providing a constant current while the voltage polarity changes at its terms. The C_c removes the DC component => V_s is around 0V

S. Bourdel

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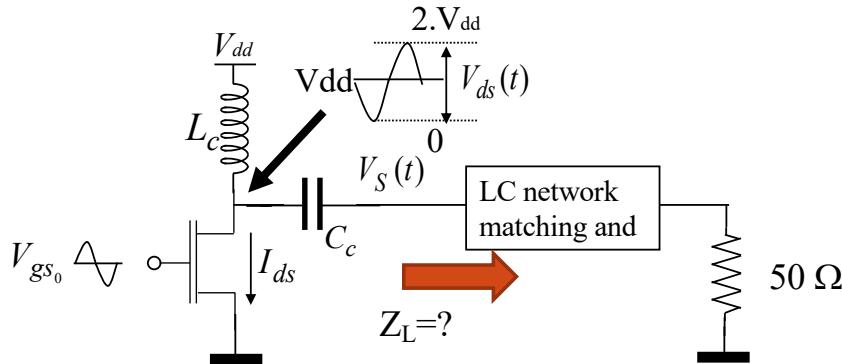
Power Amplifier

PA

Main Issue

B – 2nd solution: High pass filtering L_c-C_c (V_{gs0} is set so as I_{ds0}=Vdd/R)

Question : It is my first PA design and I use a matching network to match the output of my PA to the 50 Ω antenna. What is Z_L, the impedance seen at the PA drain ? What is the output power for a MOS having r_{ds}=250 Ω and V_{dd}=3.3V ? Conclude.



$$Z_L = r_{ds}$$

$$P_S = \frac{V_{dd}^2}{2 \cdot r_{ds}} = \frac{10}{500} = 20 \text{ mW}$$

RFIC

S. Bourdel

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The output of a PA is not power matched. Otherwise you can't deliver output power. This is obvious because the power comes from the supply, not from the signal. The power matching only makes sense for passive devices...

Power Amplifier

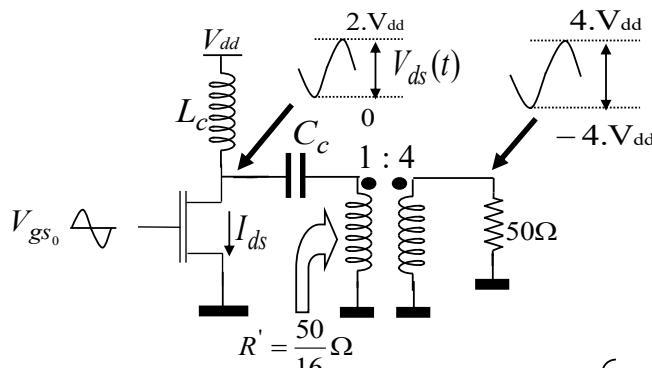
PA

Main Issue

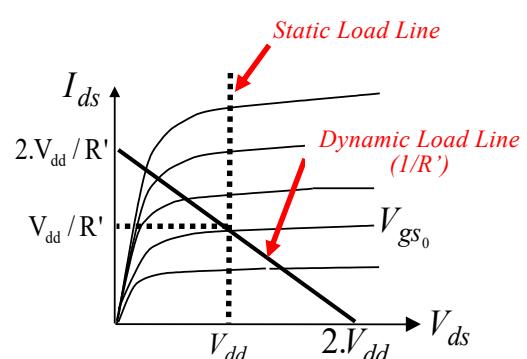
C – 3rd solution: high pass filtering L_c-C_c + step down transformer

- The impedance seen by the device is R' < R
- The power delivered by the device is provided by a high current and a low voltage

V_{gs0} is set so as I_{ds0}=Vdd/R'



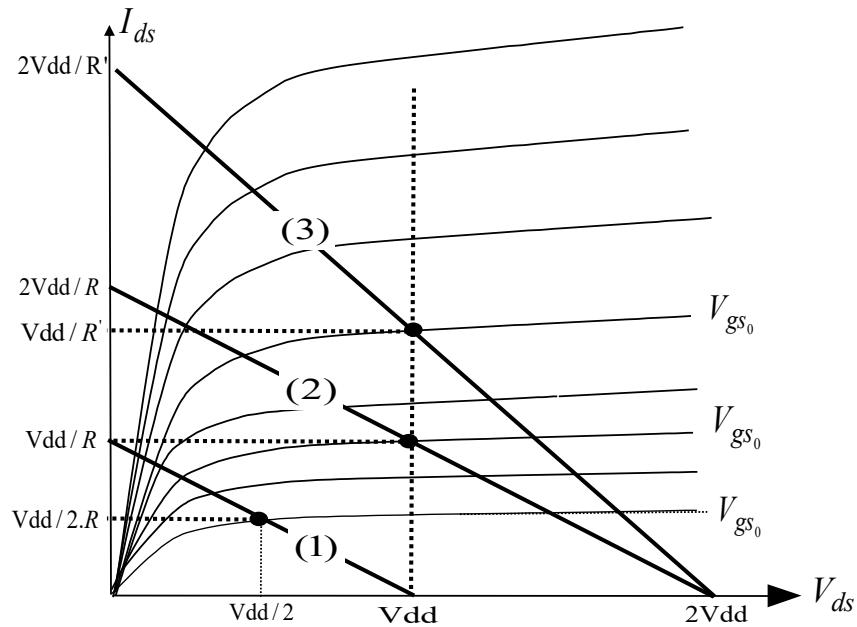
$$P_S = \frac{(4V_{dd})^2}{2.50} = 1W \quad \square \quad V_{dd} \geq 2.5V$$



- {
 - The load can be connected to the ground
 - Low V_{dd} (matched to IC constraints)
 - The MOS is no more stressed by high voltage.

This is the most often used topology

Load Line



Evolution of the load line for the 3 different topologies (1), (2) and (3)

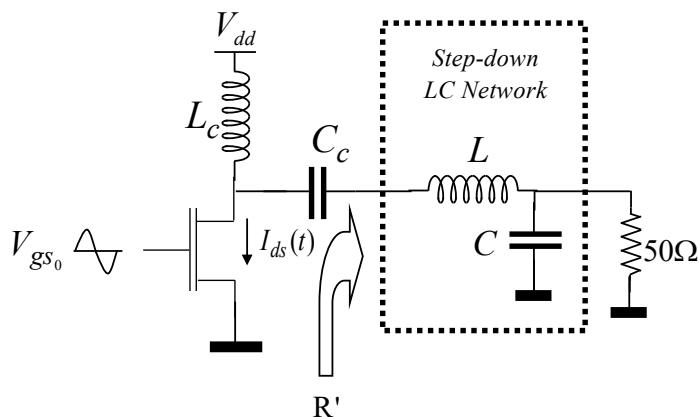
RFIC

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Main Issue

D – 4th solution: high pass filtering L_c- C_c + step down LC network (narrow band)



Exercise

The DC supply is $V_{dd} = 2V$. Calculate the LC network to deliver $P_s = 1W$ @ 2GHz in a 50Ω Impedance (A class).

Give the DC current $I_{ds0}(V_{gs0})$

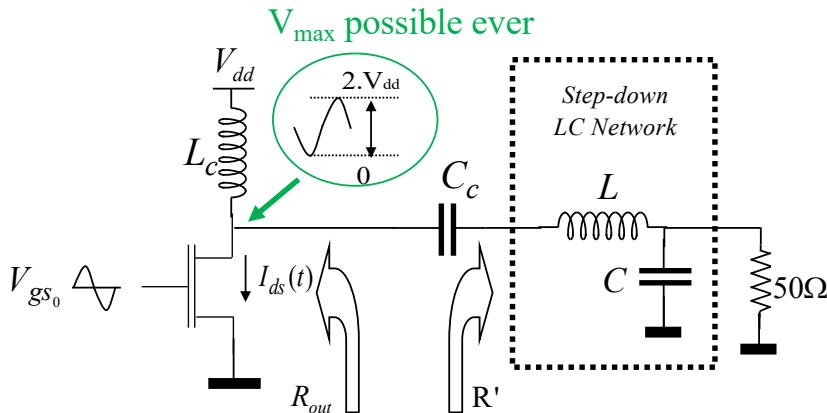
RFIC

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Main Issue

D – Power Matching (large signal) Vs Small signal matching



Small signal matching

$$Z' = Z_{out} * = R_{out} > 50\Omega$$

$$P_{S_small} = \frac{V_{out_max}^2}{2.R_{out}}$$

Large signal matching

$$Z' = R' = R_{out}/N < 50\Omega$$

$$P_{S_large} = \frac{V_{out_max}^2}{2.R'} = N \frac{V_{out_max}^2}{2.R_{out}} = N.P_{S_small}$$

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Small signal

- No reflexion
- Better efficiency

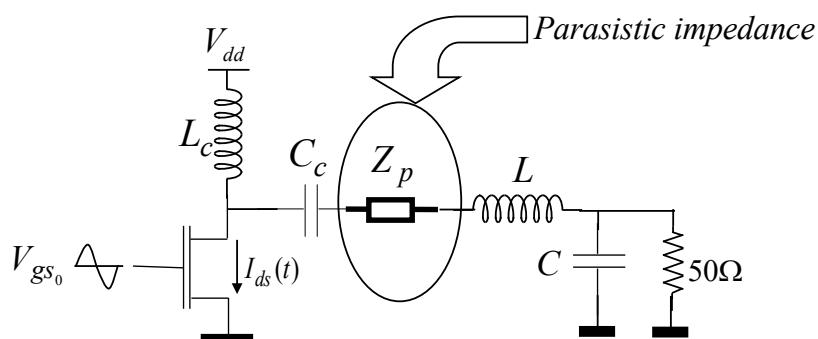
Large Signal

- Higher power
- Lower efficiency

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Effects of losses in the network due to interconnection

Because the power is delivered through very high current, this power is highly dependant on the parasitic impedance of the interconnections.



Exercise

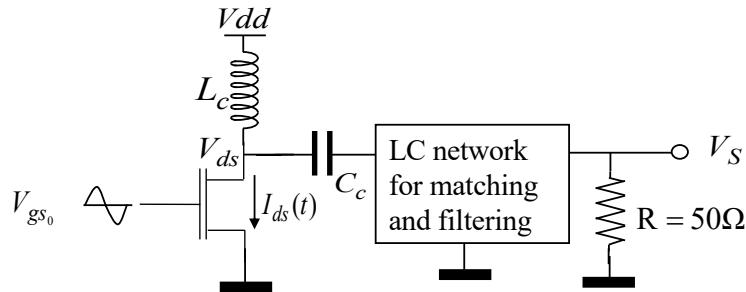
For the same amplifier sized in the previous exercise (previous slide), evaluate the Power losses in % of the ideal delivered power if $Z_p = 0.5\Omega$ if the amplifier is re-biased in the center of its load line.

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General configuration



- The LC network allows :
 - Lowering the real part of the impedance seen by the MOS
 - Filtering harmonics at the output
 - Filtering $I_{DS}(t)$ to obtain $V_{DS}(t)$ so as
 - getting a sine (sinusoidal classes)
 - or having an optimized shape (non-sinusoidal classes)

Whatever the class, if $V_{ds_min} \sim 0$ (low R_{ON} of the MOS) and because the mean value of $V_{ds}(t)$, $V_{ds_mean} = V_{dd}$, then $V_{ds_max} = 2V_{dd}$:

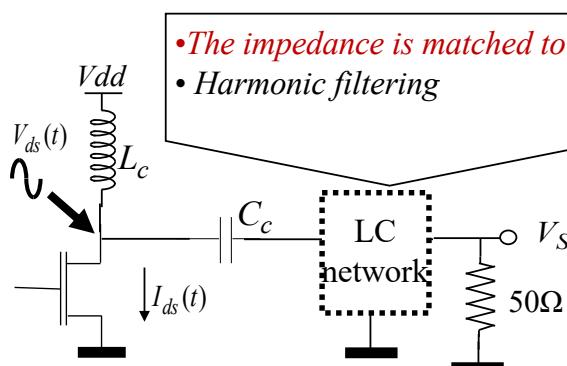
The magnitude of $V_{ds}(t)$ is closed to V_{dd} at maximal power.

Amplifier Operating Classes

Sinusoidal Classes (A,B,C)

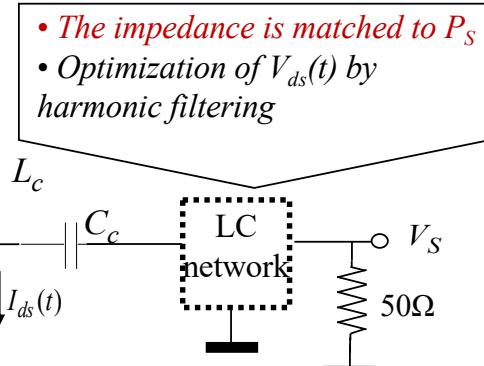
$V_{ds}(t)$ is a sine wave with mean value = V_{dd} & magnitude = V_{dd} (LC filtering of the current $I_{ds}(t)$)

- A and B Classes : linear with medium η**
- C Classe : non-linear and high η**



Non-Sinusoidal Classes (E,F)

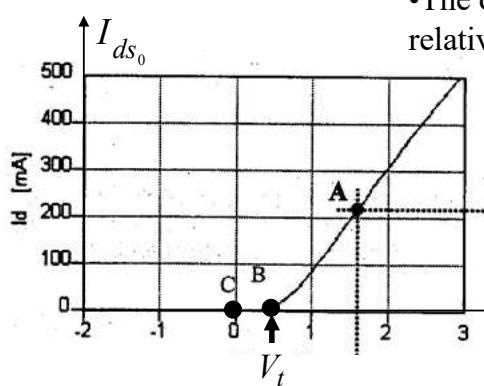
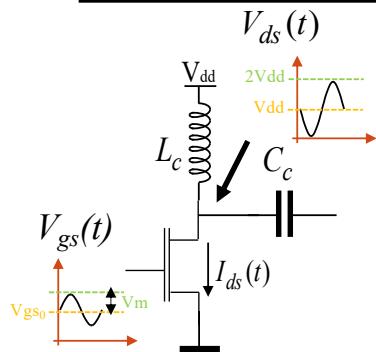
The shape of $V_{ds}(t)$ is optimized regarding $I_{ds}(t)$ Highly non-linear operating classes with very high efficiency



Power Amplifier

PA

Sinusoidal Classes



- The voltage gate is a sine :

$$V_{gs}(t) = V_{gs_0} + V_m \sin \omega_0 t$$

- The voltage V_{ds} is a sine :

$$V_{ds}(t) = V_{dd} - V_{dd} \sin \omega_0 t$$

- The current $I_{ds}(t)$ is a sine (A class) or is a part of a sine (B and C class)

- The operating class depends on the DC gate voltage V_{gs0} relatively to the threshold voltage V_t

- A Class : $V_{gs_0} > V_t$ and $V_m \leq V_{gs_0} - V_t$
The MOS is always ON

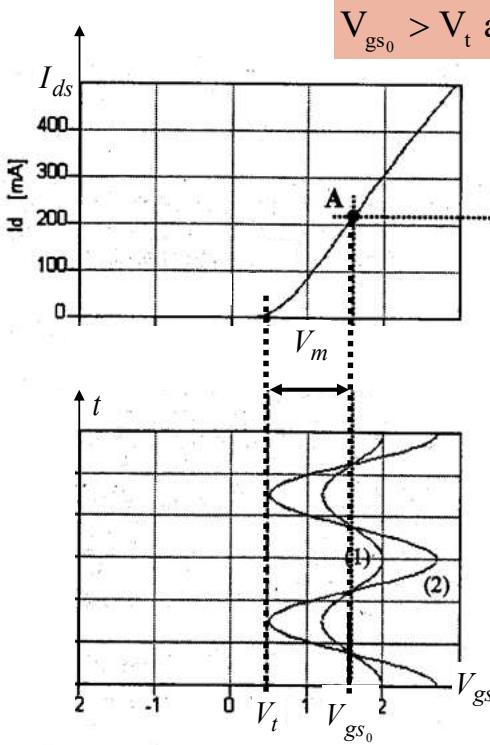
- B Class : $V_{gs_0} = V_t$
The MOS is ON during half a period

- C Class : $V_{gs_0} < V_t$ and $V_m \geq V_t - V_{gs_0}$
Time conduction is lower than half a period

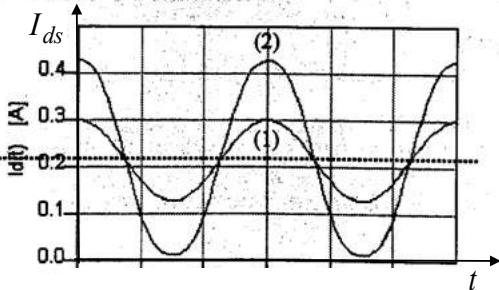
Power Amplifier

PA

A Class



$$V_{gs_0} > V_t \text{ and } V_m \leq V_{gs_0} - V_t$$



- The current I_{ds} is quasi a sine
- Linear operation
- Theoretical maximal efficiency ($V_m = V_{gs_0} - V_t$)

$$\eta = 50\%$$

→ Explanation: next slide

Power Amplifier

A Class

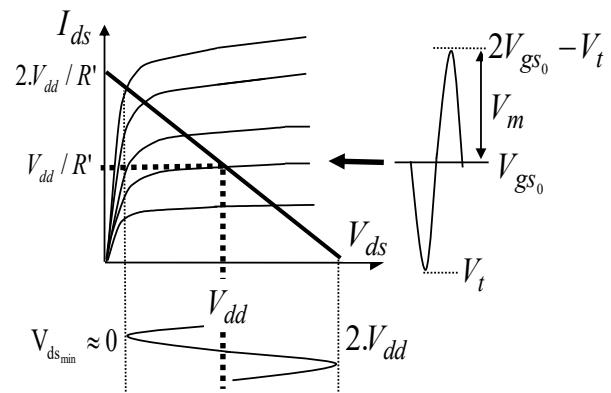
➤ Derivation of the maximal efficiency. Biasing condition :

❖ condition for input maximal dynamic:

$$V_m = V_{gs_0} - V_t$$

❖ condition for maximal linear output dynamic:

$$I_{ds0} = I_{ds}(V_{gs_0}) = \frac{V_{dd}}{R}$$

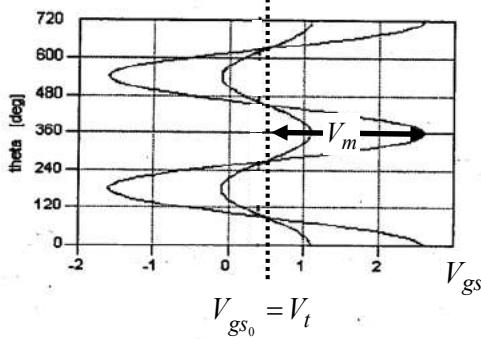
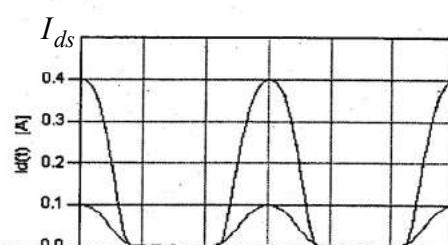
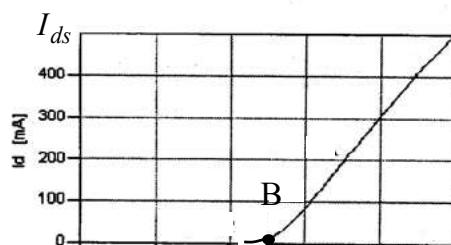


$$\eta = \frac{P_S}{P_{DC}} = \frac{\frac{V_{eff}^2}{R'}}{V_{dd} \cdot I_0} = \frac{\frac{V_{dd}^2}{2R'}}{V_{dd} \cdot \frac{V_{dd}}{R'}} = \frac{1}{2} = 50\% \quad \text{actually } V_{ds_min} > 0V \quad \Rightarrow \eta < 50\%$$

Power Amplifier

B Class

$$V_{gs_0} = V_t$$



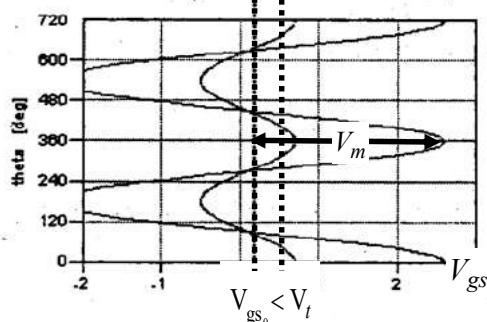
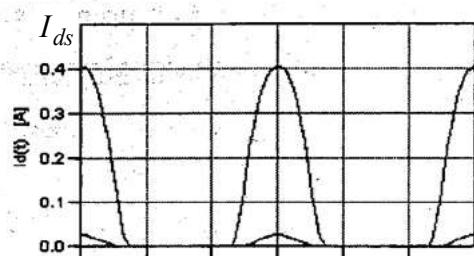
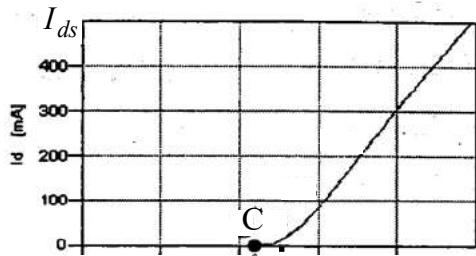
- The current I_{ds} is half a sine
- The behavior is less linear
- Theoretical max efficiency $\eta = 78\%$
Actually $V_{dsmin} > 0V \quad \Rightarrow \eta < 78\%$

→ *Explanation: next next slide*

Power Amplifier

C Class

$$V_{gs_0} < V_t$$



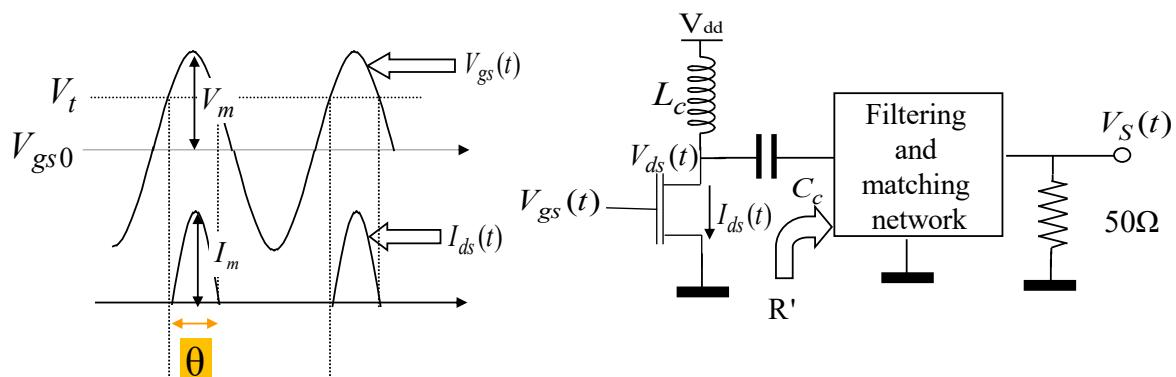
- The current I_{ds} is part of a sine
- The behavior is non-linear
- Theoretically $78\% < \eta < 100\%$

→ *Explanation: next slide*

Power Amplifier

Conduction Angle (θ) in B and C class

A- Conduction Angle θ



$$\cos\left(\frac{\theta}{2}\right) = \frac{V_t - V_{gs0}}{V_m}$$

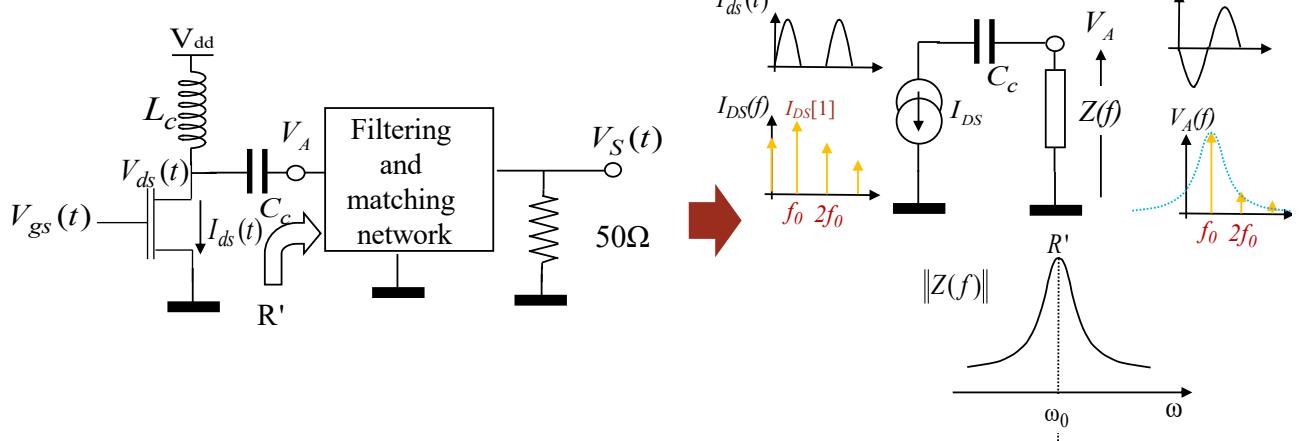
$$\theta = 2 \cdot \cos^{-1}\left(\frac{V_t - V_{gs0}}{V_m}\right)$$

- B Class : $V_{gs_0} = V_t$ $\Rightarrow \theta = \pi$
- C Class : $V_{gs_0} < V_t$ and $V_m \geq V_t - V_{gs0}$ $\Rightarrow 0^\circ < \theta < \pi$

Power Amplifier

Conduction Angle (θ) in B and C class

B- Harmonic Filtering



$$I_{DS}(f) = I_{DS}[0]\delta(0) + j \frac{I_{DS}[1]}{2}(\delta(f + f_0) - \delta(f - f_0)) + j \frac{I_{DS}[2]}{2}(\delta(f + 2f_0) - \delta(f - 2f_0)) + \dots$$

$$I_{DS}(f) = I_{DS}[0]\delta(0) + \sum_{n=0}^{+\infty} j \frac{I_{DS}[n]}{2}(\delta(f + nf_0) - \delta(f - nf_0)) = I_{DS}[0]\delta(0) + \sum_{n=0}^{+\infty} j I_{DS}(nf_0)$$

$$V_A(f) = I_{DS_AC}(f).Z(f) = j I_{DS}(f_0).Z(f_0) + j I_{DS}(2f_0).Z(2f_0) + \dots = j I_{DS}(f_0).R$$

$$V_A(t) = I_{DS}[1].\sin(\omega_0 t).R$$

RFIC

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Power Amplifier

Efficiency in B and C class

C- Derivation of the maximal efficiency $f(\theta)$.

- $V_{ds}(t) = V_{dd} - V_{dd} \sin(\omega_0 t)$

- $I_{ds}(t)$ is a part of a sine (periodical function) \Rightarrow Fourier series.

We show that the DC component $I_{ds}[0]$ and the magnitude of the first harmonic $I_{ds}[1]$ are equal to :

$$I_{ds}[0] = \frac{I_m}{\pi} \left\| \frac{\sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2}}{1 - \cos \frac{\theta}{2}} \right\| \quad \text{and} \quad I_{ds}[1] = \frac{I_m}{2\pi} \left\| \frac{\theta - \sin \theta}{1 - \cos \frac{\theta}{2}} \right\|$$

$$V_{ds}(t) = V_{dd} - V_{dd} \sin(\omega_0 t) = V_{dd} - R \cdot I_{ds}[1] \sin(\omega_0 t) \quad R: \text{resistor load}$$

$$\eta = \frac{P_S}{P_{DC}} = \frac{(1/2) \cdot R \cdot I_{ds}[1]^2}{V_{dd} \cdot I_{ds}[0]} = \frac{V_{dd} \cdot I_{ds}[1]}{2 \cdot V_{dd} \cdot I_{ds}[0]} = \frac{I_{ds}[1]}{2 \cdot I_{ds}[0]}$$

RFIC

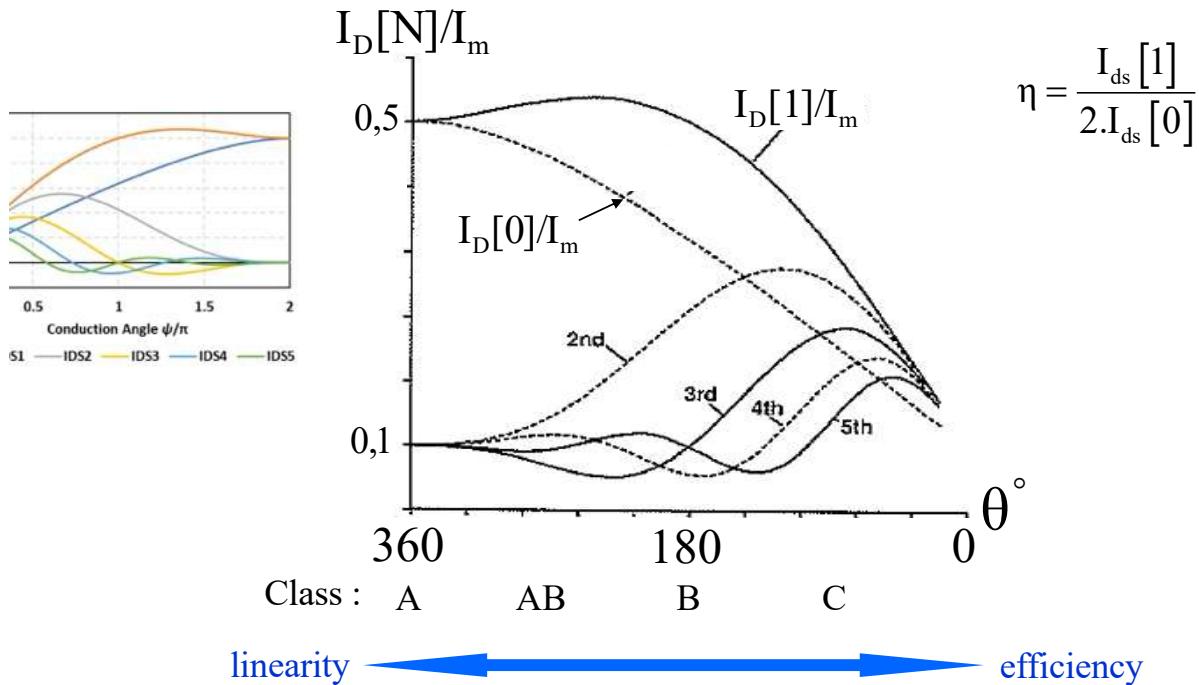
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Power Amplifier

PA

Magnitude of the harmonic ($I_D[N]$) de $I_{ds}(t)$



RFIC

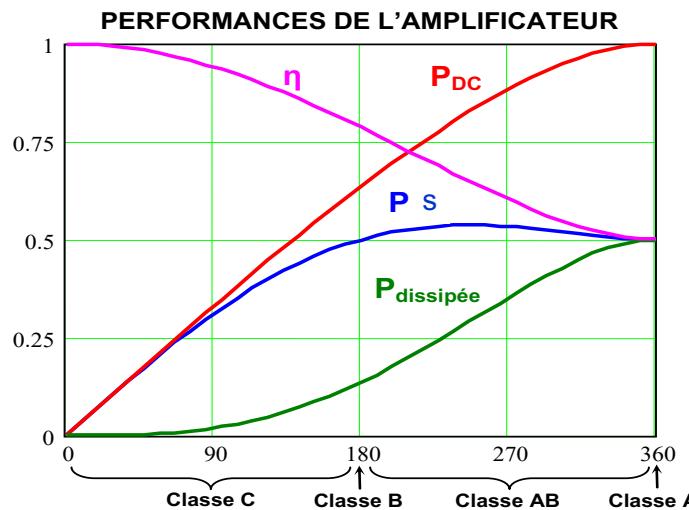
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Power Amplifier

PA

Efficiency in B and C class



DC Power (P_{DC}), Output Power (P_S), Power dissipated in the device (P_{dis})
and theoretical efficiency as a function of the conduction angle θ

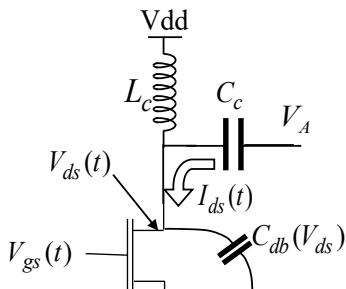
- Note : When θ decreased, η increases but in the same time the output power decreases (with constant I_m)

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Sinusoidal operating class : Sources of Non-Linearities



$$V_{gs}(t) = V_{gs0} + V_m \cos \omega t$$

1 – Linear Class (A and B class)

- Non-linearity of the transconductance $I_{ds} = f(V_{gs})$ (AM/AM)
- Non linearity of the diffusion capacitance $C_{db}(V_{ds})$ (AM/PM)

2 – Non-Linear Class (C)

- Same non-linearity as in A or B class + variation of the conduction angle with V_m (AM/AM) and (AM/PM)

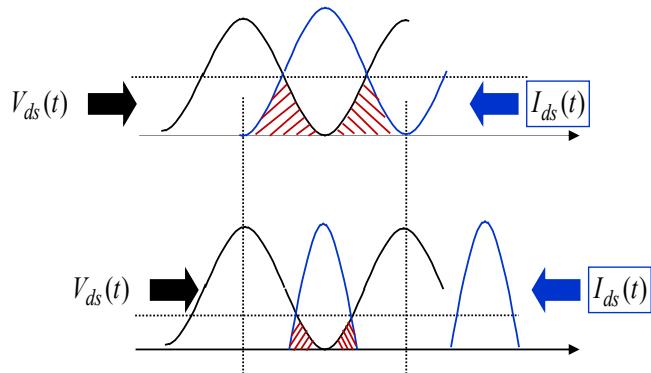
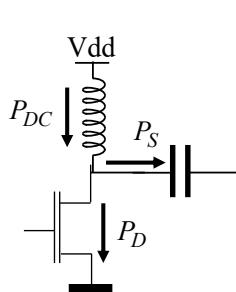
$$V_m \xrightarrow{\cos(\frac{\theta}{2})} \cos(\frac{\theta}{2}) = \frac{V_t - V_{gs0}}{V_m} \xrightarrow{I_{ds}[l]} I_{ds}[l] = f_{NL}(\theta) = f_{NL}(V_m) \xrightarrow{V_A = R \cdot I_{ds}[l]} V_A = f_{NL}(V_m)$$

The magnitude of $V_A(t)$ is a non-linear fonction of the magnitude V_m of $V_{gs}(t)$
due to the variation of the conduction angle with V_m

Power Amplifier

Efficiency limitation in sinusoidal class

The fact that the efficiency is lower than 100 % means that the mean power is dissipated into the MOS during the transition of $V_{ds}(t)$



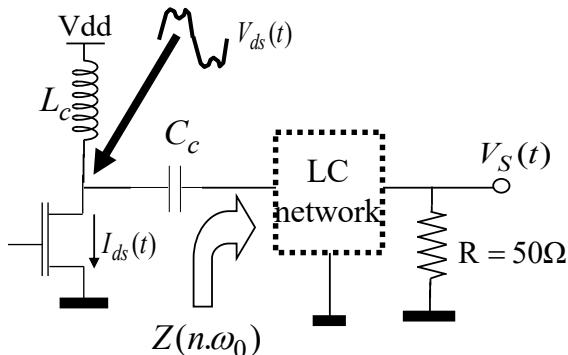
$$\eta = \frac{P_S}{P_{DC}} = \frac{P_S}{P_S + P_D} \quad P_D = \frac{1}{T} \int_0^T V_{ds}(t) \cdot I_{ds}(t) dt$$

➤A class example : $I_{ds}(t)$ is not null when $V_{ds}(t)$ exists
=> There is power consumption into the device during this time

High Efficient non-linear operating classes

In non-linear operating classes, the shape of $V_{ds}(t)$ is optimized regarding the current $I_{ds}(t)$ so as : **$V_{ds}(t)$ is near-zero when $I_{ds}(t)$ is non-zero.**

The shape of $V_{ds}(t)$ is achieved by combining odd or/and even harmonic ($n \cdot \omega_0$)
Selected (filtered) by the LC network which synthesize optimized impedance ($Z(n \cdot \omega_0)$)



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Power Amplifier

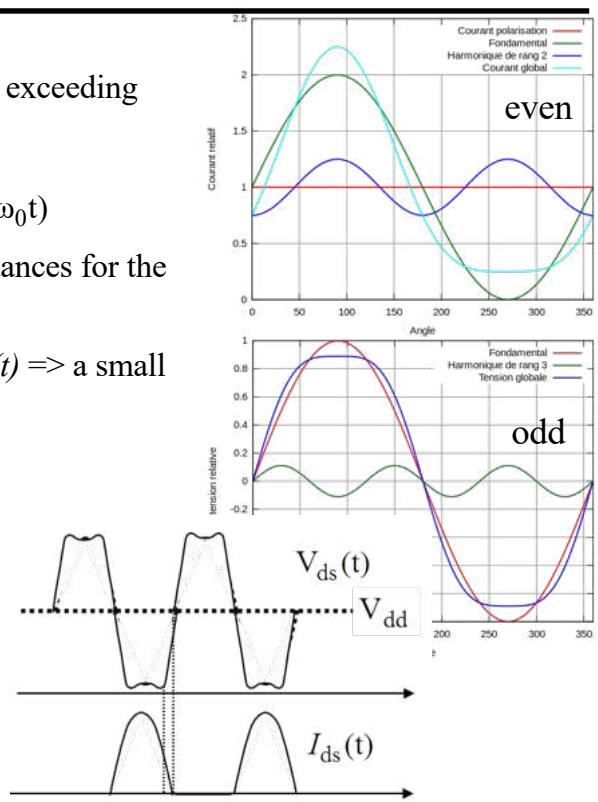
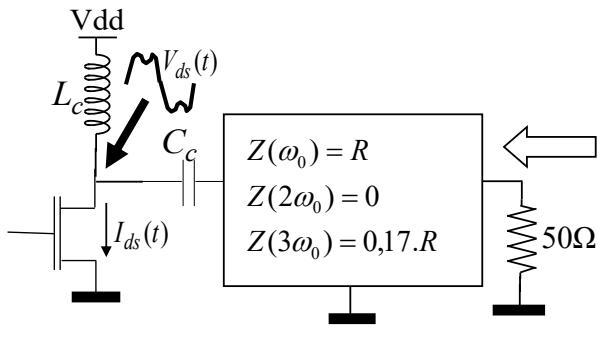
F class

- We want to maximize the fundamental without exceeding V_{dd} by adding odd harmonics

$$V_{ds}(t) \equiv V_{dd} + V_{dd} \cdot \sin(\omega_0 t) + (0.17 \cdot V_{dd}) \cdot \sin(3 \cdot \omega_0 t)$$

- The matching network achieves required impedances for the different harmonics and filters the output signal

- The overlapping is small between $V_{ds}(t)$ and $I_{ds}(t)$ => a small amount of power is dissipated inside the device.



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Linearization Technic

Sinusoidal Classes (A,B,C)

A and B Classes are quite linear but have low efficiency

Non-Sinusoidal Classes (E,F)

High efficiency and low linearity

Solution

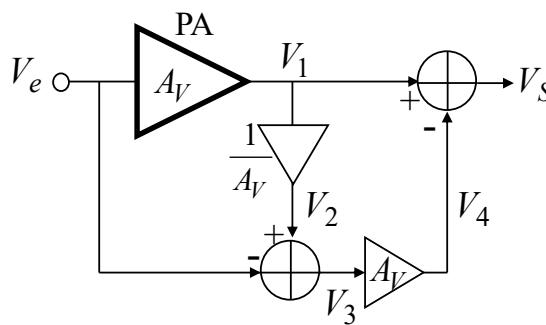
Non-Sinusoidal Classes + linearization techniques

Efficiency+ Linearity

Linearization Technic

Signal V_1 at the output of the non-linear PA is equivalent to the sum of a error signal V_d with the input signal V_e multiplied by the gain A_V :

$$V_1 = A_V \cdot V_e + V_d$$



The linearization system gives :

$$V_2 = \frac{1}{A_V} V_1 = V_e + \frac{V_d}{A_V} \quad (1/A_V < 1: no distortion)$$

$$V_3 = V_2 - V_e = \frac{V_d}{A_V}$$

$$V_4 = A_V \cdot V_3 = V_d$$

$$V_S = V_1 - V_4 = A_V \cdot V_e$$

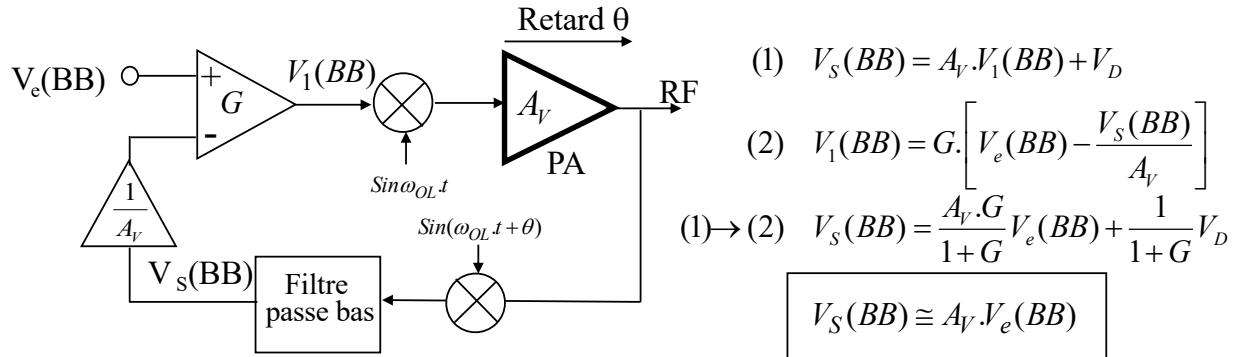
•**Pros.** : Stability whatever the delay in the loop

•**Cons.** : efficiency sensitive to mismatch and delays in the loop

Power Amplifier

Feedback Linearization Technique

This feedback system uses a loop back which can cause instability (especially at high frequency because the effect of the delay in the loop increases). The solution is to implement the loop back in baseband before the modulation process.



•Pros. : Less sensitive to gain mismatch and delay

•Cons. : Need a double loop for I/Q modulation
--> Increases complexity and consumption

Integrated RF Front-End

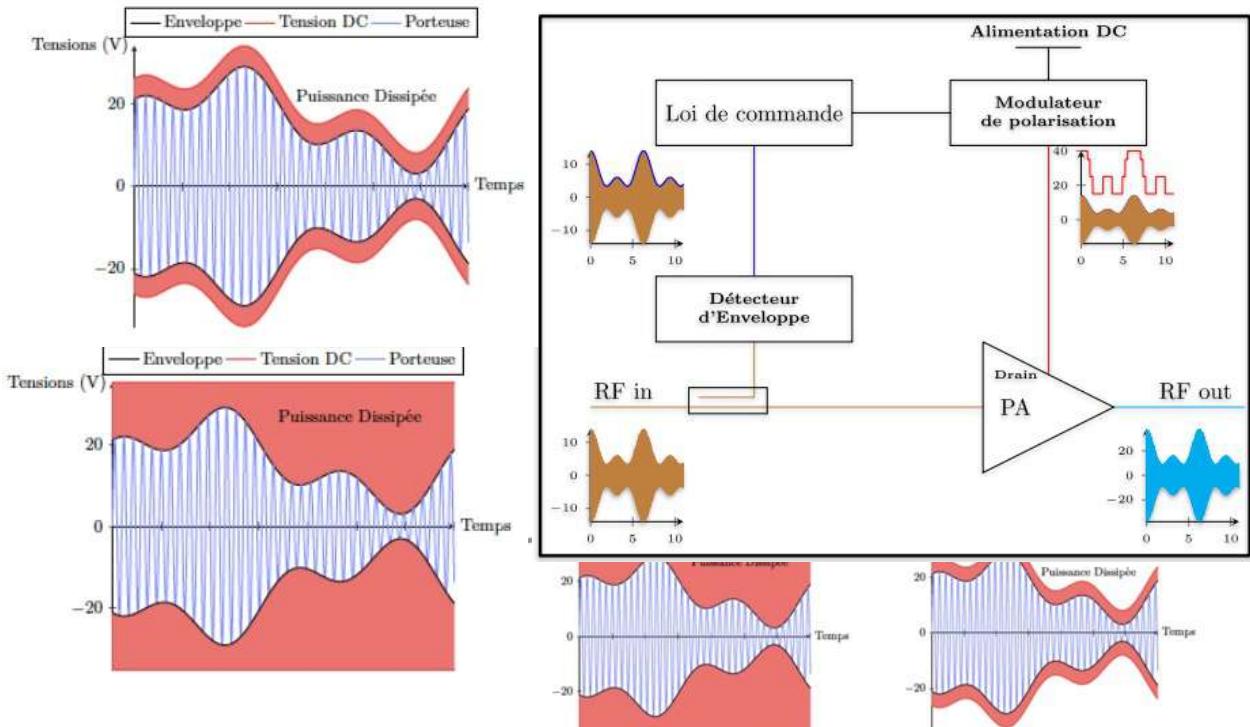
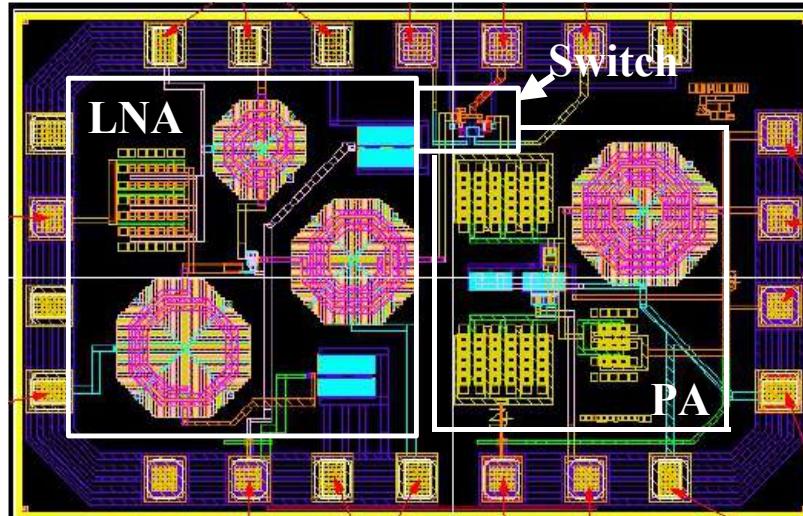
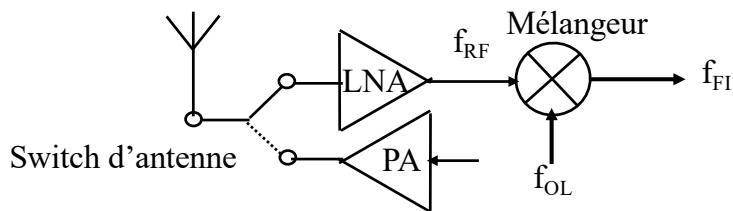


Figure 4 : Signaux amplifiés avec une polarisation fixe et polarisation modulée

Integrated RF Front-End



RFIC

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Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

➤ Design methodologies for RF building blocs

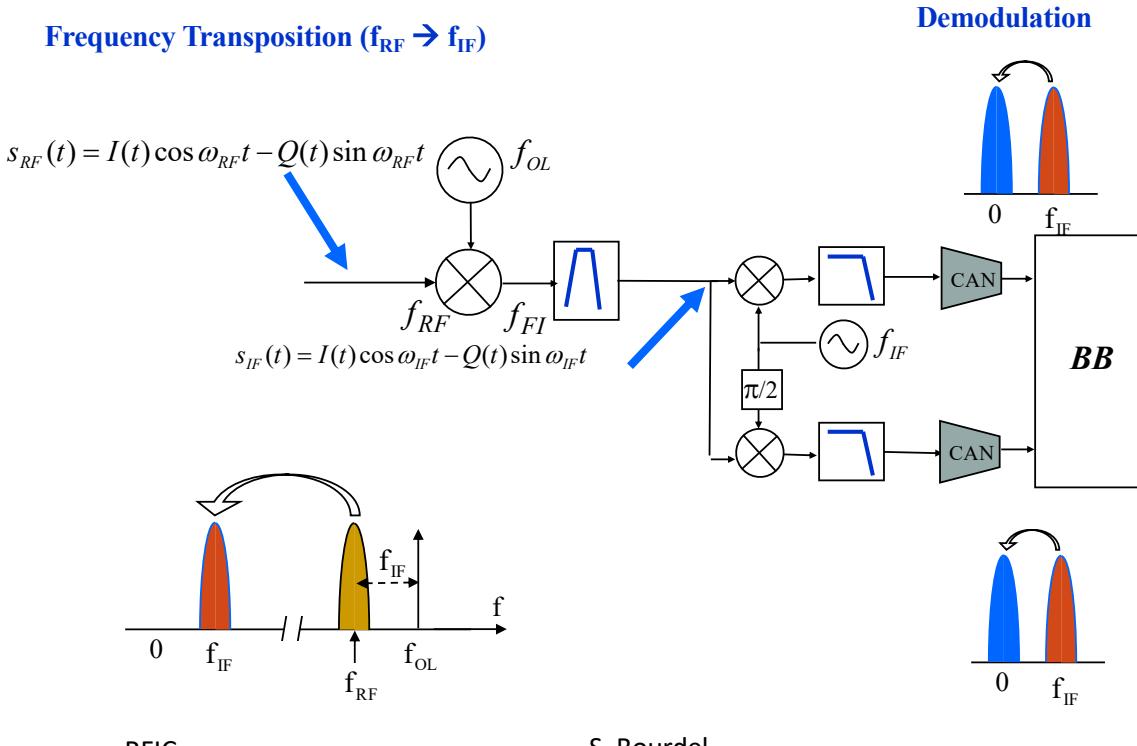
- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

RF receiver architecture

Heterodyne Structure



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RF receiver architecture

Heterodyne Structure

➤ Pros.

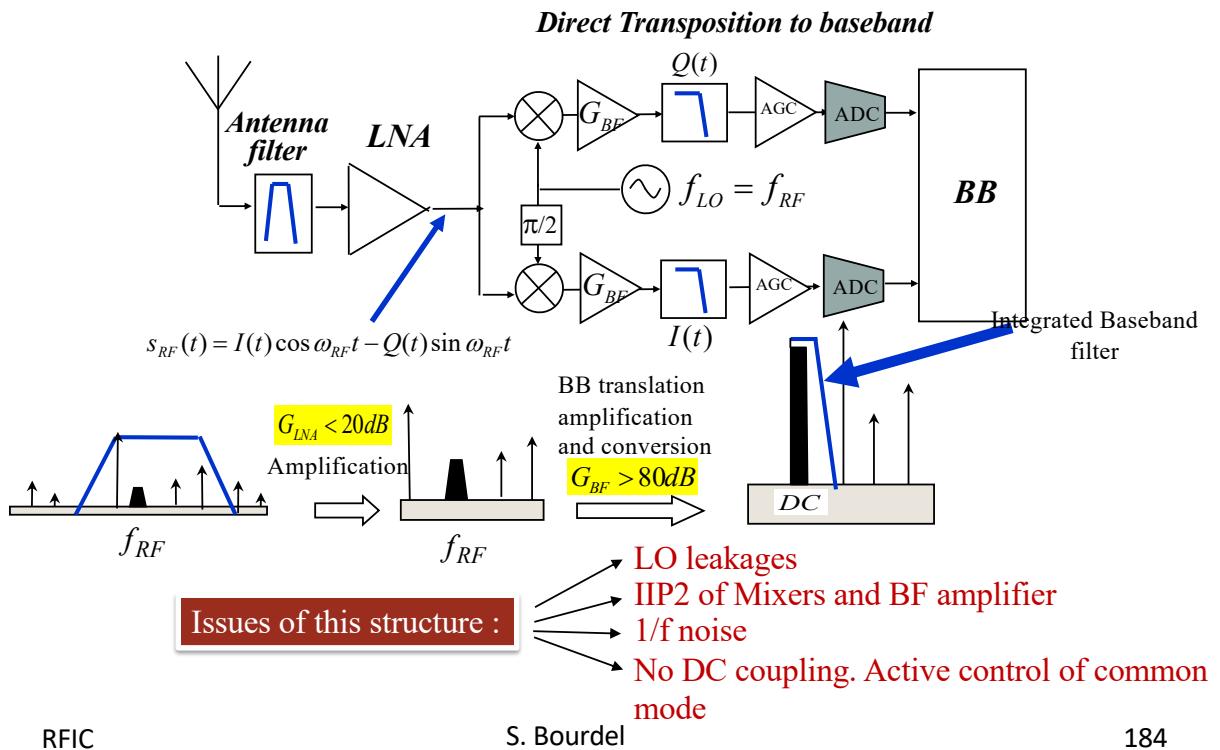
- ✓ Very good tradeoff between NF and IIP3 (large dynamic): medium gain before IF and very high gain after IF filtering.
- ✓ Low sensitivity to DC coupling (high gain bandpass amplifier and DC coupling)
- ✓ Very good tradeoff between sensitivity and selectivity

➤ Cons.

- ✓ Sensitive to image rejection (need an image filter)
- ✓ 4 filtering stages: hybrid technologies (Image and IF filters are not integrated)
- ✓ High consumption (large number of stages)
- ✓ No reconfiguration (GSM+UMTS+GPS)
- ✓ 1/f noise

RF receiver architecture

Zero IF Structure ($F_{RF} = F_{LO}$)

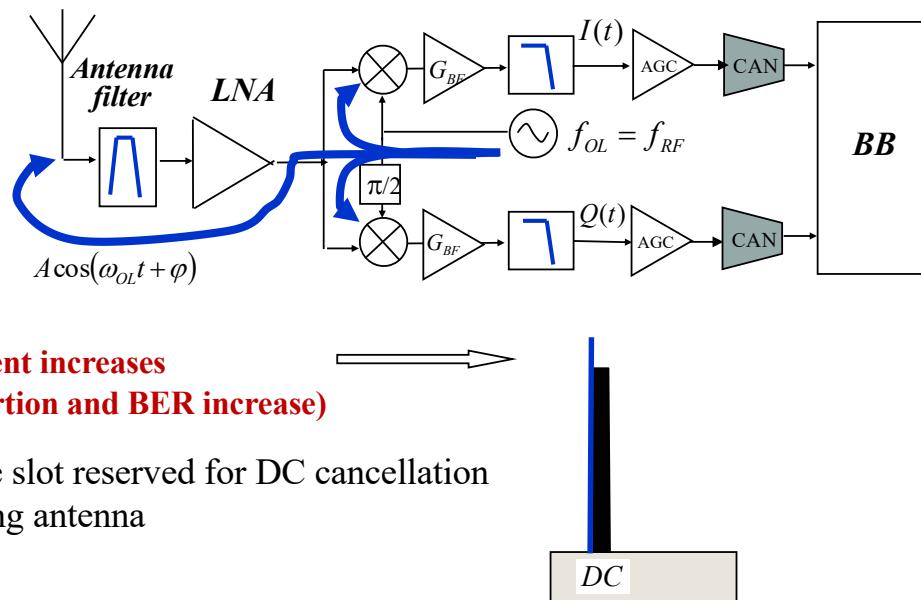


RF receiver architecture

Zero IF Structure ($F_{RF} = F_{LO}$)

Self Mixing due to LO leakages

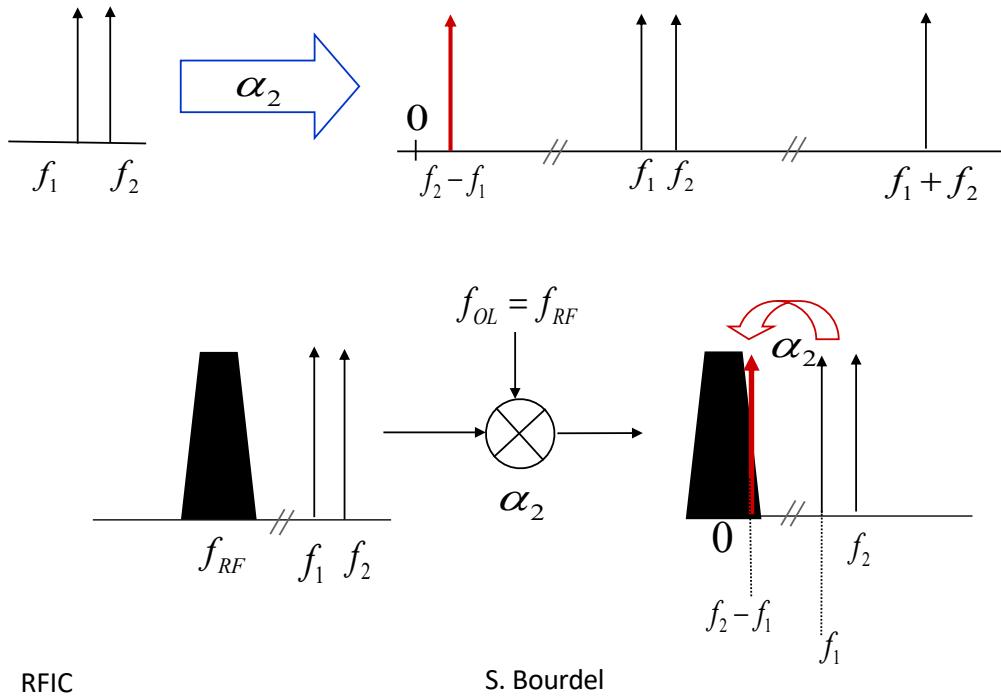
$$s_{RF}(t) = I(t) \cos \omega_{RF} t + Q(t) \sin \omega_{RF} t + A \cos(\omega_{OL} t + \varphi)$$



RF receiver architecture

Zero IF Structure ($F_{RF} = F_{LO}$)

IM2 effect



RFIC

S. Bourdel

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RF receiver architecture

Zero IF Structure ($F_{RF} = F_{LO}$)

➤ Pros .

- ✓ Low power consumption (the number of stages is reduced)
- ✓ No image filtering.
- ✓ Channel selection filter is low frequency and can be integrated
- ✓ Very well suited to fully integration
- ✓ Well suited for multi-standard (no FI)

➤ Cons.

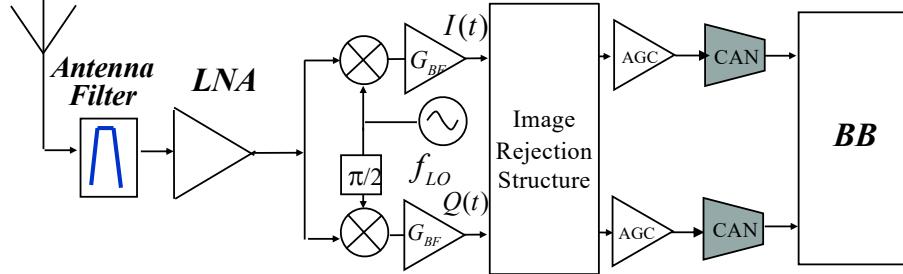
- ✓ Mixers and BF amplifier must be highly linear (very sensitive to blocker)
- ✓ Baseband filters must be high order (few filters in the chain)
- ✓ Very sensitive to DC offset. (IM2, no DC coupling, ...)
- ✓ 1/f noise

RF receiver architecture

Low IF Structure ($F_{RF} \sim F_{LO}$)

Best trade-off integration performances

$$s_{RF}(t) = I(t) \cos \omega_{RF} t + Q(t) \sin \omega_{RF} t$$



Low-IF : No DC offset issue (IIP2, self-mixing, ...) but it is difficult to achieve image rejection which are close to the received signal

Solution : image rejection structure with large bandwidth. The image rejection is achieved after mixing which is better for integration and multi-standard.

RF receiver architecture

Image rejection : negative frequencies

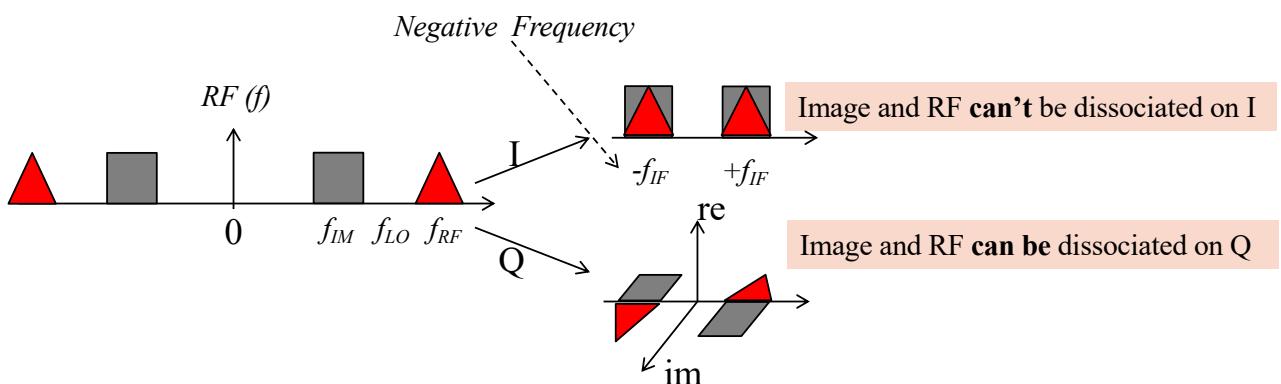
Issue and properties.

Hypothesis: a real modulation is considered and $f_{RF} = f_{LO} + f_{IF}$ $f_{im} = f_{LO} - f_{IF}$

$$s_{RF}(t) = a(t) \cos(\omega_{RF} t) + a_{im}(t) \cos(\omega_{im} t)$$

$$I_{IF} = s_{RF}(t) \cos(\omega_{LO} t) = \frac{1}{2} a(t) \cos(\omega_{IF} t) + \frac{1}{2} a_{im}(t) \cos(-\omega_{IF} t) + \dots = \frac{1}{2} a(t) \cos(\omega_{IF} t) + \frac{1}{2} a_{im}(t) \cos(\omega_{IF} t) + \dots$$

$$Q_{IF} = -s_{RF}(t) \sin(\omega_{LO} t) = -\frac{1}{2} a(t) \sin(-\omega_{IF} t) + \frac{1}{2} a_{im}(t) \sin(-\omega_{IF} t) + \dots = \frac{1}{2} a(t) \sin(\omega_{IF} t) - \frac{1}{2} a_{im}(t) \sin(\omega_{IF} t) + \dots$$



Exercise: generalize this demonstration for IQ RF and image signals:

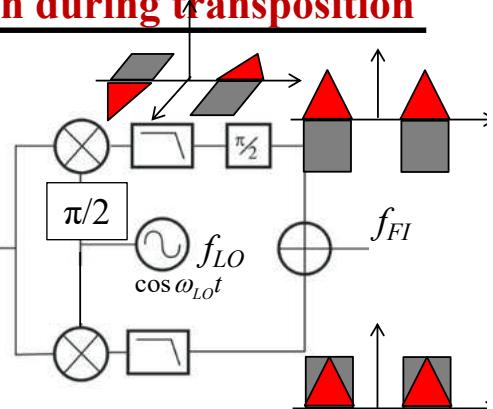
$$s_{RF}(t) = I(t) \cos(\omega_{RF} t) - Q(t) \sin(\omega_{RF} t) + I_{im}(t) \cos(\omega_{im} t) - Q_{im}(t) \sin(\omega_{im} t)$$

RF receiver architecture

Solving the image filter problem: rejection during transposition

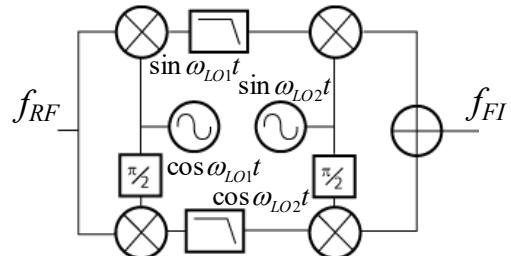
Hartley Structure

- + No rejection filter.
- Narrow band (phase shifter)
- Sensitive to IQ mismatch ($\text{IRR} = -60\text{dB}$)
- No image suppression after mixing (Low-IF)



Weaver Structure

- + No rejection filter.
- + wideband (multi-std)
- Low Sensitive to IQ gain mismatch
- High Sensitive to IQ phase mismatch
- No image suppression after mixing (Low-IF)



→ How to remove image after mixing??

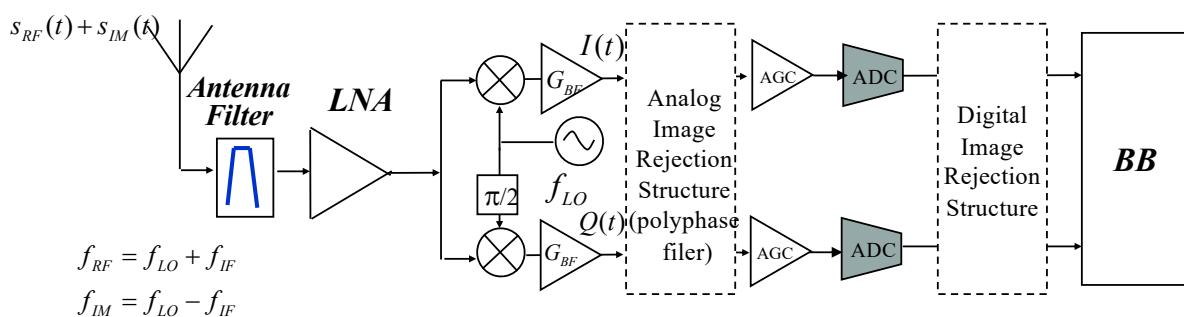
RF receiver architecture

Low IF Structure ($F_{RF} \sim F_{LO}$)

Best trade-off integration performances

$$s_{RF}(t) = I(t) \cos \omega_{RF} t - Q(t) \sin \omega_{RF} t$$

$$s_{IM}(t) = I_{IM}(t) \cos \omega_{IM} t - Q_{IM}(t) \sin \omega_{IM} t$$

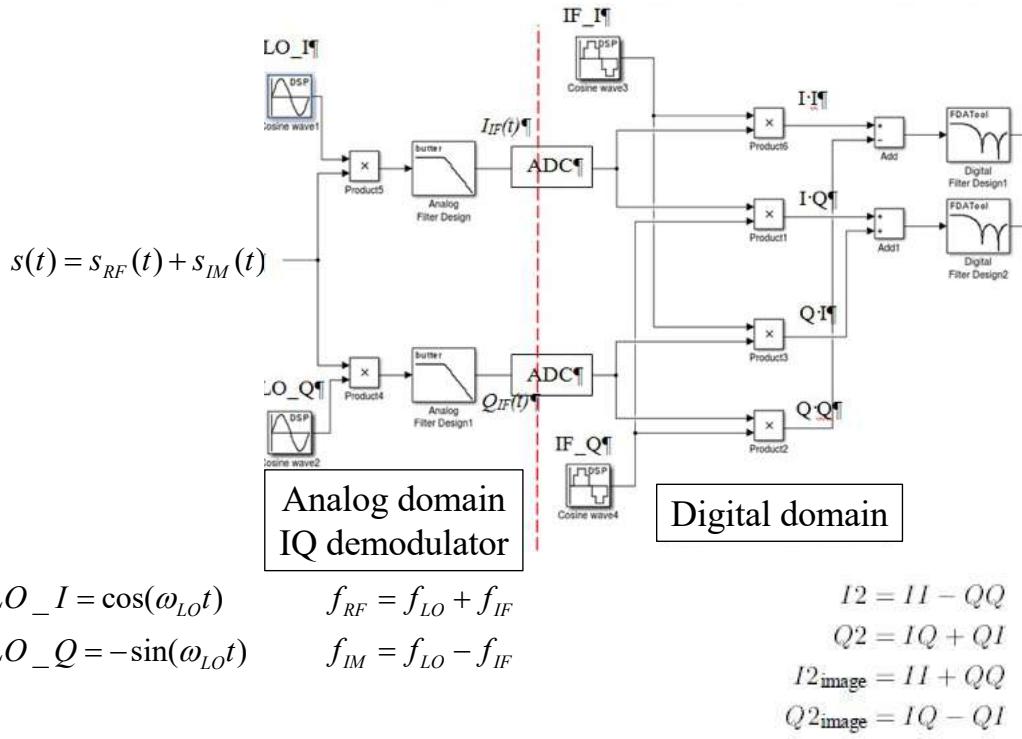


Low-IF : No DC offset issue (IIP2, self-mixing, ...) but it is difficult to achieve image rejection which is close to the received signal, no 1/f noise

Solution : image rejection structure with large bandwidth. The image rejection is achieved after mixing which is better for integration and multi-standard. It can be implemented in analog (polyphase filter) or digital domains.

RF receiver architecture

Image rejection in digital domain



RF receiver architecture

Image rejection in digital domain

For the signal of interest $s_{RF}(t)$:

$$I = II - QQ$$

$$Q = IQ + QI$$

For the image signal $s_{IM}(t)$:

$$I_{IM} = II + QQ$$

$$Q_M = IQ - QI$$

Note: image rejection ratios I_{IM}/I and Q_{IM}/I will be mainly affected by the imperfections (amplitude & phase imbalances) of the analog IQ demodulator located before ADCs.

Glas, Jack PF. "Digital I/Q imbalance compensation in a low-IF receiver," Global Telecommunications Conference, 1998. IEEE, 3:1461-66.

RF receiver architecture

Synchronisation Issue : Carrier suppression

Low-IF

- The received signal must be multiplied by an exact (synchronized) replica of the carrier (coherent demodulation)
- A *Costas loop* is often used
It is a PLL which is not sensitive to phase shift keying

$$R_{FI-BPSK}(t) = A(t) \cos(\omega_{FI}t + \varphi_E) \text{ avec } A(t) = \sum_0^K a_k g(t - kT_s) \text{ et } a_k = \pm 1$$

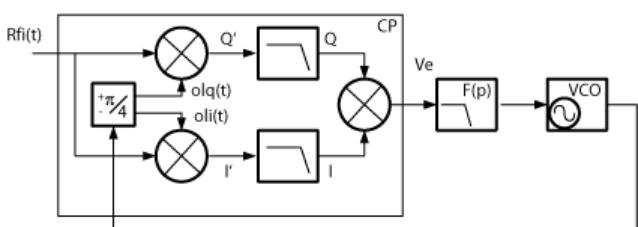
$$I' = A(t) \cos(\omega_{FI}t + \varphi_E) B \cos(\omega_{FI}t + \varphi_R)$$

$$I = \frac{A(t)B}{2} \cos(\Delta\varphi); \quad Q = \frac{A(t)B}{2} \sin(\Delta\varphi)$$

$$V_e(\Delta\varphi) = \frac{B^2}{8} \sin(2\Delta\varphi)$$

$$R_{FI}(t) = A(t) \cos(\omega_{FI}t + \varphi(t) + \varphi_E)$$

Carrier recovery System (PLL)



Zero-IF

Digital algorithms are used (derotator)

Outline

➤ Analog RF signal processing basis

➤ RF Basis

- Main metrics used in RF
- Impedance transformation & Matching Networks
- Non-linearity effects
- Noise Figure

➤ Technology and device models for RFIC

- Active devices (MOS & Bipolar)
- Passive devices (resistors, capacitors, inductors)

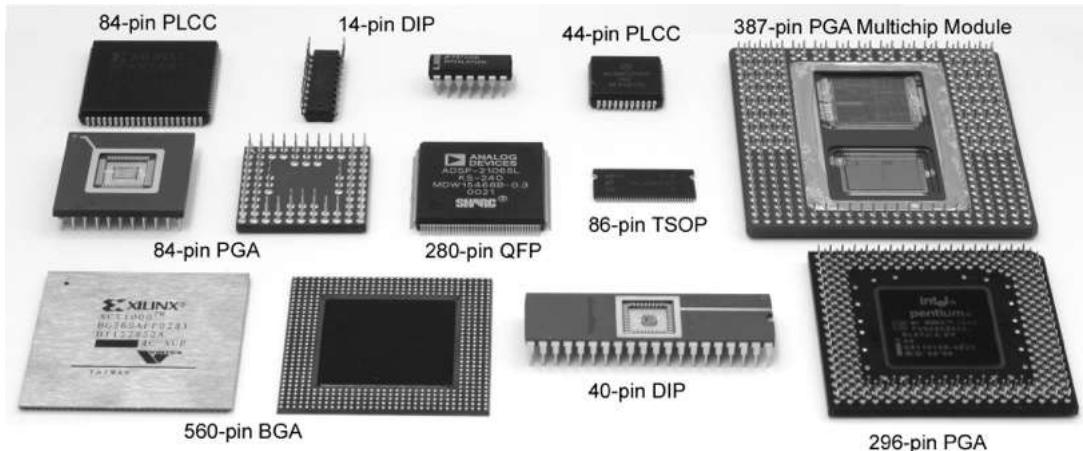
➤ Design methodologies for RF building blocs

- Low Noise Amplifier (LNA)
- Mixers
- Voltage Controlled Oscillators (VCO).
- Power Amplifier (PA)

➤ RF Front End Architecture

- Receiver topologies
- Sub-sampling Receiver

Packaging



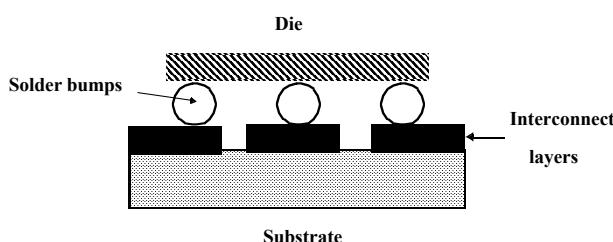
RFIC

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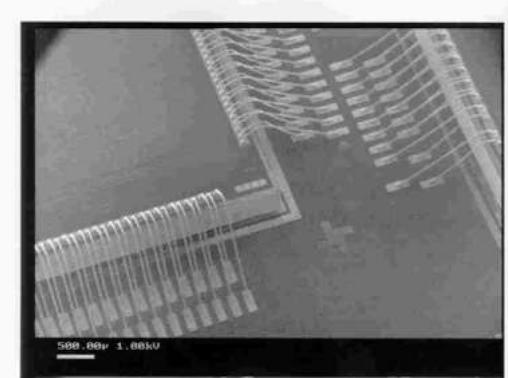
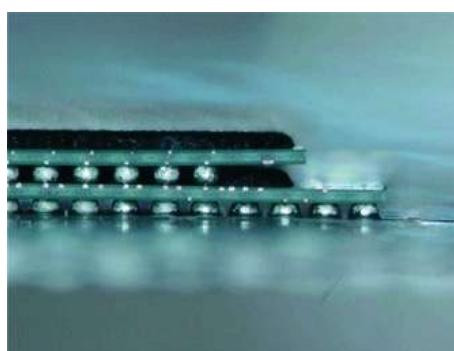
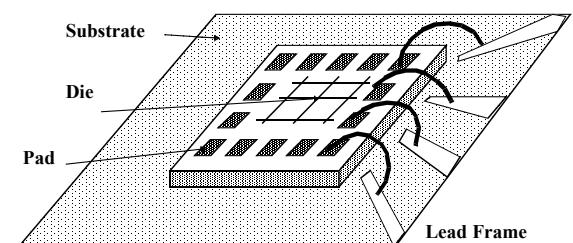
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Packaging

Ball Bonding



Wire Bonding



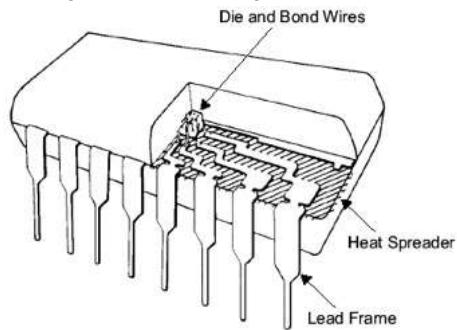
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Chip-to-Package Bonding

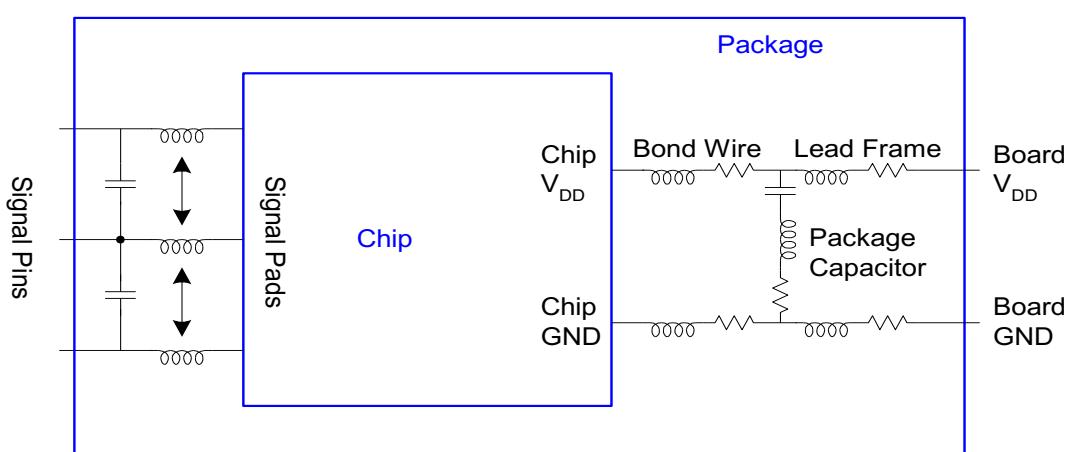
- Traditionally, chip is surrounded by *pad frame*
 - Metal pads on 100 – 200 μm pitch
 - Gold *bond wires* attach pads to package
 - Lead frame* distributes signals in package
 - Metal *heat spreader* helps with cooling



• From [Adnan Aziz](http://www.ece.utexas.edu/~adnan/vlsi-05/) <http://www.ece.utexas.edu/~adnan/vlsi-05/>

Package Parasitics

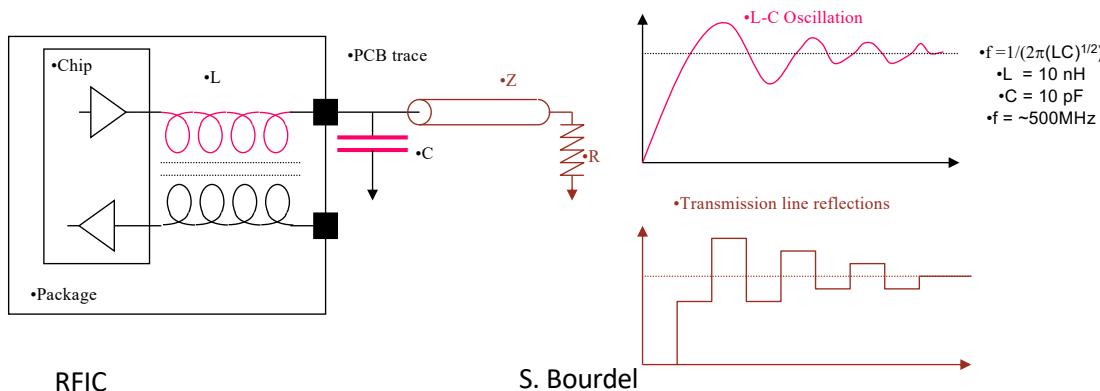
- Use many V_{DD} , GND in parallel
 - » Inductance, I_{DD}



• From [Adnan Aziz](http://www.ece.utexas.edu/~adnan/vlsi-05/) <http://www.ece.utexas.edu/~adnan/vlsi-05/>

Signal Interface

- Transfer of IC signals to PCB
 - Package inductance.
 - PCB wire capacitance.
 - L - C resonator circuit generating oscillations.
 - Transmission line effects may generate reflections
 - Cross-talk via mutual inductance



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Package parameters

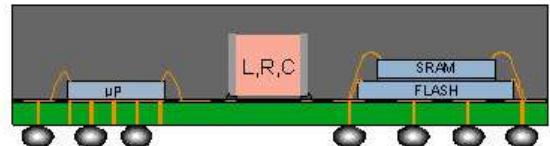
Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

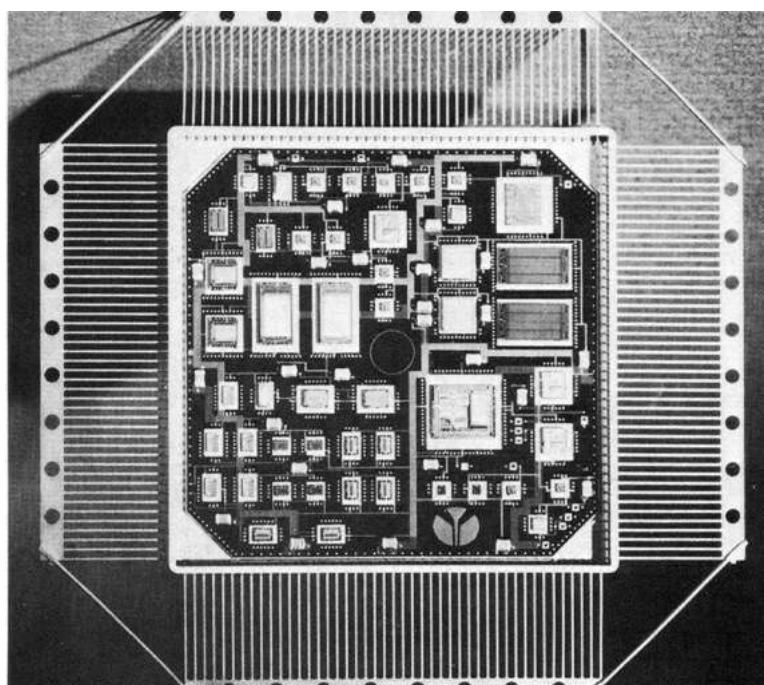
SoC has to overcome

- Technical Challenges:
 - Increased System Complexity.
 - Integration of heterogeneous IC technologies.
 - Lack of design and test methodologies.
- Business Challenges:
 - Long Design and test cycles
 - High risk investment
 - Hence time to market.
- Solution
 - System-in-a-Package

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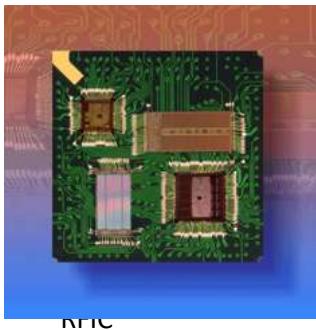


Multi-Chip Modules (MCM)

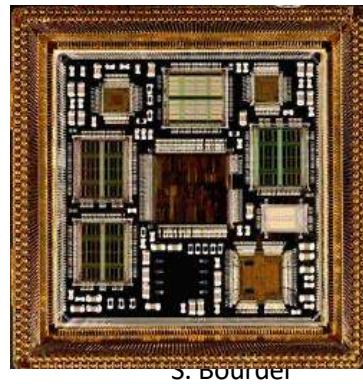


Multi-Chip Modules (MCM)

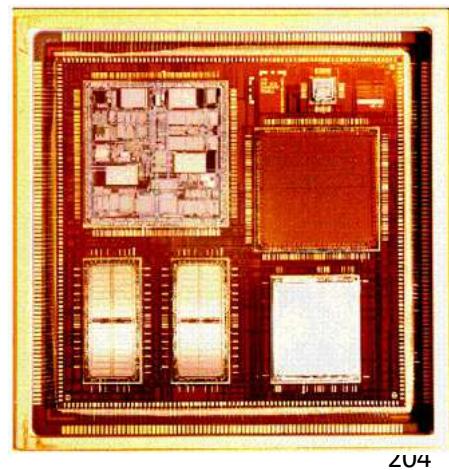
- Increase integration level of system (smaller size)
- Decrease loading of external signals > higher performance
- No packaging of individual chips
- Problems with known good die:
 - Single chip fault coverage: 95%
 - MCM yield with 10 chips: $(0.95)^{10} = 60\%$
- Problems with cooling
- Still expensive



RFIC



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ZU4

Complete PC in MCM



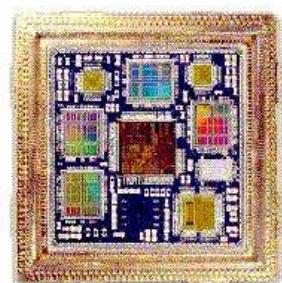
intel®
pentium™

28552-100-3Y23Z
7CLMP INDEX-615
L210692-4723
INTEL® 9297

intel®

PCset
S682371FB
L6353336
S297
INTEL® '94

Same functionality in
4 times smaller size



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