CE 6305, Homework 3 Answers

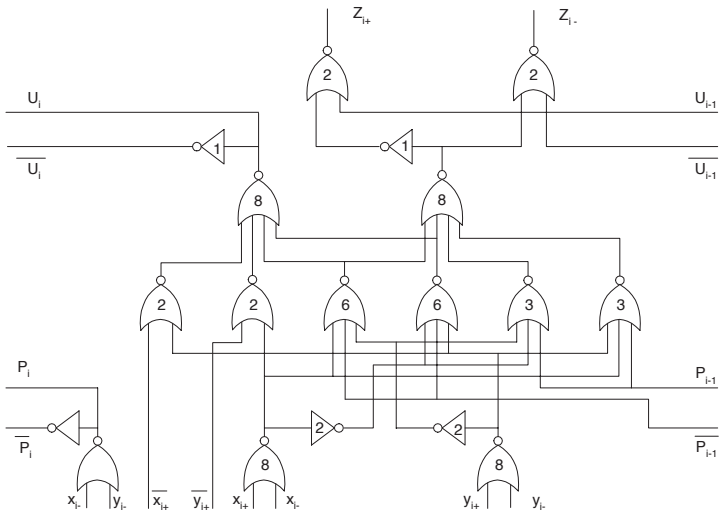
1. Give an efficient logic design for the adder cells of a BSD (redundant binary) adder with digit set $\{-1, 0, 1\}$ using the standard representation of the three digits. The objective is to minimize the worst case delay.

   Compute the worst case delay in terms of I, an inverter delay and, for a gate with fan-in f_i and fan-out f_o, assume the delay is If_if_o.

   Answer:

   See paper by Takagi et.al. There are 6-three input gates, 7-two input gates and 6-inverters if NOR gates are used.

   Here is my version of their circuit with NOR gates and inverters:



   The delays for each gate are indicated in the gate symbol. The worst case delay path sums to $27I$.

2. Determine the minimum numeric range of the interstage transmission signal t_i in a radix 16 General Sign Digit redundant system with digit set $[-8, 12]$. Compute suitable break-points for the output and transmission signal for the range of interstage sum signals $p_i = [-16, 24]$.

   Answer: For digit set $[-\alpha, \beta] = [-8, 12]$ and radix $r = 16$,

   $$\lambda \geq \frac{\alpha}{r-1} = \frac{8}{15}$$

   Choose $\lambda = 1$

   $$\mu \geq \frac{\beta}{r-1} = \frac{12}{15}$$

   Choose $\mu = 1$.

   Therefore the interstage carry t_i has range $[-1, 1]$

   The intermediate sum p_i has range $[-16, 24]$

   For p_i in range $[-16, -5]$, t_i can be -1 and a carry-in of $+1$ can be absorbed.

   For p_i in range $[-7, 11]$, t_i can be 0 and a carry-in of $[-1, 1]$ can be absorbed.

   For p_i in range $[9, 24]$, t_i can be $+1$ and a carry in of -1 can be absorbed.

   Combining these:

p_i	$[-16, -8]$	$[-7, -5]$	$[-4, 8]$	$[9, 11]$	$[12, 24]$
t_{i+1}	-1	$[-1, 0]$	$[0]$	$[0, 1]$	1

   Suitable break points are as follows:

p_i	$[-16, -9]$	$[-8, 7]$	$[8, 24]$
t_{i+1}	-1	0	$+1$

   Given that $p_i =< abcdef >$, including the sign bit, a, and the two bits of $t_{i+1} =< rs >$ with coding $< rs >= 10 \rightarrow t_{i+1} = -1, < rs >= 00 \rightarrow t_{i+1} = 0, < rs >= 01 \rightarrow t_{i+1} = +1$, Boolean expressions for r and s are:

   $$\begin{aligned} r &= a\, b\, \overline{c} \\ s &= \overline{a}\, \overline{b}\, c \end{aligned}$$

3. Is the representation of zero unique in the above GSD system? Explain.

   Answer:

   Yes, there is only one way to represent zero.

4. Devise an efficient way to negate a GSD number in this system.

   Answer:

   This will be a 2-stage process with intermediate sum p_i and carry t_{i+1}.

   To make sure there is no carry propagation during the negation, in each column, the first stage should give a result p_i in the range $[-7, 12]$ since we need to defend against a carry-in of -1 (see below).

   Digits with values in the range $[-8, 7]$ can just be negated by swapping their plus and minus components.

   Digits with values in the range $[8, 12]$ must cause a carry of -1 and a corresponding sum with range $[4, 8]$. We just subtract the digit from 16 to get the new digit and carry -1.

   In the second step we combine the intermediate sums and carries from the first stage.