CE 6305, Homework 3

1. Give an efficient logic design for the adder cells of a BSD (redundant binary) adder with digit set $\{-1, 0, 1\}$ using the standard representation of the three digits. The objective is to minimize the worst case delay.

   Compute the worst case delay in terms of I, an inverter delay and, for a gate with fan-in f_i and fan-out f_o, assume the delay is If_if_o.

2. Determine the minimum numeric range of the interstage transmission signal t_i in a radix 16 General Sign Digit redundant system with digit set $[-8, 12]$. Compute suitable break-points for the output and transmission signal for the range of interstage sum signals $p_i = [-16, 24]$.

3. Is the representation of zero unique in the above GSD system? Explain.