CS/CE/EE 6305 Home Work 1

1. In a k bit 2's complement binary adder, there are k identical stages. Stage i has inputs x_i, y_i, and carry in c_i. It produces outputs sum_i and c_{i+1} according to the following truth table:

c_{i+1}	sum_i	x_i	y_i	c_i
0	0	0	0	0
0	1	0	0	1
0	1	0	1	0
1	0	0	1	1
0	1	1	0	0
1	0	1	0	1
1	0	1	1	0
1	1	1	1	1

   Consider a radix -2 adder, where the position weights are

$$\{(-2)^{k-1}, (-2)^{k-2}, \cdots (-2)^1, (-2)^0\}$$

   Decide on the inter-stage signal(s) for this adder and give a corresponding truth table. The inter-stage signal(s) must not skip over stages.

2. Prove that a value V represented by the 2's complement bit vector $\langle a_{k-1}, a_{k-2}, \cdots, a_1, a_0 \rangle$ has value

$$V = -a_{k-1} \times 2^{k-1} + \sum_{i=0}^{k-2} a_i 2^i$$

3. Say that a value V is represented in a k bit 2's complement system. Show the steps necessary to transform this representation of V into a 2's complement representation in $2k$ bits.

4. Instead of using the 2's complement system for representing negative values, someone suggests a *bias* scheme, where a bias B is added to any positive or negative value V before conversion to binary. Discuss the choice of B necessary to simplify the conversion process and to balance the negative and positive ranges.

   Give details of the steps necessary to (i) add two values and (ii) to negate a value within the bias representation.