

KTMT - Kiến trúc máy tính nè

Kiến trúc máy tính _ hợp ngữ (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)





Question 5 Complete	Identify the correct sequence to update a page onto a flash memory?						
Marked out of	Step 3 the entire block is being read from flash into RAM then request data in page is update ▼						
	Step 1 the entire block of flash memory are erased ▼						
	Step 2 The entire block from RAM then is written back to the flash memory ▼						
	Your answer is incorrect.						
Question 6	Choose correct set of registers for x86 processor						
Complete Marked out of 1.00	Data pointer to source memory in extra segment ES: SI ▼						
1.00	Pointer to variable in stack SS: BP ▼						
	Instruction pointer CS: IP ▼						
	Data pointer in data segment DS: BX ▼						
	Your answer is correct.						
Question 7	Match the definition of flag bits in PSW						
Complete Marked out of 1.00	contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation						
1.00	determine the direction for moving or comparing data between memory areas DF						
	determine whether an external interrupts are to be ignored or processed						
	the processor switches to single-step mode						
	Your answer is correct.						
Question 8	What are components of Von Neumann, namely IAS computer?						
Complete Marked out of 1.00	Select one or more: Monitor						
	✓ Memory						
	□ Punched card reader☑ CPU						
	✓ I/O Equipments						
	Your answer is correct.						
Question 9	Which is not correct about MOORE law?						
Complete Marked out of	Select one or more:						
1.00	The number of transistors that could be put on a single chip was doubling every year						
	✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ Library 2000. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowadays. ✓ The number of transistors that could be put on a single chip was triple every year nowaday. ✓ The number of transistors that could be put on a single chip was triple every year nowaday. ✓ The numb						
	 ✓ Likely triple after 2000 The number of transistors that could be put on a single chip was doubling every year except 1970s 						
	and the manufacture of the one of						
	Your answer is correct.						

Complete	
Marked out of	Select one or more:
1.00	
	✓ Speculative execution
	Faster CPU internal bus
	Your answer is correct.
Question 11	To balance the super speed of CPU with the slow response of memory, which of the following measures have been made by engineers in system design?
Complete	Select one or more:
Marked out of 1.00	■ To move data directly by DMA
	✓ Make wider data bus path
	Make use of both on-chip and off-chip cache memory
	✓ Using higher-speed bus and us hierarchy
	Your answer is correct.
	four driswer is correct.
Question 12	What is the meaning of Amdahl's law in processor performance evaluation?
Complete	
Marked out of	Select one:
1.00	 the cost reduce when moving from single-core to multicore processor
	 the potential speedup of a program using multiple processor compared to a single processor
	 the speedup of a multicore processor when increasing system bus speed
	the maximum speedup of a multicore processor
	Your answer is correct.
Question 13	What are the processor's instruction categories
Question 13	What are the processor's instruction categories
Complete	What are the processor's instruction categories Select one or more:
-	
Complete Marked out of	Select one or more: ✓ Data processing
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory ✓ Processor - I/O
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory ✓ Processor - I/O
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory ✓ Processor - I/O ✓ Processor - Memory
Complete Marked out of	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA)
Complete Marked out of	Select one or more: ✓ Data processing ✓ Control □ Processor - Cache memory ✓ Processor - I/O ✓ Processor - Memory
Complete Marked out of	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA)
Complete Marked out of	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA)
Complete Marked out of 1.00	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA) Your answer is correct. In computer, how does the processor serve multiple interrupt request from devices?
Complete Marked out of 1.00 Question 14	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA) Your answer is correct. In computer, how does the processor serve multiple interrupt request from devices? Select one:
Complete Marked out of 1.00 Question 14 Complete	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA) Your answer is correct. In computer, how does the processor serve multiple interrupt request from devices?
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Complete Marked out of 1.00 Question 14 Complete Marked out of	Select one or more: Data processing Control Processor - Cache memory Processor - I/O Processor - Memory Memory - Memory (DMA) Your answer is correct. In computer, how does the processor serve multiple interrupt request from devices? Select one: The processor can not process multiple interrupt requests
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For better speed, in CPU design, engineers make use of $\,$ the following techniques:



Question 15 Complete Marked out of 1.00	Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation? Select one: Bus Arbiter Programmed I/O Direct Memory Access (DMA) Bus master Your answer is correct.
Question 16 Complete Marked out of 1.00	When many devices of different transmission speed connect to the same bus, the overall system performance suffers. How did the design engineers resolved this: Select one: PCI Express bus PCI bus Split system bus into local bus and memory bus Multiple-Bus hierarchies
	Your answer is correct.
Question 17 Complete Marked out of 1.00	What are the features of direct-mapping cache organization? Select one or more: ✓ Thrash> low hit ratio ☐ faster ✓ Simple and inexpensive ☐ small cache memory
	Your answer is correct.
Question 18 Complete Marked out of 1.00	Which ones are not correct for static RAM? Select one or more: Cost per bit is higher than dynamic RAM faster than dynamic RAM because they are made from capacitor Cheaper than dynamic RAM because simpler chip controller Cost per bit is lower than dynamic RAM
	Your answer is partially correct. You have correctly selected 2.
Question 19 Complete Marked out of 1.00	Which one is not correct? Select one or more: ✓ EEPROM is erasable by exposing under UV ☐ PROM is non-volatile memory ✓ EPROM is erasable electrically ✓ Flash memory can only be erased electrically byte by byte
	Your answer is correct.

Question 20 Complete Marked out of	Which statements are correct for HDDs? Select one or more:
1.00	
	b. Head, Track, Sector are key parameters for access data on hard disk
	c. Bits are store randomly on disk surfaces
	d. Head, Track, Cylinder are key parameters for access data on hard disk
	Your answer is correct.
Question 21 Complete	What is correct about the function of TRIM command in SSD?
Marked out of	Select one:
1.00	 Allow SSD to allocate memory pages in blocks properly for faster access
	Allow SSD to defragment scattered data stored in separate pages
	• Allow OS to notify SSD the presence of occupied blocks of data which are no longer in use and can be erased internally
	 Allow SSD to manage occupied pages and remove them automatically for later use
	Your answer is correct.
Question 22	Which set of registers are valid for addressing a memory location?
Complete Marked out of	Select one or more:
1.00	✓ DS:SI
	✓ DS:BX
	□ SS:DI
	✓ CS:IP
	Your answer is correct.
Question 23	Which are valid based index addressine?
Complete	Which are valid based index addressing?
Marked out of	Select one or more:
1.00	
	SP+DI]
	DX+SI]
	Your answer is correct.
Question 24	Which are valid index addressing?
Complete Marked out of	Select one or more:
1.00	✓ [SI]
	[DX]
	■ [BX]
	□ [BP]
	Your answer is partially correct.
	You have correctly selected 1.

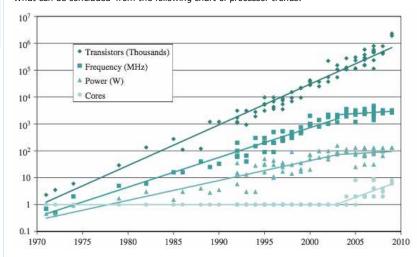


Question 25	8088 is 16 bit processor, the maximum addressable memory is:
Complete	Select one:
Marked out of 1.00	○ 64M
	○ 1024K
	○ 640K
	○ 640M
	Your answer is correct.
Question 26	Which are correct about the data registers of IA-32 processors:
Complete	
Marked out of	Selectione or more:
1.00	✓ Lower halves of the 16-registers an be used as 8-bit data registers: AH,AL,BH,BL,CH,CL,DH,DL
	✓ complete 32-bit registers: EAX, EBX, ECX, EDX
	Lower halves of the 32-registers an be used as 4 16-bit data registers: AX,BX,CX,DX
	■ Higher halves of the 32-bit registers can be used as 16-bit registers: EAH,EAL,EBH,EBL,ECH,ECL,EDH,EDL
	Your answer is correct.
Question 27	Which are correct about 32 bit index registers of IA-32 processors:
Complete	Select one or more:
Marked out of 1.50	✓ EDI: 32 bit pointer to destination memory in data movement instructions
1.50	ESH,EDH: 16 bit pointers to higher memory above 1M
	✓ DI: 16 bit pointer to destination memory in data movement instructions
	✓ SI: 16 bit pointer to source memory in data movement instructions — Total Control of the Control of th
	✓ ESI: 32 bit pointer to source memory in data movement instructions
	Your answer is correct.
Question 28	Which statement is correct about interrupt vector table?
Complete	Colort one or mare)
Marked out of 1.00	Select one or more: Store in the ending area of 1024K of the main memory
	▼ Take up 1024 bytes in the main memory
	Store on disk
	✓ Store in the beginning area of the main memory
	Store in the beginning area of the main memory
	Your answer is correct.
Question 29	Part of memory as shown in figure
Complete	Address 1D48 1D49 1D4A 1D4B 1D4C 1D4D 1D4E 1D4F
Marked out of 1.00	Value 03 7F F5 2D 5A 12 7B C0
	The value of DX register follows the execution of MOV DX, [1D4D] is 127B. What is the endian type of this computer system
	Select one: little-endian
	level-endian
	big-endian
	onon-endian
	Your answer is correct.

Question 30 Complete Marked out of 1.00	Value 03 7F F5	figure 1 1D4B 1D4C 1D4D 1D4E 1D4F 2D 5A 12 7B C0 ows the execution of MOV BX, [1D49] is F57F. What is the endian type of this computer system
	Your answer is correct.	
Question 31 Complete Marked out of 0.50	The value in CS is 1FD0h what is Answer: 3CD5H	s the location of next instruction from 00000h if Instruction pointer is 3CD4h
Question 32 Complete Marked out of	Select correct items to describe l	
1.00	code size of program	small code size ▼
	Assembly code	simpler ▼
	Instruction set Bytes per instruction	Complex ▼ different for variety of instructions ▼
	Your answer is correct.	
Question 33 Complete Marked out of	What best describe the Spatial a Temporal locality be exploited by	nd Temporal Locality? v keeping recently used instruction and data in cache memory and by exploiting a cache hierarchy
1.00	Cratial	using larger cache blocks and by incorporating prefetching mechanisms into the cache control logic 🔻
	Your answer is correct.	

Complete
Marked out of
1.00

What can be concluded from the following chart of processor trends:



Select one:

- The multi-core processors and level off clock speed help to make heat dissipation of CPU chip less
- The number of transistors in chips produce more heat dissipation
- Heat dissipation in processor chip is increasing year after year since 1970
- The processor speed keeps increasing after 2003

Your answer is correct.

Question 35

Complete
Marked out of
1.00

To evaluate processor performance, the following indicators and formulas are used:

$$\label{eq:cycles} \text{Cycles per instruction} \qquad CPI = \ \frac{\sum_{i=1}^{n} (CPI_i \times I_i)}{I_c}$$

Time to execute a program $T = I_c \times CPI \times \tau$

Or
$$T = I_c \times [p + (m \times k)] \times \tau$$

In which:

p: the number of processor cycles needed to decode and execute the instruction

m: the number of memory references needed

k: the ratio between memory cycle time and processor cycle time

τ: cycle time = 1/f

Which of the following system attributes affects $\emph{\textbf{I}}\emph{\textbf{c}}$ (the number of instructions of a program)

Select one or more:

- Cache and memory hierarchy
- Processor implementation
- ✓ Instruction set architecture
- Compiler technology

Your answer is correct.

Question 36

Complete Marked out of 1.00 To evaluate processor performance, the following indicators and formulas are used:

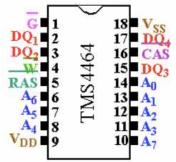
Which of the following system attributes affects cycle time $\boldsymbol{\tau}$

Select one or more:

- Processor implementation
- Compiler technology
- Instruction set architecture
- Cache and memory hierarchy

Question 37 Key parameters to consider when evaluating processor hardware include: Complete Select one or more: Marked out of ✓ reliability 1.00 performance power consumption databus size Address bus size ✓ cost Your answer is correct. Question 38 A memory chip has 12 address pins, determine the maximum memory words of this chip? Complete Select one: Marked out of 2048K 1.00 0 2048 **4000** 4096 Your answer is correct. Question 39 Which of the following best describe the memory chip with pinout as shown below: Marked out of 1.00 17 DQ 16 CAS

Complete



DQ: Data pinout

Select one:

- DRAM 64Kx4-bit
- SRAM 256Kx1-bit
- DRAM 16Kx4-bit
- SDRAM 64Kx4-bit



Question 40 Choose the correct structure of memory chip as shown below Complete 24 VCC Marked out of 23 A₈ 22 A₉ 21 W 20 G 1.00 19 A₁₀ 18 S Note: DQ: Data pinout Select one: DRAM 2Kx8-bit SRAM 1Kx16-bit SRAM 2Kx8-bit DRAM 1Kx16-bit Your answer is correct. Question 41 The three key characteristics of memory are: capacity, access time and cost. Which of the following relationships hold for a variety of memory technologies? Complete Marked out of Select one or more: 1.00 ✓ Faster access time, greater cost per bit ■ Higher capacity, higher access time Greater capacity, smaller cost per bit Greater capacity, slower access time Your answer is correct. Question 42 A SRAM memory chip labeled 32x8bit. Which of the following is correct pinout regarding address and data lines? Select one: Marked out of 32 address pins, 3 data pins 1.00 32 address pins, 4 data pins 5 address pins, 3 data pins 15 address pins, 8 data pins Your answer is correct. Question 43 In the interconnection system, the number of address lines are governs by Complete Select one: Marked out of 1.00 I/O Module CPU data bus line Memory size

Question 44 For memory hierarchy below, which relationship hold when moving downward Complete Marked out of 1.00 Select one or more: ✓ Increasing access time Decreasing cost per bit Decreasing frequency of access by the processor the processor accesses more often Increasing capacity Your answer is correct. Question 45 Identified correct addressing mode of the following instructions? • MOV AX, BX Register 1.50 MOV BP, [BX+SI] Base relative plus index ▼ MOV AX, ARRAY [BX+SI] Base plus index MOV AX, [BX] Register indirect



MOV AX,[1234h] Direct MOV AX, 3540h Immediate

Your answer is partially correct. You have correctly selected 4.

Question 46 Complete

Marked out of 1.00

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction MOV AX, [1D4B] executed

Answer: 5A2D

Complete
Marked out of
1.00

Part of memory shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of EAX follow the execution of this code

MOV BX, 1D4C MOV EAX, [BX]

Answer: 125A

Question 48

Complete
Marked out of
1.00

the memory stack area of a program shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of SP register is 1D48. What is the value of SI follows the execution of POP SI

Answer: 1D48

Question 49

Complete
Marked out of
1.00

the memory stack area of a program shown in figure

Address 1D50 1D51 1D52 1D53

Value AF 90 71 DA

The value of SP register is 1D50. What is the value of SP follows the execution of **PUSH SI**

Answer: 1D4F

Question 50 Complete

Marked out of 3.00

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs

Instruction Type	Instruction Count (millions)	Cycles Per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

Determine the effective, CPI, MIPS rate and execution time for each machine.

CPI_b 1.92 ▼

CPU Time_a 0.2 ▼

CPU Time_b 0.23 ▼

CPI_a 2.22 ▼

MIPs_b 104 ▼

MIPs_a 90 ▼

Question 51 Complete	Choose correct RAID volume definitions for a request 2T storage.						
Marked out of 2.00	RAID 1 - Mirror volume 2 x 2T HDDs are needed, no data lost when the primary storage fails						
	Spanned Volume 2T HDD + more HDDs to extend storage, no fault tolerance, data lost when one HDD fails ▼						
	RAID 0 - Striped volume 2 x 1T HDDs are needed, enhance data transfer, no fault tolerance, data lost when one HDD fails 🔻						
	RAID5 Volume At least 3 x 2T HDDs, fault-tolerance, no data lost, no down-time ▼						
	Your answer is correct.						
Question 52 Complete Marked out of 1.00	Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 30% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 30% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor? Select one: 10% 15% 17% 23%						
	Your answer is correct.						
Question 53 Complete Marked out of	the drive rotates at 3600 rpm. What is average access time. Given: Rotational delay = $1/(2r)$, where r is the rotational speed in revolutions per second						
1.00	Answer: 16.3 ms ▼						
	Return to: 12 March - 18 M →						





Nhóm 06-07-08CLC - Kiến trúc máy tính và hợp ngữ

Bắt đầu vào lúc Saturday, 8 April 2017, 1:12 PM

State Finished

Kết thúc lúc Saturday, 8 April 2017, 1:22 PM

Thời gian thực 10 phút 13 giây

hiên

Điểm 22,25/22,25

Điểm 10,00 out of 10,00 (**100**%)

Câu hỏi 1

Đúng

Đạt điểm 1,00 trên 1,00

₱ Đặt cờ

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number 57 (in hex) to decimal.

Answer: 5,75

Câu hỏi 2

Đúng

Đạt điểm 1,50 trên 1,50

P Đặt cờ

A system programmer needs to divide -6247 by 300 (decimal). Instruct him to code in debug (number must be in hex) and the result should be?

Step 1: MOV AX,E799 ▼

Step 2: CDW ▼ ✓

Step 3: MOV BX,012C ▼ 🛶

Step 4: IDIV BX ▼ ✓

Result:

AX = FFEC ▼

DX = FF09 ▼ ✓

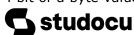
Your answer is correct.

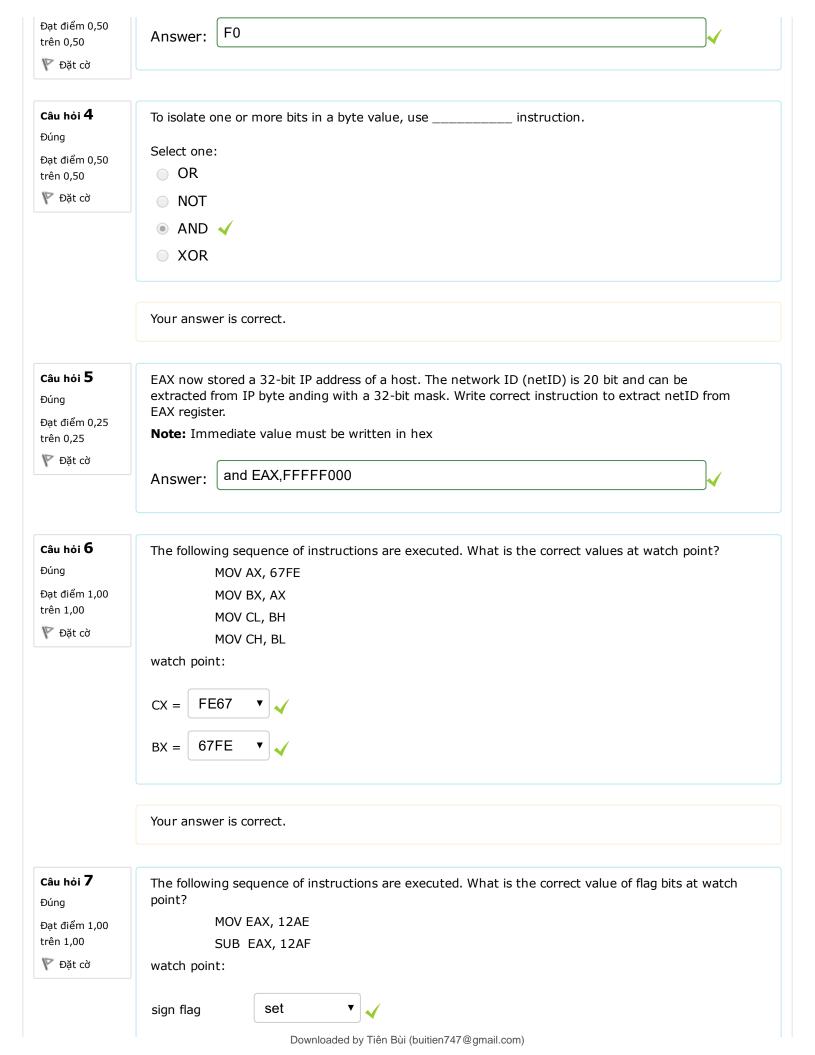
Câu hỏi **3**

Đúng

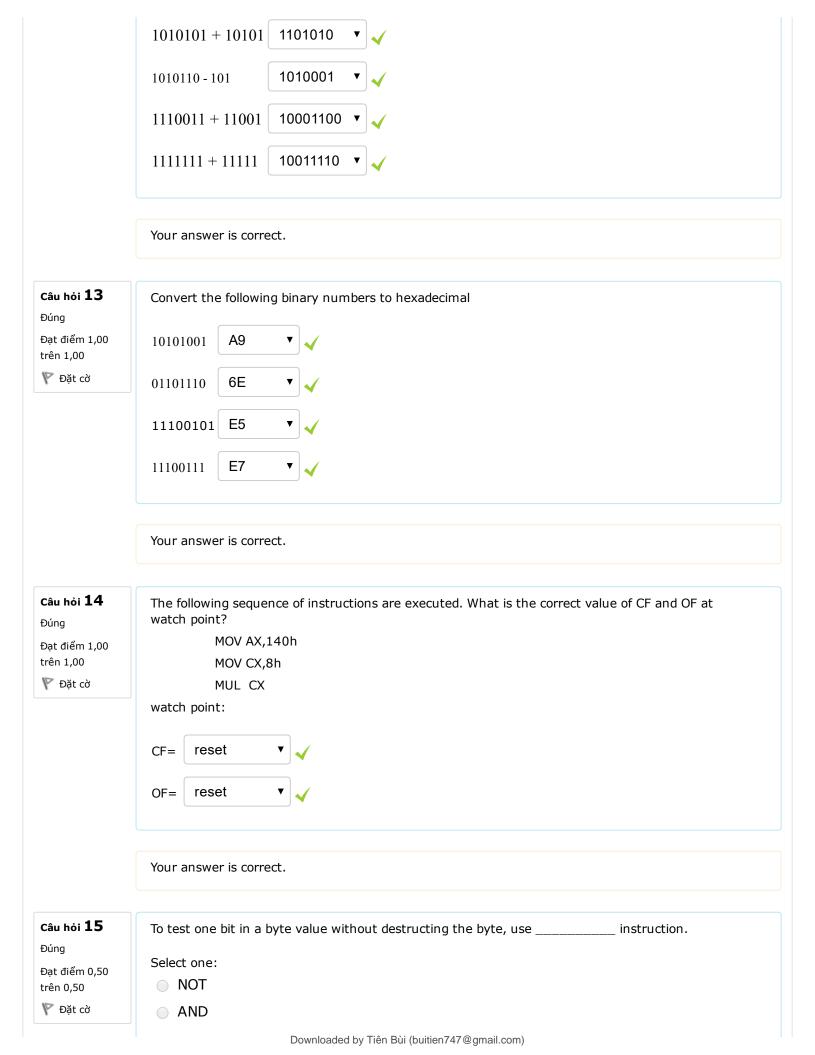
Write mask byte (in hex) to clear the lower 4 bit of a byte value with AND instruction.

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	Zero flag (OF) = reset ▼ ✓			
	Carry flag (CF) = set ▼ ✓			
	Your answer is correct.			
Câu hỏi 8 Đúng Đạt điểm 1,00 trên 1,00	Physical address of the stack pointer is 2DA82, stack segment located at 1DAE. Computer the value of SP register? Answer: FFA2			
Câu hỏi 9 Đúng Đạt điểm 1,00	Match the following hexadecimal numbers to octal E7 347 ▼ ✓			
trên 1,00	6E 156 ▼ ✓			
	A9 251 ▼ ✓			
	Your answer is correct.			
Câu hỏi 10 Đúng	Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D			
Đạt điểm 1,00 trên 1,00 P Đặt cờ	Answer: f 100 1FF 0D ✓			
Dặt co				
Câu hỏi 11	Given 8-bit floating-point binary format:			
Đát điểm 1,00 trên 1,00	1 (sign) + 3 (exponent) + 4 (mantissa) Convert the 8-bit floating point number E7 (in hex) to decimal.			
P Đặt cờ	Answer: ☐-11,5 ✓			
Câu hỏi 12 Đúng	Match the correct answer for binary operations on the left			
Đạt điểm 1,50 trên 1,50	1111111 - 111 1111000 🔻 🎺			
₩ Đặt cờ	1100111 - 111			
	This document is available free of charge on Studocu			
	Downloaded by Tiên Bùi (buitien747@gmail.com)			



•	TEST	√
	OR	

Your answer is correct.

Câu hỏi 16

Đúng

Đạt điểm 1,00 trên 1,00

Pặt cờ

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24

Initially, AX=BX=CX=DX=0, SI=121

What are value of CX,DX after execution of the following instructions?

MOV DX, [SI]

MOV CX, [SI+2]

Your answer is correct.

Câu hỏi 17

Đúng

Đạt điểm 1,00 trên 1,00

Păt cờ

Select correct match for register values at watch points:

MOV AX, 152D

ADD AX, 003F

watch point #1:

ADD AH, 10

watch point #2:

watch point #2:

AH = 25

watch point #1:

location

AL = 6C

Your answer is correct.

Câu hỏi 18

Đúng

Đạt điểm 1,00 trên 1,00

Păt cờ

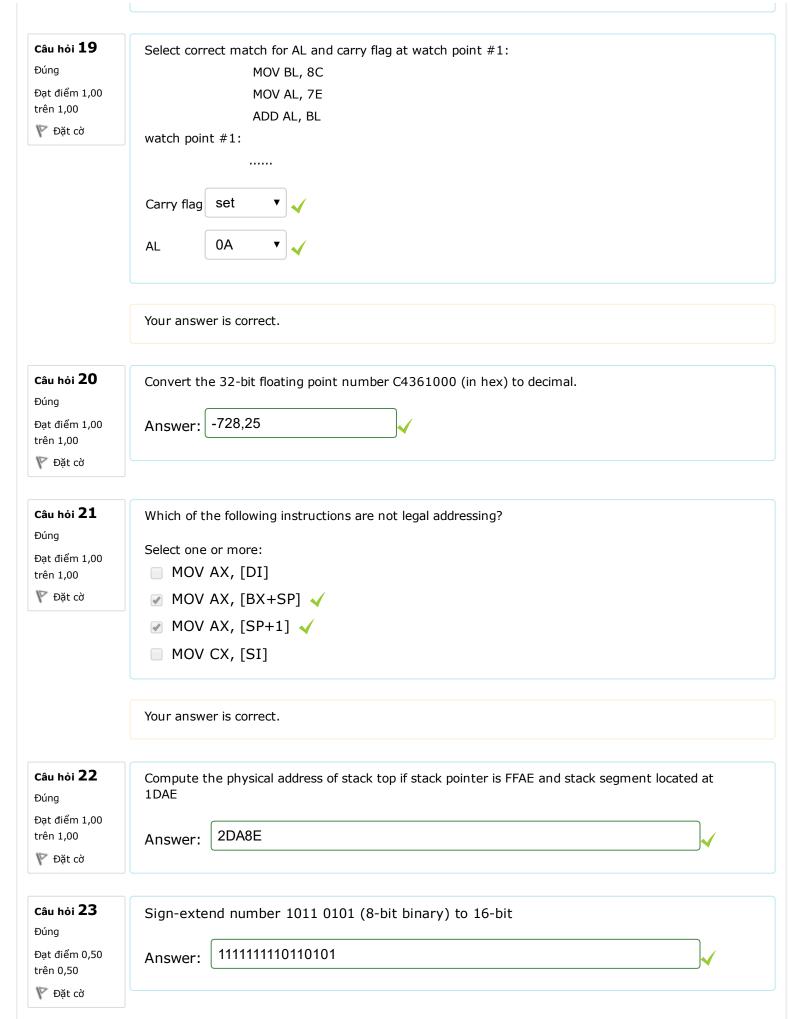
5F54F This document is available free of charge on Answer:





A memory location located in extra segment which now has value of 564F. This memory managed

by ES:SI register-pair. SI now points to 905F. Compute the physical address of this memory



Câu hỏi 24 Đúng Đạt điểm 1,00 trên 1,00 P Đặt cờ

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

MOV AX,30

MOV CX,FFFF

MUL CX

watch point:

Your answer is correct.

Finish review







THE EXAM PERFORMANCE PROGRAM INFORMATION TECHNOLOGY CENTER

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Dashboard ► Học kỳ 2 năm 2016 - 2017 ► Lớp Chất lượng cao ► CAAL240180_16_2_8506 ► General ► Kiểm tra cuối kỳ đề 1

Started on Monday, 5 June 2017, 1:12 PM

State Finished

Completed on Monday, 5 June 2017, 2:22 PM

Time taken 1 hour 9 mins

Complete

Marked out of 1.20

```
Consider the following assembly instruction sequence
     CMP DL, 0
     JB x_label
     CMP DL, 9
     JA a_label
     ADD DL, 30h
     JMP x_label
a_label:
     CMP DL, 0Fh
     JA x_label
     ADD DL, 37h
x_label:
     MOV AL, DL
watch point:
Choose correct value of AL register at watch point for different value of DL?
DL=10
           38h
DL=8
           41h
DL=55h
           55h
DL=0FFh OFFh
```

Question 2

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of CF and OF at watch point?

MOV AX,FFF6h

MOV CX,1000h

IMUL CX

watch point:

Question 3 Which could be correct ones for the destination operand in a data movement instruction? Select one or more: ☑ register immediate data ☑ memory location all choices are correct Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit)). Answer: 10010111 Question 5 Complete Marked out of 0.50 Select one: intrasegment indirect mode intrasegment mode intrasegment direct mode intrasegment direct mode Question 6 Complete Marked out of 1.20 Marked out of 1.20 Marked out of 1.20 Answer: 1144403968 Convert the 32-bit floating point number 44363800 (in hex) to decimal.		
Select one or more: register immediate data memory location all choices are correct Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit). Answer: 10010111 Question 5 Complete Marked out of 0.50 Select one: intrasegment indirect mode intrasegment mode intrasegment direct mode Question 6 Complete Complete		Which could be correct ones for the destination operand in a data movement instruction?
Pregister immediate data memory location all choices are correct Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st bit). Answer: 10010111 Answer: 10010111 Answer: 10010111 Select one: intrasegment indirect mode intrasegment mode intrasegment direct mode intrasegment direct mode intrasegment direct mode Ouestion 6 Convert the 32-bit floating point number 44363800 (in hex) to decimal.	Complete	Select one or more:
immediate data	Marked out of 0.50	
wemmory location all choices are correct Question 4		
Question 4 Complete Marked out of 1.20 Question 5 Complete Marked out of 0.50 Answer: 10010111 Guestion 5 Complete Marked out of 0.50 Guestion 6 Complete Convert the 32-bit floating point number 44363800 (in hex) to decimal.		
Question 4 Complete Marked out of 1.20 Question 5 Complete Marked out of 0.50 Guestion 5 Complete Marked out of 0.50 Guestion 6 Complete Convert the 32-bit floating point number 44363800 (in hex) to decimal.		
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Answer: 10010111 Question 5 Complete Marked out of 0.50 Select one: intrasegment indirect mode intrasegment mode intrasegment direct mode intrasegment direct mode intrasegment direct mode Ouestion 6 Complete Complete Answer: 10010111 If the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is call Select one: intrasegment mode intrasegment mode Ouestion 6 Convert the 32-bit floating point number 44363800 (in hex) to decimal.	Question 4	Write mask byte (in hex) to clear bit 2nd, 3rd, 5th of a byte value with AND instruction (LSB is 1st
Answer: 10010111 Question 5 Complete Marked out of 0.50 Select one: intrasegment indirect mode intrasegment mode intrasegment direct mode intrasegment direct mode intrasegment direct mode Ouestion 6 Complete Complete Answer: 10010111 If the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is call Select one: intrasegment indirect mode Ouestion 6 Convert the 32-bit floating point number 44363800 (in hex) to decimal.	Complete	bit).
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Select one: intrasegment indirect mode intrasegment mode intrasegment mode intrasegment direct mode Convert the 32-bit floating point number 44363800 (in hex) to decimal.	Complete	current one, then the jump instruction is call
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intersegment mode intrasegment mode intrasegment direct mode Convert the 32-bit floating point number 44363800 (in hex) to decimal.		
intrasegment mode intrasegment direct mode Question 6 Complete Complete		
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Question 6 Complete Complete Convert the 32-bit floating point number 44363800 (in hex) to decimal.		intrasegment mode
Complete Complete		intrasegment direct mode
Complete Complete		
	Question 6	Convert the 32-bit floating point number 44363800 (in hex) to decimal.
Marked out of 1.20	Complete	
	Marked out of 1.20	Answer: 1144403968

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AX,FFFF

MOV CX,5

MUL CX

watch point:

set

Question 8

Complete

Marked out of 0.50

In multiplication instruction, when the source operand is 16 bit, how can the result be taken?

Select one:

- from AX:DX pair
- from AX
- from EAX
- from DX:AX pair

Question 9

Complete

Marked out of 1.00

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24

Initially, AX=BX=CX=DX=0, SI=128

What are value of AX,DX after execution of the following instructions?

MOV EDX, [SI]

MOV EAX, [SI+4]

Complete

Marked out of 1.00

Which statements are correct for HDDs?

Select one or more:

- Head, Track, Sector are key parameters for access data on hard disk
- Bits are stored on tracks
- Head, Track, Cylinder are key parameters for access data on hard disk
- Bits are store randomly on disk surfaces

Question 11

Complete

Marked out of 0.50

Which are correct action for SCASW string operation if DF is set (=1)

Select one or more:

- compare value in AL register with memory location pointed by DS:[SI]
- decrease DI by 2
- compare value in AL register with memory location pointed by ES:[DI]
- ✓ increase DI by 2

Question 12

Complete

Marked out of 1.00

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24

SI = 120, DI = 128

Select correct sequence of instructions to subtract words at [DI] from [SI] then store the result at memory location 12A

Step 1:	MOV AX, [SI]	

Question 13 Complete Marked out of 0.50	The instruction that supports addition when carry exists is Select one: DAS SBB ADC ADD
Question 14 Complete Marked out of 1.00	In computer, how does the processor serve multiple interrupt request from devices? Select one: Each device are assigned an interrupt priority, the device with lower priority will be served. Device with higher priority will use interrupt enable flag The processor can not process multiple interrupt requests Each device are assigned an interrupt priority, the device with higher priority will be served.
Question 15 Complete Marked out of 1.00	The following sequence of instructions are executed. What is the correct value of flag bits at watch point? MOV AL, 80 MOV BL, 2 MUL BL watch point: Overflow flag (OF) = reset Carry flag (CF) = set V
Question 16 Complete Marked out of 0.50	To test one bit in a byte value without destructing the byte, use instruction. Select one: AND OR NOT TEST

Question 17 Complete Marked out of 1.00 Which a Select of

Which are correct about the data registers of IA-32 processors:

Select one or more:

- Lower halves of the 32-registers an be used as 4 16-bit data registers: AX,BX,CX,DX
- omplete 32-bit registers: EAX, EBX, ECX, EDX
- Lower halves of the 16-registers an be used as 8-bit data registers: AH,AL,BH,BL,CH,CL,DH,DL
- ✓ Higher halves of the 32-bit registers can be used as 16-bit registers: EAH,EAL,EBH,EBL,ECH,ECL,EDH,EDL

Question 18

Complete

Marked out of 1.20

Convert 0.1015625 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa)

Answer: Thay thuong tinh cho em 7d qua mon, em cam on!

Question 19

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV DL,FF

MOV AL, F6

IMUL DL

watch point:

Question 20

Complete

Marked out of 1.00

Choose correct features for SRAM and DRAM

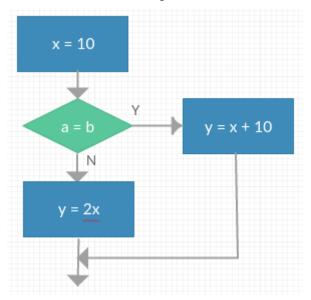
SRAM Faster access time, cost more per bit, smaller size

DRAM Slower access time, cheaper cost per bit, can manufacture with larger size

Complete

Marked out of 1.20

Given a flowchart of an algorithm:



Select the correct instruction sequence:

Select one or more:

- mov dl,10
 - cmp al,bl
 - jz n_label
 - mov cl,1
 - shl dl,cl
 - jmp e_label
 - n_label:
 - add dl,10
 - e_label:
 - mov dh,dl
- mov dl,10
 - cmp al,bl
 - jnz n_label
 - add dl,10
 - jmp e_label
 - n_label:
 - mov cl,1
 - shr dl,cl
 - e_label:
 - mov dh,dl
- ✓ mov dl,10
 - cmp al,bl
 - jnz n_label
 - add dl,10
 - jmp e_label
 - n_label:
 - mov cl,1
 - shl dl,cl
 - e_label:
 - mov dh,dl

mov dl,10
cmp al,bl
jnz n_label
add dl,10
mov dh,dl
jmp e_label
n_label:
mov cl,1
shl dl,cl
e_label:
mov dh,dl

Question 22

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL, 0F

ADD AL, F1

watch point:

Question 23

Complete

Marked out of 0.50

Which are correct action for STOSB string operation if DF is reset (=0)

Select one or more:

- decrease DI by 1
- Store 8-bit value from AL into memory location pointed by DS:[SI]
- increase DI by 1
- Store 8-bit value from AL into memory location pointed by ES:[DI]

Question 24 Complete Marked out of 1.00	What are components of Von Neumann, namely IAS computer? Select one or more: I/O Equipments Monitor CPU Memory Bus Punched card reader
Question 25 Not answered Marked out of 1.00	Compute the physical address of the next instruction will be execute if instruction pointer is 091D and code segment located at 1FAF Answer:
Question 26 Complete Marked out of 1.00	Which set of registers are valid for addressing a stack memory location? Select one or more: SS:BP SS:BX DS:SI SS:SP
Question 27 Complete Marked out of 0.50	The instruction that is used for finding out the codes in case of code conversion problems is Select one: XOR JCXZ XLAT XCHG

Complete

Marked out of 0.50

To clear one or more bits in a byte value, use _____

Select one:

- OR
- NOT
- AND
- XOR

Question 29

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

instruction.

MOV AL,-5

SUB AL,124

watch point:

not defined 🔻

reset

set

set

Question 30

Complete

Marked out of 1.00

the memory stack area of a program shown in figure

Address	1D50	1D51	1D52	1D53
Value	AF	90	71	DA

The value of SP register is 1D50. What is the value of SP follows the execution of PUSH SI

Answer: 90

Question 31

Complete

Marked out of 1.00

Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D

Answer: ADD 0D, 256[100]

Complete

Marked out of 0.50

Which are correct action for LODSB string operation if DF is reset (=0)

Select one or more:

- increase SI by 1
- Load 8-bit value at memory location pointed by ES:[DI] into AL
- Load 8-bit value at memory location pointed by DS:[SI] into AL
- decrease DI by 1

Question 33

Complete

Marked out of 1.20

```
Given a code snippet:
```

```
int n = 10;
do {
```

n--;

 $\}$ while (n > 0);

Which ones are the equivalent logic sequence of instructions in Assembly

Select one or more:

```
mov cx, 10
```

a_label:

__iabci.

dec cx

cmp cx, 0

jz e_label

jmp a_label

e_label:

✓ mov cx, 10

a_label:

.....

dec cx

loop a_label

mov cx, 10

a_label:

.

dec cx

cmp cx,0

jz a_label

mov cx, 10

a_label:

.....

loop a_label

Question 34 Complete

Marked out of 1.00

For better speed, in CPU design, engineers make use of the following techniques:

Select one or more:

- Speculative execution
- Branch prediction
- Faster CPU internal bus
- Pipelining

Question 35

Complete

Marked out of 0.50

In multiplication instruction, when the source operand is 8 bit, _____ will be multiplied with source.

Select one:

- Whatever general purpose register
- BX
- AL
- \bigcirc AX

Question 36

Complete

Marked out of 1.00

Which are valid based index addressing?

Select one or more:

- [BX+SI]
- ✓ [BX+DI]
- [DX+SI]
- [SP+DI]

Question 37

Complete

Marked out of 1.00

Memory dump at 1D20:0200 as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers: DS = 1D20, SI = 200, BX = 202, AX = 0103

Identify correct value of AX register after XLAT instruction is executed.

Complete

Marked out of 1.20

```
Given a code snippet (ax, bx are none negative integers):
if (ax >= bx)
  ax -=bx;
else
  bx -=ax;
What is the equivalent logic sequence of instructions in Assembly
Select one:
   cmp ax,bx
    jbe a_label
    sub ax,bx
    jmp x_label
   a_label:
    sub bx,ax
   x_label:
cmp ax,bx
    jb a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
cmp ax,bx
    ja a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
```

cmp ax,bx jnbe a_label sub ax,bx jmp x_label a_label: sub bx,ax

x_label:

Question 39 Complete Marked out of 0.50	The instruct Select one: Immedi direct register index	ate	OV AX, 0	005h be	longs to	which ac	Idressing	g mode?		
Question 40	Part of com	puter m	emory is	shown	in figure					
Complete	Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F	
Marked out of 1.00	Value	03	7F	F5	2D	5A	12	7B	C0	
	What is the		f AX reg	ister afte	er instruc	tion MO \	/ AX, [1I	D4B] exe	ecuted	
Question 41	Which of the	e followi	ing instru	uctions a	re not va	alid?				
Complete										
Marked out of 0.50	Select one of MOV A									
		_	۷)							
	MOV A		N.							
	✓ MOV D									
	✓ MOV S	P, SS:[S	51+2]							

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

MOV AX,0020

MOV CX,0010

MUL CL

watch point:

Question 43

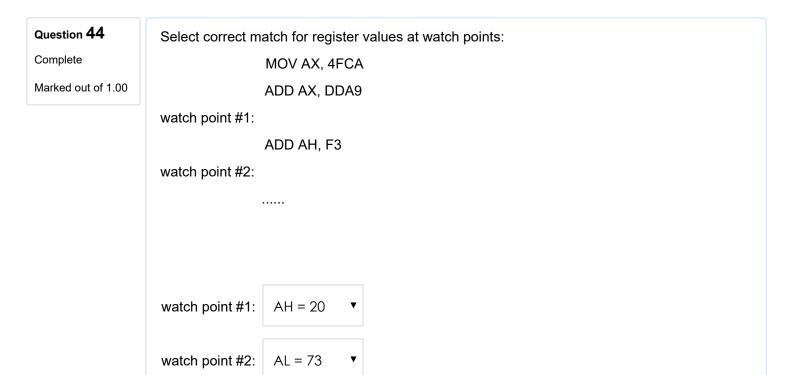
Complete

Marked out of 1.00

Basic functions that a computer can perform including:

Select one or more:

- Data movement
- Direct memory access
- Control
- Data storage
- Interrupt
- Data processing



Question 45 Complete

Marked out of 1.20

05:

CWD

Hereafter is instruction sequence to compute the sum of 8 bytes starting at memory address 200. Two lines of code are possibly missing. Choose correct one to fill in? 01: _; possibly missing code 02: MOV AL, 0

03: MOV CX, 8 04: Loop_label: 05: _; possibly missing code 06: ADD AX, [SI]; 07: INC SI LOOP Loop_label 08: 01: MOV SI, 200

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Started on Monday, 5 June 2017, 1:11 PM

State Finished

Completed on Monday, 5 June 2017, 2:20 PM

Time taken 1 hour 9 mins

Question	1	

Complete

Marked out of 1.20

Convert the 32-bit floating point number 44363C00 (in hex) to decimal.

Answer: 1144404992

Question 2

Complete

Marked out of 0.50

The instruction that subtracts 1 from the contents of the specified register/memory location is

Select one:

- SUB
- DEC
- SBB
- INC

18/5/2018 Question **3**

Complete

Marked out of 1.00

Kiểm tra cuối kỳ đề 2

Memory dump at 1D20:0200 as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers:

DS = 1D20, ES = 1D20,

DI = 20A, SI = 208,

BX = 202, AX = 0103, CX = 0003

and flag bit DF = 1

What is the correct value of AX, SI, DI registers after the instruction REP LODSW is executed?

DI = 0202h
$$\checkmark$$

AX = 5040h \checkmark

SI = 5547h \checkmark

Question 4

Complete

Marked out of 0.50

Which are correct action for SCASW string operation if DF is reset (=0)

Select one or more:

- compare value in AL register with memory location pointed by DS:[SI]
- decrease DI by 2
- increase DI by 2
- compare value in AL register with memory location pointed by ES:[DI]

Question 5

Complete

Marked out of 1.50

Which are correct about the Pointer registers of IA-32 processors:

Select one or more:

- Base Pointer (BP): The 16 bit pointer refers to stack memory
- Stack Pointer (SP): the 16 bit pointer to the top of stack
- Instruction Pointer (IP): the 16 bit register points to the next instruction to be execute
- Base Pointer (EBP): The 32 bit pointer refers to stack memory
- Stack Pointer (ESP): the 32 bit pointer to the top of stack
- Instruction Pointer (EIP): the 32 bit register points to the next instruction to be execute

Question 6 Complete Marked out of 1.00	What are components of Von Neumann, namely IAS computer? Select one or more: Punched card reader Bus Monitor Memory I/O Equipments CPU
Question 7 Complete Marked out of 1.00	Which statements are correct for HDDs? Select one or more: ☐ Head, Track, Cylinder are key parameters for access data on hard disk ☑ Head, Track, Sector are key parameters for access data on hard disk ☐ Bits are store randomly on disk surfaces ☑ Bits are stored on tracks
Question 8 Complete Marked out of 0.50	The instruction that loads effective address is Select one: LAHF LDS LEA LES
Question 9 Not answered Marked out of 1.00	Enter debug command to fill 250 bytes in the memory segment FED5 in computer memory starting from 100 with value AD Answer:



Complete	EBX, EDX at watch point?
Marked out of 1.00	MOV EAX,00002000
	MOV EBX,00100000
	MUL EBX
	watch point:
	EAX = 00000002 ▼
	EDX = 00000000 ▼
	EBX = 00021000 ▼
Question 11	Convert 39887.5625 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa) in hex
Not answered	
Marked out of 1.20	Answer:
Question 12	The instruction, MOV AX, 1234h is an example of
Complete	
Marked out of 0.50	Select one:
	Immediate addressing mode
	based index addressing mode
	 direct addressing mode
	register addressing mode

The following sequence of instructions are executed. What is the correct value of EAX,

Question 10

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL, 78

MOV BL, 2

MUL BL

watch point:

Question 14

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL,-5

ADD AL,132

ADD AL,1

watch point:

Question 15

Complete

Marked out of 1.00

In computer, how does the processor serve multiple interrupt request from devices?

Select one:

- Device with higher priority will use interrupt enable flag
- Each device are assigned an interrupt priority, the device with higher priority will be served.
- The processor can not process multiple interrupt requests
- Each device are assigned an interrupt priority, the device with lower priority will be served.

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Question 16	the instruction, JMP C008:2000h is an example of									
Complete										
Marked out of 0.50	Select one or more:									
	intersegment jump									
	far jump									
	near jump									
	✓ intrasegment mode									
Question 17	In multiplication instruction, the result is taken from AX means the source operand is									
Complete	bit									
Marked out of 0.50	Select one:									
	8									
	16									
	None of the choices are correct									
	4									
Question 18	Memory dump at 1D20:0200 shown as below:									
Complete	1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70									
Marked out of 1.00	Given value of registers:									
	DS = 1D20, ES = 1D20, DI = 20A									
	The following sequence of instructions is being executed:									
	MOV SI,208h									
	MOV AX,0040h									
	MOV CX,000Ah									
	CLD									
	REPNZ SCASB									
	watch point:									
	What is the correct value of AX, SI, DI registers at watch point?									
	SI = 020Ch ▼									
	DI = 4030h ▼									
	AX = 020Bh ▼									

Question 19 What is the correct value of SI, AL (in hex) at watch point: Complete 01: MOV SI, 300h 02: MOV AL, 10h Marked out of 1.00 03: MOV CX, 7 04: Loop_label: 05: MOV [SI], AL ADD AL,10h 06: INC SI 07: 08: LOOP Loop_label watch point: SI 308h

Question 20 Physical address

Not answered register which no

AL =

70h

Marked out of 1.00

Physical address of a memory location is 5FE2E. This memory address located by DI register which now has value of 993E. Compute the memory address of data segment register

Answer:

Question 21

Complete

Marked out of 1.00

Basic functions that a computer can perform including:

Select one or more:

- Direct memory access
- Data movement
- Data processing
- Control
- Interrupt
- Data storage



Complete

Marked out of 1.20

```
Given a code snippet:
int ax, bx;
if (ax >= bx)
  ax -=bx;
else
  bx -=ax;
What is the equivalent logic sequence of instructions in Assembly
Select one:
cmp ax,bx
    jbe a_label
    sub ax,bx
    jmp x_label
   a_label:
    sub bx,ax
   x_label:
cmp ax,bx
    jl a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
cmp ax,bx
    jge a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
cmp ax,bx
    ja a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
```

Complete

Marked out of 1.20

```
Given an assembly code copying the memory buffer Buff1 to Buff2:
     PUSH DS
     POP ES
     LEA SI, Buff1
     LEA DI, Buff2
     MOV CX,20
     ;--- Start of block
cp_loop:
     MOV AL, Byte Ptr [SI]
     MOV Byte Ptr ES:[DI], AL
     INC SI
     INC DI
     LOOP cp_loop
     ; ---End of block
Choose equivalent string operations in place of block code from ---Start of block to ---End
of block
Select one or more:
       CLD
   cp_loop:
      MOVSB
      LOOP cp_loop
```

Question 24

Complete

Marked out of 0.50

After each execution of POP instruction, the stack pointer is

Select one:

increment by 1

CLD cp_loop:

CLD

STD cp_loop: MOVSB

REP MOVSB LOOP cp_loop

REP MOVSB

LOOP cp_loop

- increment by 2
- decrement by 2
- decrement by 1



Question 25	Given a row of memory image in debug							
Complete	0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24							
Marked out of 1.00	Initially, AX=BX=CX=DX=0, SI=128							
	What are value of AX,DX after execution of the following instructions?							
	MOV EDX, [SI]							
	MOV EAX, [SI+4]							
	EDX = 99007524 ▼							
	EAX = 203E8099 ▼							
Question 26	Dort of moment chause in figure							
Not answered	Part of memory shown in figure							
	Address 1D48 1D49 1D4A 1D4B 1D4C 1D4D 1D4E 1D4F							
Marked out of 1.00	Value 03 7F F5 2D 5A 12 7B C0							
	What is the value of AH follow the execution of this code:							
	MOV BX, 1D4D							
	MOV AX, [BX]							
	Answer:							
	Allower.							
. 07								
Question 27	Which are valid based indexed addressing?							
Complete	Select one or more:							
Marked out of 1.00	□ [SP][SI]							
	■ [BP][SI]							
	□ [DX][DI]							

Question 28 Complete Marked out of 1.20

Consider the following assembly instruction sequence XOR BX, BX CMP DL, 5 JLE a label CMP DL,17h JGE a_label MOV BX, 10h a_label: INC BX watch point: Choose correct value of BX register at watch point for different value of DL? DL=0FFh 11h DL=10 01h DL=17h 01h DL=0Ah 28h

Question 29

Not answered

Marked out of 1.00

Part of computer memory are shown in figure.

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F	
Value	03	7F	F5	2D	5A	12	7B	C0	

What is the value of AX register after instruction MOV AX, 1D49 executed

Answer:	:			
---------	---	--	--	--

Question 30

Complete

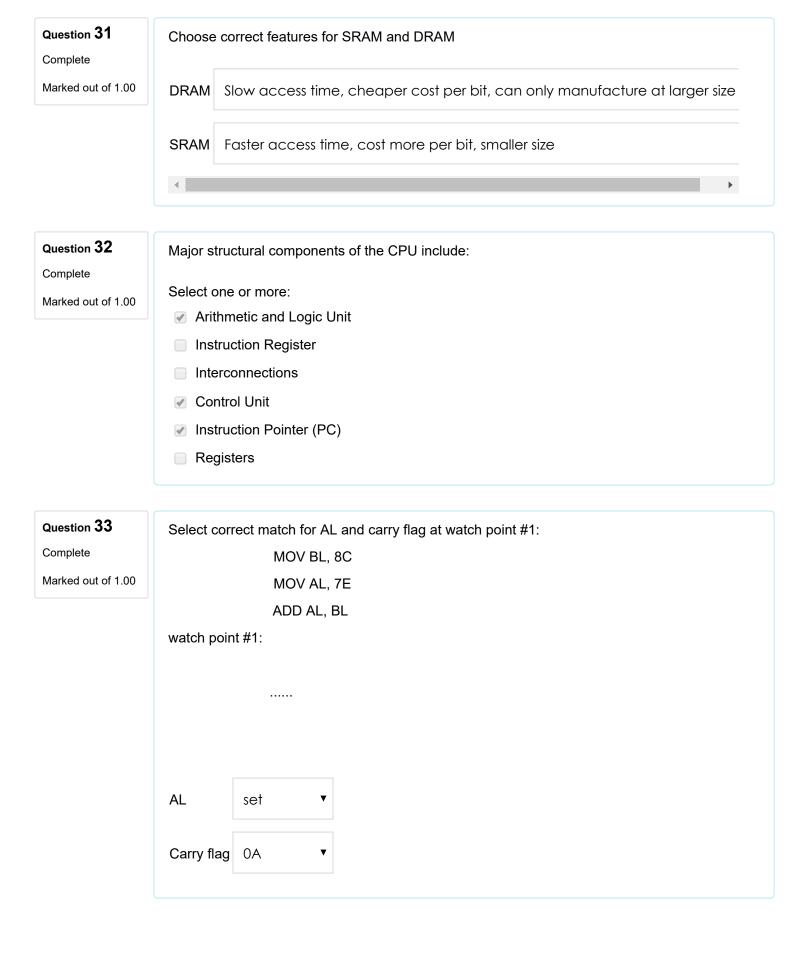
Marked out of 0.50

To set one or more bits in a byte value, use _____ instruction.

Select one:

- NOT
- XOR
- AND
- OR





Complete

Marked out of 1.20

```
Given a code snippet:
if (a>=0 && a <=9)
  x = a + 30h;
else if (a >=10 && a <=15)
  x = a + 55;
The logic of the above code snippet in assembly is (with missing lines):
01:
        CMP DL, 0
02:
        -----; possibly missing code
03:
        CMP DL, 9
04:
        -----; possibly missing code
05:
        ADD DL, 30h
06:
        -----; possibly missing code
a_label:
08:
        CMP DL, 0Fh
        -----; possibly missing code
09:
10:
        ADD DL, 55
x_label:
12:
        MOV AL, DL
Choose correct missing instructions in the above sequence of instructions
02:
     JMP a_label ▼
06:
     JMP x_label
04:
     empty
09:
     empty
```

Complete

Marked out of 1.50

Given a row of memory image in debug

072C:FFF0 00 00 00 01 00 00 2C 07 - 07 01 2C 07 17 72 00 00

SS=072C, SP=FFF8, DS = 072C

Assume the stack now stores two (2) 16-bit parameters and one (1) 16-bit return address in following order: stack top (return address) >> parameter #1 >> parameter #2.

The following sequence of instructions are executed. What is the correct values at watch points?

MOV BP, SP

watch point #1 (BP):

MOV AX, [BP+2]

watch point #2 (AX):

ADD AX, [BP+4]

watch point #3 (AX):

MOV DI, 120

MOV [DI], AX

watch point #1:

AX = 2C07

watch point #2:

BP = FFF8

watch point #3:

SUB AX, [SI]

Complete

Marked out of 1.20

Given a code snippet to look for a value (from AL) in memory buffer Buff

Buff DB 11,22,33,44,55

.....

01: LEA DI, Buff

02: -----; possibly missing code

03: MOV AL,3304: MOV CX,5

a_label:

05: -----; possibly missing code

06: CMP Byte Ptr [DI],AL

07: -----; possibly missing code

08: LOOPNZ a_label

...

Choose correct missing instructions in the above sequence of instructions

05: INC DI ▼

07: DEC DI ▼

02: Empty

Question 37

Complete

Marked out of 0.50

In multiplication instruction, when the value of source operand is 12 (decimal), the other operand is loaded in AX. Which registers can be used to load source operand?

Select one or more:

✓ DX

BX

CL

AX

DL



Question 38 Complete Marked out of 1.00	The following sequence of instructions are executed. What is the correct value of AX and DX (in hex) at watch point? MOV AX,FFF6h MOV CX,1000h IMUL CX watch point: AX= FFF6 DX= 6000 T
Question 39 Complete Marked out of 0.50	the instruction, CMP to compare source and destination operands by Select one: comparing subtracting dividing adding
Question 40 Complete Marked out of 0.50	To test one bit in a byte value which can be destructive. use instruction. Select one: TEST AND OR NOT
Question 41 Complete Marked out of 0.50	Which are correct input for XLAT instruction Select one or more: ✓ DS:[BX] pointed to look-up table DS:[SI] pointed to look-up table look-up index must be loaded into DL look-up index must be loaded into AL

Complete

Marked out of 0.50

Which are correct action for LODSW string operation if DF is reset (=0)

Select one or more:

- ✓ increase SI by 2
- Load 16-bit value at memory location pointed by DS:[SI] into AX
- Load 16-bit value at memory location pointed by ES:[DI] into AX
- decrease DI by 2

Question 43

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV DL,19

MOV AL, F6

IMUL DL

watch point:

Question 44

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, DX at watch point?

MOV DL,FF

MOV AL,42

IMUL DL

watch point:

Question 45

Not answered

Marked out of 1.20

Write mask byte (in hex) to clear the lower 4 bit of a byte value with AND instruction.

Answer:

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Started on Monday, 5 June 2017, 1:11 PM

State Finished

Completed on Monday, 5 June 2017, 2:20 PM

Time taken 1 hour 9 mins

Question	1	
Complete		

Marked out of 1.00

The fol watch	wing sequence of instructions are executed. What is the correct value of flag bits at int?
	MOV DL,FF
	MOV AL,F6
	IMUL DL
watch	int:
OF =	reset •
CE -	rocat •

Complete Marked out of 0.50 In multiplication instruction, when the source operand is 16 bit, how can the result be taken? Select one: from DX:AX pair from EAX from AX:DX pair

Question 3

Not answered

Marked out of 1.20

from AX

```
Consider the following assembly instruction sequence
     CMP DL, 0
     JB x_label
     CMP DL, 9
     JA a_label
     ADD DL, 30h
     JMP x_label
a_label:
     CMP DL, 0Fh
     JA x_label
     ADD DL, 37h
x_label:
     MOV AL, DL
watch point:
Choose correct value of AL register at watch point for different value of DL?
DL=10
          Choose... ▼
DL=8
          Choose...
DL=55h
          Choose... ▼
DL=0FFh Choose... ▼
```

Question 4 Hereafter is instruction sequence to compute the sum of 8 bytes starting at memory address 200. Two lines of code are possibly missing. Choose correct one to fill in? Complete _; possibly missing code 01: Marked out of 1.20 02: MOV AL, 0 MOV CX, 8 03: 04: Loop_label: 05: _; possibly missing code 06: ADD AX, [SI]; 07: INC SI 08: LOOP Loop_label MOV [SI],200 01:

Question 5

Complete

Marked out of 0.50

In multiplication instruction, when the source operand is 8 bit, _____ will be multiplied with source.

Select one:

CWD

05:

- AX
- BX
- AL
- Whatever general purpose register

Question 6

Complete

Marked out of 1.00

Which are valid based index addressing?

Select one or more:

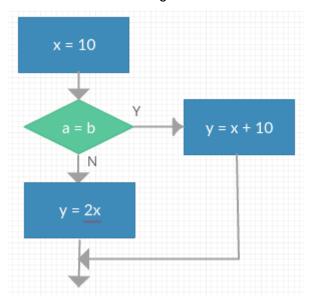
- ✓ [BX+DI]
- ✓ [DX+SI]
- [SP+DI]
- ✓ [BX+SI]



Not answered

Marked out of 1.20

Given a flowchart of an algorithm:



Select the correct instruction sequence:

Select one or more:

- mov dl,10
 - cmp al,bl
 - jnz n_label
 - add dl,10
 - jmp e_label
 - n_label:
 - mov cl,1
 - shl dl,cl
 - e_label:
 - mov dh,dl
- mov dl,10
 - cmp al,bl
 - jz n_label
 - mov cl,1
 - shl dl,cl
 - jmp e_label
 - n_label:
 - add dl,10
 - e_label:
 - mov dh,dl
- mov dl,10
 - cmp al,bl
 - jnz n_label
 - add dl,10
 - jmp e_label
 - n_label:
 - mov cl,1
 - shr dl,cl
 - e_label:
 - mov dh,dl

mov dl,10
cmp al,bl
jnz n_label
add dl,10
mov dh,dl
jmp e_label
n_label:
mov cl,1
shl dl,cl
e_label:
mov dh,dl

Question 8

Complete

Marked out of 1.00

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction MOV AX, [1D4B] executed

Answer: 2D

Question 9

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of AX, CX, DX at watch point?

MOV AX,0020

MOV CX,0010

MUL CL

watch point:

Complete

Marked out of 1.00

Which set of registers are valid for addressing a stack memory location?

Select one or more:

- DS:SI
- SS:SP
- SS:BP
- SS:BX

Question 11

Complete

Marked out of 1.00

In computer, how does the processor serve multiple interrupt request from devices?

Select one:

- Each device are assigned an interrupt priority, the device with lower priority will be served.
- Device with higher priority will use interrupt enable flag
- Each device are assigned an interrupt priority, the device with higher priority will be served.
- The processor can not process multiple interrupt requests

Question 12

Complete

Marked out of 1.00

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24

Initially, AX=BX=CX=DX=0, SI=128

What are value of AX,DX after execution of the following instructions?

MOV EDX, [SI]

MOV EAX, [SI+4]

Question 13
Complete
Marked out of 1.00

Basic functions that a computer can perform including:

Select one or more:

Data movement

Control

Interrupt

Data processing

Data storage

Direct memory access

Question 14

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AX,FFFF

MOV CX,5

MUL CX

watch point:

Not answered

Marked out of 1.20

```
Given a code snippet:
int n = 10;
do {
   n--;
\} while (n > 0);
Which ones are the equivalent logic sequence of instructions in Assembly
Select one or more:
      mov cx, 10
    a_label:
       dec cx
      cmp cx, 0
      jz e_label
      jmp a_label
    e_label:
 mov cx, 10
    a_label:
     loop a_label
 mov cx, 10
    a_label:
     ....
     dec cx
     cmp cx,0
     jz a_label
 mov cx, 10
    a_label:
     dec cx
     loop a_label
```

Question 16

Not answered

Marked out of 1.20

Write mask byte (in hex) to clear bit 2nd	, 3rd, 5th of a byte value w	ith AND instruction (LSB is 1st
bit).		

Answer:

Question 17	the memory stack area of a program shown in figure		
Complete	Address 1D50 1D51 1D52 1D53		
Marked out of 1.00	Value AF 90 71 DA		
	The value of SP register is 1D50. What is the value of SP follows the execution of PUSH SI Answer: 90		
Question 18 Complete Marked out of 0.50	To clear one or more bits in a byte value, use instruction. Select one: AND XOR OR NOT		
Question 19 Complete	The instruction, MOV AX, 0005h belongs to which addressing mode?		
Marked out of 0.50	Select one: register		
	o direct		
	index		
	Immediate		
Question 20 Complete Marked out of 1.00	Which are correct about the data registers of IA-32 processors: Select one or more: Lower halves of the 16-registers an be used as 8-bit data registers:		
	AH,AL,BH,BL,CH,CL,DH,DL		
	■ Lower halves of the 32-registers an be used as 4 16-bit data registers: AX,BX,CX,DX		



Question 21	What are components of Von Neumann, namely IAS computer?
Not answered	
Marked out of 1.00	Select one or more:
	Monitor
	Memory
	I/O Equipments
	Punched card reader
	Bus
	□ CPU

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL,-5

SUB AL,124

watch point:

Question 23

Complete

Marked out of 1.00

Enter debug command to fill 256 bytes in data segment starting from 100 with value 0D

Answer: F 100 1FF 0D

Question 24 Not answered Marked out of 0.50	Which are correct action for STOSB string operation if DF is reset (=0) Select one or more: decrease DI by 1 Store 8-bit value from AL into memory location pointed by ES:[DI] increase DI by 1 Store 8-bit value from AL into memory location pointed by DS:[SI]
Question 25 Complete Marked out of 1.00	For better speed, in CPU design, engineers make use of the following techniques: Select one or more: Pipelining Branch prediction Faster CPU internal bus Speculative execution
Question 26 Complete Marked out of 1.00	The following sequence of instructions are executed. What is the correct value of CF and OF at watch point? MOV AX,FFF6h MOV CX,1000h IMUL CX watch point: CF= reset OF= reset The following sequence of instructions are executed. What is the correct value of CF and OF and OF at watch point?
Question 27 Complete Marked out of 0.50	Which are correct action for SCASW string operation if DF is set (=1) Select one or more: decrease DI by 2 compare value in AL register with memory location pointed by ES:[DI] compare value in AL register with memory location pointed by DS:[SI] increase DI by 2

Question 28

Complete

Marked out of 1.00

Given a row of memory image in debug

0AE8:0120 13 96 D0 E0 D0 E0 A2 1E - 99 80 3E 20 99 00 75 24

SI = 120, DI = 128

Select correct sequence of instructions to subtract words at [DI] from [SI] then store the result at memory location 12A

Step 1:

MOV AX, [SI]

Step 2:

SUB AX, [DI]

Step 3:

MOV BX, 012A ▼

Step 4:

MOV [BX], AX

Question 29

Complete

Marked out of 1.00

Select correct match for register values at watch points:

MOV AX, 4FCA

ADD AX, DDA9

watch point #1:

ADD AH, F3

watch point #2:

watch point #2:

AL = 73

watch point #1:

AH = 30

Question 30

Complete

Marked out of 1.00

Compute the physical address of the next instruction will be execute if instruction pointer is 091D and code segment located at 1FAF

Answer: 2040D



Question 35

Complete

Marked out of 1.00

The following sequence of instructions are executed. What is the correct value of flag bits at watch point?

MOV AL, 0F

ADD AL, F1

watch point:

Question 36

Complete

Marked out of 1.00

Memory dump at 1D20:0200 as below:

1D20:0200 00 20 10 5D 55 47 00 90 - 00 10 20 30 40 50 60 70

Given value of registers: DS = 1D20, SI = 200, BX = 202, AX = 0103

Identify correct value of AX register after XLAT instruction is executed.

Question 37

Not answered

Marked out of 1.20

```
Given a code snippet (ax, bx are none negative integers):
if (ax >= bx)
  ax -=bx;
else
  bx -=ax;
What is the equivalent logic sequence of instructions in Assembly
Select one:
cmp ax,bx
    jnbe a_label
    sub ax,bx
    jmp x_label
   a label:
     sub bx,ax
   x_label:
cmp ax,bx
    jb a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
cmp ax,bx
    jbe a_label
    sub ax,bx
    jmp x_label
   a_label:
     sub bx,ax
   x_label:
cmp ax,bx
    ja a_label
     sub ax,bx
    jmp x_label
   a_label:
```



sub bx,ax x_label:

Question 38 Complete Marked out of 0.50	Which of the following instructions are not valid? Select one or more: MOV AX, SI MOV AX, [BP+2] MOV SP, SS:[SI+2] MOV DS, B800h
Question 39 Complete Marked out of 0.50	if the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is call
	Select one: intrasegment direct mode intrasegment mode intrasegment mode intrasegment indirect mode
Question 40 Complete Marked out of 0.50	The instruction that supports addition when carry exists is Select one: ADD ADC DAS SBB
Question 41 Not answered Marked out of 1.20	Convert 0.1015625 to IEEE 32-bit floating point format (1 sign+ 8 exponent + 23 mantissa) Answer:

Question 42 Complete Marked out of 0.50	The instruction that is used for finding out the codes in case of code conversion problems is Select one: JCXZ XCHG XLAT XOR
Question 43 Complete Marked out of 1.00	Which statements are correct for HDDs? Select one or more: Head, Track, Cylinder are key parameters for access data on hard disk Head, Track, Sector are key parameters for access data on hard disk Bits are stored on tracks Bits are store randomly on disk surfaces
Question 44 Complete Marked out of 0.50	Which are correct action for LODSB string operation if DF is reset (=0) Select one or more: increase SI by 1 Load 8-bit value at memory location pointed by ES:[DI] into AL decrease DI by 1 Load 8-bit value at memory location pointed by DS:[SI] into AL
Question 45 Complete Marked out of 0.50	To test one bit in a byte value without destructing the byte, use instruction. Select one: AND TEST NOT OR



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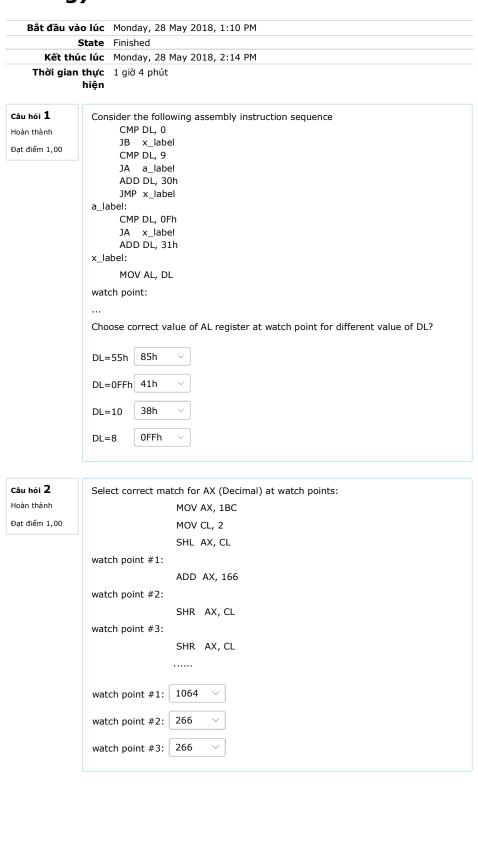






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THI Kiến trúc máy tính và hợp ngữ (Thi Chung)





Câu hỏi 3 Hoàn thành	if the location to which the control is to be transferred lies in a segment other than the current one, then the jump instruction is called
Đạt điểm 0,50	Select one:
	o intrasegment mode
	intersegment mode
	intrasegment indirect mode
	○ intrasegment direct mode
Câu hỏi 4 Hoàn thành	Structural components of computer include:
Đạt điểm 1,00	Select one or more:
	☐ Interrupt
	☑ Central processing unit
	☑ 1/0
	□ DMA
Câu hỏi 5	Which could be correct ones for the destination operand in a data movement instruction?
Hoàn thành	IIISCI UCCIOTI:
Đạt điểm 0,50	Select one or more:
	☐ immediate data
	☐ all choices are correct
	☑ register
Câu hỏi 6	the instruction, JMP C008:2000h is an example of
Hoàn thành	Select one or more:
Đạt điểm 0,50	☐ intrasegment mode
	□ near jump
	☐ intersegment jump
	☑ far jump
	_ , ,
Câu hỏi 7	Given a row of memory image in debug
Hoàn thành	0AE8:0120 13 96 D0 E0 00 40 08 42 - 99 80 3E 20 99 00 75 24
Đạt điểm 1,00	SI = 120
Dut diem 1,00	The following instruction is executed:
	MOV EAX, [SI+4] Assume the value in EAX is a 32-bit floating-point binary, what is the value of
	EAX in decimal?
	Answer: 4000

Câu hỏi 8	
Hoàn thành	Given a code snippet:
Đạt điểm 1,00	int n = 10;
Dạt tiem 1,00	do {
	n;
	} while (n > 0);
	Which ones are the equivalent logic sequence of instructions in Assembly
	Select one or more:
	☑ mov cx, 10
	a_label:
	loop a label
	loop a_label
	mov cx, 10 a_label:
	dec cx
	cmp cx,0 jz a_label
	mov cx, 10 a_label:
	dec cx
	loop a_label
	dec cx
	cmp cx, 0
	jz e_label jmp a_label
	e_label:
Hoàn thành Đạt điểm 1,00	value of AX, CX, DX at watch point? MOV AX,30 MOV CX,FFFF MUL CX watch point: CX = FFFF AX = DX 002F
Câu hỏi 10 Không trả lời Đạt điểm 0,50	Write mask byte (in hex) to set higher 4 bits in a byte value with OR instruction (LSB is the 1st bit). Answer:



Select one:	Câu hỏi 11	After executing PUSH EAX instruction, the stack pointer
oincrement by 1 oincrement by 2 Given an assembly code copying the memory buffer Buff1 to Buff2: PUSH DS POP ES LEA SI, Buff1 LEA DI, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [S1] MOV Byte Ptr ES:[D1], AL INC SI INC SI INC SI LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: SEP MOVSB LOOP cp_loop CLD CREP MOVSB LOOP cp_loop CLD CREP MOVSB Câu hỏi 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		Select one:
© decrements by 4 ○ decrement by 1 ○ increment by 2 Cau hoi 12 (Rinông trà lới PUSH DS POP ES LEA SI, Buff1 LEA DI, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ; End of block Choose equivalent string operations in place of block Select one or more: □ CLD cp_loop: MOVSB LOOP cp_loop □ STD cp_loop: MOVSB LOOP cp_loop □ CLD cp_loop: MOVSB LOOP cp_loop □ CLD REP MOVSB LOOP cp_loop □ CLD REP MOVSB LOOP cp_loop □ CLD REP MOVSB LOOP cp_loop □ CLD REP MOVSB Cau hoi 13 Hoàn thành bạt điểm 0,50 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.	Đạt điểm 0,50	O increment by 1
Câu hoi 12 Câu hoi 12 Câu hoi 12 Given an assembly code copying the memory buffer Buff1 to Buff2: PUSH DS POP ES LEA SI, Buff1 LEA DI, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ; End of block Choose equivalent string operations in place of block Select one or more: □ CLD cp_loop: MOVSB LOOP cp_loop □ STD cp_loop: MOVSB LOOP cp_loop □ CLD sp_loop: MOVSB LOOP cp_loop □ CLD STD cp_loop: MOVSB LOOP cp_loop □ CLD SEP MOVSB LOOP cp_loop □ CLD SEP MOVSB LOOP cp_loop □ CLD SEP MOVSB COMPS Select one: ○ CMPS ○ SCAS ○ CMPS ○ REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
Given an assembly code copying the memory buffer Buff1 to Buff2: PUSH DS POP ES LEA SI, Buff1 LEA DI, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ; End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop STD CSLOP cp_loop CLD cp_loop STD CSLOP cp_loop CLD cp_loop CLD cp_loop CLD REP MOVSB LOOP cp_loop CLD CD		i i i i i i i i i i i i i i i i i i i
Câu họi 12 Không trả lời Đạt điểm 1,00 Given an assembly code copying the memory buffer Buff1 to Buff2: PUSH DS POP ES LEA SI, Buff1 LEA DI, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ; End of block Choose equivalent string operations in place of block Select one or more: CLD Cp_loop: MOVSB LOOP cp_loop STD Cp_loop: MOVSB LOOP cp_loop CLD Cp_loop: MOVSB LOOP cp_loop CLD Cp_loop: MOVSB LOOP cp_loop CLD Cp_loop: REP MOVSB LOOP cp_loop CLD REP MOVSB Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		,
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PUSH DS POPE ES	Câu hỏi 12	Given an assembly code copying the memory buffer Buff1 to Buff2:
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LEA DJ, Buff2 MOV CX,20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: SEP MOVSB Select one: CCUP SELOOP cp_loop CLD REP MOVSB COMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.	Đạt điểm 1,00	POP ES
MOV CX_20 ; Start of block cp_loop: MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ; End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD cp_loop: Select one: CMPS Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
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MOV AL, Byte Ptr [SI] MOV Byte Ptr ES:[DI], AL INC SI INC DI LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD Cp_loop: MOVSB LOOP cp_loop STD Cp_loop: MOVSB LOOP cp_loop CLD Cp_loop: REP MOVSB LOOP cp_loop CLD Cp_loop: REP MOVSB LOOP cp_loop CLD Cp_loop: STD Count hoi 13 He instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
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INC SI INC DI LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD rp_loop: REP MOVSB LOOP cp_loop SEP MOVSB LOOP cy_loop CLD REP MOVSB Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
INC DI LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD REP MOVSB LOOP cp_loop CLD REP MOVSB LOOP cp_loop CLD REP MOVSB Cau hoi 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Câu hoi 14 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
LOOP cp_loop ;End of block Choose equivalent string operations in place of block Select one or more: CLD cp_loop: MOVSB LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD REP MOVSB LOOP cp_loop CLD REP MOVSB Cau hoi 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Cau hoi 14 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
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Câu hỏi 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Câu hỏi 14 Hoàn thành Dạt điểm 0,50 Câu hỏi 14 Hoàn thành Dạt điểm 0,50 Câu hỏi 14 Hoàn thành Dạt điểm 0,50		Choose equivalent string operations in place of block
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LOOP cp_loop STD cp_loop: MOVSB LOOP cp_loop CLD cp_loop: REP MOVSB LOOP cp_loop CLD REP MOVSB LOOP cp_loop CLD REP MOVSB Câu hỏi 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Câu hỏi 14 Hoàn thành Bạt điểm 0,50 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
cau hói 13 the instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
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Câu hỏi 13 Hoàn thành Đạt điểm 0,50 Câu hỏi 14 Hoàn thành Đạt điểm 0,50 Câu hỏi 14 Hoàn thành Đạt điểm 0,50 Câu hỏi 14 Hoàn thành Đạt điểm 0,50		□ CLD
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until the CX register becomes zero is Select one: CMPS SCAS CMPS REP Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
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Select one: CMPS SCAS CMPS REP Câu hỏi 14 Hoàn thành Dạt điểm 0,50 Select one: CMPS SCAS CMPS REP		
○ SCAS ○ CMPS ③ REP Câu hỏi 14 Hoàn thành Dạt điểm 0,50 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
○ CMPS ● REP Câu hỏi 14 Hoàn thành Dạt điểm 0,50 CMPS Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		
© REP Câu hỏi 14 Hoàn thành Dạt điểm 0,50 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction.		○ SCAS
Câu hỏi 14 Write mask byte (in hex) to clear all the lower 7 bits of a byte value with AND instruction. Dạt điểm 0,50		○ CMPS
Hoàn thành instruction.		
Hoàn thành instruction.	os L.2. 1 A	With and has the hard at the same of the s
Dạt điểm 0,50		
Answer: AND AL, 01111111B		
	Đặt điểm 0,50	Answer: AND AL, 011111111B

n debug 01 00 00 2C 07 - 07 01 2C 07 17 72 00 00 DS = 072C 10 (2) 16-bit parameters and one (1) 16-bit r: stack top (return address) >> parameter #1 ctions are executed. What is the correct values
01 00 00 2C 07 - 07 01 2C 07 17 72 00 00 DS = 072C o (2) 16-bit parameters and one (1) 16-bit r: stack top (return address) >> parameter #1
DS = 072C o (2) 16-bit parameters and one (1) 16-bit r: stack top (return address) >> parameter #1
o (2) 16-bit parameters and one (1) 16-bit r: stack top (return address) >> parameter #1
r: stack top (return address) >> parameter #1
ctions are executed. What is the correct values
from the contents of the specified



Không trả lời Đạt điểm 1,00 Ti W W D A S = S =	X Chọn > I Chon >
Dạt điểm 1,00 G D TI	iven value of registers: S = 1D20, ES = 1D20, DI = 20A he following sequence of instructions are executed: MOV SI,208h MOV AX,0040h MOV CX,000Ah CLD REPNZ SCASB atch point: //hat is the correct value of AX, SI, DI registers at watch point? I Chọn X Chọn I Chọn
D. TI W W D = A = S =	S = 1D20, ES = 1D20, DI = 20A the following sequence of instructions are executed: MOV SI,208h MOV AX,0040h MOV CX,000Ah CLD REPNZ SCASB atch point: //hat is the correct value of AX, SI, DI registers at watch point? I Chọn X Chọn I Chon
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W D = A = S =	MOV AX,0040h MOV CX,000Ah CLD REPNZ SCASB atch point: //hat is the correct value of AX, SI, DI registers at watch point? I Chọn X Chọn I Chon
W D = A = S =	MOV CX,000Ah CLD REPNZ SCASB atch point: //hat is the correct value of AX, SI, DI registers at watch point? X Chọn > I Chon >
W D = A = S =	MOV CX,000Ah CLD REPNZ SCASB atch point: //hat is the correct value of AX, SI, DI registers at watch point? X Chọn > I Chon >
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W D = A = S =	REPNZ SCASB atch point: /hat is the correct value of AX, SI, DI registers at watch point? I Chọn > X Chọn > I Chon >
W D = A = S =	atch point: /hat is the correct value of AX, SI, DI registers at watch point? I Chọn > X Chọn > I Chon >
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D = A = S =	/hat is the correct value of AX, SI, DI registers at watch point? I Chọn X Chọn I Chon I Chon
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câu hải 19	
câu bải 19 VA	
	/hat is the meaning of Amdahl's law in processor performance evaluation?
Hoàn thành	elect one:
Đạt điểm 1,00	the cost reduce when moving from single-core to multicore processor
	• the maximum speedup of a multicore processor
	the potential speedup of a program using multiple processor compared to a single processor
	the speedup of a multicore processor when increasing system bus speed
Câu hỏi 20 W	/hich are the correct actions for LODSW string operation if DF is reset (=0)
Hoàn thành	
Đạt điểm 0,50	elect one or more:
	□ decrease DI by 2
	☐ Load 16-bit value at memory location pointed by ES:[DI] into AX
	increase SI by 2
	Load 16-bit value at memory location pointed by DS:[SI] into AX
	hen many devices of different transmission speed connect to the same bus,
	ne overall system performance suffers. How did the design engineers resolved
Đạt điểm 1,00	iio.
S	elect one:
	PCI Express bus
	Multiple-Bus hierarchies
	PCI bus
	Split system bus into local bus and memory bus

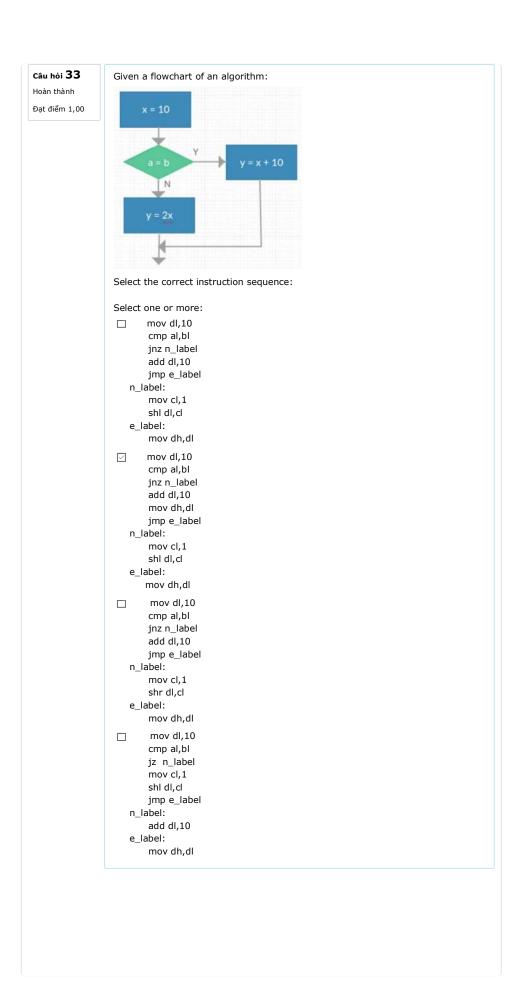
11-2-4-2-4	the instruction, CMP to compare source and destination operands by
Hoàn thành	
Đạt điểm 0,50	Select one:
	○ adding
	○ comparing
	○ dividing
	subtracting
Câu hỏi 23	To balance the super speed of CPU with the slow response of memory, which
Hoàn thành	of the following measures have been made by engineers in system design?
Đạt điểm 1,00	Select one or more:
	☐ Make use of both on-chip and off-chip cache memory
	 Using higher-speed bus and us hierarchy
	☑ To move data directly by DMA
	☑ 10 move data directly by DMA
Câu hỏi 24	The following sequence of instructions are executed. What is the correct
Hoàn thành	value of AX, DX at watch point?
Đạt điểm 1,00	MOV DL,FF
54t diein 1/00	MOV AL,42
	IMUL DL
	watch point:
	AX = FFBE \(\times \)
	AX = FFBE DX 0000 =
	DX 0000 V
Câu hỏi 25	DX 0000 V
Câu hỏi 25 Hoàn thành	DX 0000 \times In the RCR instruction, the contents of the destination operand undergoes function as
Hoàn thành	DX 0000 \ = \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Hoàn thành	DX 0000 \ = In the RCR instruction, the contents of the destination operand undergoes function as Select one: ○ carry flag is pushed into LSB then MSB is pushed into carry flag
	DX 0000 \ = 0000 \ In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành	DX 0000 \ = In the RCR instruction, the contents of the destination operand undergoes function as Select one: ○ carry flag is pushed into LSB then MSB is pushed into carry flag
Hoàn thành	DX 0000 \ = 0000 \ In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50	DX
Hoàn thành Đạt điểm 0,50 Câu hỏi 26	DX
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	DX
Hoàn thành Đạt điểm 0,50 Câu hỏi 26	DX
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	DX
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	DX 0000 \(\) = \(\) \(
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành Đạt điểm 0,50	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành Đạt điểm 0,50 Câu hỏi 27	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành Đạt điểm 0,50 Câu hỏi 27 Hoàn thành	In the RCR instruction, the contents of the destination operand undergoes function as Select one:
Hoàn thành Đạt điểm 0,50 Câu hỏi 26 Hoàn thành Đạt điểm 0,50 Câu hỏi 27 Hoàn thành	In the RCR instruction, the contents of the destination operand undergoes function as Select one:



Câu hỏi 28 Hoàn thành Đạt điểm 1,00	Select correct match for register values at watch points: MOV AX, 152D ADD AX, 003F watch point #1: ADD AH, 10 watch point #2: watch point #2: AH = 25 \cong AH = 25 \con	
Câu hỏi 29 Hoàn thành Đạt điểm 0,50	Which are the correct actions for SCASW string operation if DF is set (=1) Select one or more: ☑ decrease DI by 2 ☑ compare the value in AX register with 16-bit value at the memory location pointed by ES:[DI] and set/clear flag bits accordingly ☐ increase DI by 2 ☐ compare the value in AX register with 16-bit value at the memory location pointed by DS:[SI] and set/clear flag bits accordingly	
Câu hỏi 30 Hoàn thành Đạt điểm 1,00	What is the correct value of SI, AL (in hex) at watch point: 01:	
Câu hỏi 31 Hoàn thành Đạt điểm 1,00	Select the correct sequence of instructions to compute -1024/128 (all values are in hex). Step 1: CWD Step 2: MOV CX,80 Step 3: MOV CL,80 Step 4: IDIV CL	

pàn thành ạt điểm 1,00		otch for AL and carry flag at watch point #1: MOV BL, 8C MOV AL, 7E ADD AL, BL
	watch point #1:	
	AL 0A	
	Carry flag	<u> </u>





Câu hỏi 34 Hoàn thành	After executing the POP EAX instruction, the stack pointer		
Đạt điểm 0,50	Select one:		
	O decrements by 4		
	O decrements by 2		
	increments by 4		
	increment by 1		
Câu hỏi 35	Sign-extend number BF (8-bit binary) to 16-bit. Write result in hex		
Hoàn thành			
Đạt điểm 0,50	Answer: 191		
Câu hỏi 36	Which of the following in throughout and and welled?		
Hoàn thành	Which of the following instructions are not valid?		
Đạt điểm 0,50	Select one or more:		
Dặt diem 0,30	☑ MOV DS, B800h		
	☐ MOV AX, [BP+2]		
	✓ MOV SP, SS:[SI+2]		
	□ MOV AX, SI		
Câu hỏi 37	The following sequence of instructions are executed. What is the correct		
Hoàn thành	value of flag bits at watch point?		
Đạt điểm 1,00	MOV AL, 0F		
Dặt diem 1,00	ADD AL, F1		
	watch point:		
	natar panta		
	Zero flag (OF) reset		
	=		
	Carry flag set		
	(CF) =		
Câu hỏi 38	Major structural components of the CPU include:		
Hoàn thành	Select one or more:		
Đạt điểm 1,00	☑ Registers		
	✓ Arithmetic and Logic Unit		
	□ Instruction Pointer (PC)		
	☐ Instruction Pointer (PC)		
	☑ Interconnections		
	☑ Interconnections☑ Control Unit		
	☑ Interconnections		
	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register 		
Câu hỏi 39	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64		
Hoàn thành	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register 		
	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity 		
Hoàn thành	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64		
Hoàn thành	 ☑ Interconnections ☑ Control Unit ☐ Instruction Register Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 kB. What is the disk capacity 		
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Câu hỏi 40 Hoàn thành	What best describe the Spatial and Temporal Locality?
Đạt điểm 1,00	Tempor al be exploited by keeping recently used instruction and data in cache memory and by exploiting a cache hierarch locality
	Spatial locality be exploited by moving data between cache and memory more efficient
Câu hỏi 41	Given a code snippet:
Hoàn thành	int ax, bx;
Đạt điểm 1,00	
	if $(ax \ge bx)$
	ax -=bx;
	else
	bx -=ax;
	What is the equivalent logic sequence of instructions in Assembly
	Select one:
	jl a_label
	sub ax,bx jmp x_label
	a_label:
	sub bx,ax
	x_label:
	o cmp ax,bx
	jbe a_label sub ax,bx
	jmp x_label
	a_label:
	sub bx,ax x_label:
	cmp ax,bx
	ja a_label
	sub ax,bx
	jmp x_label
	a_label: sub bx,ax
	x_label:
	○ cmp ax,bx
	jge a_label
	sub ax,bx jmp x_label
	a_label:
	sub bx,ax
	x_label:
Câu hỏi 42	Which of the following is not a data copy/transfer instruction?
Hoàn thành	miles of the following is not a data copy/transfer instruction:
Đạt điểm 0,50	Select one or more:
_ +c a.c 0,50	☑ ADC
	□ MOV
	□ LEA
	☑ DAS
	Return to: General • ⊇

- 60 câu cấu trúc máy tính và hợp ngữ
- 1.Loại chương trình chứa mã, dữ liệu và stack trong các segment riêng là?
- a.EXE b.Doc c.Com d.ASM
- 2.Khi nạp một chương trình exe vào bộ nhớ để thực thi, trình nạp lưu địa chỉ của PSP trong các thanh ghi DS ES, địa chỉ của stack trong thanh ghi _SS__và kích thước của stack trong thanh ghi _SP_
- 3.Lệnh_POP CX__khôi phục word từ nơi mã SP trỏ tới trong stack vào thanh ghi CX và tầng SP
- 4.Chỉ dẫn _END_kết thúc định nghĩa chương trình
- 5.Phát biểu DB 12 DUP(50) định nghĩa 12 byte được khởi động với giá trị___50
- (Toán tử DUP dùng để lặp lại các dữ liệu với số lần quy định. Cú pháp: Count DUP(Các dữ liệu) -> lặp lại các dữ liệu với số lần Count.)
- 6.Giả sử Intel 8086 ở real mode,offset là 24h,thanh ghi segment chứa 0B500h,tính địa chỉ vật lý
- a.0B524h b.0B5024h c.24B5h d.240B5h
- 7.Một chương trình COM hạn chế trong một_SEGMENT__và kích thước tối đa là_64K__
- 8.Lệnh để khởi động một thanh ghi với một địa chỉ offset là lệnh a.PUSH b.MOVZX c.LEA d.MOVSX e. C&D
- 9.Một địa chỉ_OFFSET__ bị giới hạn tới khoảng cách từ -32768 tới 32767 bye trong phạm vi cùng segment
- 10.Cờ_CF_ chứa một bít nhớ(0 hoặc 1) từ bit trật tự cao trong các thao tác toán học và một số lệnh dịch và quay.
- 11.Cờ _SF__ được set theo dấu sau 1 thao tác số học : dương set là 0 âm set là 1.
- 12.Kí tự Hex cho phím Tab là 09 cho Line feed là _A__và carriage return là_D_

Các ký tự điều khiển thường dùng là:



ASCII code (Hex) SYMBOL FUNCTION 7 BEL beep 8 BS backspace 9 HT tab A LF line feed D CR carriage return 13. Chức năng 02H của ngắt 10h xác định vị trí con trỏ 14. Mạch hỗ trợ nào không được tìm thấy trong hệ thống 8086 ở chế độ min a.Cache controller b.Clock generator c.Bus controller d.Trang lanch(k0 rõ nữa) 15.Cò D xác định hướng xử lý chuỗi: trái sang phải sử dụng lệnh CLD để xoá cờ D, phải sang trái sử dụng lệnh STD để set cờ D. 16.Giá trị số dương lớn nhất đối với số có dấu trong thanh ghi 8 bit là 127 17.Để nhân byte với byte, số bị nhân chứa trong thanh ghi AL, và số nhân là 1 byte trong bộ nhớ hoặc thanh ghi, sau khi nhân, tích số được chứa trong thanh ghi AX 18.Đối với phép chia, lệnh DIV xử lý dữ liệu không dấu, còn lệnh IDIV xử lý dữ liệu có dấu 19.Lênh AAA kiểm tra xem số Hex tân cùng bên phải của AL lớn hơn 9 hoặc cờ A có =1__ số Hex tận cùng bên trái trong _AL__ 20. Trong hệ thống vi xử lý Bus là: Một nhóm các dây nối các tp trong hệ thống máy tính. Bus đc dùng để truyền địa chỉ, dữ liệu, thông tin điều khiển giữa vi xử lý và bộ nhớ các thiết bị IO. Truyền Dữ Liệu, Thông Tin

21. Trong hệ thống vi xử lý, trước khi thực hiện chương trình được chứa

trong

a.Trong cổng vào ra b.Các bộ đệm trong vi xử lý c.Trên Bus dữ liệu d.Trong bộ nhớ bán dẫn

22.Khi có hàng đợi lệnh chương trình sẽ thực hiện nhanh dơn do: a.Không mất chu kỳ lấy lệnh từ bộ nhớ

b.Quá trình lấy lệnh thực hiện đồng thời với quá trình thực hiện lệnh

c.Quá trình thực hiện lệnh diễn ra nhanh hơn

d.Quá trình lấy lệnh diễn ra nhanh hơn

23.Để truy cập bộ nhớ CPU cung cấp địa chỉ gì cho bộ nhớ

a.Logic b.Vật lý c.Độ dời(offset) d.Đoạn(segment)

24. Thanh ghi DX là một thanh gi

a.Đa năng b.Đoạn c.Địa chỉ d.Dữ liệu

25. Nhóm các thanh ghi sau đây đều có thể sử dụng để giữ địa chỉ độ dời khi truy cập bộ nhớ dữ liệu?

a.IP,SP,AH,AL b.CS,DS,ES,SS c.BX,BP,DI,SI d.AX,BX,CX,DX

26. Thanh ghi nào được mặc định giữ số điểm trong các lệnh lặp? a.BX b.CX c.AX d.DX

27. Các thanh ghi nào giữ kết quả trong các lệnh nhân chia 16bit?

a.AX và BX b.AX và DI c.AX và DX d.AX và CX

28.Cờ Zero(ZF) của CPU 80286 được lặp lên 1 khi:

a.Kết quả các phép tính bằng 0

b.Kết quả các phép tính khác 0

c.Kết quả các phép tính lớn hơn 0

d. Kết quả các phép tính nhỏ hơn 0

29. Các khai báo dữ liệu sau, khai báo nào không bị lỗi

a. Xon DB 1,2,3,fh

b.Yes DB 4,7,h,9

c.Rel DB 19,7,6,10,3

d.Anh DB 9,3,8,7,0 // 1 byte

Tên biến mảng DB/DW/DD Các giá trị khởi đầu *Ví du:*

M1 DB 4,5,6,7,8,9

30. Trong chế độ địa chỉ chỉ số nền, dữ liệu sử dụng trong lệnh nằm



trong một ô nhớ có địa chỉ bằng

- a. Giá trị chứa trong thanh ghi BX hoặc BP
- b. Giá trị chứa trong thanh ghi DI hoặc SI
- c. Giá trị chứa trong thanh ghi BX hoặc BP cộng với trị chứa trong DI hoặc SI cộng với độ dời
- d. Giá trị chứa trong thanh ghi DI hoặc SI cộng với một số độ dời

31. Sau khi thực hiên các lênh

MOV AH,05

MOV AL,03

XCHG AH,AL

a.AH=03,AL=05 b.AH=AL=03 c.AH=AL=05 d.AH=05,AL=03

32.(k0 rõ)

thì sau khi thực hiện các lệnh

MOV AL,3

LEA BX,LP

XFLAT

sẽ được

a.BX=1000H, AL=27H b.0000H,AL=27 c.BX=0027h,AL=0

d.BX=1000H,AL=1Bh

33.Giả sữ AL=9, AH=7, sau khi thực hiện các lệnh sau AX sẽ có giá trị bằng

ADD AL, AH

DAA

ADD AX,3030H

ADD AL, AH

AAA

a.0007h b.0037h c.3803h d.3037h

34.Giả sử AX=9,BX=12 sau khi thực thi lệnh CMP AX,BX sẽ có:

a.CF=0,ZF=0 b.CF=0,ZF=1 c.CF=1,ZF=0 d.CF=1,ZF=1

35.Giả sử AH=02,AL=03 sau khi chạy lệnh MUL AH sẽ được:

a.AH=02 b.AH=06 c.AH=0 d.AH=03

36.Giả sử AL chứa mã ASCII của một số từ 0 đến 9 sau lệnh AND

AL,0FH thì

- a.AL=0 b.AL là mã BCD của số đó
- c.AL vẫn là mã ASCII của số đó d.AL=0FH
- 37.Để đảo trạng thái các bit trong một thanh ghi có thể
- a.XOR nó với 00H b.OR nó với FFH c.AND nó với FFH d.XOR nó với FFH
- 38.Giả sử AL=35H,CL=4 sau lệnh SHR AL,CL sẽ được
- a.AL=5,CL=0 b.AL=3,CL=4 c.AL=3,CL=0 d.AL=5,CL=4
- 39.Lệnh JPE M chuyển điều khiển chương trình tới nhãn M khi
- a.PF=1 b.ZF=0 c.ZF=1 d.PF=0
- 40. Sau lệnh LOOP các giá trị nào có thể bị thay đổi
- a.BX và CF b.BX và ZF c.CX và CF d.CX và ZF
- 41. Hàm 02 ngắt 21h của Dos là hàm
- a.Trả điều khiển về hê điều hành
- b.Hiện một ký tự lên màn hình
- c.Hiện một chuỗi kí tự lên màn hình
- d.Nhập một ký tự từ bàn phím
- 42.Bù 2 của sô 00101111 là
- a.10110111 b.01010100 c.11001000 d.11010001
- 43. Hàng đợi lệnh cho phép bộ xử lý làm gì
- a.Cho qua các lệnh không mong muốn
- b.Xử lý nhiều lệnh tại một thời điểm
- c.Chờ cho lệnh kế được thực thi
- d.Tìm trước và nạp các lệnh
- 44. Stack segment chứa
- a.Bộ nhớ chỉ đọc
- b.Dữ liệu được định nghĩa của một chương trình bằng số, và vùng làm việc
- c.Các giá trị mà một chương trình cần lưu tạm thời
- d.Các lệnh máy để thực thi
- 45.Ký hiệu nào chỉ ra rằng các kí tự theo sau nó là các chú thích a.Khoảng trắng b.Dấu phẩy c.Dấu sao d.Dấu chấm phẩy



- 46.Để chạy từng lệnh trong đoạn chương trình dùng debug, ta dùng lệnh
- a.R Xem or sửa nd thanh ghi
- b.A Dịch một ct ra mã máy
- c.P Chạy từng bước
- d.Q Thoát khỏi ct debug và trở về hệ điều hành
- 47. Trong một chương trình exe ta phải
- a.Khởi động giá trị cho thanh ghi AX
- b.Khởi động giá trị cho thanh ghi DS
- c.Không cần khởi động giá trị cho DS
- d.Cả ba câu trên đều sai
- 48.Lệnh MOVSB mỗi lần di chuyển một byte dữ liệu từ nguồn vào đích, đồng thời tăng hoặc giảm các thanh ghi DI,SI một đơn vị
- 49.Để đưa nội dung từ công 1234h vào thanh ghi AL,ta dùng lệnh
- a.IN 1234h b.IN AL,1234h c.MOV DX,1234h và IN AL,DX d.MOV AL,DX
- 50.Để điều chỉnh phép trừ 2 số BCD dạng nén, ta dùng lệnh
- a.DAS b.AAS c.AAA d.DAA
- 51. Mục đích của tín hiệu BHE là gì?
- a.Cho phép truy cập byte cao của một từ
- b.Cho phép truy cập byte thấp hoặc word
- c.Cho phép truy cập toàn bộ một word
- d.Cho phép treo bus
- 52. Tại sao 8086 có bus địa chỉ và dữ liệu được ghép kênh
- a.Để tăng hiệu suất
- b.Cho phép bộ nhớ chậm hơn
- c.Để đơn giản hoá mạch bên ngoài
- d.Để tiết kiệm số chân của vi xử lý
- 53.8086 có bus dữ liệu và địa chỉ được ghép kênh, làm thế nào để phân kênh.
- a.Mạch chốt b.Bus transceiver c.Bus controller d.Mạch phát xung clock 54.Một chu kỳ bus của 8086 mất ít nhất 4 chu kỳ xung clock, nếu vi xử lý có tần số xung clock là 4MHz, tốc độ tối đa của bus dữ liệu là :

a.4Mb/s b.4MB/s c.2MB/s d.20MB/s

55. Cái gì sau đây không phải là đặc điểm của 8086

a. Hoàn toàn tương thích ngược với 8086

b.Bộ nhớ vật lý 16MB

c.Hỗ trợ real mode và protected mode

d.Các thanh ghi đa dụng 32 bit //16 bit

56. Protected mode trong 80286 thực hiện để hỗ trợ

a.Các hê điều hành đa nhiêm

b.Over...processes

c.Bô nhớ cache

d.....Security

57. Mục đích chính của bộ xử lý 8038

a.Điều khiển bộ nhớ cache

b.truy cập đĩa...nhanh

c.Thực hiện nhanh các thao tác....

d.Tưng bộ nhớ vật lý

58.Để dịch ngược nội dung bộ nhớ ra mã hợp ngữ ta dùng lệnh:

a.A b.R c.U d.F

59. Dùng lệnh....để nạp nội dung của tập tin COM vào bộ nhớ ở địa chỉ offset...

a.N 300 b.l 100 c.W 100 d.P 100

60.Để thi hành lệnh trong debug ta dung lệnh

a.P b.T c.R d.Cå a và b