1.
1ms ------> 64 refresh
250ns -------> ?refresh
số refresh của 1 memory cycle = 0.016 (times/s)
-> 16 times/ms
percentage of the memory's total operating time =(0.016*150/250)*100
= 0.96%

Bài Tập Internal Memory

1. Consider a dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to refreshes?
2. Figure 5.16 shows a simplified timing diagram for a DRAM read operation over a bus. The access time is considered to last from **t**1 to **t**2. Then there is a recharge time, lasting from **t**2 to **t**3, during which the DRAM chips will have to recharge before the processor can access them again.
   a. Assume that the access time is 60 ns and the recharge time is 40 ns. What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 1-bit output?

Memory cycle time = Taccess + Trecharge
= 60+40=100ns

Data rate = 1/cycle time * number of bits per access
= 1/100ns * 1 = 10Mb/s

   b. Constructing a 32-bit wide memory system using these chips yields what data transfer rate?

if memory cycles tranfers 32 bits of data => data transfer rate = 32*10 = 320 Mbs

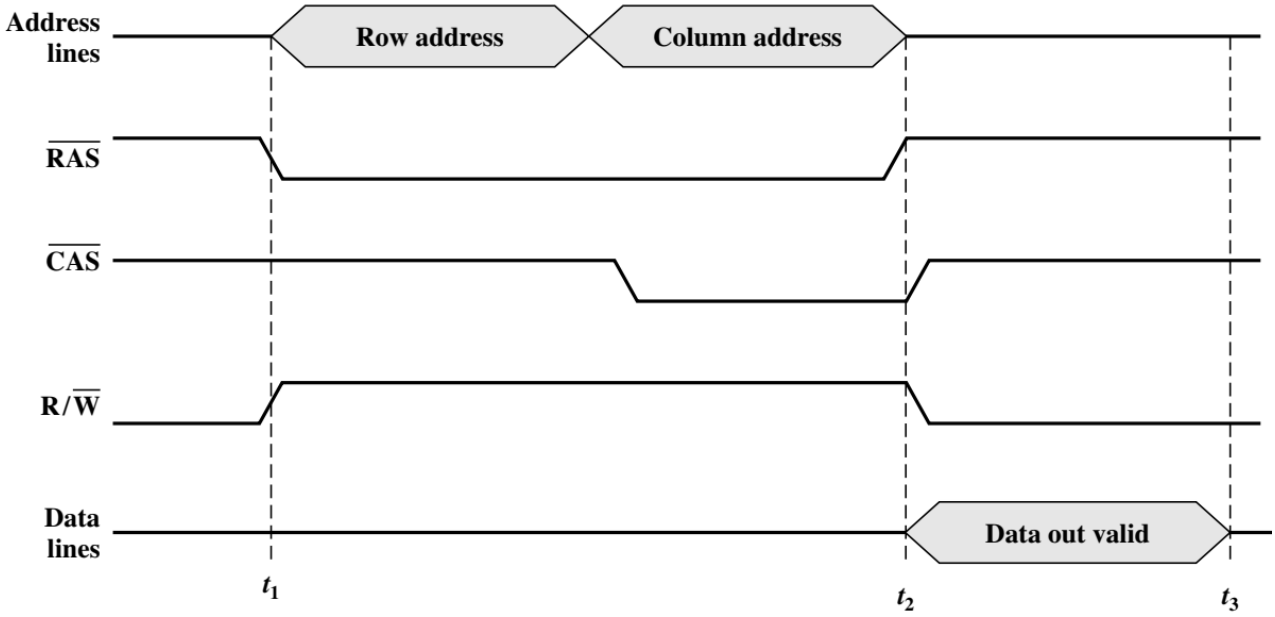


Figure 5.16 Simplified DRAM Read Timing

3. Figure 5.6 indicates how to construct a module of chips that can store 1 MByte based on a group of four 256-Kbyte chips. Let's say this module of chips is packaged as a single 1-Mbyte chip, where the word size is 1 byte. Give a high-level chip diagram of how to construct an 8-Mbyte computer memory using eight 1-Mbyte chips. Be sure to show the address lines in your diagram and what the address lines are used for.

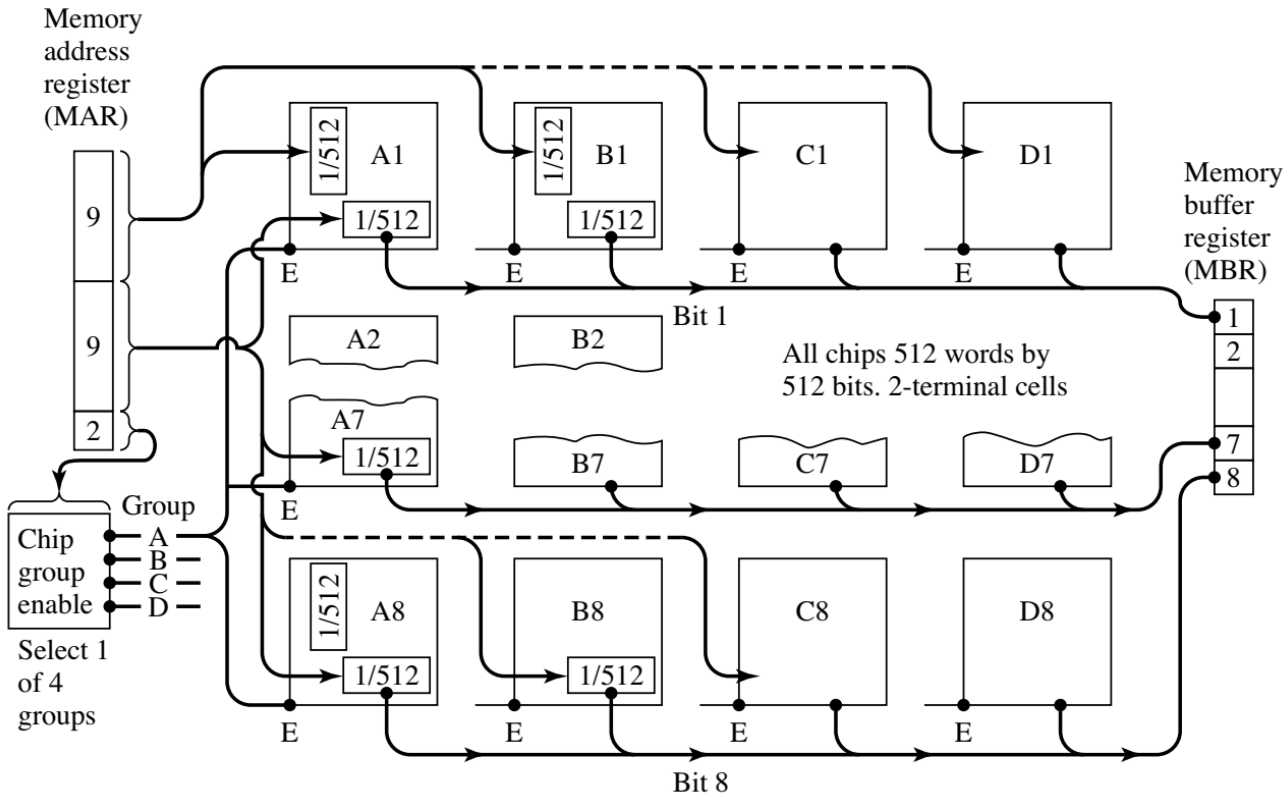


Figure 5.6 1-Mbyte Memory Organization

4. **For each configuration (a-c), state how many bits are needed for each of the following:**
   - **Virtual address**
   - **Physical address**
   - **Virtual page number**
   - **Physical page number**
   - **Offset**

   a. **32-bit operating system, 4-KB pages, 1 GB of RAM**
   b. **32-bit operating system, 16-KB pages, 2 GB of RAM**
   c. **64-bit operating system, 16-KB pages, 16 GB of RAM**
5. **On a typical Intel 8086-based system, connected via system bus to DRAM memory, for a read operation, RAS is activated by the trailing edge of the Address Enable signal (Figure 3.19). However, due to propagation and other delays, does not go active until 50 ns after Address Enable returns to a low. Assume the latter occurs in the middle of the second half of state T1 (somewhat earlier than in Figure 3.19). Data are read by the processor at the end of T3. For timely presentation to the processor, however, data must be provided 60 ns earlier by memory. This interval accounts for** propagation delays along the data paths (from memory to processor) and processor data hold time requirements. Assume a clocking rate of 10 MHz.
   a. How fast (access time) should the DRAMs be if no wait states are to be inserted?
   b. How many wait states do we have to insert per memory read operation if the access time of the DRAMs is 150 ns?

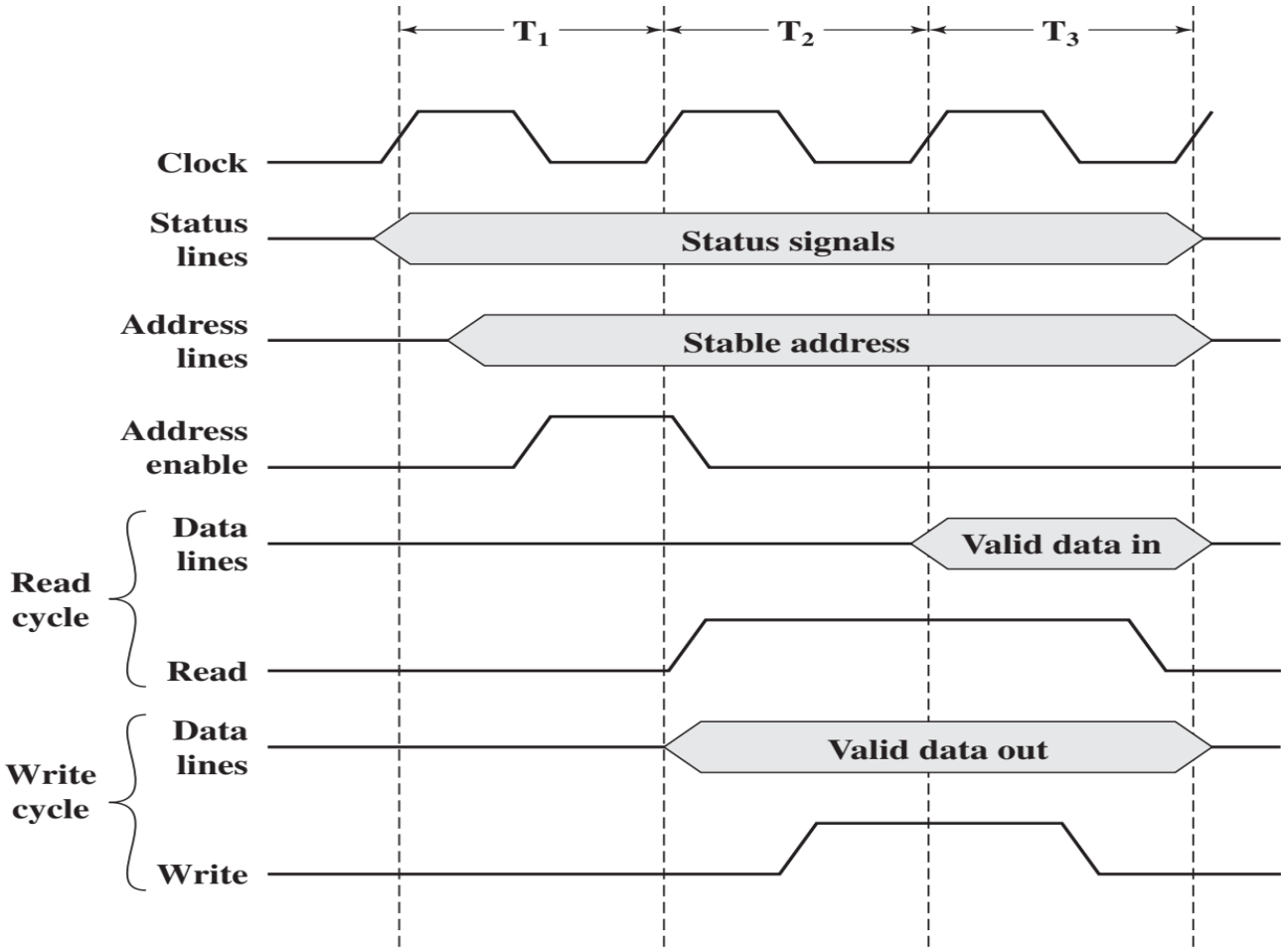


Figure 3.19 Timing of Synchronous Bus Operations

6. The memory of a particular microcomputer is built from 64Kx 1 DRAMs. According to the data sheet, the cell array of the DRAM is organized into 256 rows. Each row must be refreshed at least once every 4 ms. Suppose we refresh the memory on a strictly periodic basis.

a. What is the time period between successive refresh requests?

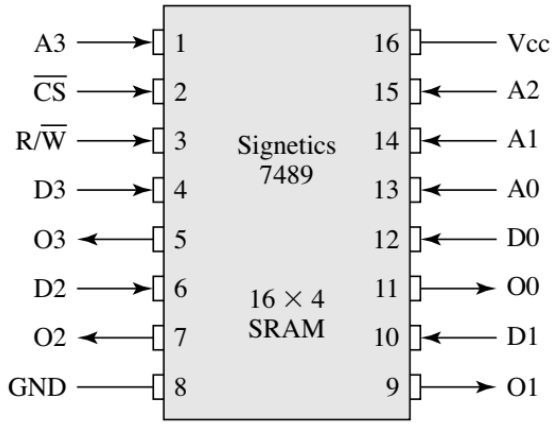
b. How long a refresh address counter do we need?

7. Figure 5.17 shows one of the early SRAMs, the 16 4 Signetics 7489 chip, which stores 16 4-bit words.

a. List the mode of operation of the chip for each CS/ input pulse shown in Figure 5.17c.

b. List the memory contents of word locations 0 through 6 after pulse n.

c. What is the state of the output data leads for the input pulses h through m?

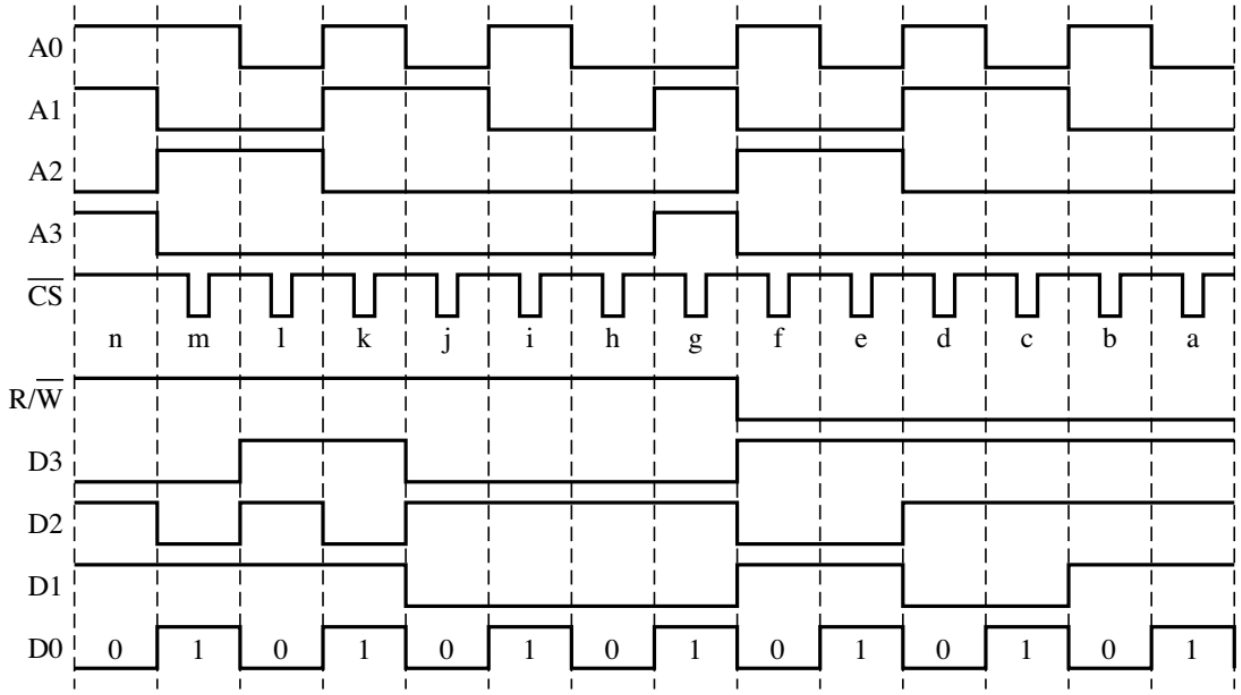


(a) Pin layout

Operating Mode	Inputs			Outputs
	$\overline{CS}$	R/$\overline{W}$	D*n*	O*n*
Write	L	L	L	L
	L	L	H	H
Read	L	H	X	Data
Inhibit writing	H	L	L	H
	H	L	H	L
Store - disable outputs	H	H	X	H

H = high voltage level
L = low voltage level
X = don't care

(b) Truth table



(c) Pulse train

Figure 5.17 The Signetics 7489 SRAM

8. Design a 16-bit memory of total capacity 8192 bits using SRAM chips of size 64 1 bit. Give the array configuration of the chips on the memory board showing all required input and output signals for assigning this memory to the lowest address space. The design should allow for both byte and 16-bit word accesses.