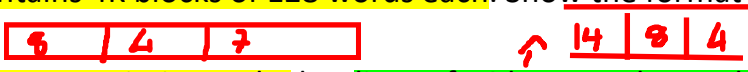
câu 1: 1 set có 4 lines, tổng cộng có 64 lines
-> số sets = 64/4 = 16 -> s = 4 bits
128 words each block = 2^7 -> b = 7 bits
(cần 7 bits để xác định được ô nhớ trong khối)
memory contains 4K blocks = 2^2*2^10 = 2^12
which means tag bit + set bit = 12 => t = 8 bits

câu 2: mỗi line 16 bytes và tổng bộ nhớ cache là 8kB
-> số line = 2^3*2^10/2^4 =2^9
-> số set = số line / 2 = 2^8 -> s = 8 bits

size of line in cache memory = size of a block in main memory
= 16 bytes -> b = 4 bits
-> số block = 64mb/16 = 2^22 which means
t + s = 22 -> t = 14

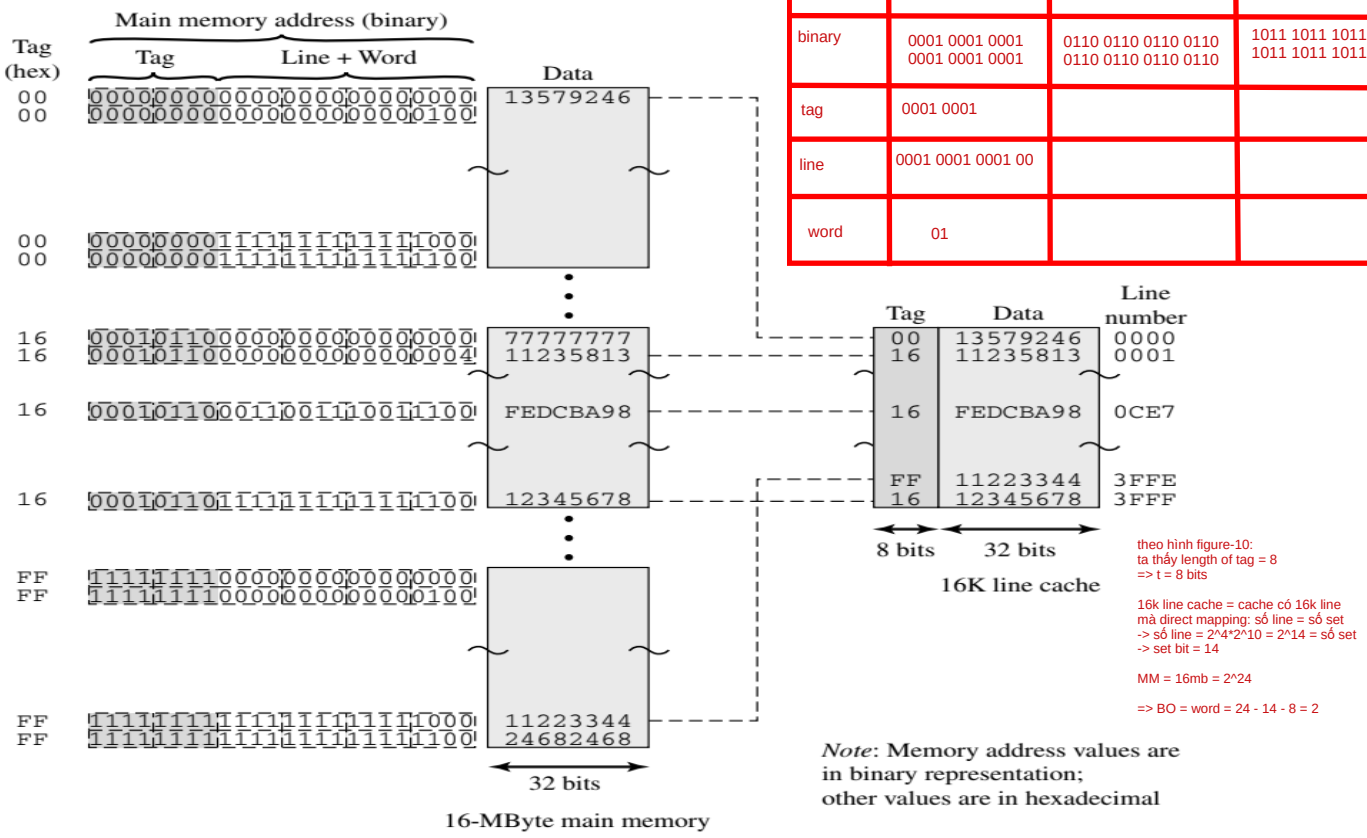
Bài Tập Bộ Nhớ Cache

1. A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.



2. A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.
3. For the hexadecimal main memory addresses 111111, 666666, BBBBBB, show the following information, in hexadecimal format:
   a. Tag, Line, and Word values for a direct-mapped cache, using the format of Figure 4.10
   b. Tag and Word values for an associative cache, using the format of Figure 4.12
   c. Tag, Set, and Word values for a two-way set-associative cache, using the format of Figure 4.15

CPU request	111111	666666	BBBBBB
binary	0001 0001 0001 0001 0001 0001	0110 0110 0110 0110 0110 0110 0110 0110	1011 1011 1011 1011 1011 1011 1011 1011
tag	0001 0001		
line	0001 0001 0001 00		
word	01		



theo hình figure-10:
ta thấy length of tag = 8
=> t = 8 bits

16k line cache = cache có 16k line
mà direct mapping: số line = số set
-> số line = 2^4*2^10 = 2^14 = số set
-> set bit = 14

MM = 16mb = 2^24

=> BO = word = 24 - 14 - 8 = 2

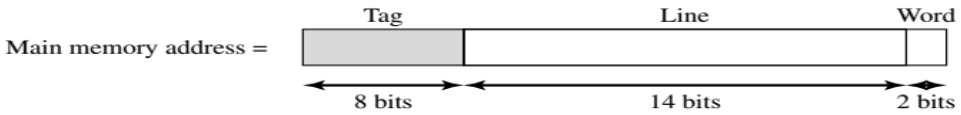
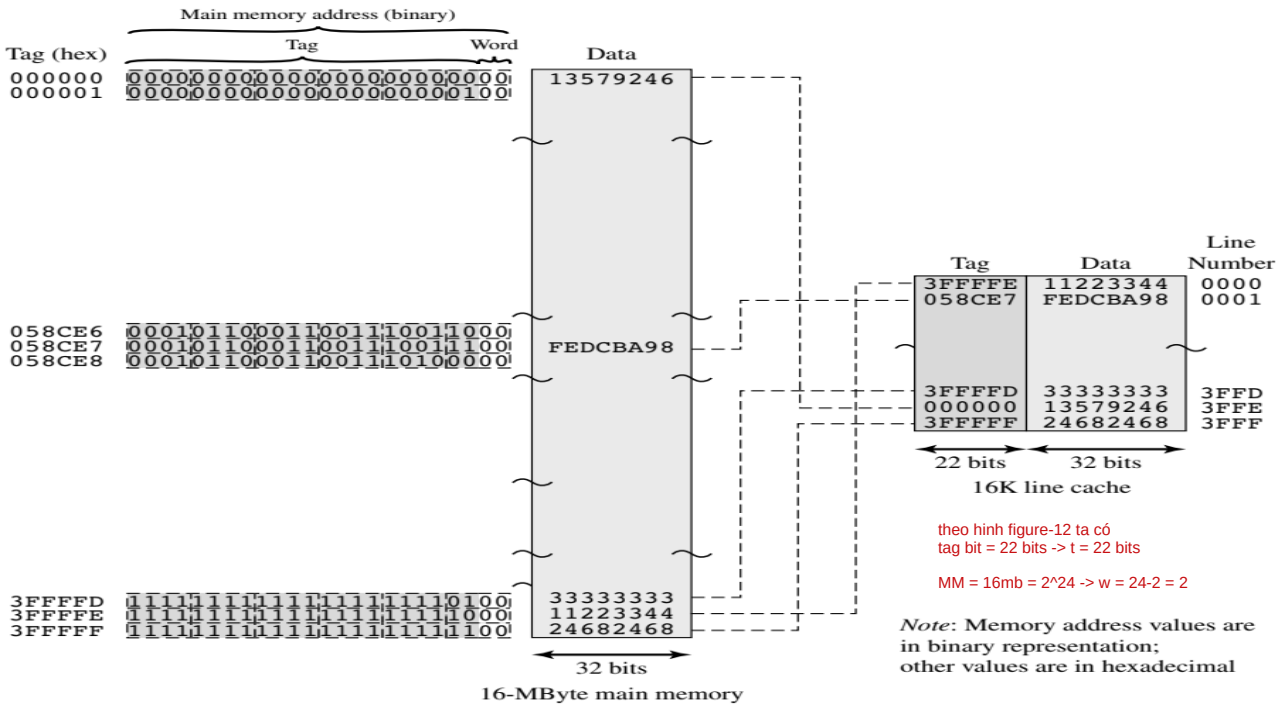


Figure-10



theo hình figure-12 ta có
tag bit = 22 bits -> t = 22 bits

MM = 16mb = 2^24 -> w = 24-2 = 2

theo figure 4.15 ta có:
tag bit = 9 bits -> t = 9

number of line = 2^14 = number of block
2-way -> số set = số line/2 = 2^13
-> s = 13

MM size = 2^24

-> w = 2

Figure- 12

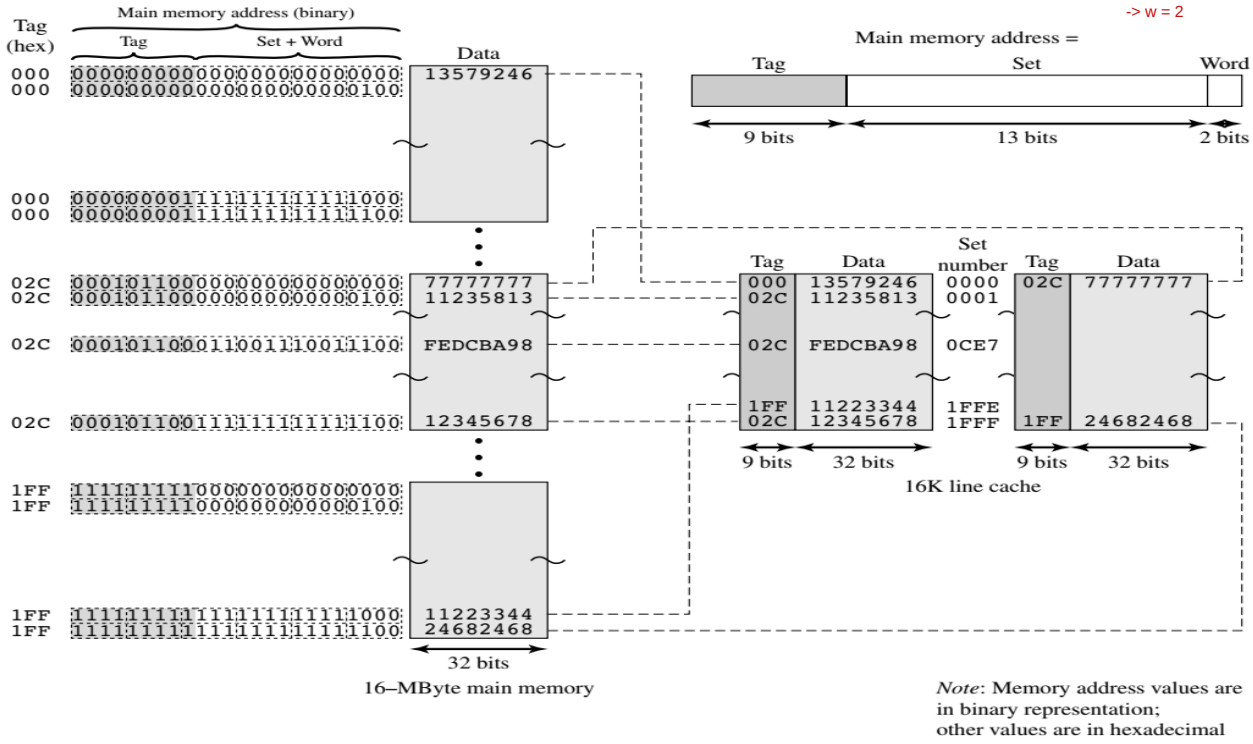


Figure 4.15 Two-Way Set Associative Mapping Example

4. List the following values:

a. For the direct cache example of Figure 4.10: address length, number of addressable units, block size, number of blocks in main memory, number of lines in cache, size of tag

4a. 4.10
tag 8 set 14 block 2
address length = 8+4+12=24
number of addressable unit = s^24 bytes or words
block size = 2^2
number of blck = mm/block size = 2^22
num of line in cache = 2^14
size of taf = 8 bits

b.

b. For the associative cache example of Figure 4.12: address length, number of addressable units, block size, number of blocks in main memory, number of lines in cache, size of tag tương tự câu a

c. For the two-way set-associative cache example of Figure 4.15: address length, number of addressable units, block size, number of blocks in main memory, number of lines in set, number of sets, number of lines in cache, size of tag question says that " there are four 32 bits words which means one word is of 32 bit therefore for four words we will have 128 bits, so to represent this we need 7 bits na.!!

5. Consider a 32-bit microprocessor that has an on-chip 16-KByte four-way set-associative cache.Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped? 2^14 line size of four 32-bit words line size = 4*32bit = 16 bytes => số line = 2^14/2^4 = 2^10 số set = số line/4 = 2^8 -> s = 8 bits 10101011110011011110/ 10001111/ 1000 block size = 4 bits set size = 8 bits tag size = 20 bits

6. Given the following specifications for an external cache memory: four-way set associative; line size of two 16-bit words; able to accommodate a total of 4K 32-bit words from main memory; used with a 16-bit processor that issues 24-bit addresses. Design the cache structure with all pertinent information and show how it interprets the processor's addresses.

7. The Intel 80486 has an on-chip, unified cache. It contains 8 KBytes and has a four-way set-associative organization and a block length of four 32-bit words. The cache is organized into 128 sets. There is a single "line valid bit" and three bits, B0, B1, and B2 (the "LRU" bits), per line. On a cache miss, the 80486 reads a 16-byte line from main memory in a bus memory read burst. Draw a simplified diagram of the cache and show how the different fields of the address are interpreted. vlock length od four 32-bit words -> 1 word = 32 bits = 4 bytes = 2^2 -> size of blok = 32 * 4 = 128 = line size = 2^4 -> number of line = cache/line size =2^13 / 2^4 = 2^9 -> s = 7, b = 4, t = 2

8. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. block size = line size = 8 bytes = 2^3 set bit = line bit = 5 => a. tag bit = 16-3-5=8 bit

a. How is a 16-bit memory address divided into tag, line number, and byte number?

b. Into what line would bytes with each of the following addresses be stored?
0001 0001 0001 1011 tag = 0001 0001, set = 0001 1, block offset = 011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

d. How many total bytes of memory can be stored in the cache?

e. Why is the tag also stored in the cache?

9. A set-associative cache has a block size of four 16-bit words and a set size of 2. The cache can accommodate a total of 4096 words. The main memory size that is cacheable is 64K 32 bits. Design the cache structure and show how the processor's addresses are interpreted.

10. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units,

number of blocks in main memory, number of lines in cache,
size of tag.

b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

c. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

11. Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes.

a. For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache.

b. Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache.

c. For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully-associative cache.

d. For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way set-associative cache.

12.