Quiz 2 - Chúc các bạn thành công

Kiến trúc máy tính _ hợp ngữ (Trường Đại học Sư phạm Kỹ thuật Thành phố Hồ Chí Minh)

Câu hỏi 1

Hoàn thành

Đạt điểm 1,00

Đặt cờ

the memory stack area of a program shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

The value of esp register is 0x00001d48. What is the value of esi after the execution of **pop esi**

Answer: 1D4C

Câu hỏi 2

Hoàn thành

Đạt điểm 1,00

Đặt cờ

Match the definition of flag bits in PSW

determine the direction for moving or comparing data between memory areas — OF

contains the carry of 0 or 1 from the leftmost bit after an arithmetic operation — CF

determine whether an external interrupts are to be ignored or processed — IF

the processor switches to single-step mode — TF

Câu hỏi 3

Hoàn thành

Đạt điểm 1,00

Đặt cờ

Given 8-bit floating-point binary format:

1 (sign) + 3 (exponent) + 4 (mantissa)

Convert the 8-bit floating point number A6 (in hex) to decimal.

Answer: -0,6875

Câu hỏi 4

Hoàn thành

Đạt điểm 2,00

Xóa cờ

Consider a 4-way set associative mapped cache of size 64 KB with block size 256 bytes. The size of main memory is 1MB.

Find:

1. Number of bits in tag 6
2. Tag directory size 192 bytes

Câu hỏi 5

Hoàn thành

Đạt điểm 0,50

Đặt cờ

The instruction, MOV AX, 0x1234 is an example of _____ when the operand 0x1234 is mentioned?

Select one:

- direct addressing mode
- Immediate addressing mode
- register addressing mode
- based index addressing mode

Câu hỏi 6

Hoàn thành

Đạt điểm 2,00

Xóa cờ

Consider a fully associative mapped cache of size 32 KB with block size 256 bytes. The size of main memory is 512 KB. Find

1. Number of bits in tag 11

2. Tag directory size 176 Bytes

Câu hỏi 7

Hoàn thành

Đạt điểm 0,50

Đặt cờ

The instruction, mov ax, word[ebx] is an example of _____ when the operand [ebx] is mentioned?

Select one:

- register indirect addressing mode
- direct addressing mode
- Immediate addressing mode
- register addressing mode

Câu hỏi 8

Hoàn thành

Đạt điểm 2,00

Đặt cờ

Consider a 4-way set associative mapped cache of size 64 KB with block size 512 bytes. The size of main memory is 4MB.

Find:

1. Number of bits in tag 8

2. Tag directory size 128 bytes

Câu hỏi 9

Hoàn thành

Đạt điểm 1,00

Xóa cờ

What are the features of direct-mapping cache organization?

Select one or more:

- [x] faster
- [ ] Thrash --> low hit ratio
- [x] Simple and inexpensive
- [ ] small cache memory

Câu hỏi 10

Hoàn thành

Đạt điểm 1,00

Đặt cờ

Convert the 32-bit floating point number 44363800 (in hex) to decimal.

Answer: 728,875

Câu hỏi 11

Hoàn thành

Đạt điểm 2,00

Xóa cờ

A computer system has main memory size = 4MB with 16 bytes block size. The direct-mapped cache memory operates alongside having 2^{12} cache lines.

Consider 2 consecutive bytes in the main memory starting at 0x3f15ab.

The tag bits would be (binary) 165 , and cache index for the 1st byte would be (hex) 0x 1651 (hex digit in lowercase)

Câu hỏi 12
Hoàn thành
Đạt điểm 0,50
Đặt cờ

Sign-extend number 0E (8-bit binary) to 16-bit. Write result in hex

Answer: 0000000000001110

Câu hỏi 13
Hoàn thành
Đạt điểm 1,00
Đặt cờ

Given 8-bit floating-point binary format:
1 (sign) + 3 (exponent) + 4 (mantissa)
Convert the 8-bit floating point number 68 (in hex) to decimal.

Answer: 12

Câu hỏi 14
Hoàn thành
Đạt điểm 1,00
Xóa cờ

Bus is a shared transmission medium, multiple devices connect to it but only one at a time can successfully transmit. Which component in computer facilitates this operation?

Select one:
- Direct Memory Access (DMA)
- Bus Arbiter
- Bus master
- Programmed I/O

Câu hỏi 15
Hoàn thành
Đạt điểm 0,50
Đặt cờ

8088 is 16 bit processor, the maximum addressable memory is:

Select one:
- 640M
- 64M
- 640K
- 1024K

Câu hỏi 16
Hoàn thành
Đạt điểm 1,00
Xóa cờ

Part of computer memory is shown in figure

Address	1D48	1D49	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F
Value	03	7F	F5	2D	5A	12	7B	C0

What is the value of AX register after instruction mov ax, **word[0x1d4b]** executed

Answer: 2D

Câu hỏi 17
Hoàn thành
Đạt điểm 1,00
Đặt cờ

Choose correct features for SRAM and DRAM

SRAM: Faster access time, cost more per bit, smaller size
DRAM: Slower access time, cheaper cost per bit, can manufacture with larger size

Câu hỏi 18

Hoàn thành

Đạt điểm 5,00

Đặt cờ

A 1MB cache memory that organized in 128-bytes blocks, operates along with the main memory of 8GB.

1. The number of address bits used to index the main memory: 33
2. The number of bits used to index a particular memory block: 7
3. The number of bits used to index the cache: 35
4. The number of bits used to index every cache line: 13
5. The number of bits used to index every single byte on a cache line: 56

Câu hỏi 19

Hoàn thành

Đạt điểm 2,00

Đặt cờ

A computer with 128-byte main memory, the cache is direct-mapped 32 bytes, line size is 8 bytes.
A series of memory accesses requested by the CPU are 0x08 0x11 0x0F 0x24 0x1E 0x27.
What is the correct hit/miss ratio?

- 2/6
- 1/6
- 0/6
- 3/6

Câu hỏi 20

Hoàn thành

Đạt điểm 4,00

Đặt cờ

A 64KB direct-mapped cache organized in 32 bytes lines. The main memory size is 4MB.

1. The number of Tag bits of the cache is 6
2. The number of bits used to index a particular cache line: 5
3. The number of bits used to index the cache: 5
4. The number of bits used to index every single byte on a cache line: 2