EXERCISE 1 – BRANCH PREDICTION (5 points)

In a standard 5-stage pipeline MIPS 32-bit architecture, with signed integer representation. Given the following assembly code, and a "bootstrapping" scenario where R0 is set to 1, R1 is set to 300.

```
LOOP:   LD      F3   0     (R0)
        ADDD    F1   F3    F3
        ADDI    R1   R1    3000
LOOP2:  MULTD   F2   F2    F3
        SUBI    R1   R1    3
        BNEZ    R1   LOOP2
        SUBI    R0   R0    2
        BNEZ    R0   LOOP
```

Answer the following questions:

Question 1: How many iterations for LOOP and LOOP2?

Question 2: Given a 1-bit BHT branch predictor, how many mispredictions are we going to observe?

Question 3: In changing the branch predictor, and in using a 2-bit BHT, how many mispredictions are we going to observe?

Question 4: Considering the answers to question 2 and 3, is the obtained result inline with theoretical characteristics of the two predictors?