Problem 1

In this problem, you will port code to a simple **3-issue VLIW machine,** and schedule it to improve performance.

Details about the 3-issue VLIW machine with 3 fully pipelined functional units:

- Integer ALU with 1 cycle latency to next Integer/FP
- Integer ALU with 2 cycle latency to next Branch
- Memory Unit with 3 cycle latency
- Floating Point Unit with 3 cycle latency (it can complete one add or one multiply per clock cycle)
- Branch completed with 1 cycle delay slot (branch solved in ID stage)
- In the Register File, it is possible to read and write at the same address at the same clock cycle

C Code:

```
for(int i=0; i<N; i++)
        C[i] = A[i]*A[i] + B[i];
```

Assembly Code:

```
loop: ld   f1, 0(r1)
      ld   f2, 0(r2)
      fmul f1, f1, f1
      fadd f1, f1, f2
      st   f1, 0(r3)
      addi r1, r1, 4
      addi r2, r2, 4
      addi r3, r3, 4
      bne  r3, r4, loop
```

Problem 1.A

Considering **one iteration** of the loop (except for the last one), **schedule** the assembly code for the 3-issue VLIW machine in the following table.

Schedule the assembly code by using the **list-based scheduling,** but do not use any software pipelining or loop unrolling. You do not need to write in NOPs (can leave blank).

	Integer ALU	Memory Unit	FPU
C0	`addi r1, r1, 4`	`ld f1, 0(r1)`	
C1	`addi r2, r2, 4`	`ld f2, 0(r2)`	
C2			
C3			`fmul f1, f1, f1`
C4			
C5			
C6			`fadd f1, f1, f2`
C7			
C8			
C9	`addi r3, r3, 4`	`st f1, 0(r3)`	
C10			
C11	`bne  r3, r4, loop`		
C12	`(br delay slot)`		

How long is the critical path? **12 cycles** [1]

What performance did you achieve in FP ops per cycle? **2/12**

What performance did you achieve in cycles per loop iteration? **12/1**

What code efficiency did you achieve? **9/36**

What loop overhead did you achieve? **2 cycles per iteration** [1]

[1] Cycle 12 can be used for the next iteration

Problem 1.B

Based on the solution obtained in Problem 1.A, **reschedule to further optimize** the assembly code for the 3-issue VLIW machine in the following table.

	Integer ALU	Memory Unit	FPU
C0	`addi r1, r1, 4`	`ld f1, 0(r1)`	
C1	`addi r2, r2, 4`	`ld f2, 0(r2)`	
C2	`addi r3, r3, 4`		
C3			`fmul f1, f1, f1`
C4			
C5			
C6			`fadd f1, f1, f2`
C7			
C8	`bne r3, r4, loop`		
C9	`(br delay slot)`	`st f1, -4(r3)`	
C10			
C11			

How long is the Critical Path? **10 cycles**[1]
What performance did you achieve in FP ops per cycle? **2/10**
What performance did you achieve in cycles per loop iteration? **10/1**
What code efficiency did you achieve? **9/30**
What loop overhead did you achieve? **No overhead** [1]

[1] Cycle 10 can be used for the next iteration

Problem 1.C

Unroll two iterations of the loop (so two iterations of the original loop are done for each branch in the new assembly code)

Unrolled Assembly Code (no scheduled)

```
loop:ld   f1, 0(r1)
     ld   f2, 0(r2)
     fmul f1, f1, f1
     fadd f1, f1, f2
     st   f1, 0(r3)
     ld   f3, 4(r1)
     ld   f4, 4(r2)
     fmul f3, f3, f3
     fadd f3, f3, f4
     st   f3, 4(r3)
     addi r1, r1, 8
     addi r2, r2, 8
     addi r3, r3, 8
     bne  r3, r4, loop
```

Considering **one iteration of the unrolled loop, schedule** the assembly code for the 3-issue VLIW machine in the following table **by using list-based scheduling:**

	Integer ALU	Memory Unit	FPU
C0		`ld f1, 0(r1)`	
C1	`addi r1, r1, 8`	`ld f3, 4(r1)`	
C2		`ld f2, 0(r2)`	
C3	`addi r2, r2, 8`	`ld f4, 4(r2)`	`fmul f1, f1, f1`
C4			`fmul f3, f3, f3`
C5			
C6			`fadd f1, f1, f2`
C7			`fadd f3, f3, f4`
C8			
C9		`st f1, 0(r3)`	
C10	`addi r3, r3, 8`	`st f3, 4(r3)`	
C11			
C12	`bne  r3, r4, loop`		
C13	`(br delay slot)`		

How long is the Critical Path? **13 cycles** [1]
What performance did you achieve in FP ops per cycle? **4/13**
What performance did you achieve in cycles per loop iteration? **13/2**
What code efficiency did you achieve? **14/39**
What loop overhead did you achieve? **2 cycles per 2 iterations** [1]

[1] Cycle 13 can be used for the next iteration

Problem 1.D

Based on the solution obtained in Problem 1.A, **reschedule to further optimize** the assembly code for the 3-issue VLIW machine in the following table.

	Integer ALU	Memory Unit	FPU
C0		`ld f1, 0(r1)`	
C1	`addi r1, r1, 8`	`ld f3, 4(r1)`	
C2		`ld f2, 0(r2)`	
C3	`addi r2, r2, 8`	`ld f4, 4(r2)`	`fmul f1, f1, f1`
C4	`addi r3, r3, 8`		`fmul f3, f3, f3`
C5			
C6			`fadd f1, f1, f2`
C7			`fadd f3, f3, f4`
C8			
C9	`bne r3, r4, loop`	`st f1, -8(r3)`	
C10	`(br delay slot)`	`st f3, -4(r3)`	
C11			
C12			

How long is the Critical Path? **11 cycles** [1]
What performance did you achieve in FP ops per cycle? **4/11**
What performance did you achieve in cycles per loop iteration? **11/2**
What code efficiency did you achieve? **14/33**
What loop overhead did you achieve? **No overhead** [1]

[1] Cycle 11 can be used for the next iteration