EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from ACA – Como exam held on 01/07/2013)

Let us consider a computer with a L1 cache and L2 cache memory hierarchy with the following parameters: Processor Clock Frequency = ***1 GHz*** ; Hit Time $_{L1}$ = 1 clock cycle ; Hit Rate $_{L1}$ = 95%; Hit Time $_{L2}$ = 5 clock cycles; Hit Rate $_{L2}$ = 90% ; Miss Penalty $_{L2}$ = 15 clock cycles; Memory Accesses Per Instruction = 78% ; CPI exec = 3

1. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2}$ = Miss Rate$_{L1}$ x Miss Rate$_{L2}$= 0.05 x 0.1 = 0.005 → 0.5%

2. How much is the AMAT?

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x (Hit Time$_{L2}$ + Miss Rate$_{L2}$ x Miss Penalty$_{L2}$) = 1 clock cycle + 0.05 x (5 + 0.1 x 15) clock cycles = 1.325 clock cycles

3. How much is the impact on CPU time of the L2 cache with respect to an IDEAL L2 cache?

CPU$_{time}$ = IC x (CPI$_{exec}$ + MAPI x MR$_{L1}$ x HT$_{L2}$ + MAPI x MR$_{L1\,L2}$ x MP$_{L2}$) x T$_{CLK}$

= IC x (3 + 0.78 x 0.05 x 5 + 0.78 x 0.5 x 15) x T$_{CLK}$ = IC x 9.045 x T$_{CLK}$

CPU$_{time\ IDEAL\ L2}$ = IC x (CPI$_{exec}$ + MAPI x MR$_{L1}$ x HT$_{L2}$) x T$_{CLK}$ = IC x (3 + 0.78 x 0.05 x 5) x T$_{CLK}$ = IC x 3.195 x T$_{CLK}$

CPU$_{time}$ /CPU$_{time\ IDEAL\ L2}$ = 9.045 / 3.195 = 2.83 times slower

Let us assume to introduce an L3 cache with Hit time $_{L3}$ = 8 clock cycles and Hit Rate $_{L3}$ = 92%.

4. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2\,L3}$ = Miss Rate$_{L1}$ x Miss Rate$_{L2}$ x Miss Rate$_{L3}$ = 0.05 x 0.1 x 0.08 = 0.0004 → 0.04%

Being L3 the Last Level Cache, we can assume that now Miss Penalty $_{L3}$ = 15 clock cycles (as the previous case where the L2 cache was the LLC and Miss Penalty $_{L2}$ was 15 clock cycles)

5. How much is Miss Penalty $_{L2}$?

Miss Penalty $_{L2}$ = Hit Time $_{L3}$ + Miss Rate$_{L3}$ x Miss Penalty$_{L3}$ = (8 + 0.08 x 15) clock cycles = 9.2 clock cycles

6. How much is Miss Penalty $_{L1}$?

Miss Penalty$_{L1}$ = Hit Time$_{L2}$ + Miss Rate$_{L2}$ x Miss Penalty$_{L2}$ = (5 + 0.1 x 9.2) clock cycles = 5.92 clock cycles

7. How much is the AMAT?

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Miss Penalty$_{L1}$ = 1 clock cycle+ 0.05 * 5.92 clock cycles = 1.296 clock cycles

OR we can calculate AMAT as:

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x (Hit Time$_{L2}$ + Miss Rate$_{L2}$ x (Hit Time$_{L3}$ + Miss Rate$_{L3}$ x Miss Penalty$_{L3}$))= Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Hit Time$_{L2}$ + Miss Rate $_{L1\,L2}$ x Hit Time$_{L3}$ + Miss Rate $_{L1\,L2\,L3}$ x Miss Penalty$_{L3}$ = (1 + 0.05 x 5 + 0.005 x 8 + 0.0004 x 15) = 1.296 clock cycles

EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from ACA – Como 12/09/2013)

Let us consider a computer with a L1, L2 and L3 cache memory hierarchy with the following parameters: Processor Clock Frequency = ***1 GHz*** ;
Hit Time $_{L1}$ = 1 clock cycle ; Hit Rate $_{L1}$ = 95%;
Hit Time $_{L2}$ = 4 clock cycles; Hit Rate $_{L2}$ = 92% ;
Hit Time $_{L3}$ = 8 clock cycles; Hit Rate $_{L3}$ = 90% ; Miss Penalty $_{L3}$ = 15 clock cycles;

1. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2\,L3}$ = Miss Rate$_{L1}$ x Miss Rate$_{L2}$ x Miss Rate$_{L3}$ = 0.05 x 0.08 x 0.1 = 0.0004 → 0.04%

2. How much is Miss Penalty $_{L2}$?

Miss Penalty $_{L2}$ = Hit Time $_{L3}$ + Miss Rate$_{L3}$ x Miss Penalty$_{L3}$ = (8 + 0.1 x 15) clock cycles = 9.5 clock cycles

3. How much is Miss Penalty $_{L1}$?

Miss Penalty$_{L1}$ = Hit Time$_{L2}$ + Miss Rate$_{L2}$ x Miss Penalty$_{L2}$ = (4 + 0.08 x 9.5) clock cycles = 4.76 clock cycles

4. How much is the AMAT?

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Miss Penalty$_{L1}$ = 1 clock cycle+ 0.05 * 4.76 clock cycles = 1.238 clock cycles

OR we can calculate AMAT as:

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x (Hit Time$_{L2}$ + Miss Rate$_{L2}$ x (Hit Time$_{L3}$ + Miss Rate$_{L3}$ x Miss Penalty$_{L3}$))= Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Hit Time$_{L2}$ + Miss Rate $_{L1\,L2}$ x Hit Time$_{L3}$ + Miss Rate $_{L1\,L2\,L3}$x Miss Penalty$_{L3}$ = (1 + 0.05 x 4 + 0.004 x 8 + 0.0004 x 15) = 1.238 clock cycles

5. Given Memory Accesses Per Instruction = 78% ; CPI exec = 3, how much is the impact on CPU time of the L1 and L2 cache when considering an IDEAL L3 cache ?

IDEAL L3 cache means Hit Rate $_{L3}$ = 100% therefore Miss Penalty $_{L2}$ = Hit Time $_{L3}$ = 8 clock cycles

CPU$_{time\ IDEAL\ L3}$ = IC x (CPI$_{exec}$ + MAPI x MR$_{L1}$ x HT$_{L2}$ + MAPI x MR$_{L1\,L2}$ x MP$_{L2}$) x T$_{CLK}$

= IC x (3 + 0.78 x 0.05 x 4 + 0.78 x 0.05 x 0.08 x 8) x T$_{CLK}$ = IC x 3.18 x T$_{CLK}$

EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from HP book 5th Ed. on page B-31)

Let us consider a computer with a L1 cache and L2 cache memory hierarchy. Suppose that in 1000 memory references there are 40 misses in L1 and 20 misses in L2.

1. What are the various miss rates?

Miss Rate $_{L1}$ = 40 /1000 = 0.04 → 4%

Miss Rate $_{L2}$ = 20 /40 = 0.5 → 50%

Global Miss Rate for Last Level Cache:

Miss Rate $_{L1\,L2}$ = Miss Rate$_{L1}$ x Miss Rate$_{L2}$= 0.04 x 0.5 = 0.02 → 2%

Assume the Hit Time $_{L1}$ = 1 clock cycle ; Hit Time $_{L2}$ = 10 clock cycles; Miss Penalty $_{L2}$ = 200 clock cycles; Memory Accesses Per Instruction = 150%

2. How much is the AMAT?

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x (Hit Time$_{L2}$ + Miss Rate$_{L2}$ x Miss Penalty$_{L2}$) = 1 clock cycle + 0.04 x (10 + 0.5 x 200) clock cycles = 5.4 clock cycles

3. How much is the average memory stall cycles per instruction?

Avg. Memory Stalls per Instr. = Misses per Instr.$_{L1}$ HT$_{L2}$ + Misses per Instr.$_{L2}$ MP$_{L2}$

= MAPI x MR$_{L1}$ x HT$_{L2}$ + MAPI x MR$_{L1\,L2}$ x MP$_{L2}$ = 1.5 x 0.04 x 10 + 1.5 x 0.02 x 200 = 6.6 clock cycles

Please notice that if we subtract the L1 hit time from AMAT and then multiply by the (average) memory accesses per instruction, we get the same Avg. Memory Stalls per Instr. :

(AMAT - Hit Time$_{L1}$) x MAPI = (5.4 -1) x 1.5 = 6.6 clock cycles = Avg. Memory Stalls per Instr.