Course on Advanced Computer Architectures
EXAM 27/06/2019 – Please write by PEN in CAPITAL LETTERS & BLACK/BLUE!!!

EXERCISE 3: CACHE COHERENCY (5 points)

Consider the following access pattern on a two-processor system with a direct-mapped, write-back cache with one cache block and a two cache block memory.

Assume the **MESI protocol** is used, with **write-back** caches, **write-allocate,** and **write-invalidate** of other caches. Please complete the following table:

Cycle	After Operation	P0 cache block state	P1 cache block state	Memory at block 0 up to date?	Memory at block 1 up to date?
0	P0: read block 1	Exclusive (1)	Invalid	Yes	Yes
1	P1: read block 0				
2	P0: write block 1				
3	P1: read block 0				
4	P0: write block 0				
5	P1: write block 1				
6	P0: write block 0				
7	P0: read block 1				
8	P1: read block 1				
9	P0: write block 1				
10	P1: write block 1				

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SOLUTION:

Cycle	After Operation	P0 cache block state	P1 cache block state	Memory at block 0 up to date?	Memory at block 1 up to date?
0	P0: read block 1	Exclusive (1)	Invalid	Yes	Yes
1	P1: read block 0	Exclusive (1)	Exclusive (0)	Yes	Yes
2	P0: write block 1	Modified (1)	Exclusive (0)	Yes	No
3	P1: read block 0	Modified (1)	Exclusive (0)	Yes	No
4	P0: write block 0	Modified (0)	Invalid	No	Yes
5	P1: write block 1	Modified (0)	Modified (1)	No	No
6	P0: write block 0	Modified (0)	Modified (1)	No	No
7	P0: read block 1	Shared (1)	Shared (1)	Yes	Yes
8	P1: read block 1	Shared (1)	Shared (1)	Yes	Yes
9	P0: write block 1	Modified (1)	Invalid	Yes	No
10	P1: write block 1	Invalid	Modified (1)	Yes	No