From embedded systems to high performance computing

problems and solutions while waiting for the IOT

Speaker
Prof. William Fornaciari
Politecnico di Milano – Dipartimenti di Elettronica, Informazione e Bioingegneria
Via Ponzio 34/5, 20133 Milano, Italy
william.fornaciari@polimi.it

Summary

- General Computing challenges
- Drivers for the evolution
- Show-stoppers
- Application of the innovation to some fields of interest
- Examples from innovation projects (videos)
- Question time & Discussion

It's cross related…it's complicated

- Applications are pushing
  – Cost mass market compatible
  – Invasion in all the aspects of the life
  – Volumes

- Technology evolve
  – Integration scale
  – New materials and programming paradigms

- What is making the meeting in the middle «complicated»?
  – CMOS technology is arriving to the limit
  – Cost of new basic technologies is sometimes unaffordable
  – Power/energy wall
  – Data proliferation
  – Hard to move from invention to innovation
  – Design methodology is exploiting humans (fortunately)

Let’s start with an example: P3S project

- Target groups
  - Children with cognitive and motor disability (e.g. autistic kids)
  - Hospitalized Children
    - Their caregivers
    - Therapists
    - Educators
    - Parents
  - Regular children and families (in the longer term)

TARGET GROUPS: Some numbers

Cognitive Disorder

25 M
children

(Developmental Disabilities Monitoring Network 2014)

Motor or intellectual disability

5-7%
world population

(Annual Rep. US congress 2010)

Autism

1 in 68
children

The fastest growing disability in US: + 70% in the last 10 year
(US Center for Disease Control and Prevention, 2014)

NEEDS

1. Playful & Embodied Learning

- play and bodily interaction (tangible manipulation of objects, physical movements in space)
  - stimulates cognitive processes & sensor-motor capacities
  - in all contexts of children's life

Therapeutic Center

Hospital

School

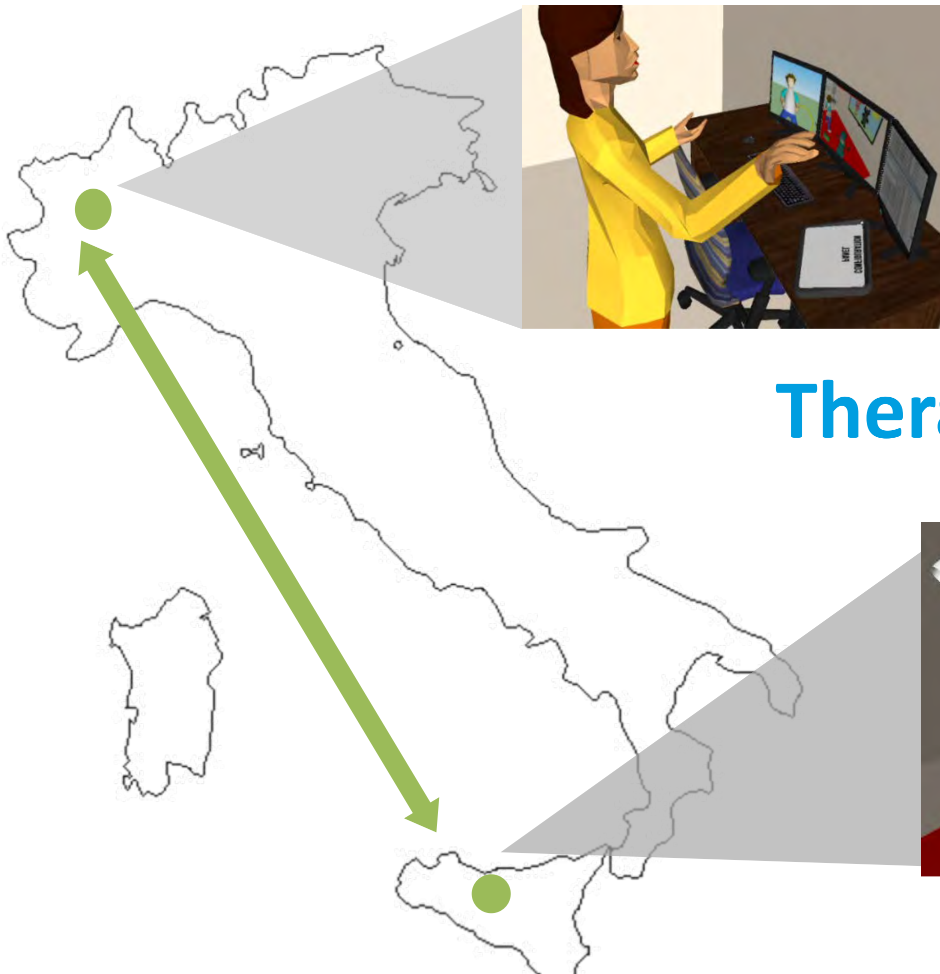
Home

Public Playground

2. New forms of therapy and learning

Need – remote therapy

Smart Spaces → Playful Smart Spaces → Playful Supervised Smart Spaces



Therapist

Home, School

P3S CONCEPT: Playful Smart Space

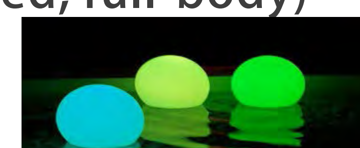
A multisensory “installation” integrated in children’s living environments

Physical space enriched with

- Multimedia virtual worlds

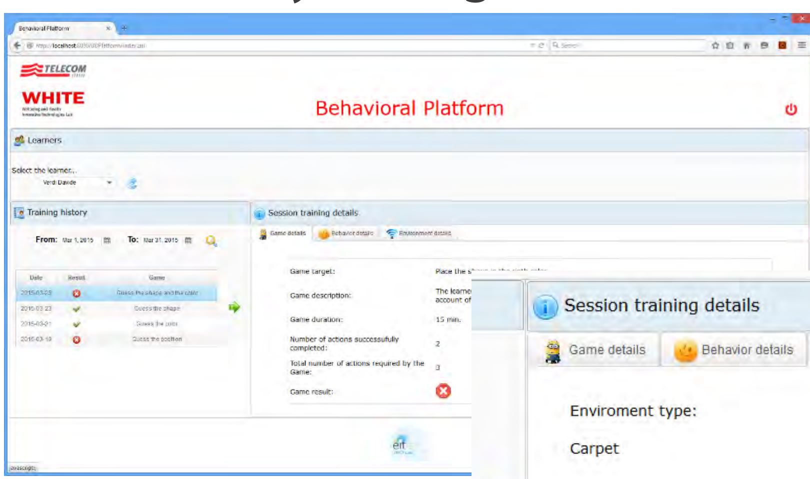
on large displays or projected on the floor/wall/ceiling

- “smart” objects (e.g. smart lights, smart toys, …)
- multiple interaction paradigms (tangible, motion-based, full-body)



P3S Concept: Playful Supervised Smart Space

- emote sensing and live monitoring of users’ interactions
- automatic collection of behavioral data
  - interaction logs
  - ECG monitoring via wearable devices
- remote (manual or semi-automatic) customization of UX parameters
- data analysis (algorithms and interfaces)

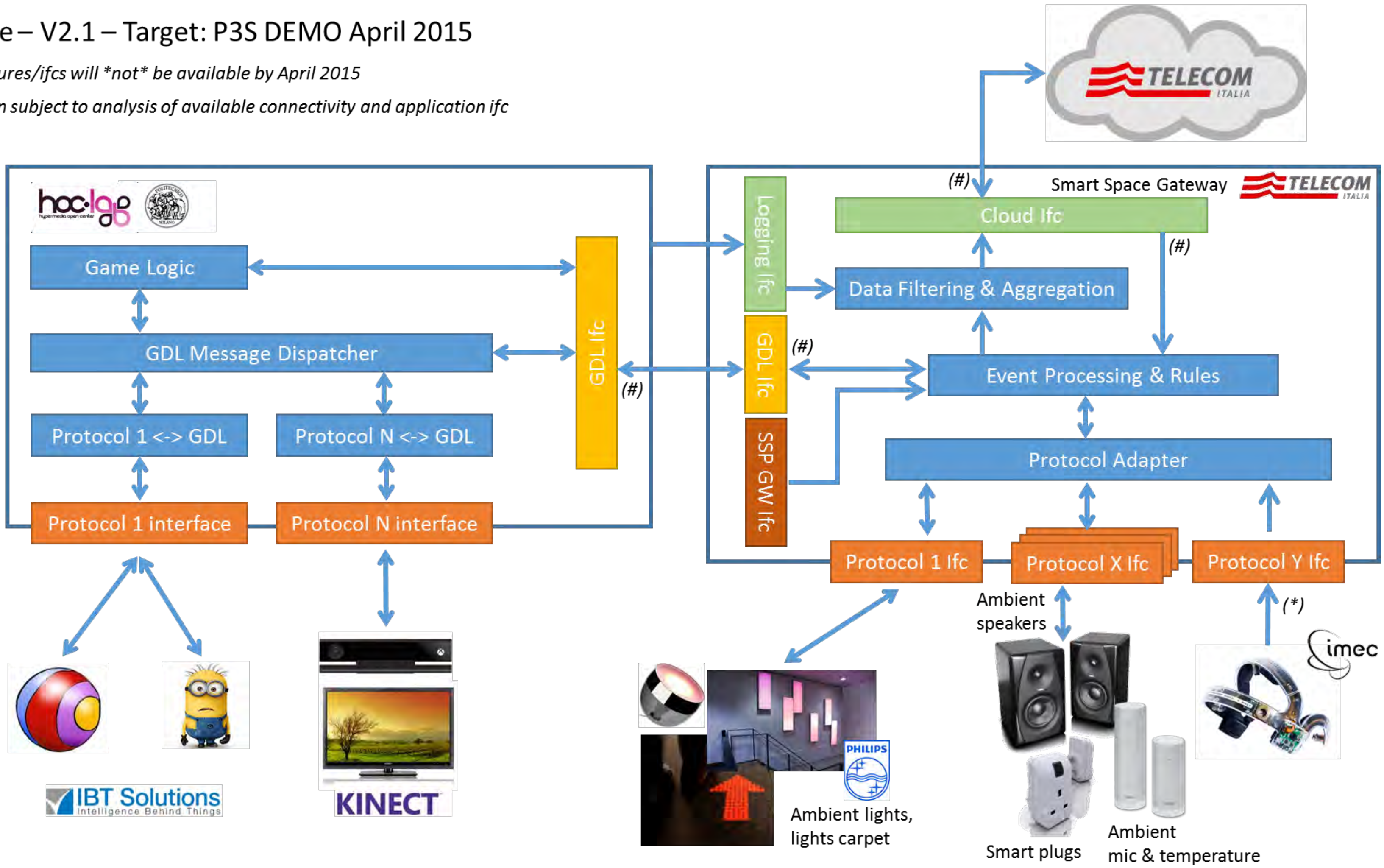


P3S architecture

Architecture – V2.1 – Target: P3S DEMO April 2015

*(#) = these features/ifcs will *not* be available by April 2015*

(*) = integration subject to analysis of available connectivity and application ifc

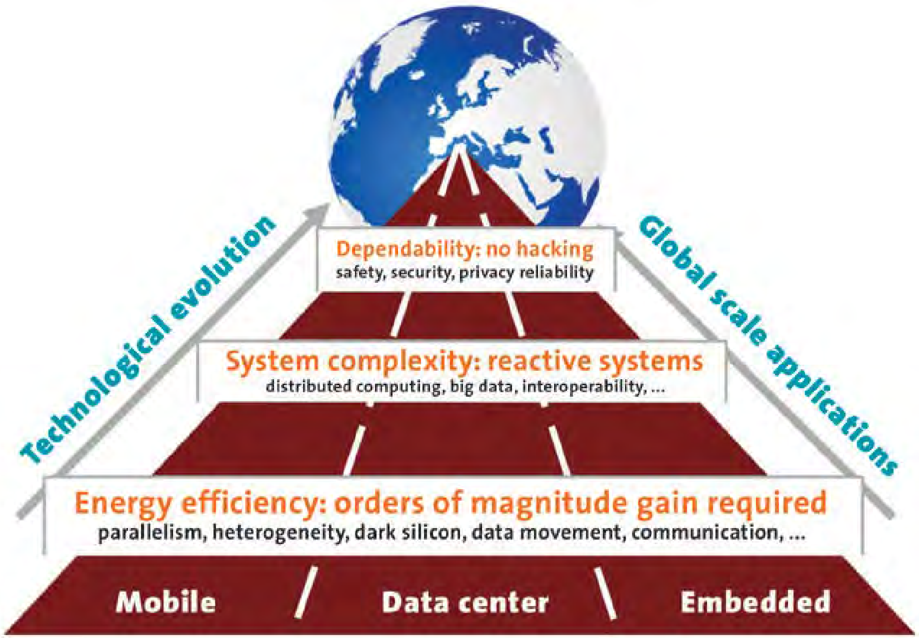


Requirements of a so vertical application

- Sensors possibly wearable
- Computing units
  - Low power for the sensors
  - High Performance Computing for data processing in the cloud
- Communication
  - Bandwidth to the cloud
  - Low power short range for wearable sensors
- Massive storage (in perspective)
- In-field experiments with prototypes and volunteers
- Customizability
- Standardization and compliance to regulations
- Affordable cost
- Design of interoperable software, distribuited architecture
- Hardware interoperability
- Players capable to enter into the market, from the concepts to the product it is a long way to come

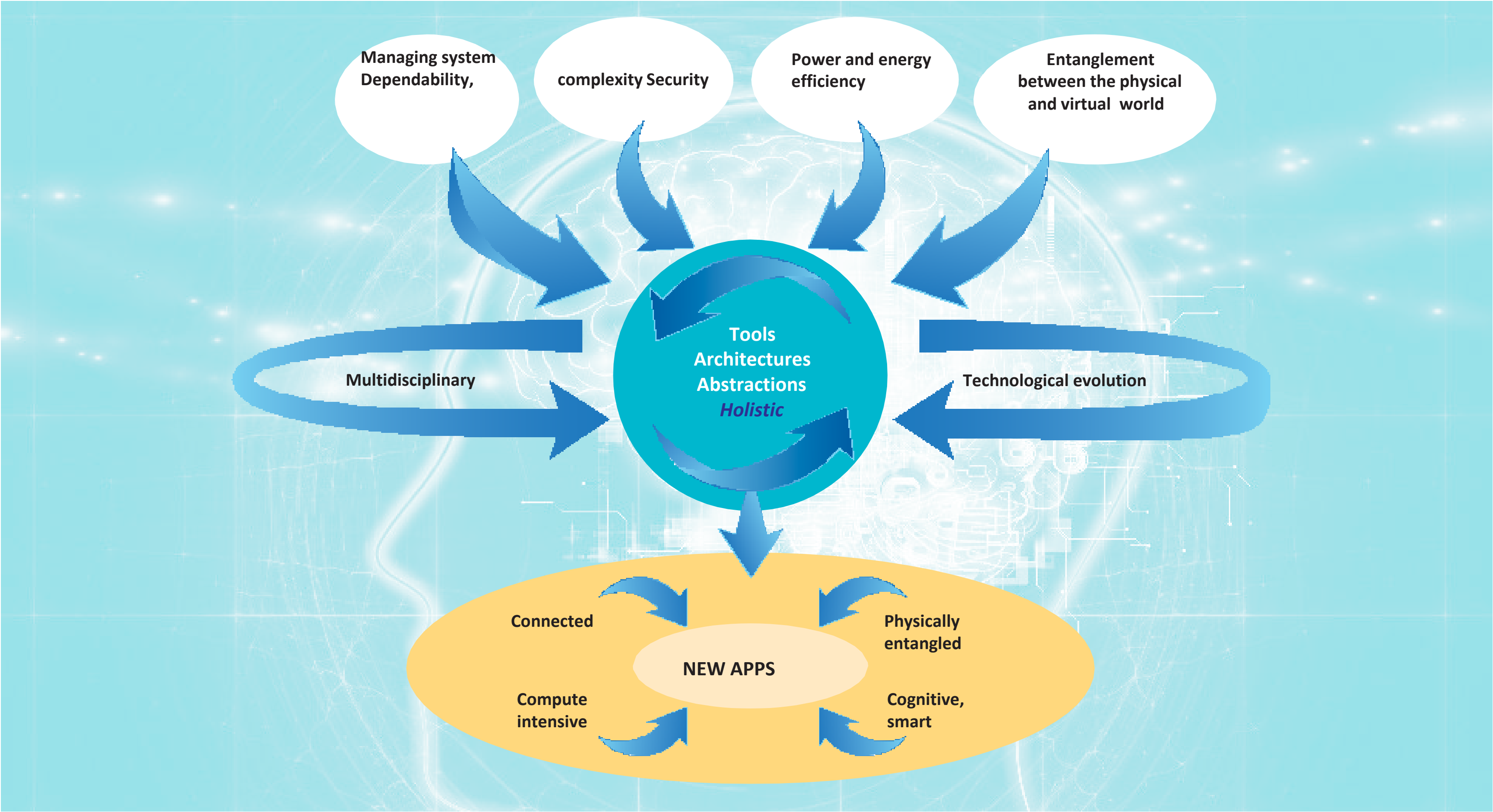
Is the current technology mature enough to substain the evolution of such type of systems/applications?

Main topics from the HiPEAC 2020 vision



- Energy and power dissipation: the newest technology nodes made things even worse
- Dependability, which affects security, safety and privacy, is a major concern
- Complexity is reaching a level where it is nearly unmanageable, and yet still grows due to applications that build on systems of systems

Application needs



Application needs (cont'd)

- They will be compute-intensive, i.e. they will require efficient hardware and software components, irrespective of their application domain: embedded, mobile or data center

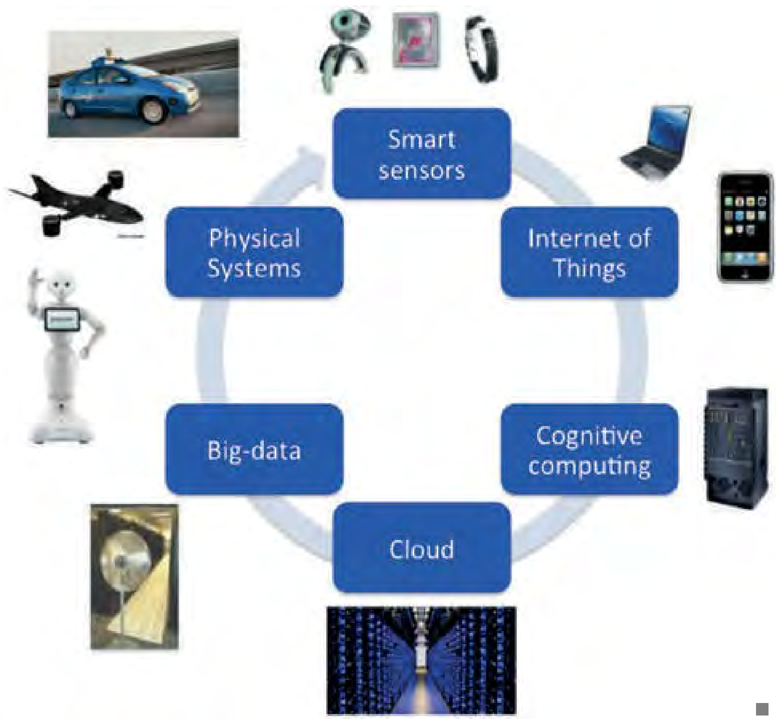
- They will be connected to other systems, wired or wireless, either always or intermittently online. In many cases they will be globally interconnected via the Internet

- They will be entangled physically, which means that they will not only be able to observe the physical environment that they are operating in, but also to control it. They will become part of our environment

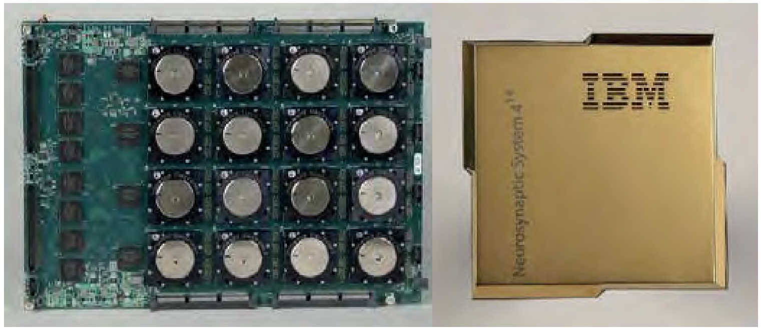
- They will be smart, able to interpret data from the physical world even if that data is noisy, incomplete, analog, remote, etc

All future killer applications will have these four characteristics, albeit not all to the same extent

Entanglement btw physical and virtual world



- The virtual, digital world and the real, physical world are being connected in the Internet of Things and in Cyber-Physical Systems
- Cognitive computing is making the interface, often driving big-data analytics and data mining



- SyNAPSE chip (IBM), a brain inspired computer architecture powered by 1 million neurons and 256 million synapses
- It is the largest chip IBM has ever built at 5.4 billion transistors and consists of 4096 neurosynaptic cores
- This architecture is meant to solve a wide class of problems from vision, audition and multi-sensory fusion at very low power

Small savings → great impact!

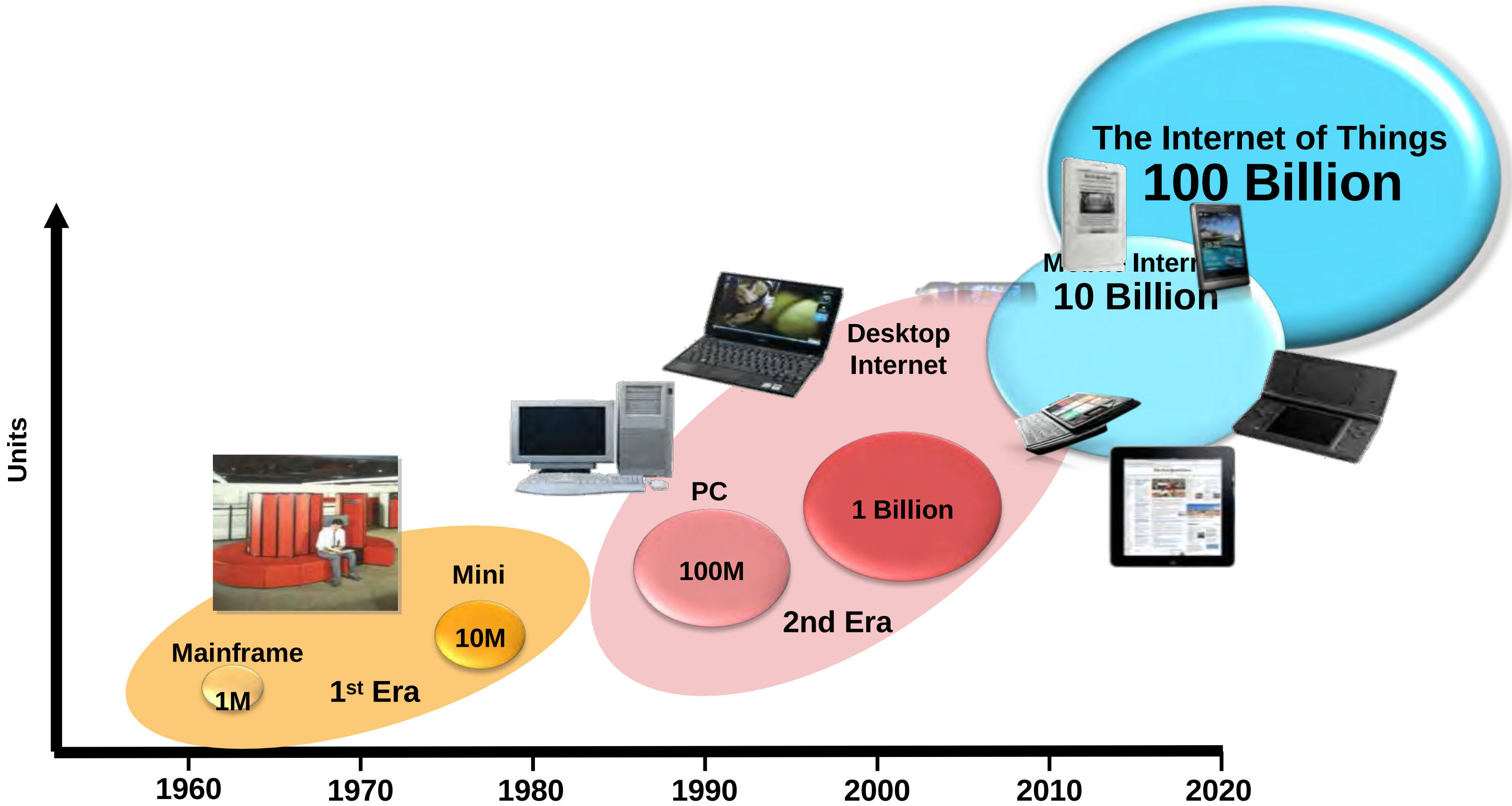
Industrial Internet: The Power of 1 Percent

What if... Potential Performance Gains in Key Sectors

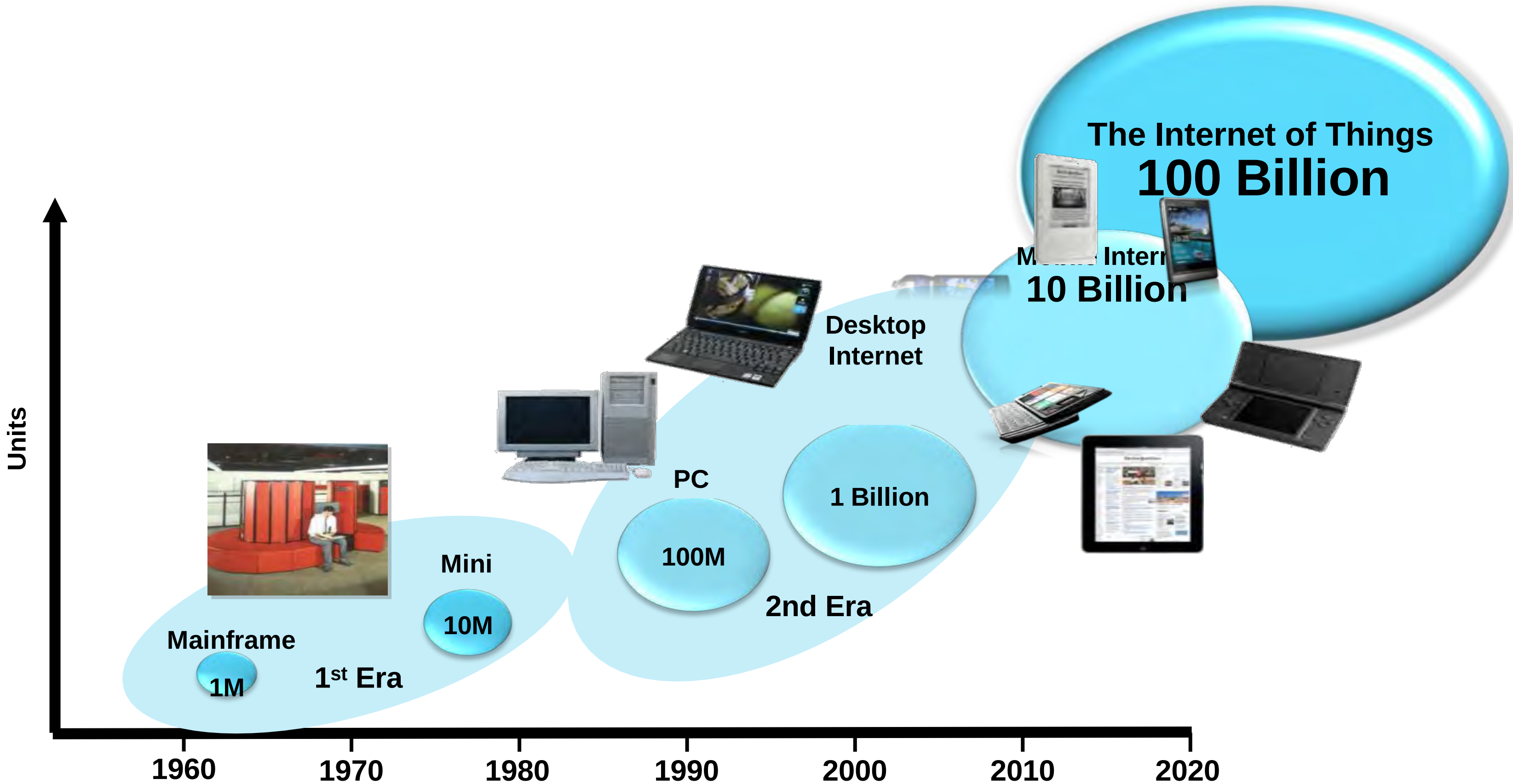
Industry	Segment	Type of Savings	Estimated Value over 15 Years (Billion nominal US dollars)
Aviation	Commercial	1% Fuel Savings	$30B
Power	Gas-fired Generation	1% Fuel Savings	$66B
Healthcare	System-wide	1% Reduction in System Inefficiency	$63B
Rail	Freight	1% Reduction in System Inefficiency	$27B
Oil & Gas	Exploration & Development	1% Reduction in Capital Expenditures	$90B

Note: Illustrative examples based on potential one percent savings applied across specific global industry sectors.
Source: GE estimates

The Eras of Computing



The Eras of Computing



Industry Changes in Requirements

Evolution of the industry-driving metric

Industry Changes in Requirements

Functionality

Evolution of the industry-driving metric

Up to 1980s

Supercomputers & mainframes

Industry Changes in Requirements

Evolution of the industry-driving metric

Functionality

Functionality / $

Up to 1980s

Supercomputers & mainframes

1990s

The personal computer

Industry Changes in Requirements

Evolution of the industry-driving metric

Functionality

$\frac{\text{Functionality}}{\$}$

$\frac{\text{Functionality}}{\text{Power} \times \$}$

Up to 1980s

Supercomputers & mainframes

1990s

The personal computer

2000s

Notebooks

Industry Changes in Requirements

Evolution of the industry-driving metric

Up to 1980s	1990s	2000s	2010s
Functionality	$\frac{\text{Functionality}}{\$}$	$\frac{\text{Functionality}}{\text{Power} \times \$}$	$\frac{\text{Functionality}}{\text{Energy} \times \$}$
Supercomputers & mainframes	The personal computer	Notebooks	Mobiles & mobility

Strategic Direction

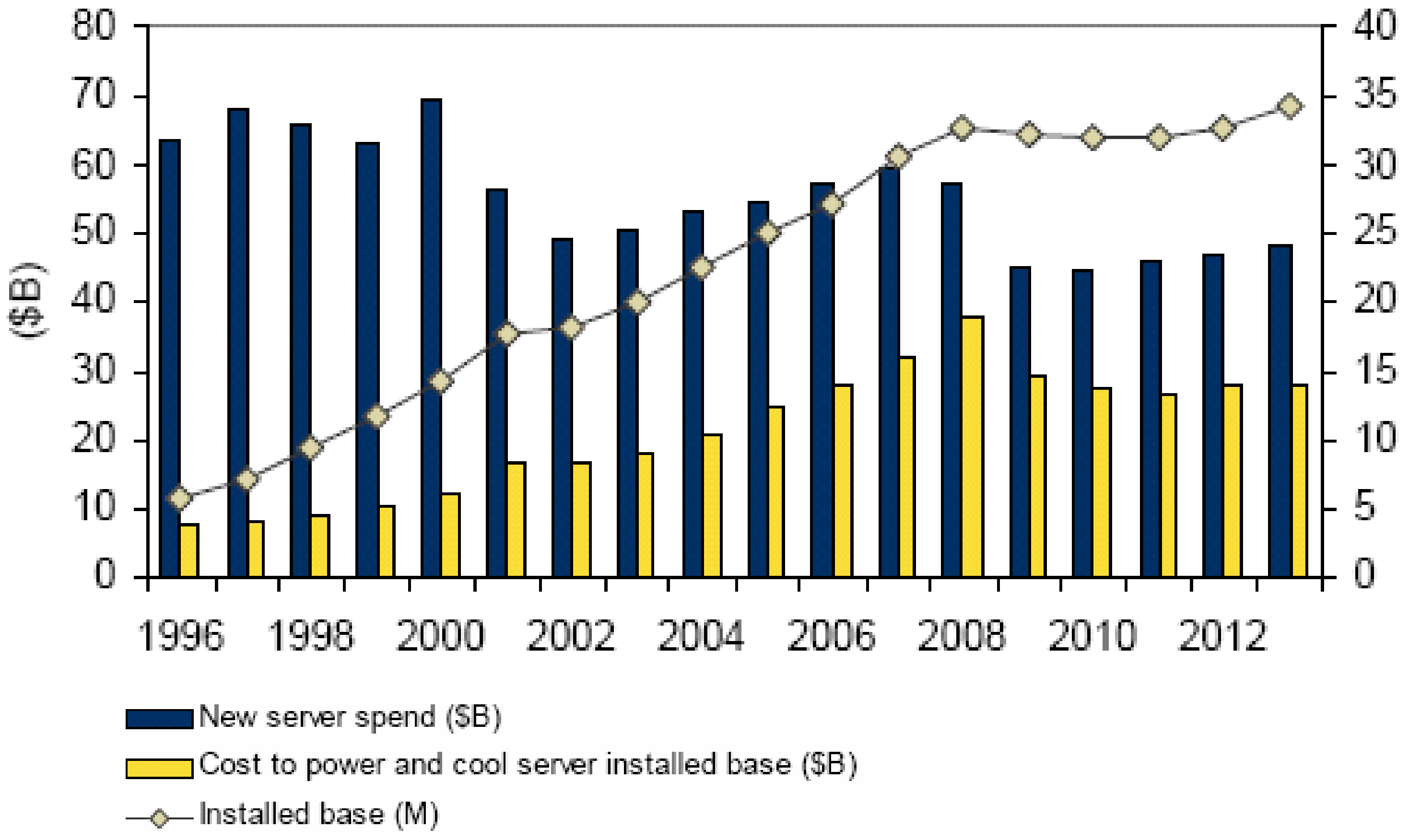
The bad news: this is a very hard metric to optimize for

$$\frac{\textbf{Functionality}}{\textbf{Energy}\times\$}$$

The good news: if you crack it, you "own" the simpler metrics as well…

Cost of hardware versus cost of operation

- **1MW for one year costs ~1M$ (average in the US),**
- **increases 20% annually (J. Hamilton, Amazon, Google DC summit May 11**



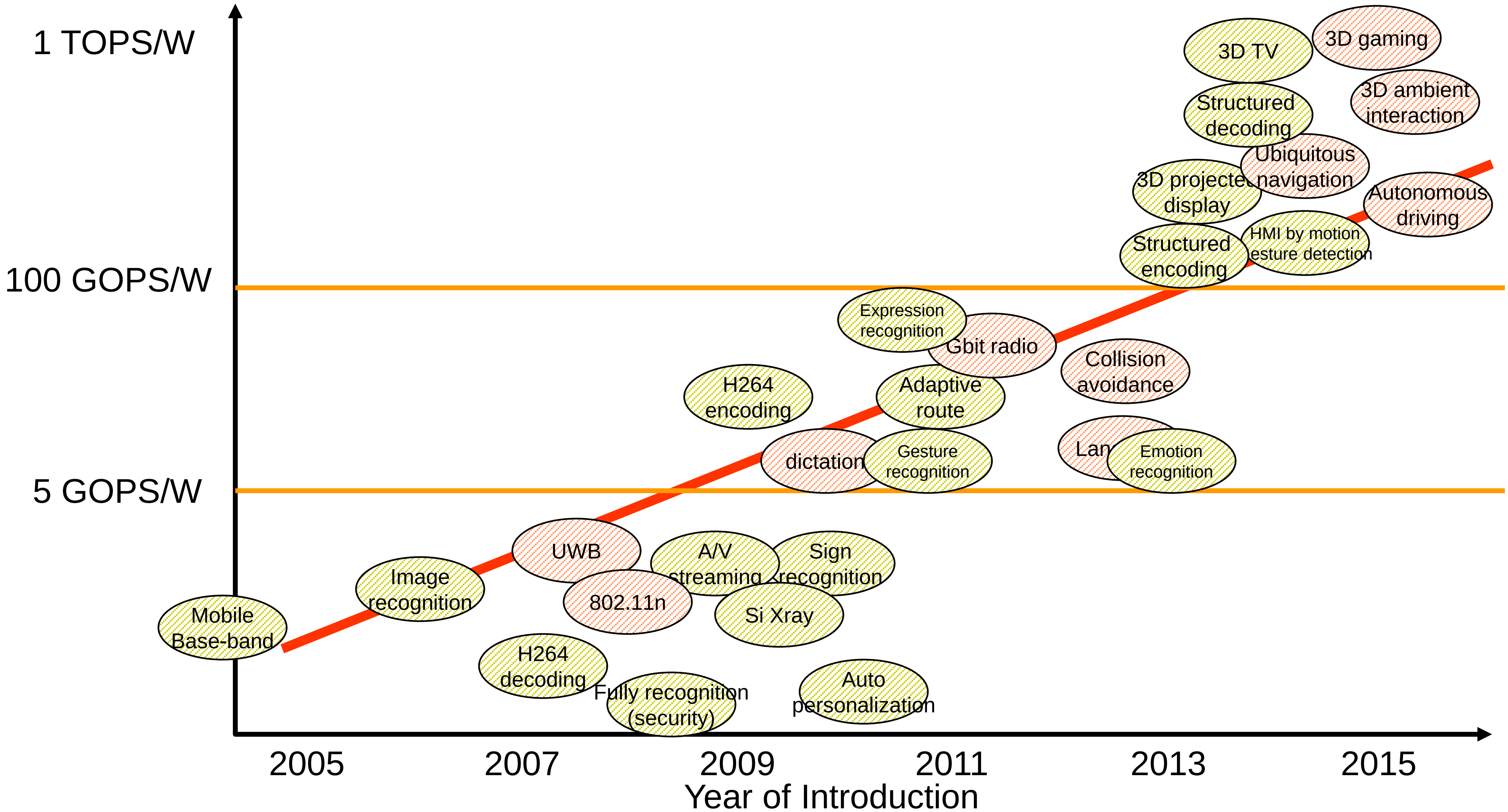
Modern application requirements

LIFE-CRITICAL

MOBILE

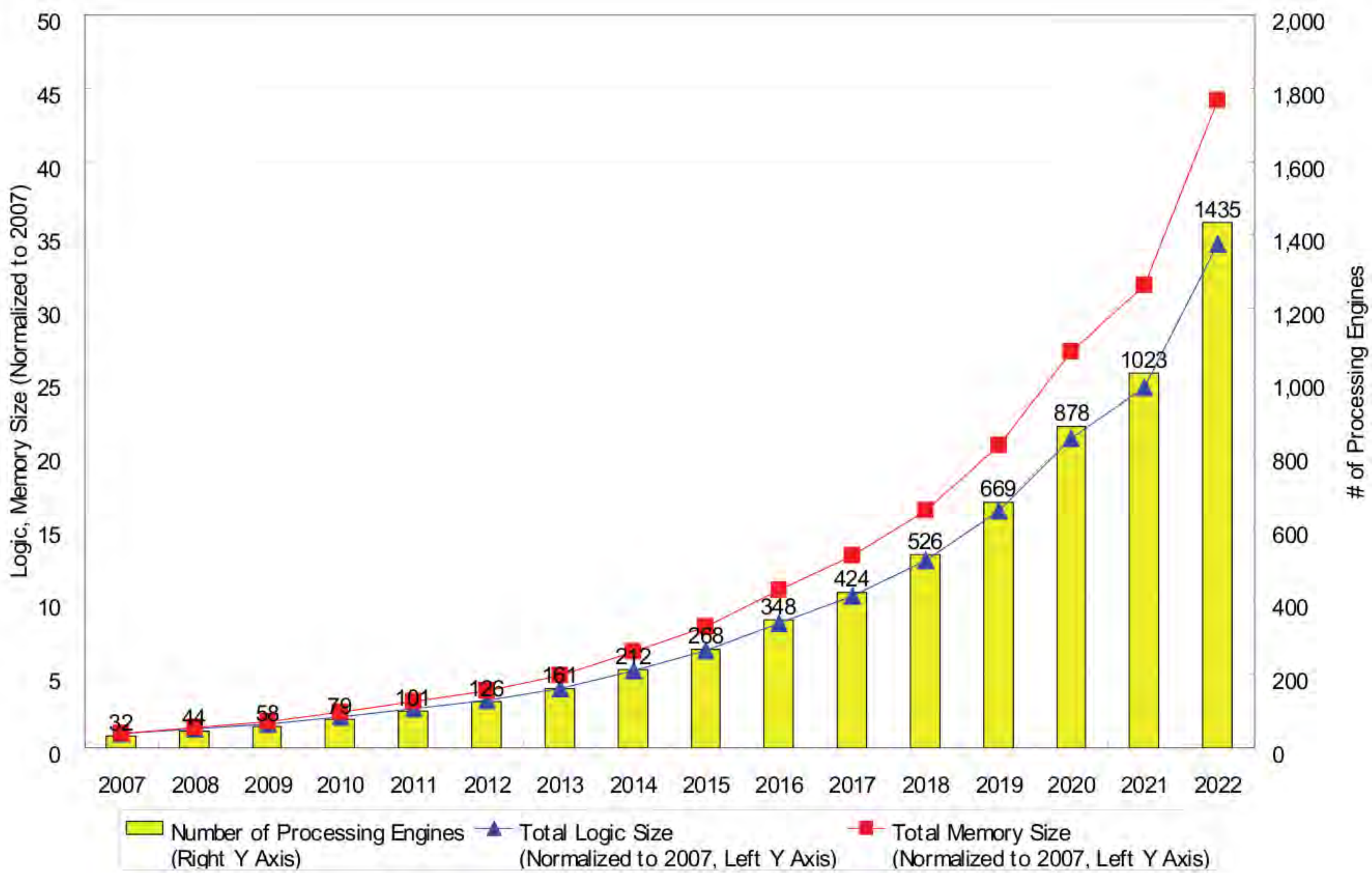
PROCESSING POWER

Market application rush

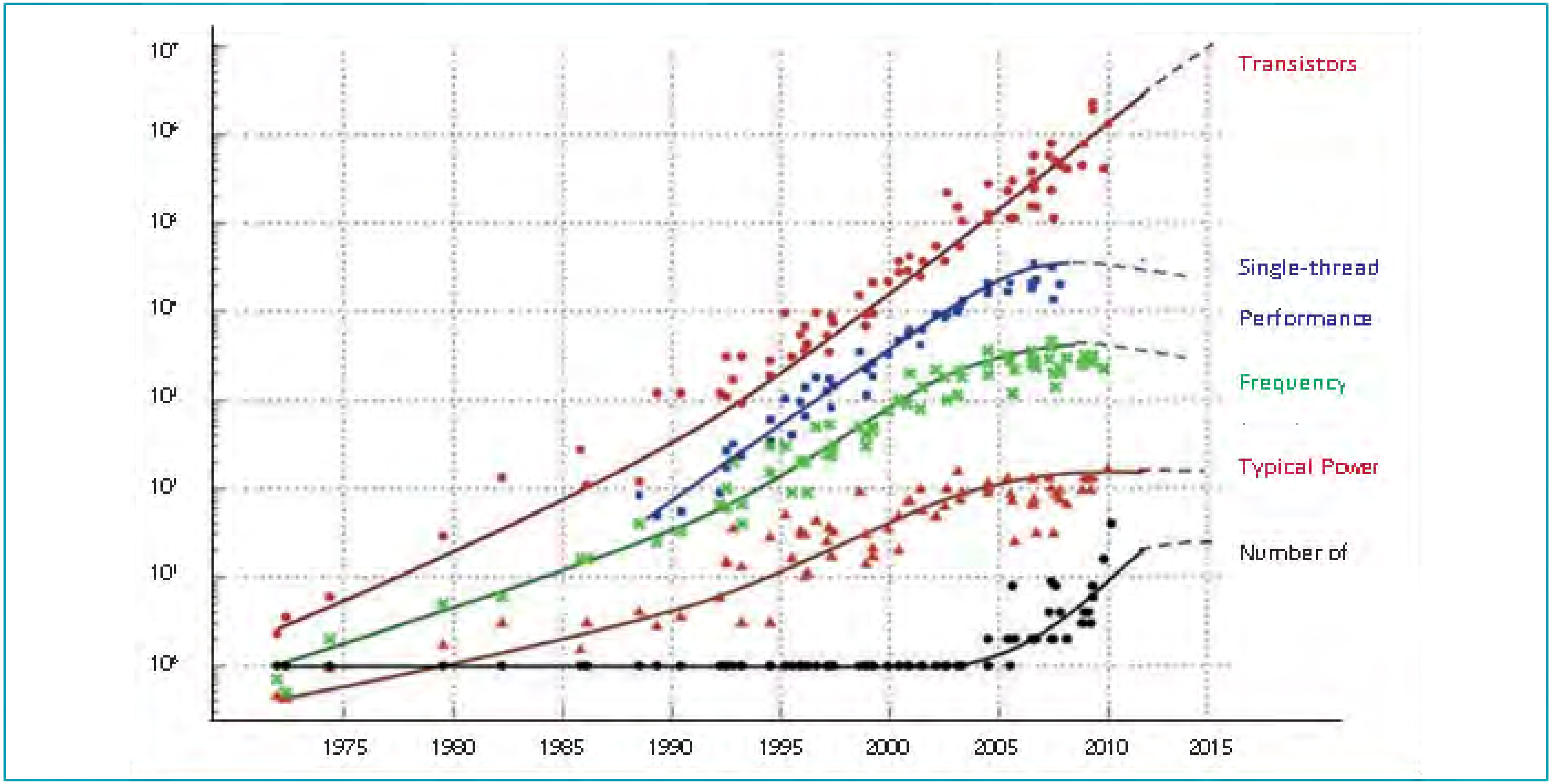


Increasing processing demand

- MPSoC architectures evolution
  - Many core, multi core, heterogeneous computing



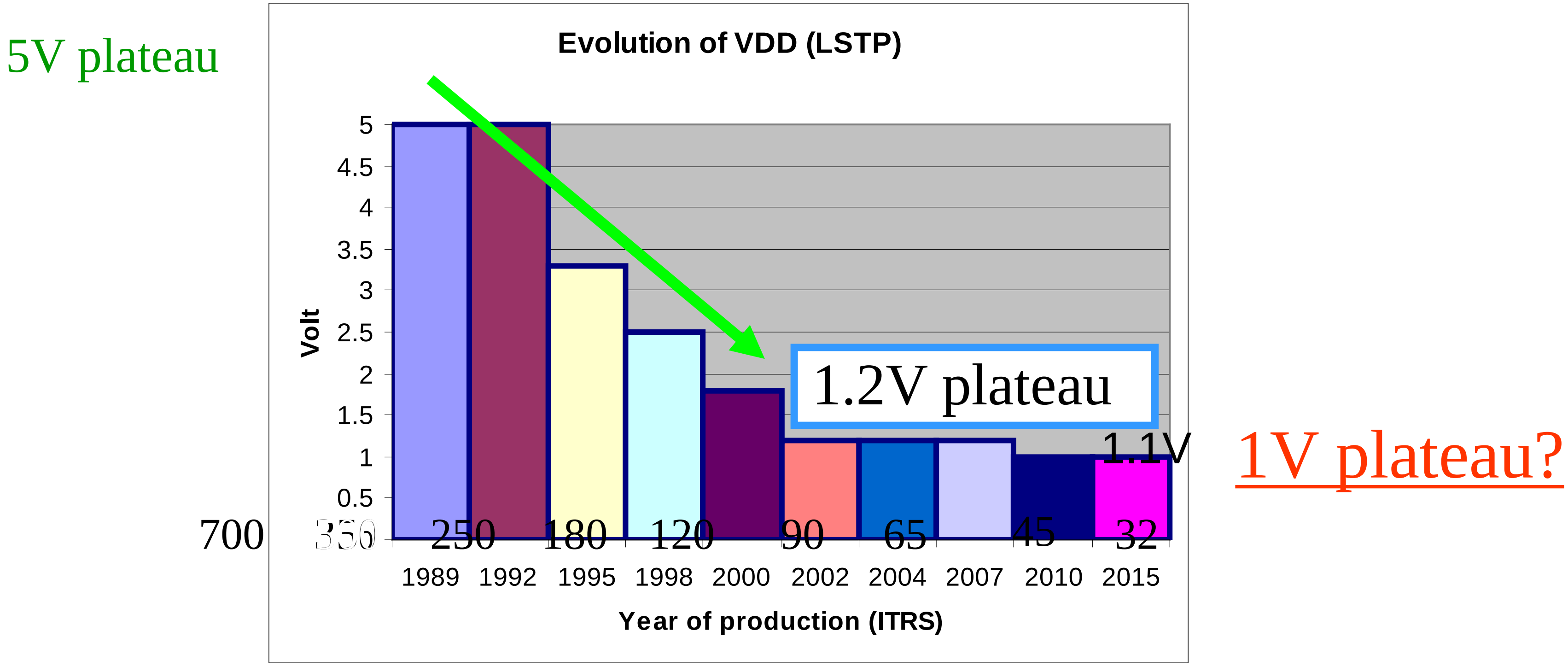
Towards the dark silicon



- Not-exploitable computing power due to limited power dissipation
- Part of the silicon area is …»dark silicon»

VDD is no more scaling down

Regular decrease
5V to 1.2V (0.7x per node)



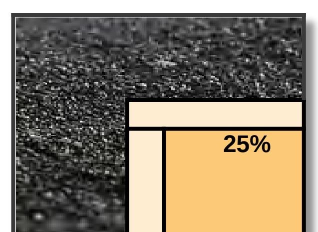
Creation of dark silicon

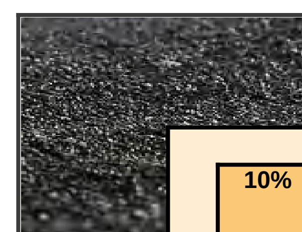
Node	45nm	22nm	11nm
Year	2008	2014	2020
$Area^{-1}$	1	4	16
Peak freq	1	1.6	2.4
Power	1	1	0.6

$(4 \times 1)^{-1} = 25\%$

$(16 \times 0.6)^{-1} = 10\%$

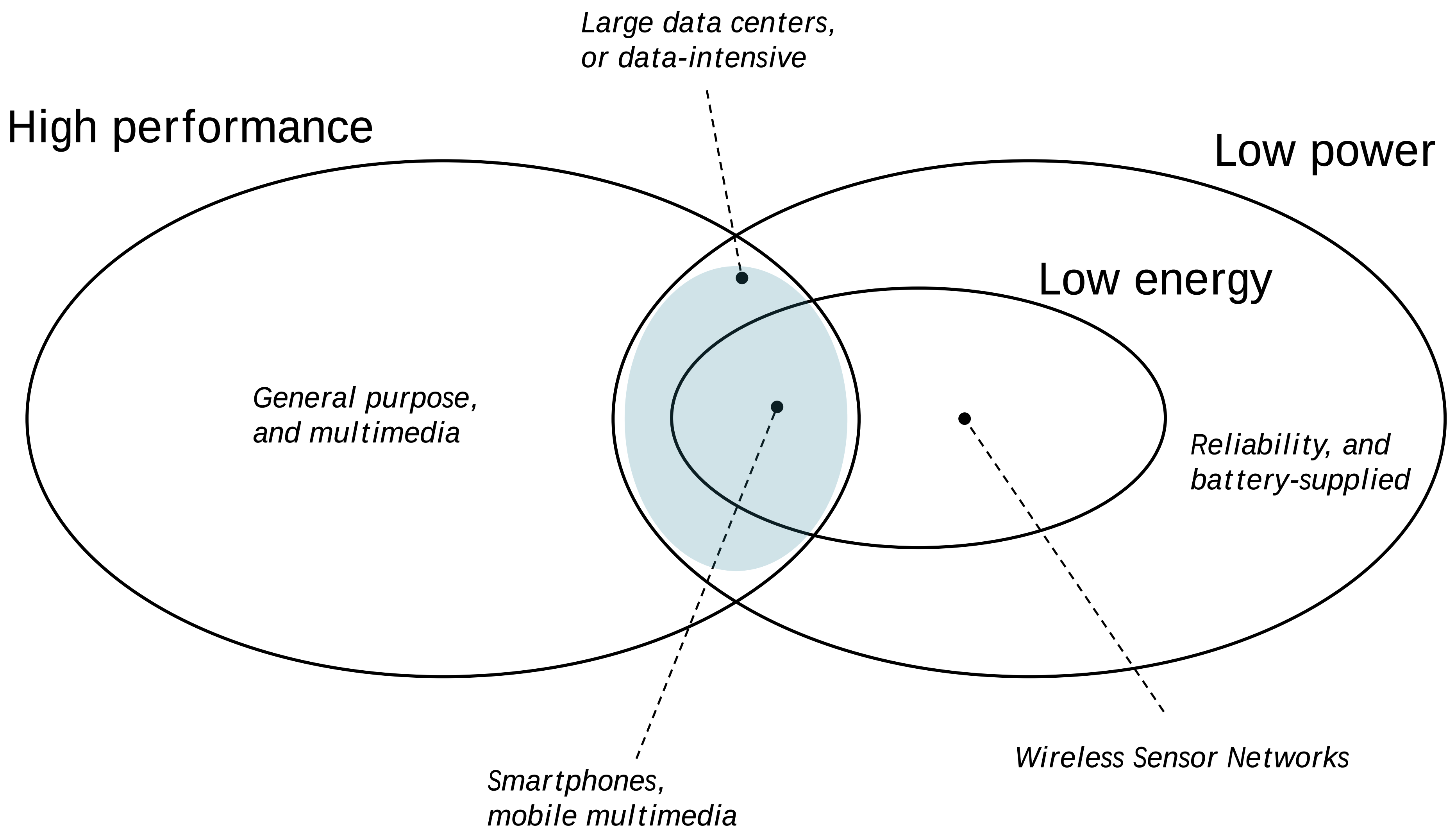
Exploitable Si
(in 45nm power budget)





Source: ITRS 2008

Application scenarios



What we can do

- We can have more transistors

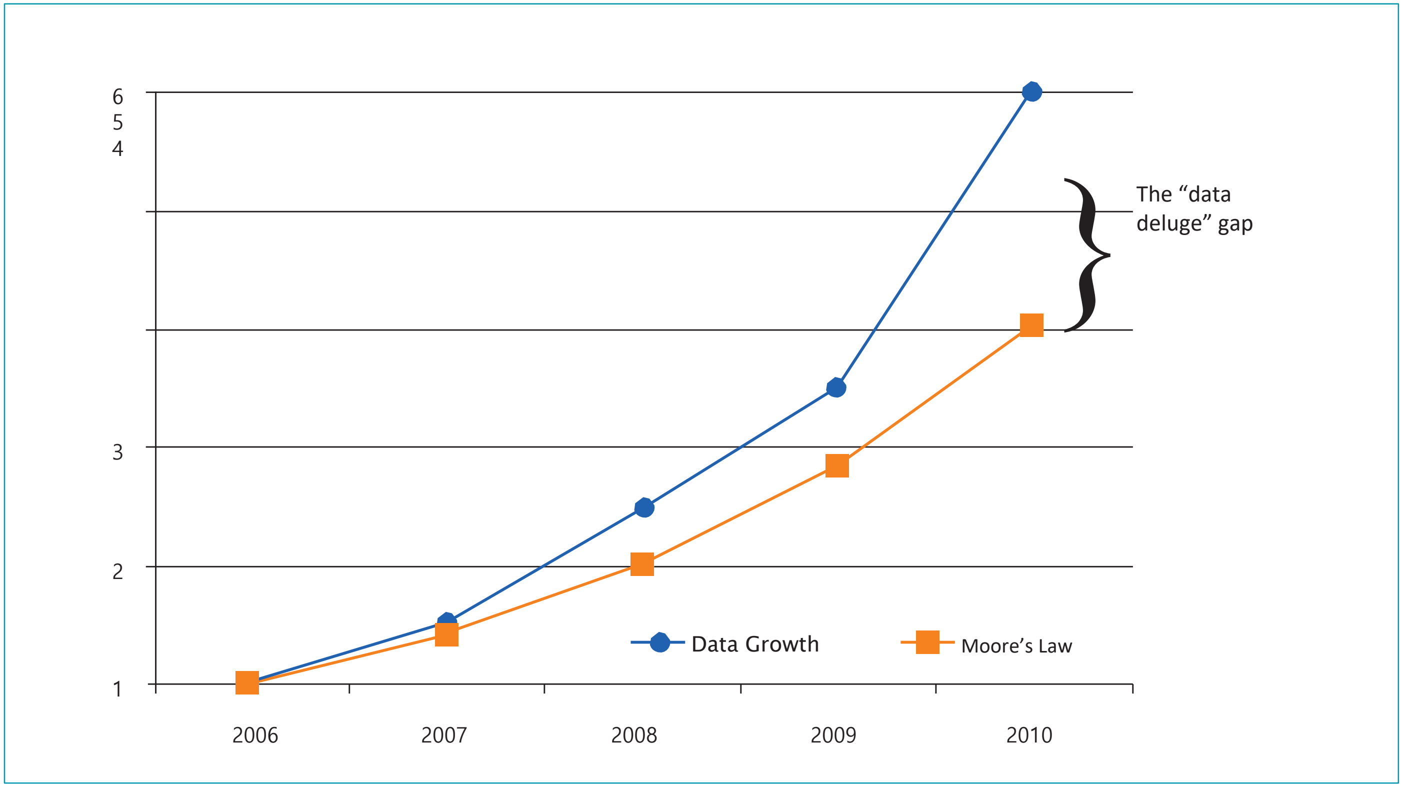
- We just can't power them all at the same time

- We need to use these extra transistors in new ways
  - Multicores
  - Many-cores
  - Domain-specific processors

- It all points to heterogeneous processing
  - And aggressive power management

- Computing to be done in the most efficient place

Now you have the bicyle...



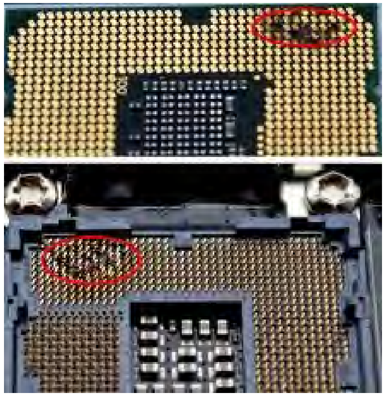
- Data growth vs. Moore's Law trends in the last 5 years
- Data "deluge" means that we are heading towards a world where we will have more data available than we can process

The Networks-on-Chip Reliability Wall

Small transistors = Big problems
- Process Variation
- Physical Failure
- Aging mechanisms (NBTI)
  - (device performance decreases over years)

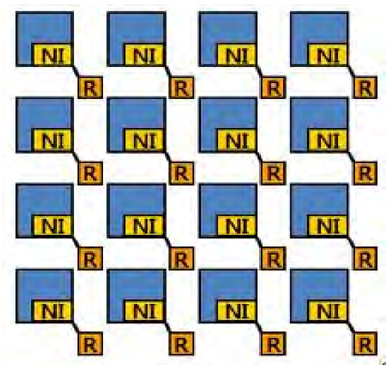
Small transistors = more packed transistors
(VLSI integration)
- Increased power density
- Thermal issues

"Reliability will be a barrier to future scaling"
Shekhar Borkar,
Intel Fellow



"Reliability will be a first class design constraint"
Chuck Moore,
AMD Senior Fellow

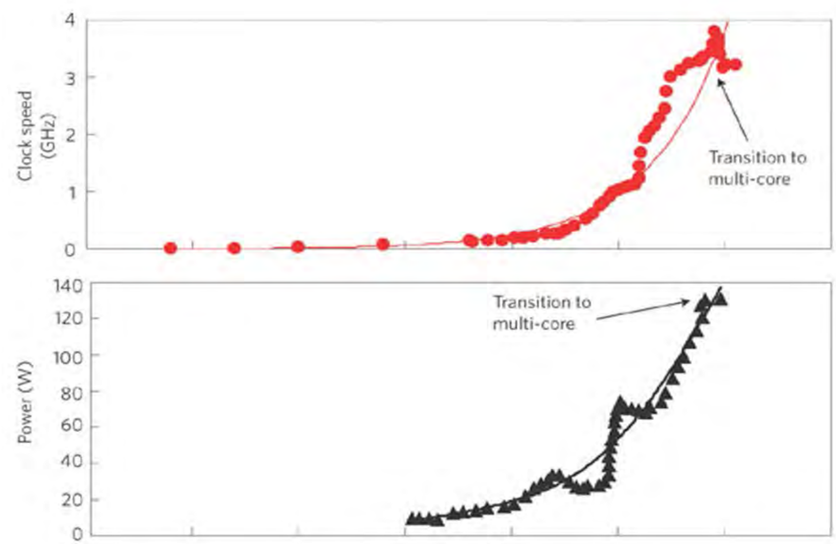
Network-on-Chip and Power-Performance



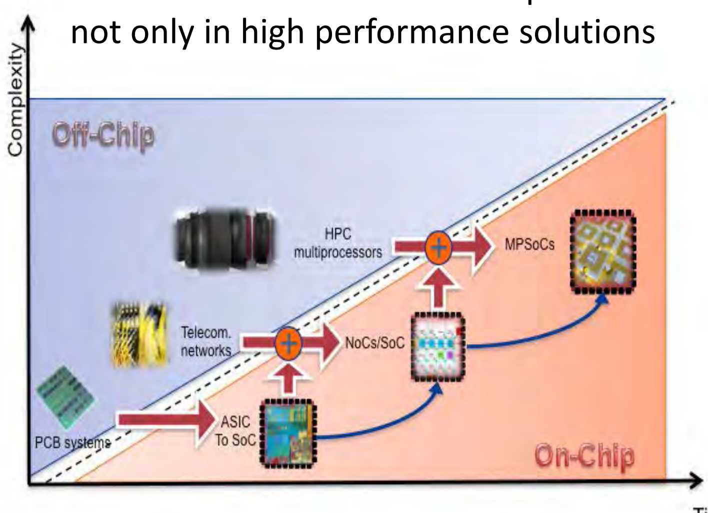
Network-on-Chip (NoC): multi-core flexible/scalable interconnect [1]
traditional communication subsystems cannot ensure adequate power/performance trade-off (buses, P2Ps, crossbars)

- ***NoC power can be up to 30% of the total chip [3]***
- ***NoC performance greatly influences the multicore [1,3]***

Power wall
performance are not free. Multi-core to optimize power performance trade-off **[2]**

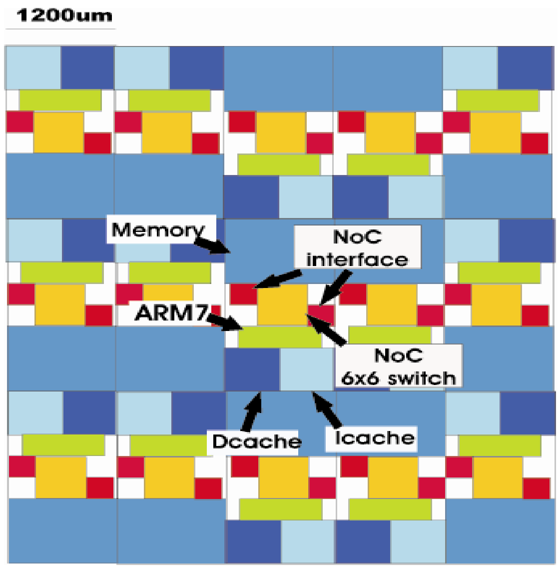


Single-core -> Multi-core architectures
there is a need for even more performance not only in high performance solutions

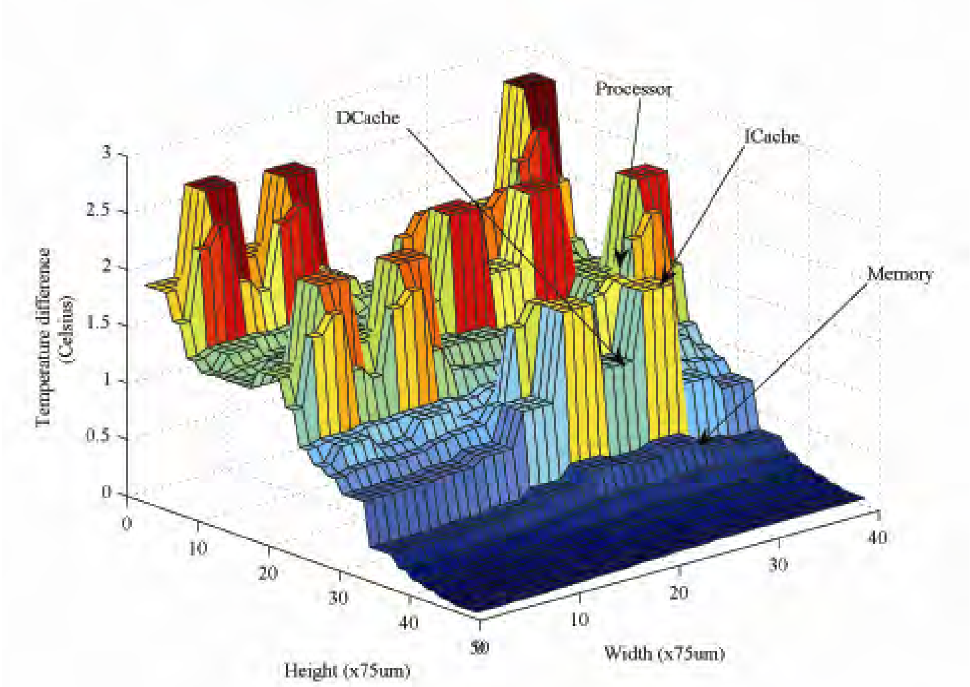


[1] G. de Micheli and L. Benini. Networks on chip: A new paradigm for systems on chip design. In DATE '02, page 418, Washington, DC, USA, 2002.
[2] A. Majumdar. “Helping chips to keep their cool”. Nature Nanotechnology, April 2009, pp. 214-215.
[3] Hoskote, Y., S. Vangal, A. Singh, N. Borkar, and S. Borkar (2007) “A 5-GHz Mesh Interconnect for a Teraflops Processor,” Micro, IEEE, 27(5), pp. 51–61.

Hot spots and Thermal problems



Chip floorplan



Steady state temperature

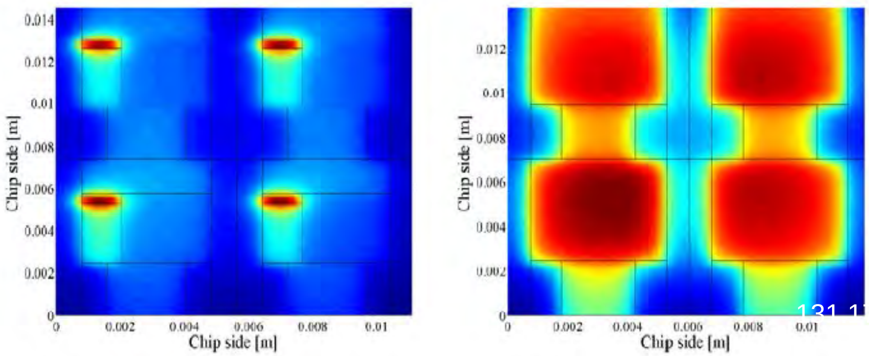
Some hot spots in steady state:

- Silicon is a good thermal conductor (only 4x worse than Cu) and temperature gradients are likely to occur on large dies
- Lower power density than on a high performance CPU

  (lower frequency and less complex HW)

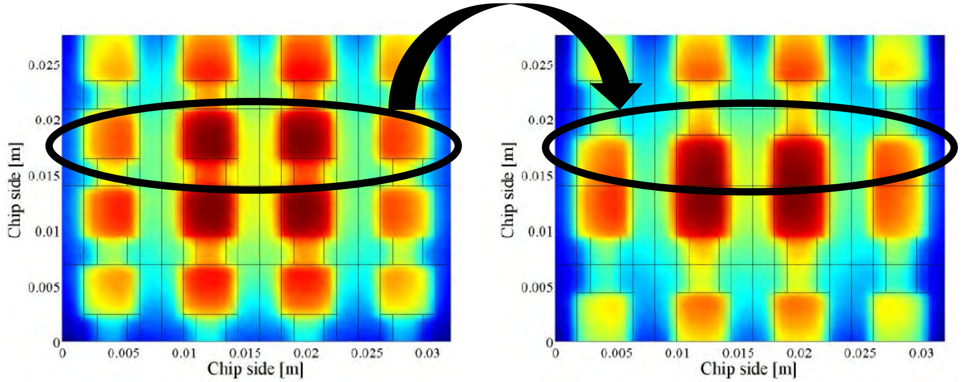
Thermal oriented analysis and design

Multiple levels of detail



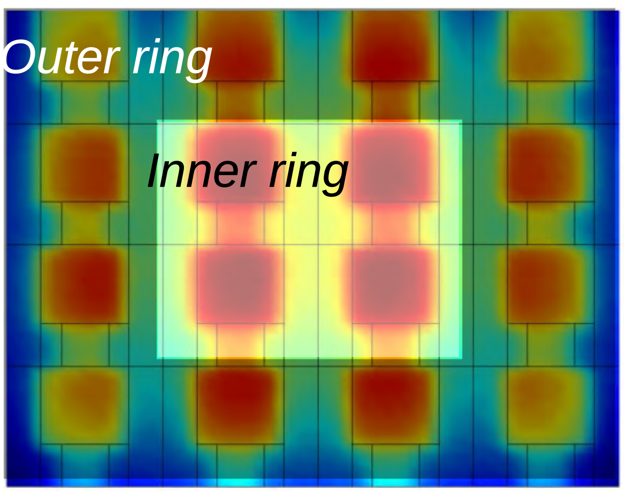
(a) Highest detail level (b) Lowest detail level

Different floorplan options



(a) Classical floorplan (b) Floorplan with rotation

Practical for assess methodologies, for example



Goal: Fairly balance the chip thermal map

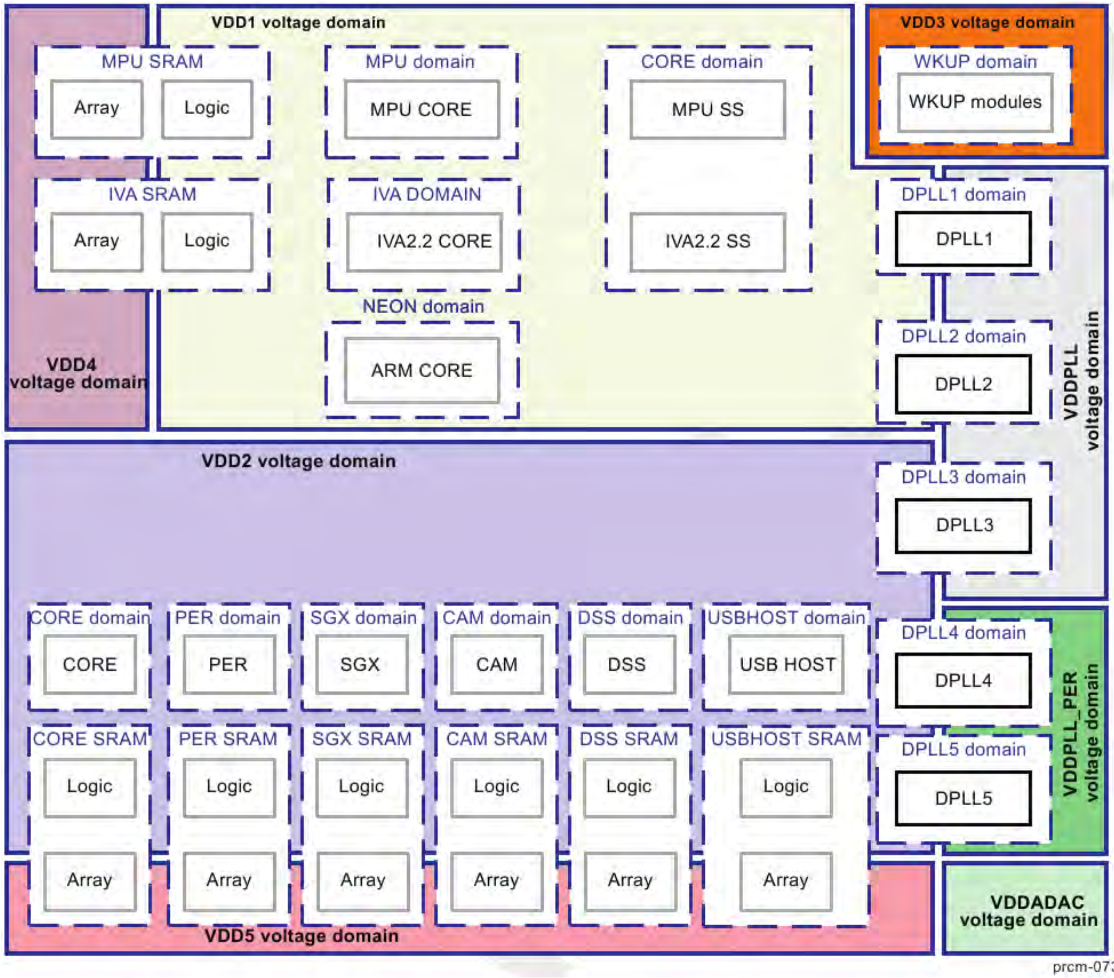
How to:

- Divide the chip in concentric rings, where a DVFS module con set frequency (**f**) and voltage (**V**)
- Collect experimental data to design-time optimize (**V,f**) pair values for each ring subject to
- Minimum difference **f** difference between each rings pair.

(HINT frequency proportional to performance and we want fairness)

Voltage and frequency scaling

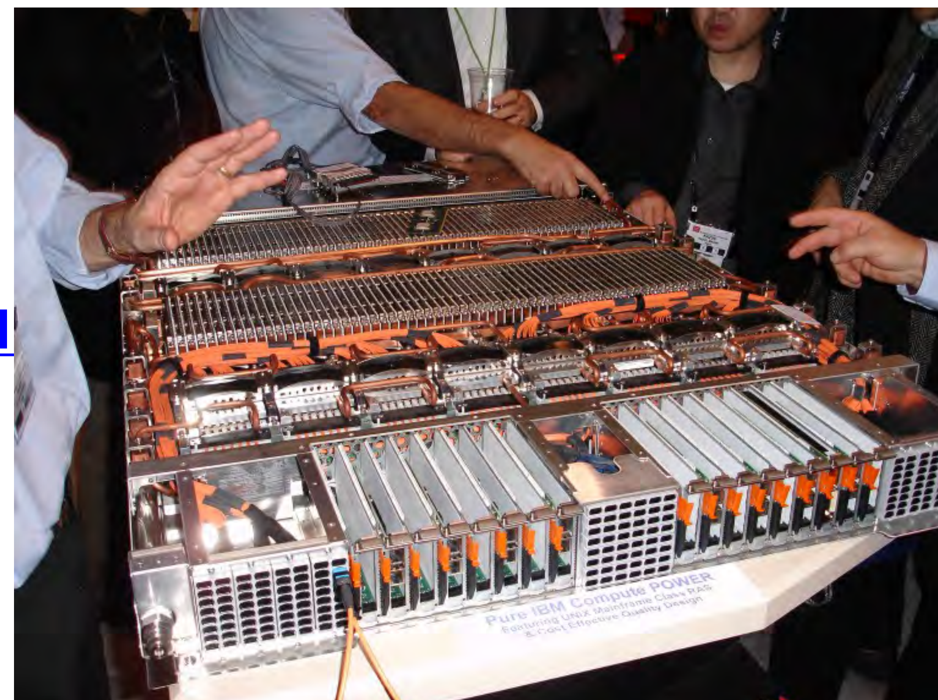
- Chips/Systems are partitioned in islands differing in terms of voltage and frequency, with the possibility to be switched off dinamically (power gating)



- OMAP Platform by Texas Instruments

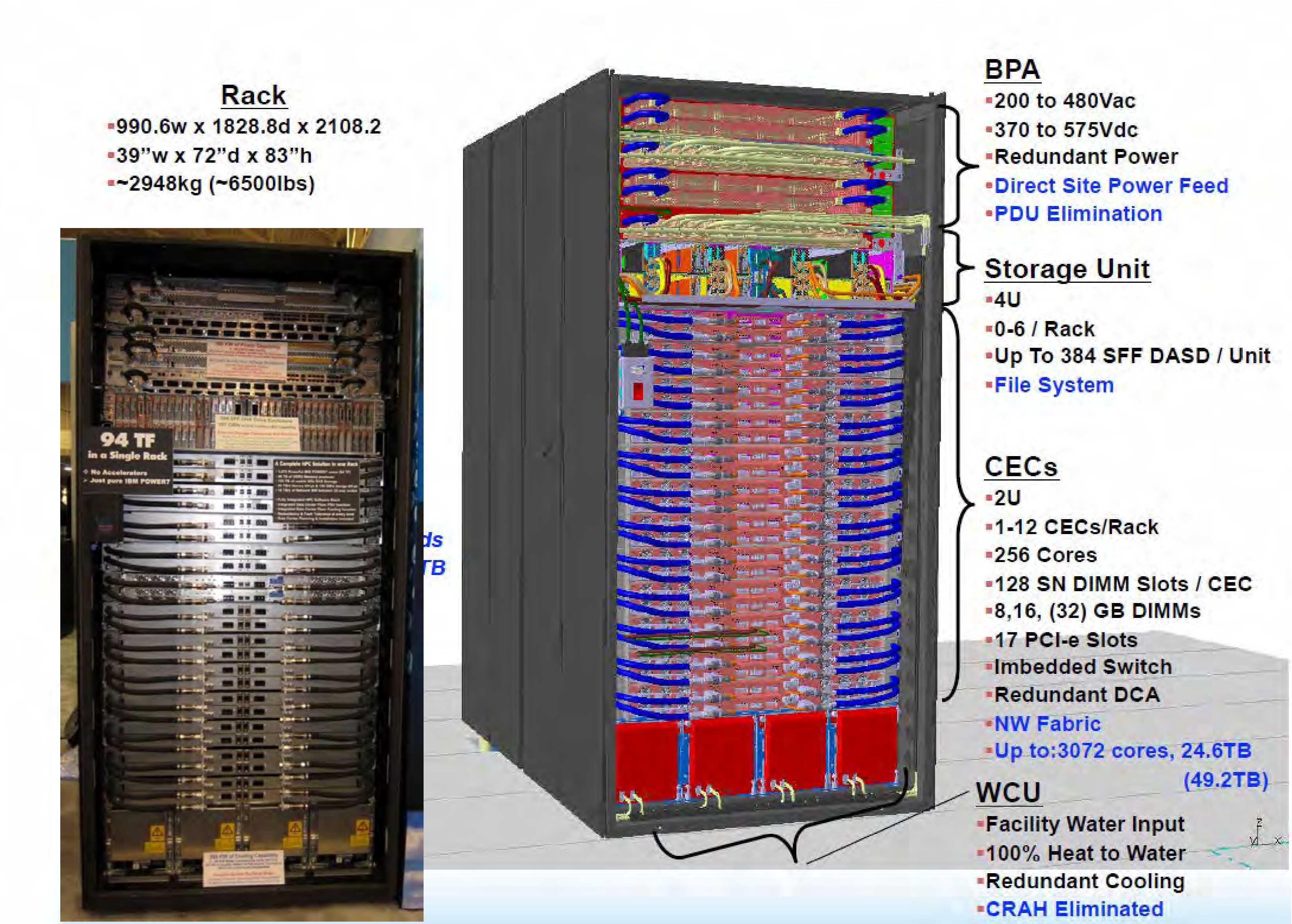
Example: blue waters by IBM

- 10 PFlop (10**16) peak performance
- 300’000 compute cores = 37’500 CPU chips = 9375 QCM = 1172 drawers = 98 racks
- 800W / QCM 7.5 MW in CPUs
- New building completed
- 24 transformers@2 MW



- http://www.ncsa.illinois.edu/Bl

Blue Waters (cont'd)



Overview of HPC Cooling Systems

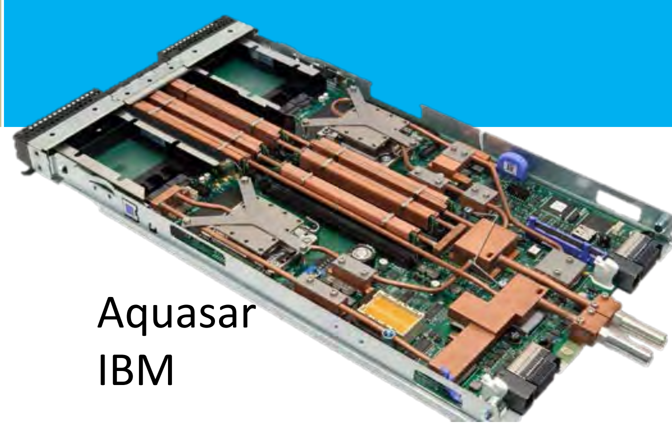
Air cooling

- Very low HTC
- Very low chip uniformity
- Large heat sinks
- Multiple air ducts in Datacenter
- Noisy
- Expensive maintenance
- Complex air management

Water cooling

+ Less fans/ducts
+ Better HTC
+ Smaller heat sinks
+ Possible heat recovery

- Large Pumps

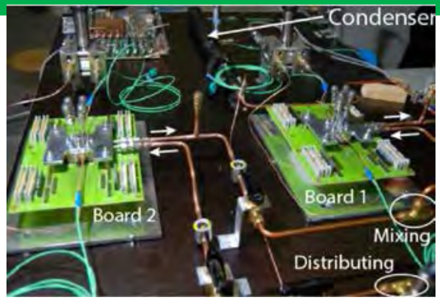


Aquasar
IBM

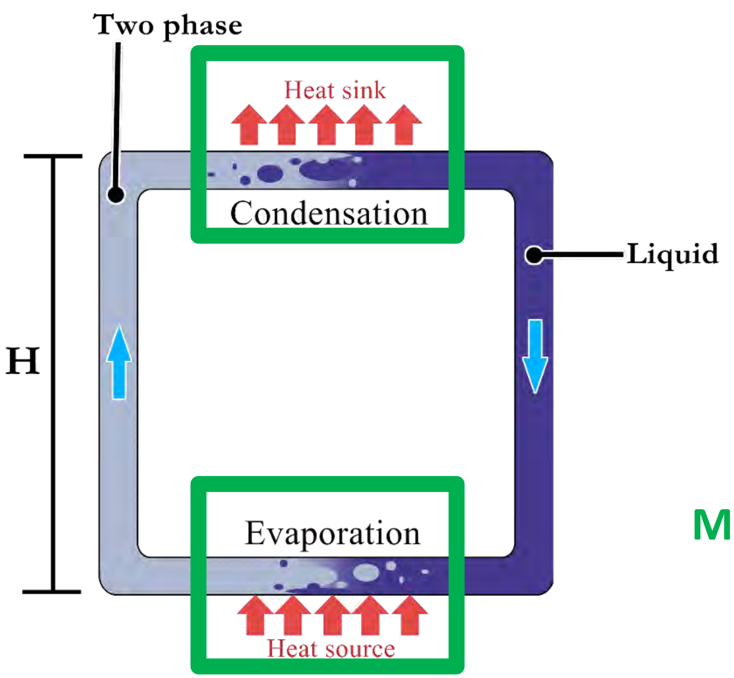
Two phase cooling

+ Smaller pump
+ Higher HTC
+ Better chip uniformity
+ Isothermal coolant
+ Good hot spot cooling
+ Possible heat recovery

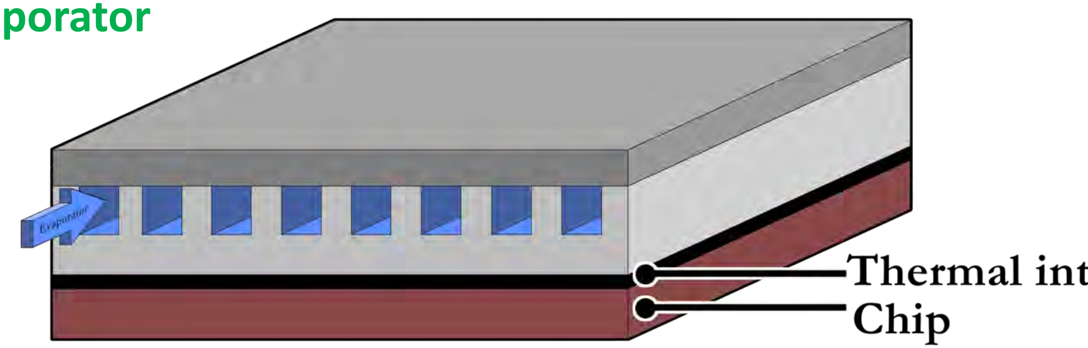
- Low pump efficency and reliability



Proposed Cooling: Thermosyphon



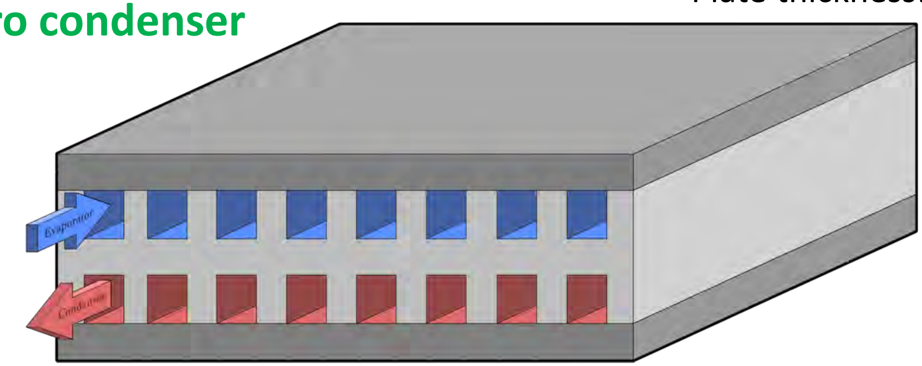
Micro evaporator



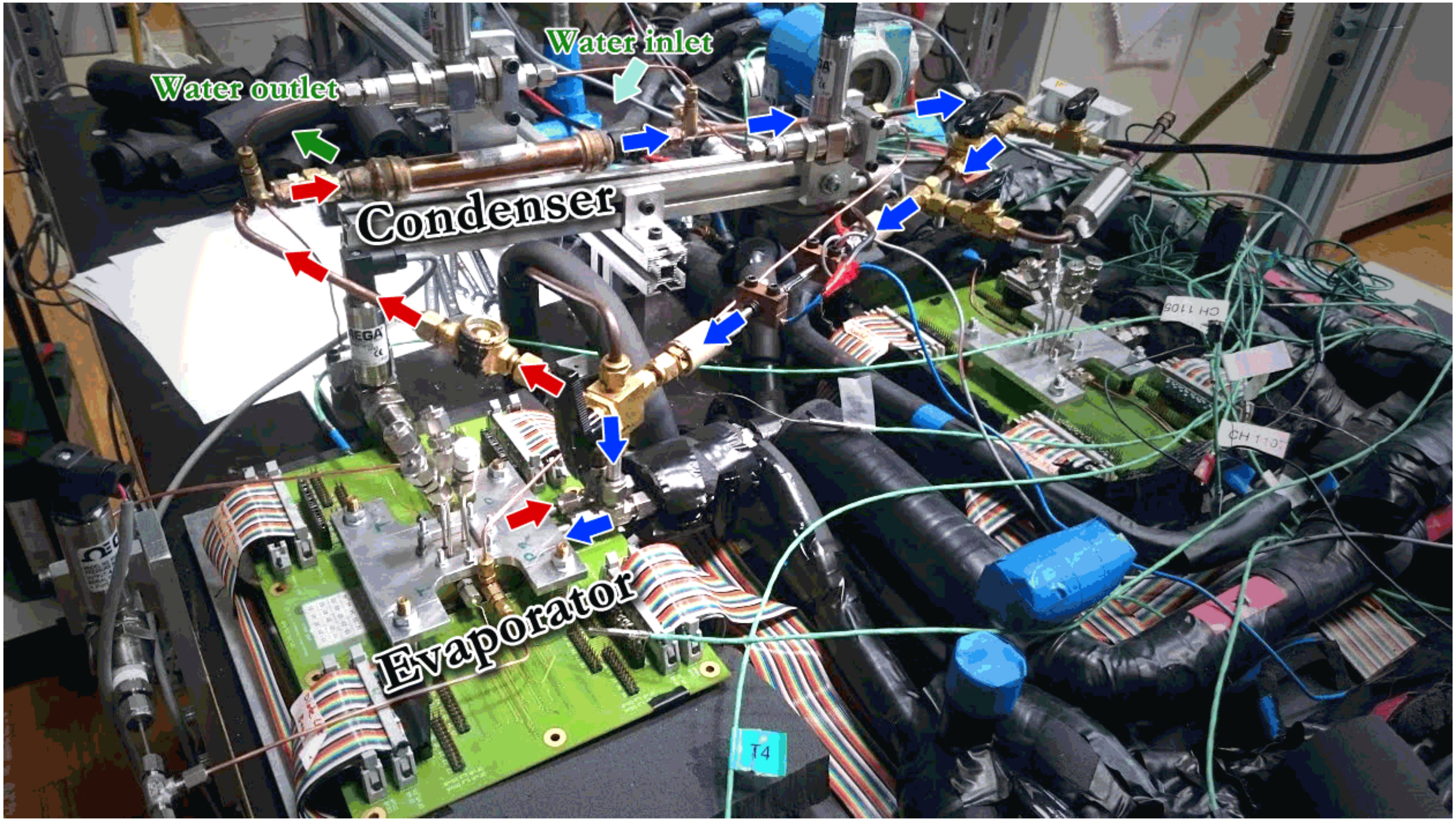
Order of magnitude:

Channel width: 0.17 [mm]
Channel height: 1.7 [mm]
Thermal interface: 80 [μm]
Plate thickness: 2 [mm]

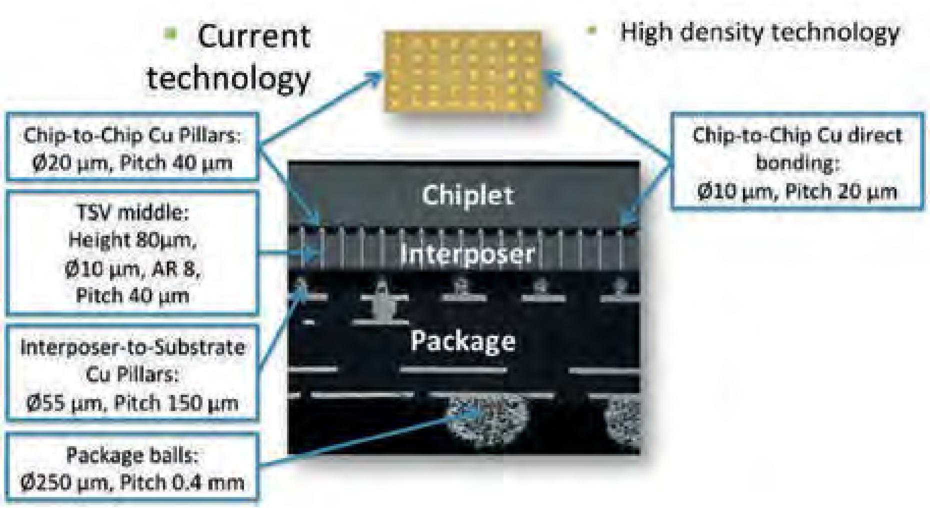
Micro condenser



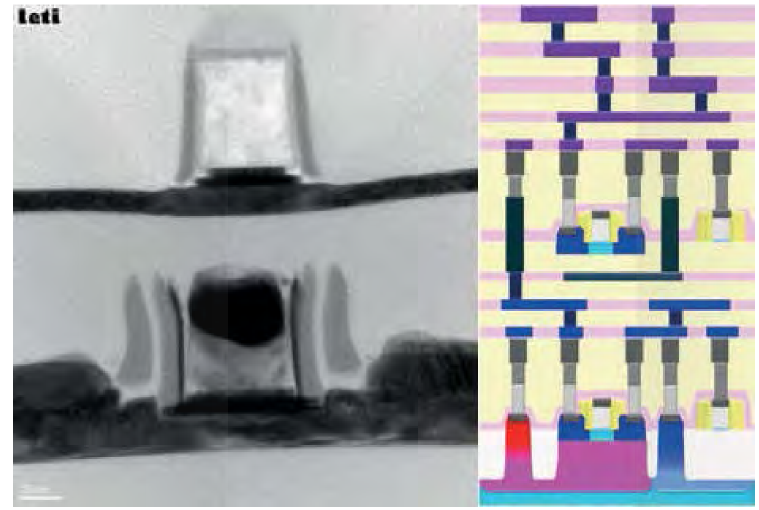
Thermosyphon Experim. Setup at EPFL



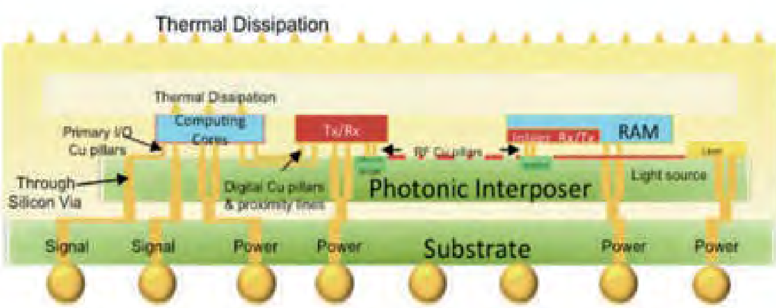
Entering into the third dimension



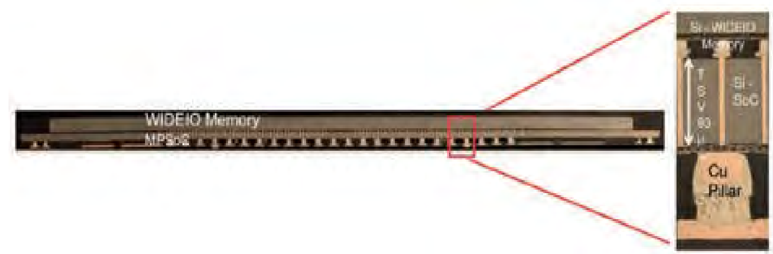
3D interconnect technology



Monolithic 3D devices: transistors are built on top of each other



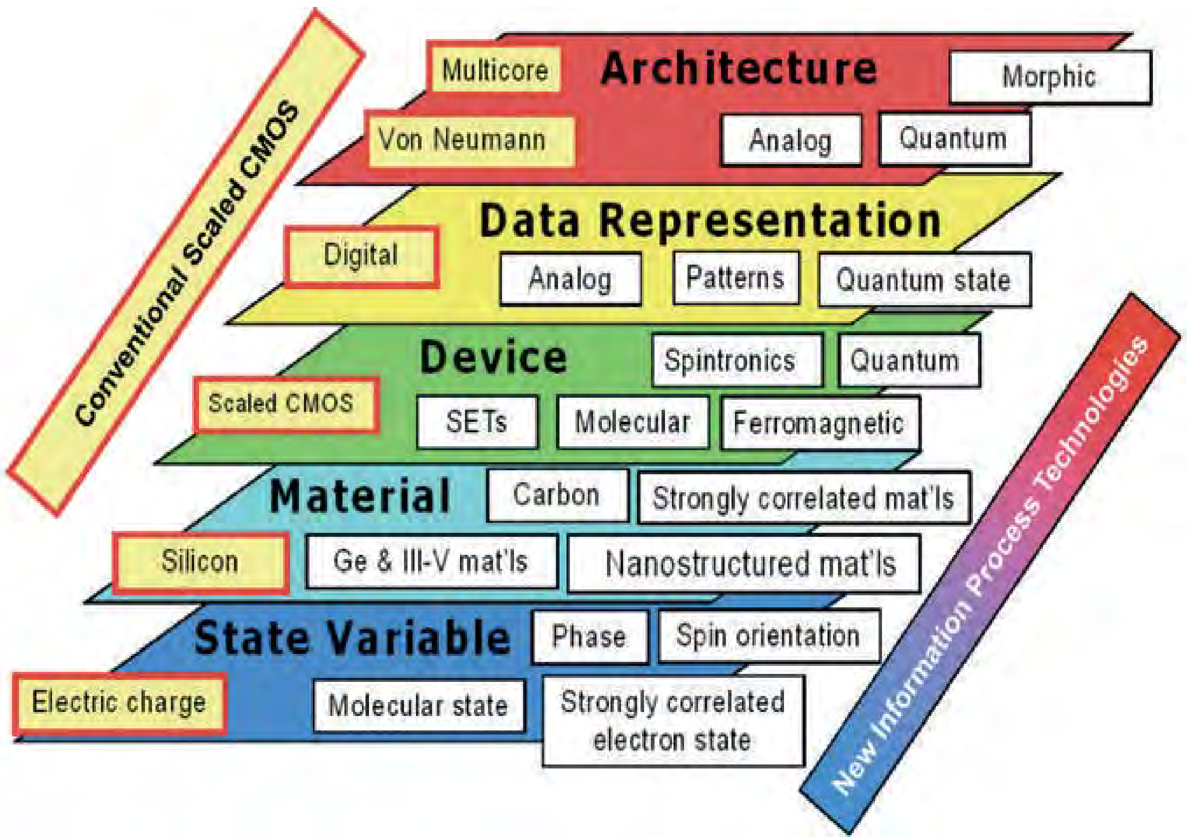
Compute module using photonic interconnect between chiplets



A Wide I/O memory stacked on top of a MPSoC

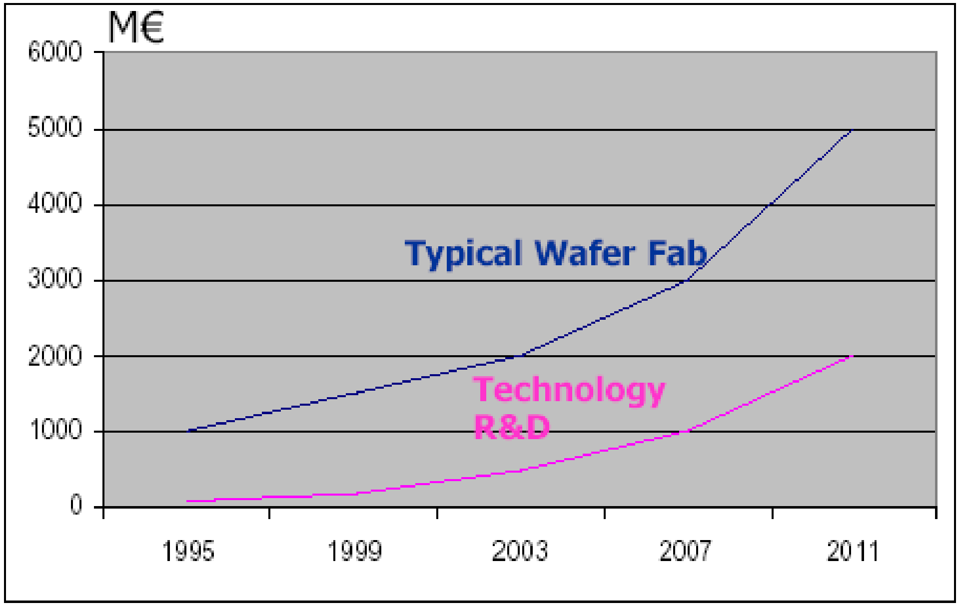
Do not forget···memory device technology

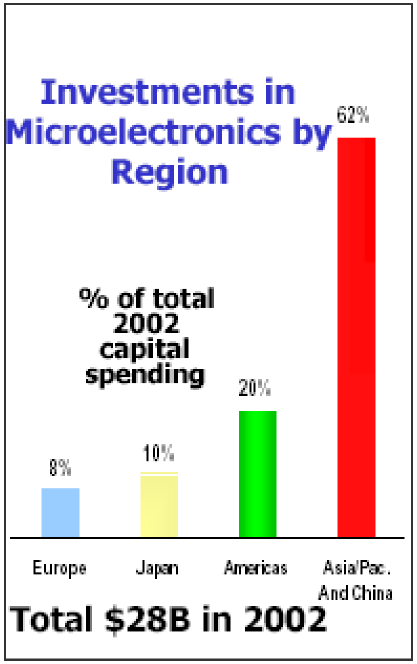
- Potential performance stagnation in the coming years?



Leadership and Competitiveness

- Europe needs to quickly fill the gap on IP architectures and Computer Science
- Maybe is too late…





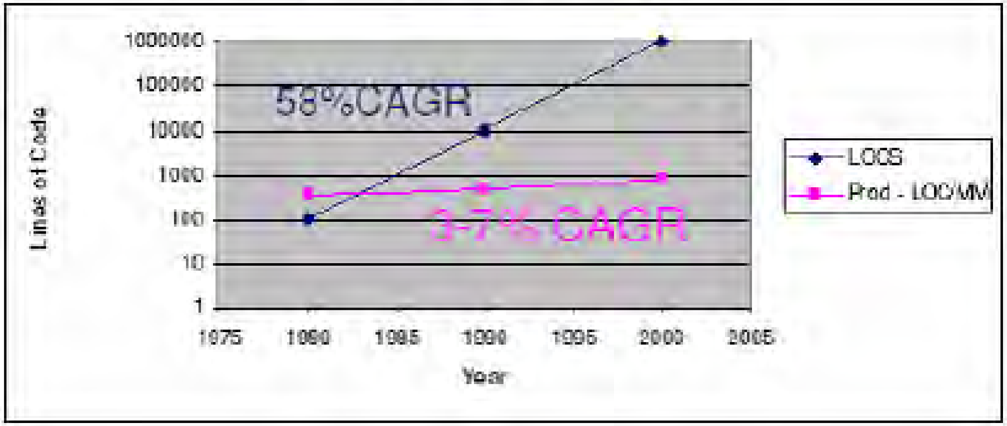
The Twilight of Moore's Law: Economics

- Market volume wall
  - only the largest volume products will be manufactured with the most advanced technology

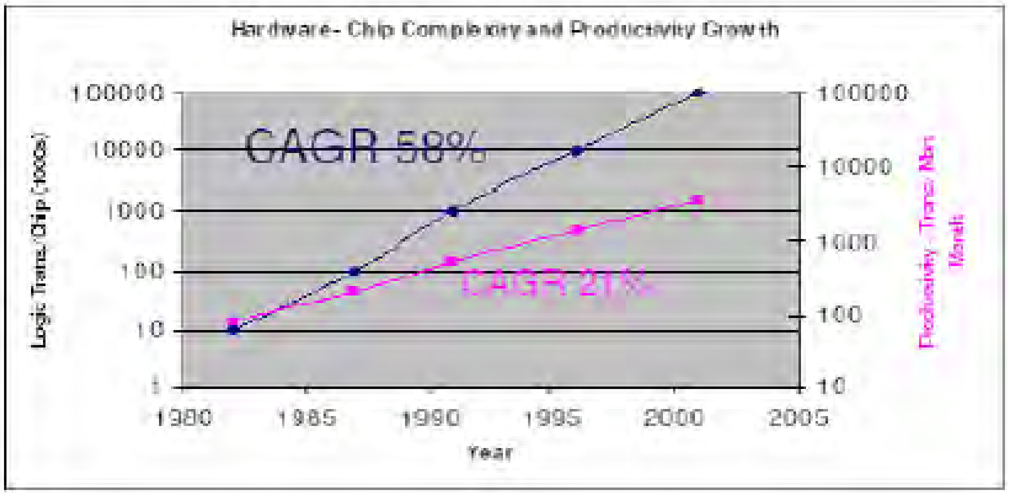
130nm	90nm	65nm/55nm	45/40nm	32/28nm	22/20nm
Altis Semiconductor					
Dongbu Hitek	Dongbu Hitek				
Freescale	Freescale				
Fujitsu	Fujitsu				
Globalfoundries	Globalfoundries	Freescale			
Grace Semiconductor	Grace Semiconductor	Fujitsu			
IBM	IBM	Globalfoundries			
Infineon	Infineon	IBM			
Intel	Intel	Infineon	Fujitsu		
Panasonic	Panasonic	Intel	Panasonic		
Renesas (NEC)	Renesas (NEC)	Panasonic	Globalfoundries		
Samsung	Samsung	Renesas (NEC)	IBM		
Seiko Epson	Seiko Epson	Samsung	Intel		
SMIC	SMIC	SMIC	Renesas (NEC)	Globalfoundries	
Sony	Sony	Sony	Samsung	Intel	
ST Microelectronics	ST Microelectronics	ST Microelectronics	SMIC	Panasonic	Globalfoundries
Texas Instruments	Texas Instruments	Texas Instruments	ST Microelectronics	Samsung	Intel
Toshiba	Toshiba	Toshiba	Toshiba	ST Microelectronics	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	ST Microelectronics
UMC	UMC	UMC	UMC	UMC	TSMC

Complexity vs productivity growth

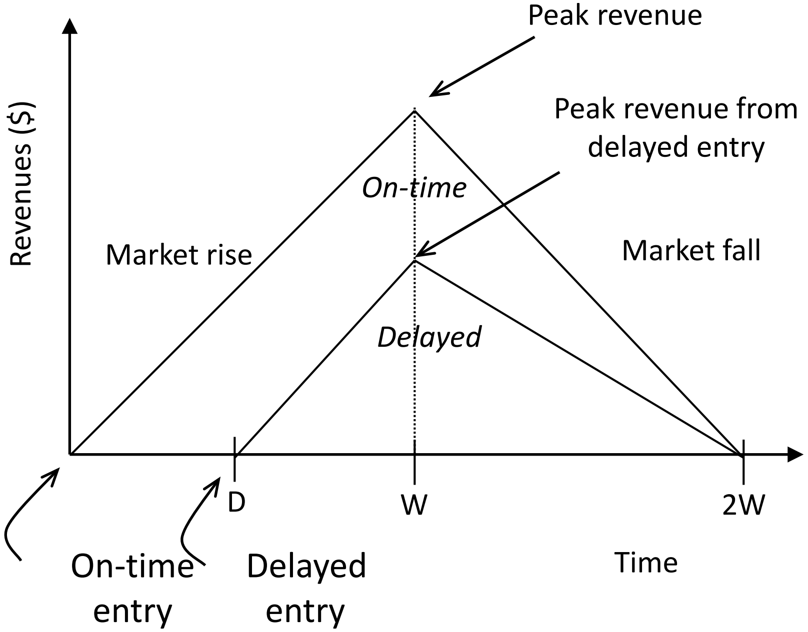
SW complexity & productivity growth



HW complexity & productivity growth



Losses due to delayed market entry



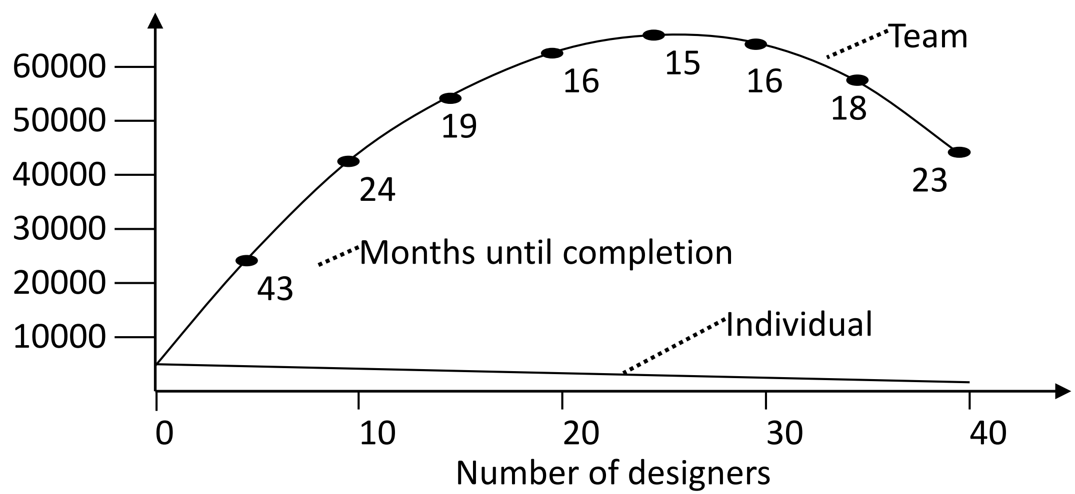
- Simplified revenue model
  - Product life = 2W, peak at W
  - Time of market entry defines a triangle, representing market penetration
  - Triangle area equals revenue
- Loss
  - The difference between the on-time and delayed triangle areas

–Lifetime 2W=52 wks, delay D=4 wks
–(4*(3*26 –4)/2*26^2) = 22%
–Lifetime 2W=52 wks, delay D=10 wks
–(10*(3*26 –10)/2*26^2) = 50%
–Delays are costly!

The mythical man-month

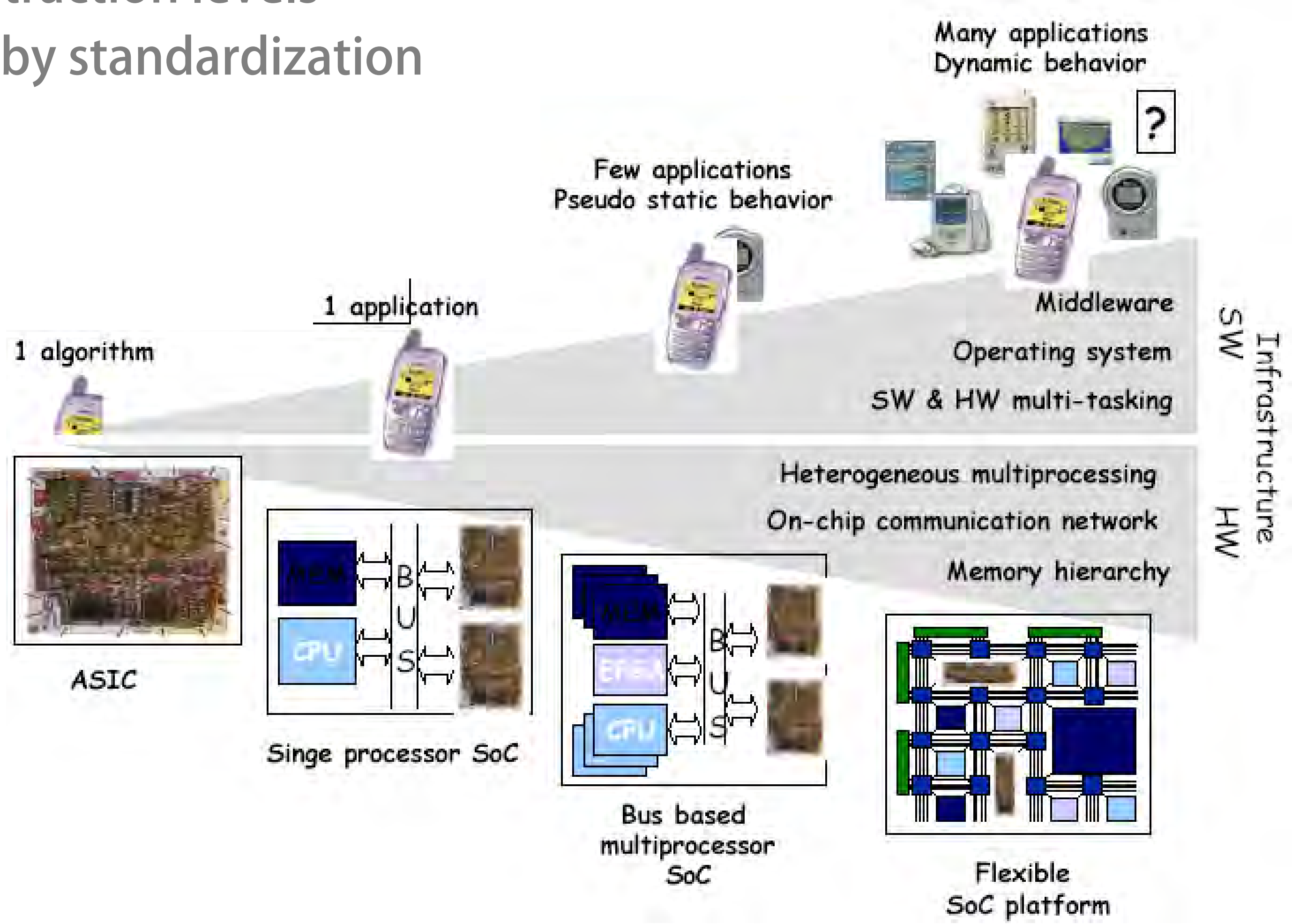
- The situation is even worse than the productivity gap indicates
- In theory, adding designers to team reduces project completion time
- In reality, productivity per designer decreases due to complexities of team management and communication
- In the software community, known as “the mythical man-month” (Brooks 1975)
- At some point, can actually lengthen project completion time! (“Too many cooks”)

- 1M transistors, 1 designer=5000 trans/month
- Each additional designer reduces for 100 trans/month
- So 2 designers produce 4900 trans/month each



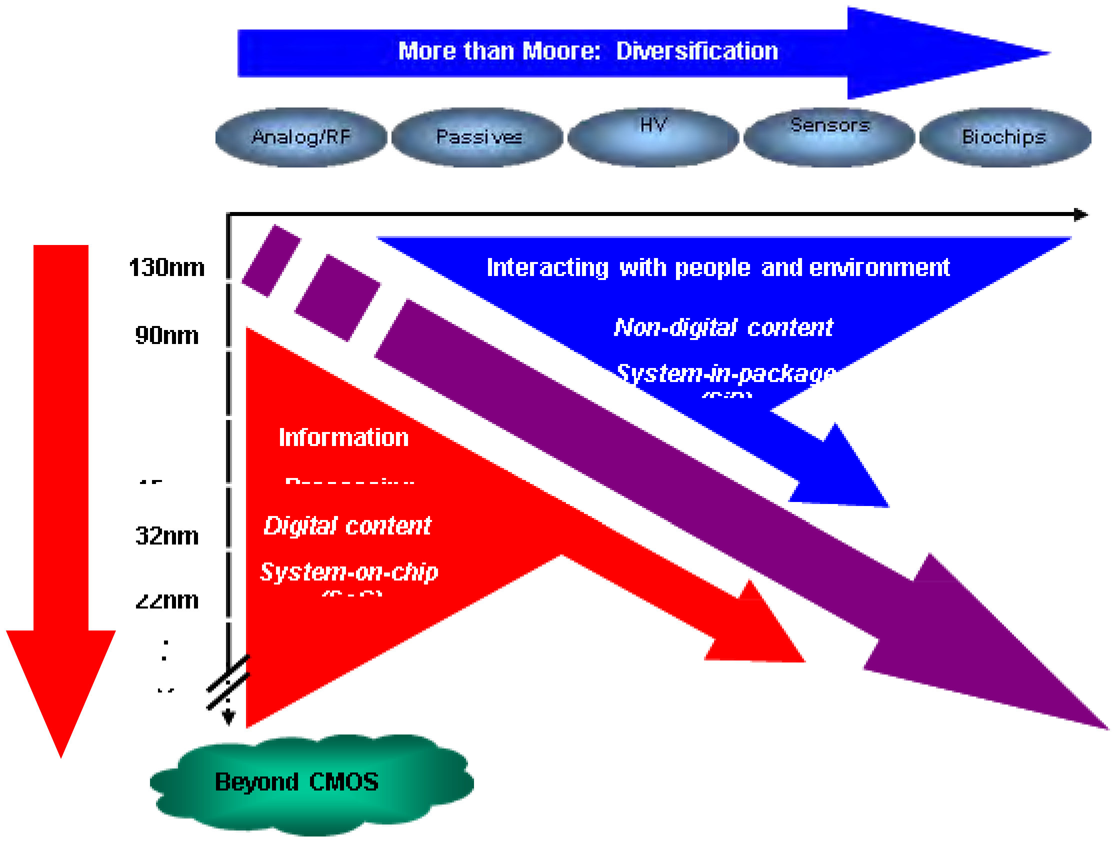
Platform based design

- Design methodology must support re-use
  - at high abstraction levels
  - supported by standardization

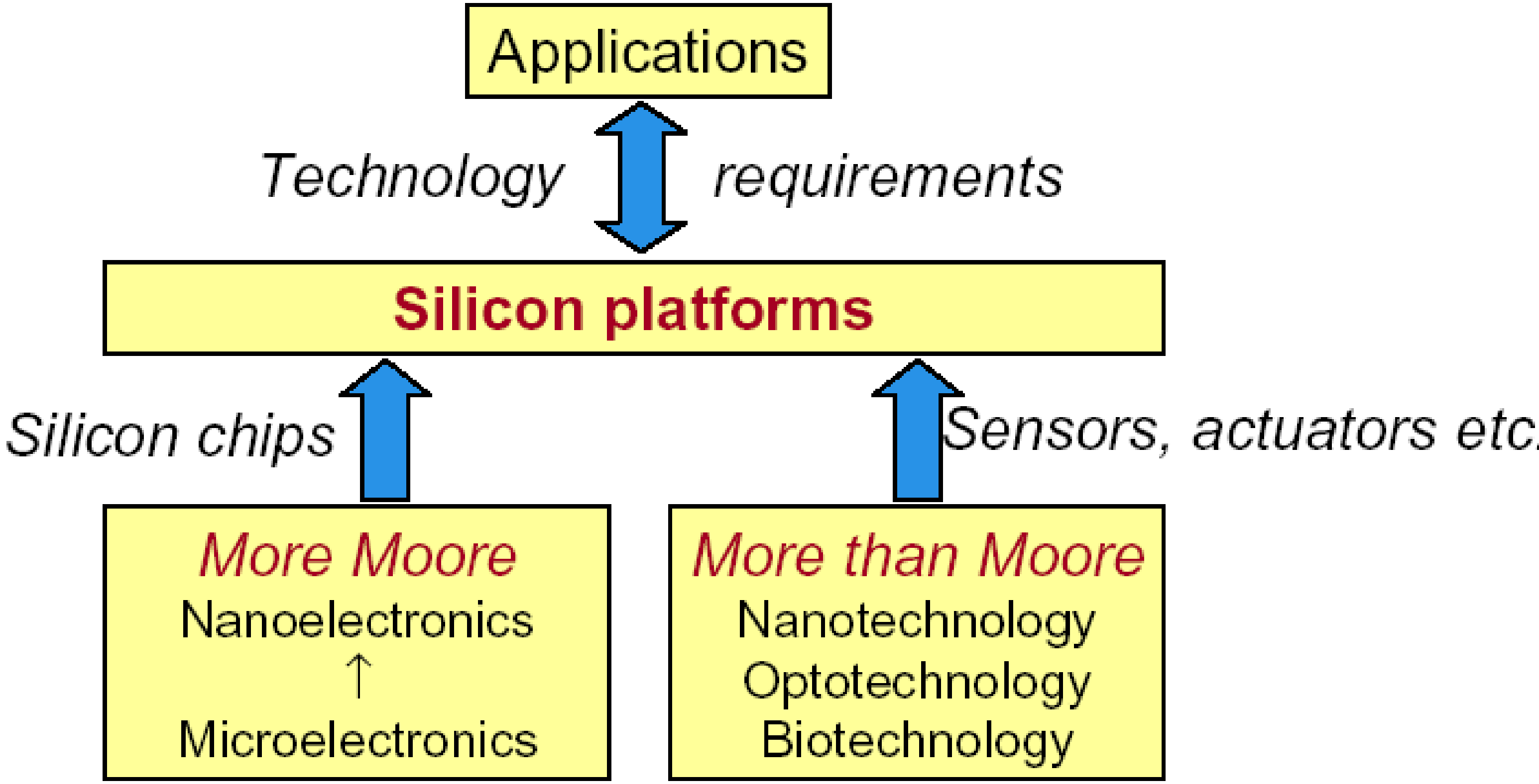


More – than - Moore

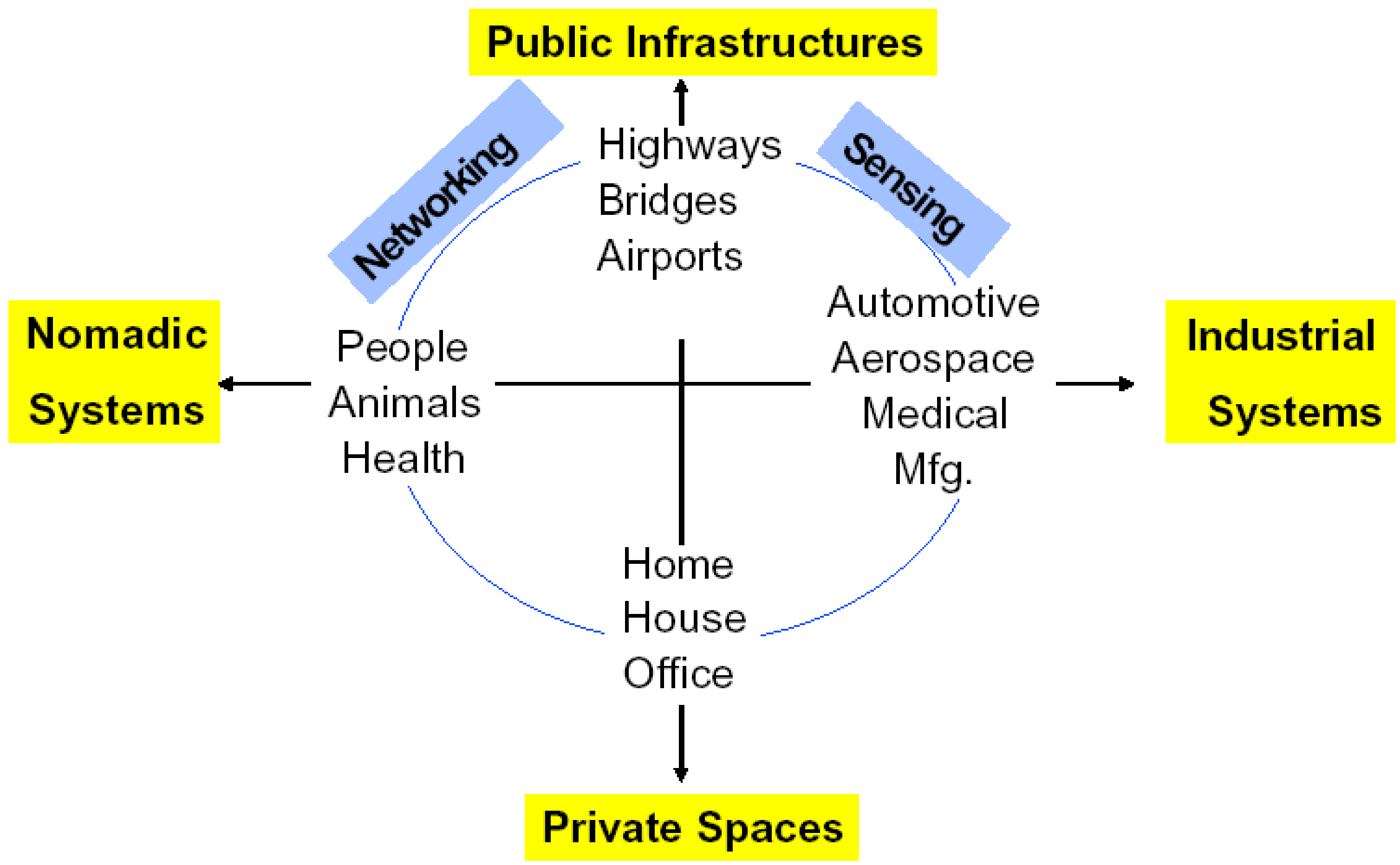
- The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”)



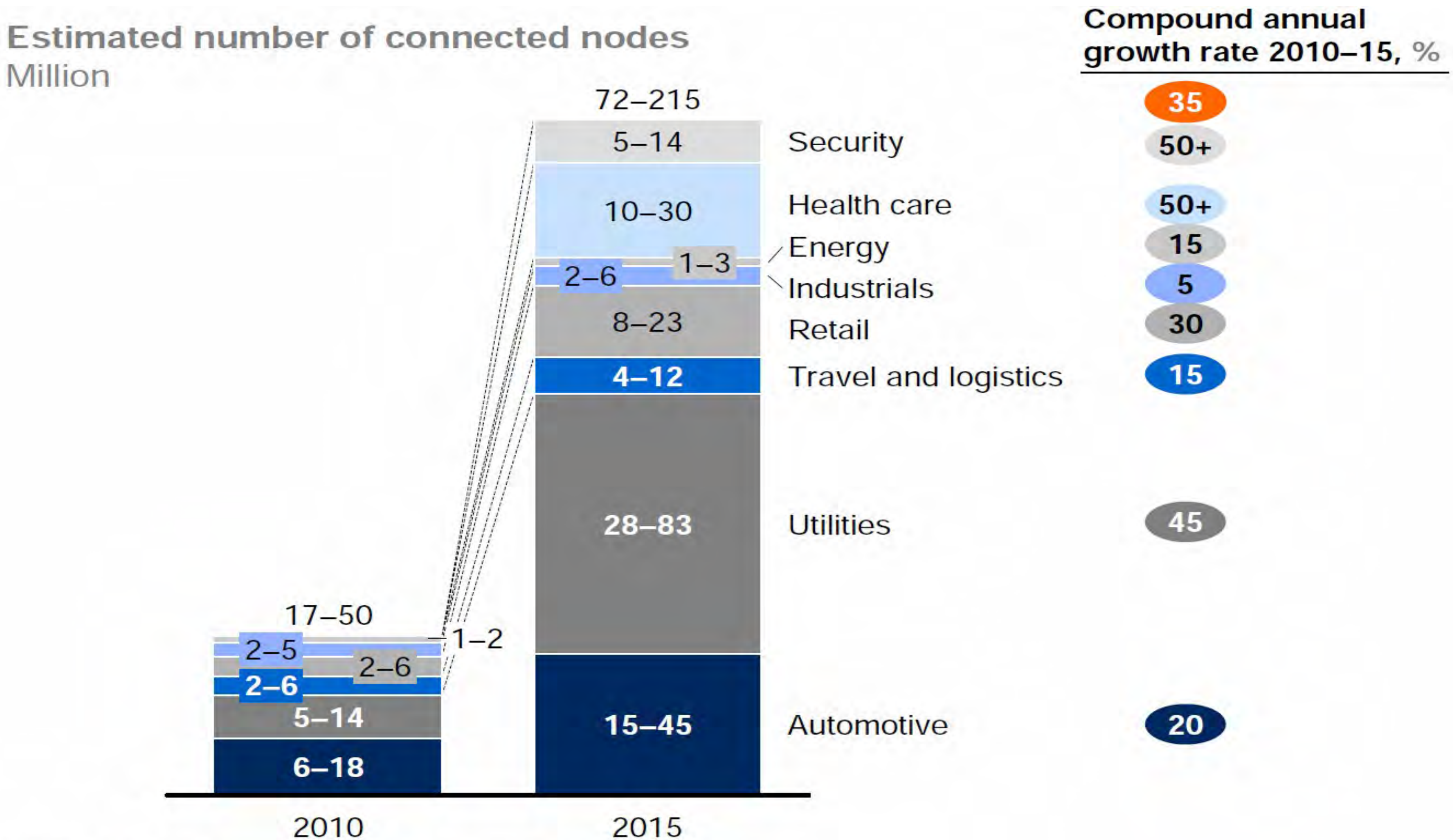
Applications in 2020: Technology requirements



Application contexts of embedded systems



Growth of connected nodes

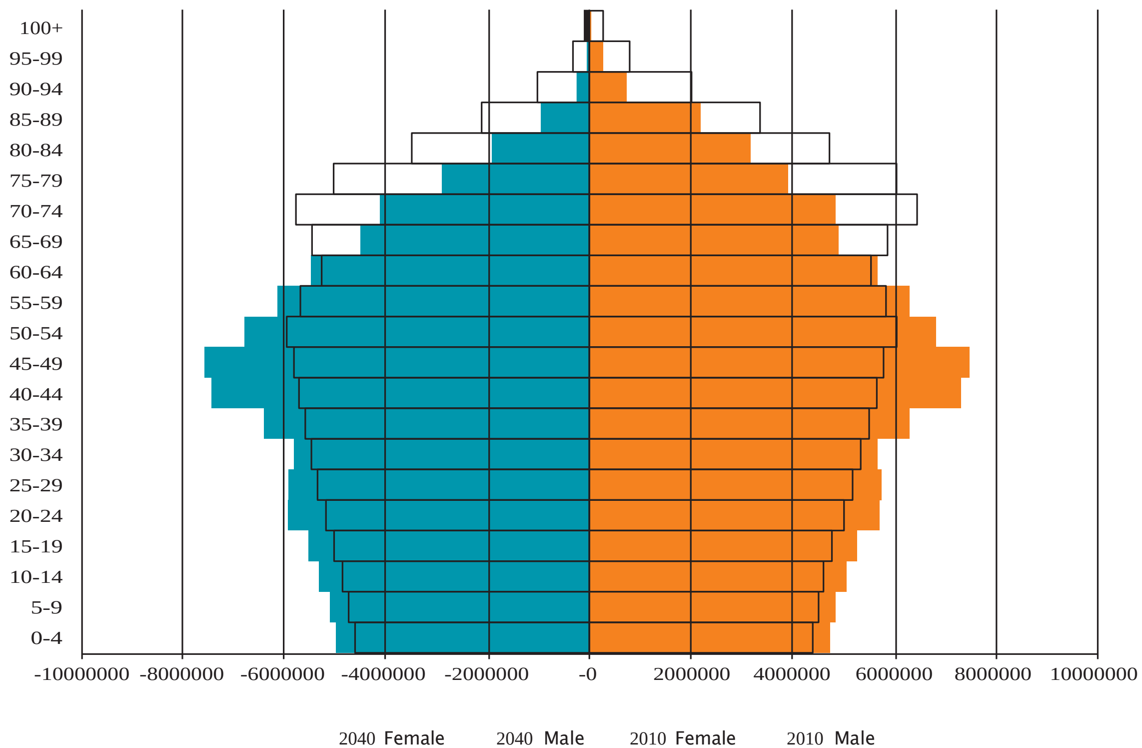


NOTE: Numbers may not sum due to rounding.
SOURCE: Analyst interviews; McKinsey Global Institute analysis

Ambient Assisten Living (AAL)

- Ageing at home vs working forever?

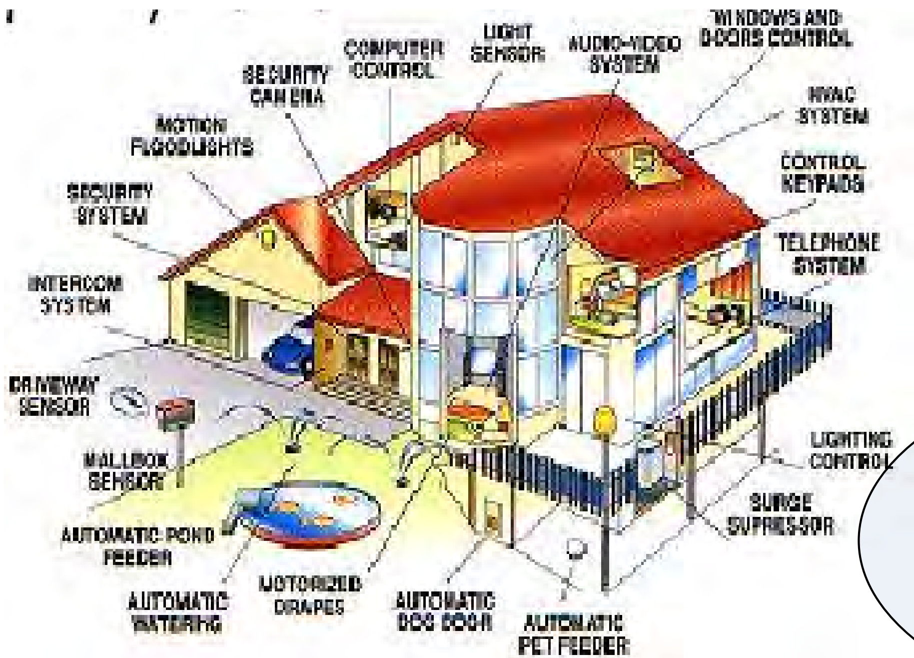
Population Structure: Western Europe, 2010 vs 2040 (projected)



Note: "Western Europe" here defined as EU-15 plus UK, CH, NO and smal adjacent islands and territories.
Source: US CENSUS IDB, available at http://www.census.gov/population/international/data/idb/informationGateway.php

Networked Embedded Intelligence

- Enabling transportation, infrastructure industries
- Leading to revolutions like the digital home
- Turning ambient dreams into reality
- Enabling sensor networks improving our quality of life



Ubiquitous
Low Power
High performance
Interconnected

Long term technology trends

- System-on-Chip (SoC)
  – Focus on full integration and lowest cost per transistor
- System-in-Package (SiP)
  – Focus on lowest cost per function and for total system
- Complementing, not competing architectures
- Each requiring a different industrial approach
  – Advanced R&D / knowledge needed
  – Different manufacturing competences

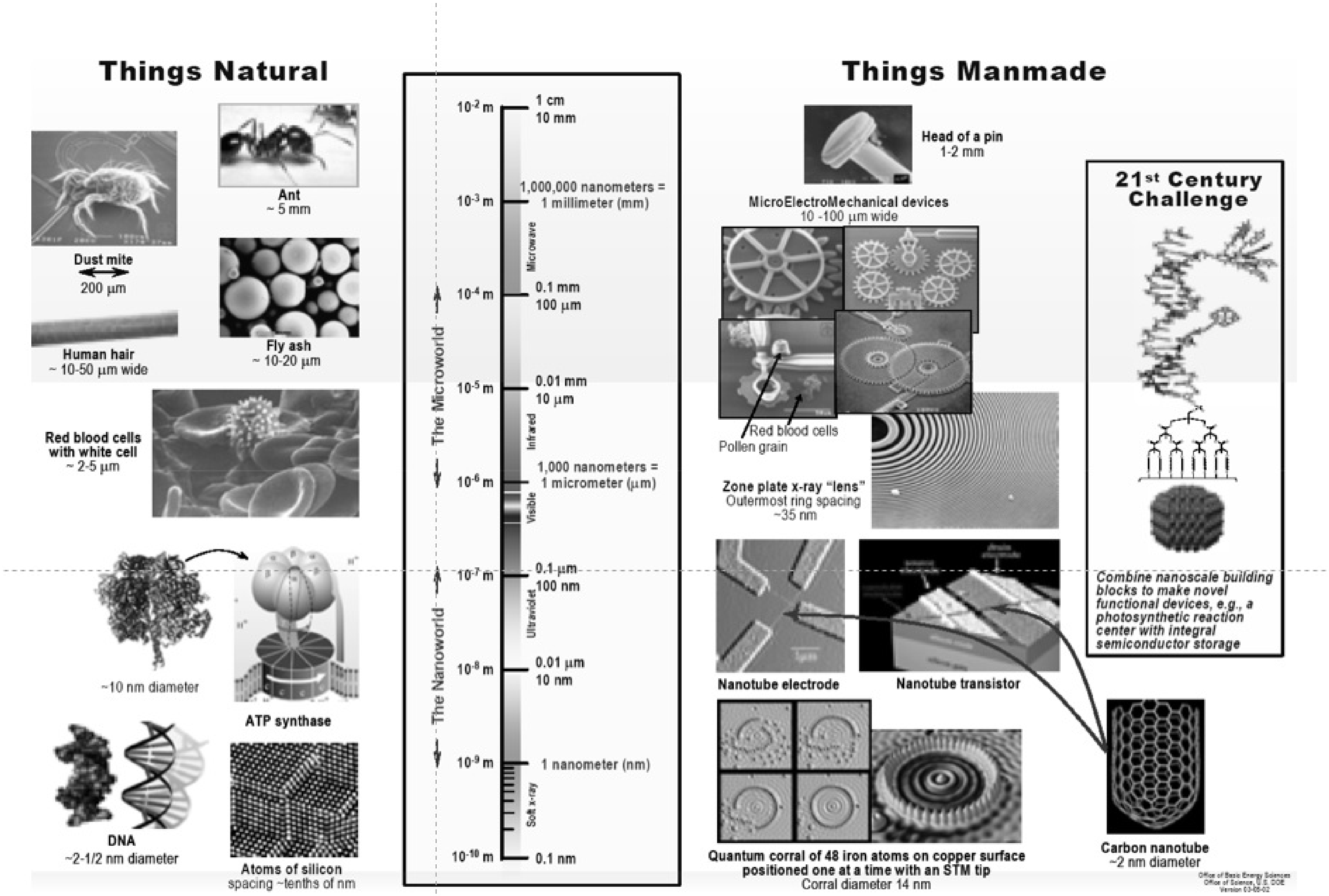
Embedded Systems 10 years from now

- Networked: from working in isolation towards communicating, networked, distributed solutions
- Secure: threatened by enormous security issues, challenging its technical and economical viability
- Complex:
  - Giga-complexity enabled by nano-technology
  - Complex through heterogeneity
  - Transducer devices
    - Sensors: Biosensors, MEMS, NEMS
    - Actuators/Interactive Screens/Displays
    - Speech input device/Handwriting input devices
  - Computing devices: more software than hardware, application domain specific, reconfigurable
  - Communication: protocols, standards, RF
- Low power: scavenging power

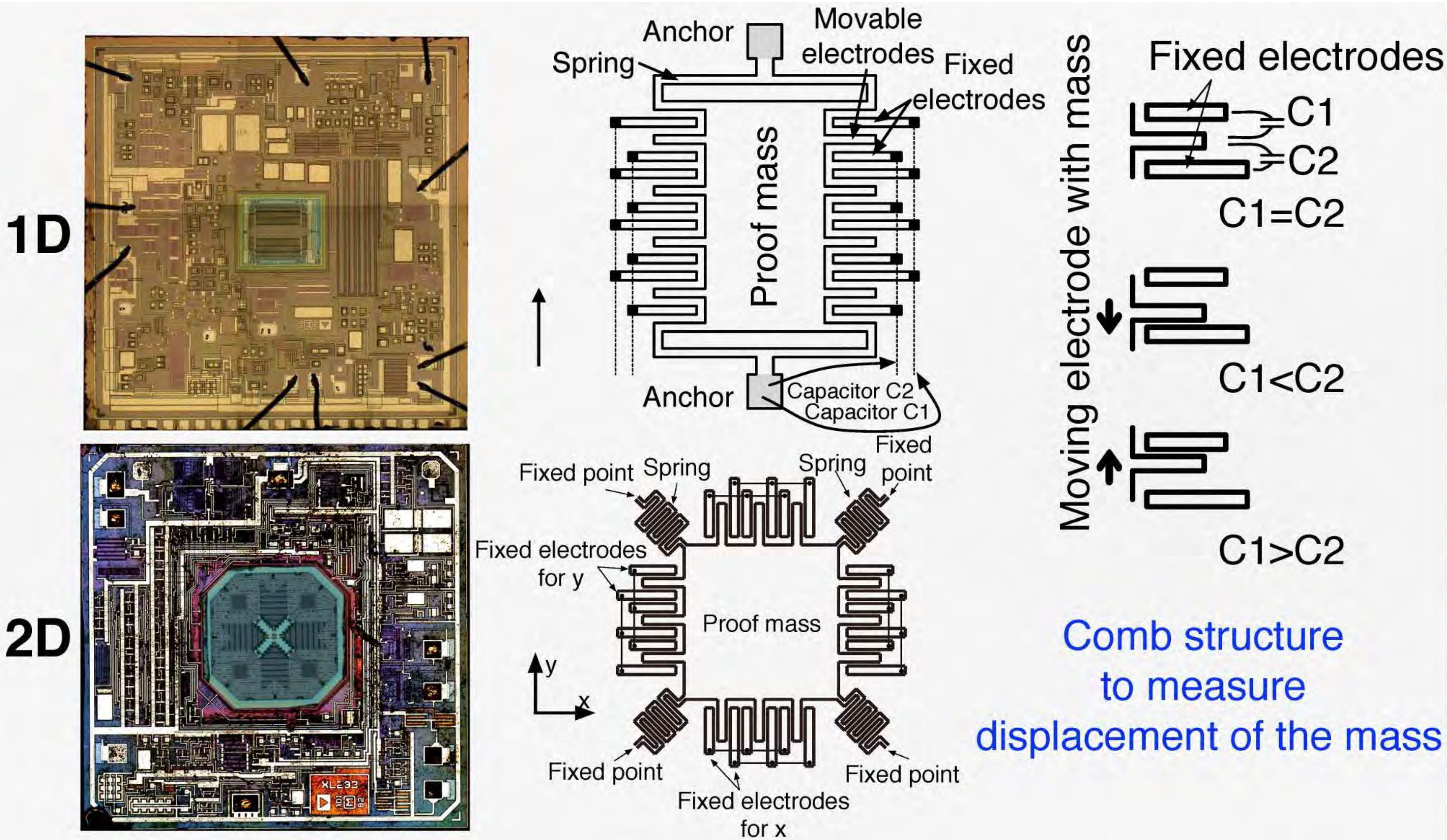
What is a MEM?

- MEMS = Micro-Electo-Mechanical Systems
  - creation of 3-dimensional structures using integrated circuits fabrication technologies and special micromachining processes
  - typically done on silicon or glass (SiO2) wafers
- MEMS Devices and Structures
  - transducers
  - microsensors and microactuators
    - mechanically functional microstructures
  - microfluidics: valves, pumps, flow channels
    - microengines: gears, turbines, combustion engines
- Integrated Microsystems
  - integrated circuitry and transducers combined to perform a task autonomously or with the aid of host computer
  - MEMS components provide interface to non-electrical world
    - sensors provide inputs from non-electronic events
    - actuators provide outputs to non-electronic events

What is the size we are talking about?

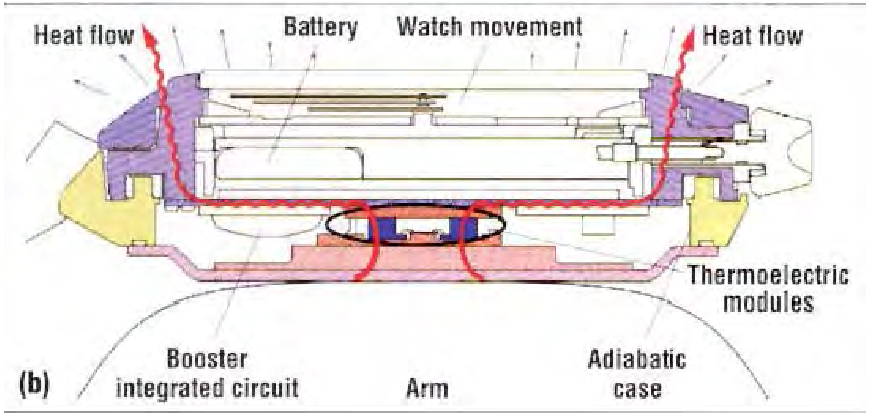


Inside an accelerometer

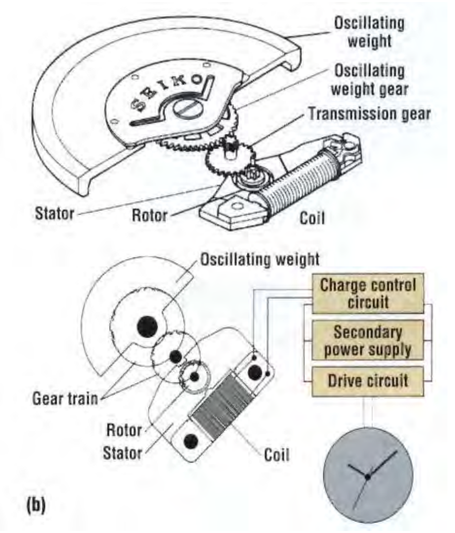


Crazy ideas on energy scavenging

- Objects with temperature gradients create energy
  - –ATMOS clock
  - –Seiko watch
  - –Driving motes at Alcoa

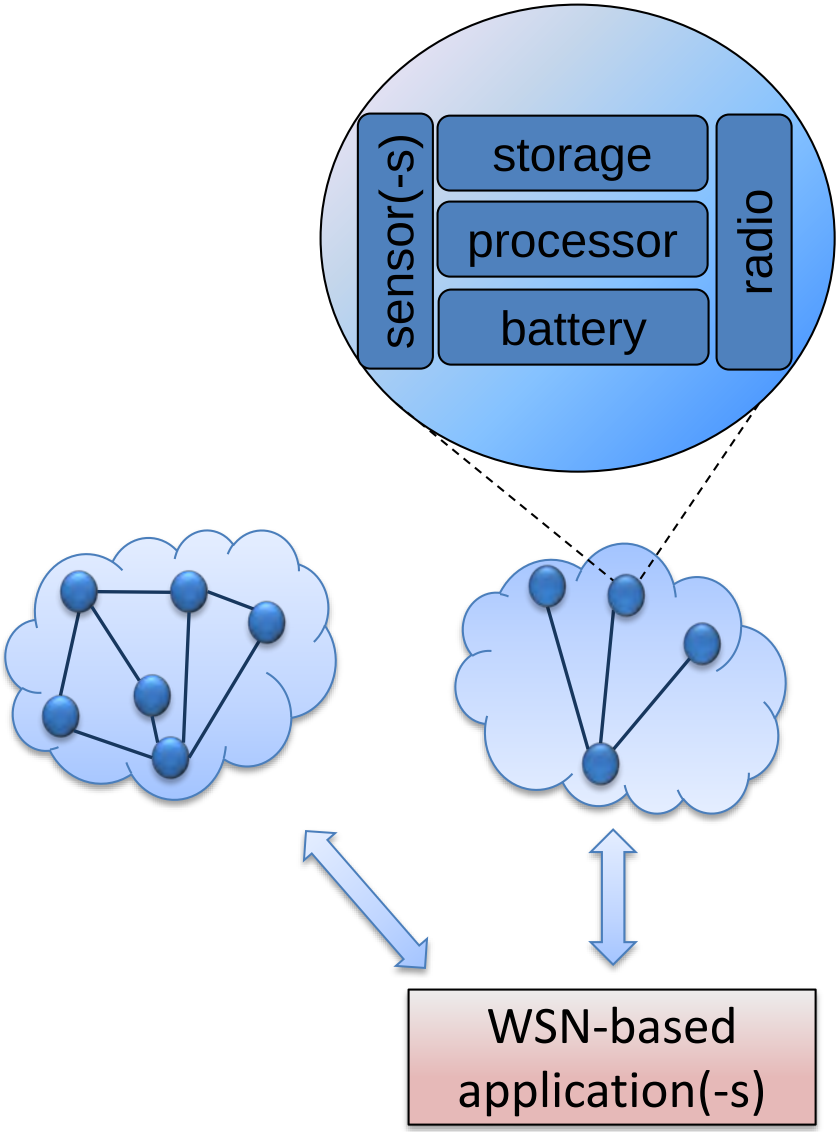


- Vibrations
  - –Self winding watches
  - –Produces 5microwatts on average when worn 1milliwatt when forcibly shaken



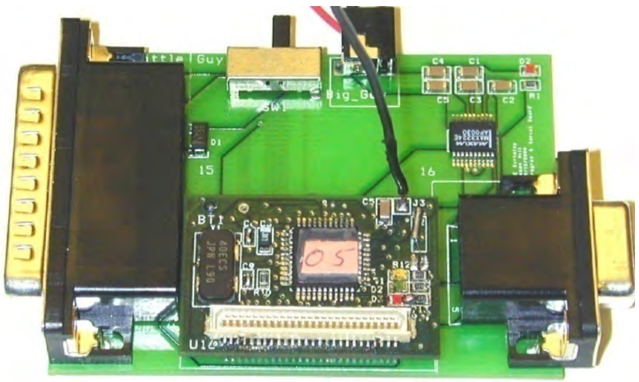
Wireless sensor node

- small (battery-powered) devices
  - sensing local conditions
  - typically with limited resources
- forming "nodes" within a wireless network
  - covering region / object of interest
- enabling (new) applications
  - based on sensor data collection, fusion, reasoning, and response

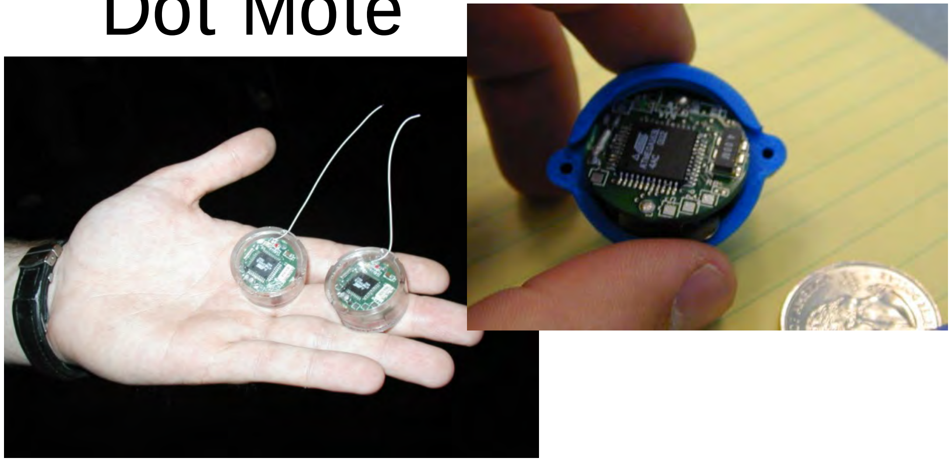


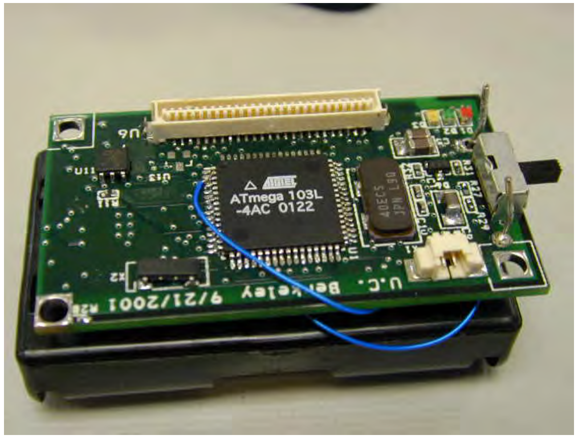
Examples of Wireless Sensor Nodes

Rene Mote



Dot Mote



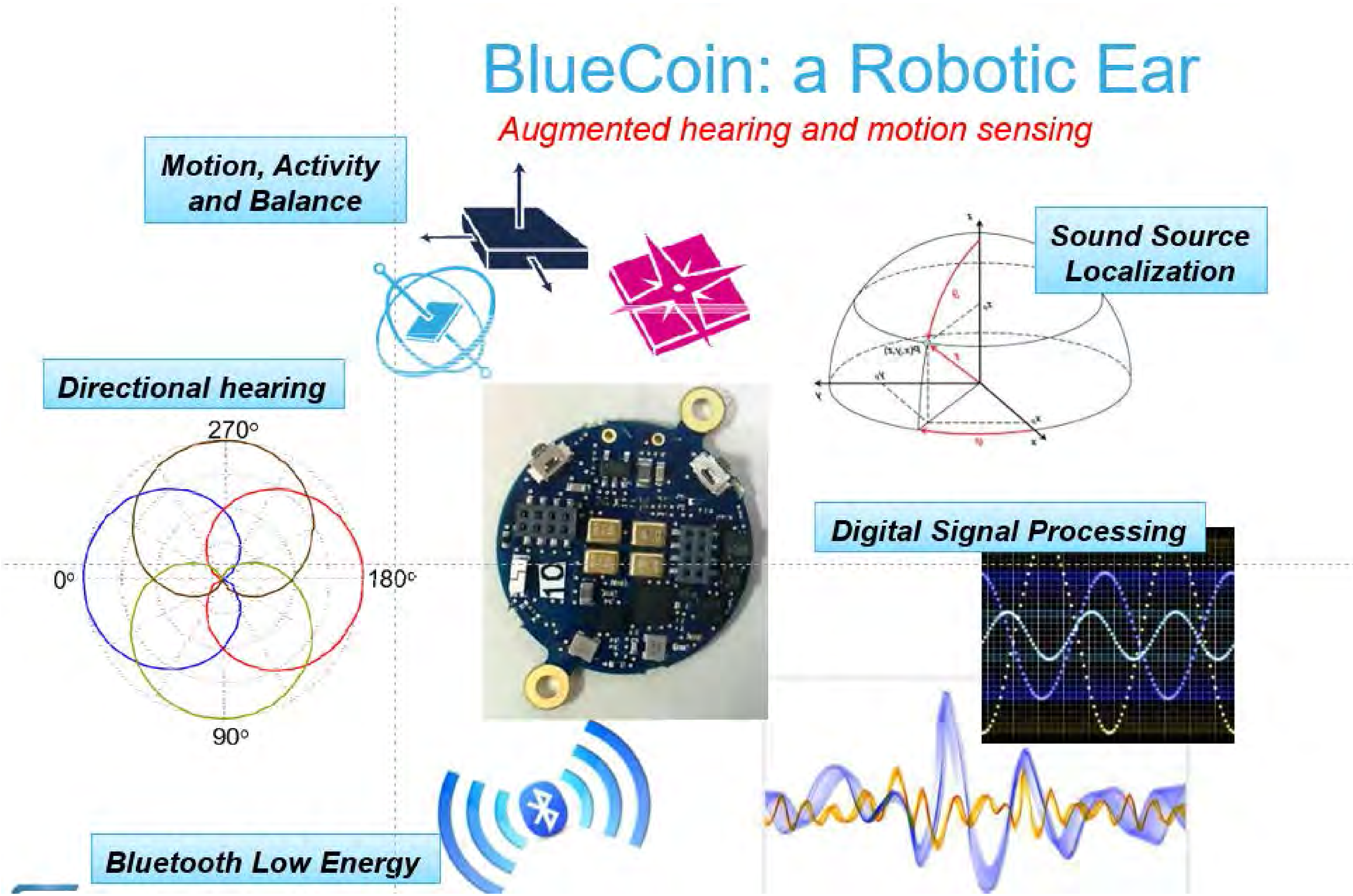


MICA Mote

BSN Mote

weC Mote

Example of platform: bluecoin by STM

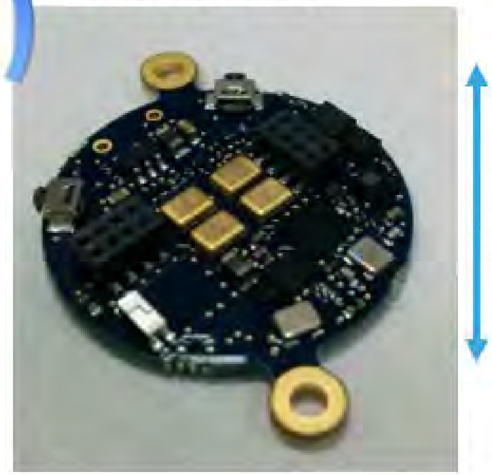


Example of platform: bluecoin by STM

- Features
  - Advanced audio processing
    - Sound Source Localization
    - Beamforming
  - Wide band audio over BLE (BlueVoice)
  - Sensor fusion
    - Inertial, environmental, acoustic.
  - Complete development kit
    - Battery holder
    - CoinStation
- Main components
  - STM32F446
    - ARM Cortex-M4F@180MHz - 128KB RAM
  - u4 Microphone Array (4x MP23DB01MM)
  - Bluetooth-Low-Energy radio (BlueNRG-MS)
    - Bluetooth 4.1, multiple role simultaneously
  - 6+3 axis inertial module (LSM6DS3+LIS3MDL)
  - Absolute pressure sensor (LPS25HB)

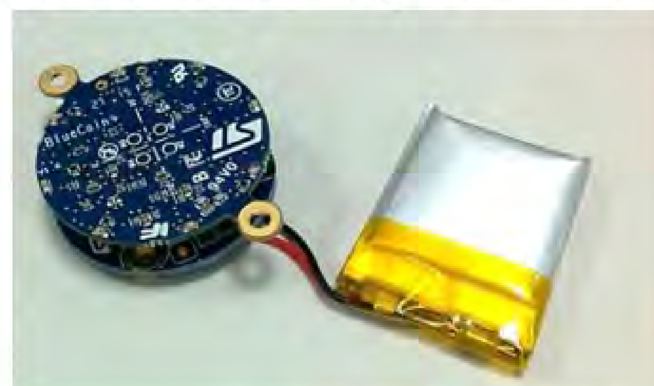
BlueCoin+

Bottom view

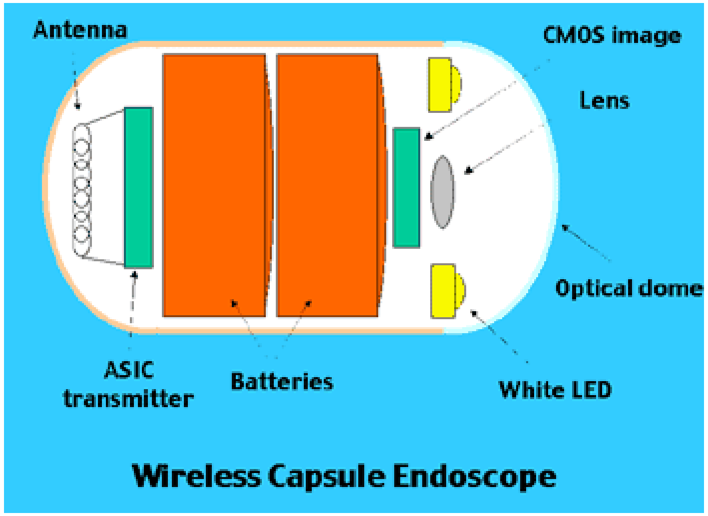


25mm

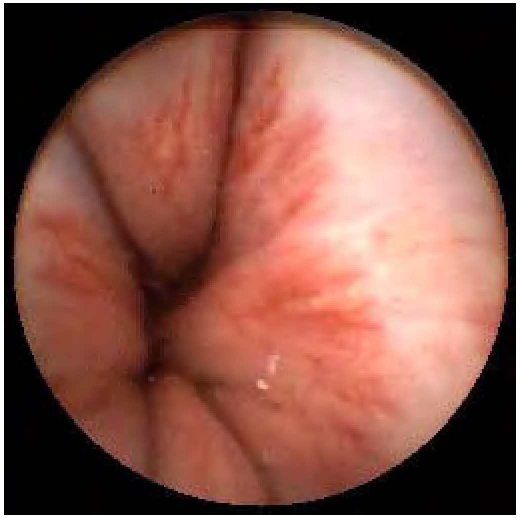
Top view + Coin battery holder + battery



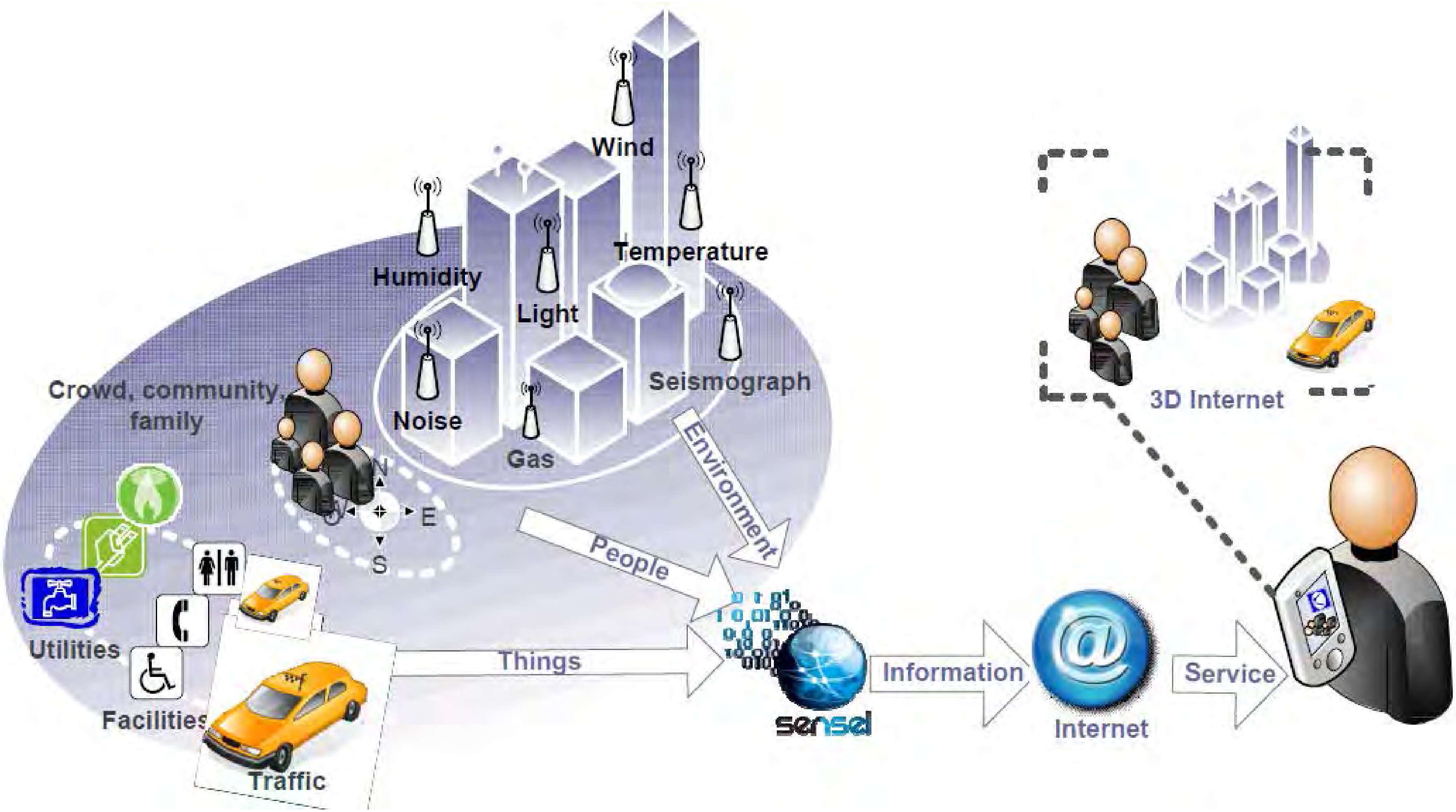
Example: Pill camera



Distal esophagus with edema and erythema. Geographic ulceration suggestive of Barret's Esophagus.



Example of use: intelligent cities (SoS)



Examples: Social network adapted to elders

- Aging population
  - Healthcare cost could double among EU member states by 2060
- eHealth Action Plan 2012-2020
  - ICT solutions should be applied to health and healthcare systems to increase their efficiency, improve quality of life and unlock innovation in health markets
- People are willing to actively participate in decisions that concern their medical condition
  - From 2007. to 2013. percentage of individuals who used Internet for health-related information increased from 24% to 44%
  - Active participation leads to better health outcomes.

Challenge

- Access to medical data provided through patient portals
  - Useful for some patients
  - Require substantial technical knowledge
- Devices used for accessing patient portals
  - Smartphone, tablets, PCs
  - Modern small screen mobile devices are too complex and/or too small for most of them to use
- Bringing ICT solutions closer to elder population
  - it is necessary to address barriers to technology adoption and consequently develop well-designed system that can be used even if the end user is technically illiterate (Independent Age, 2015)

About the speaker

William Fornaciari is Professor at Politecnico di Milano – Dipartimento di Elettronica Informazione e Bioingegneria. He published six books and over 200 papers, collecting 5 best paper awards, one certification of appreciation from IEEE and holds 3 international patents on low power design. Since 1997 he has been involved in 19 EU-funded international projects. In FP7 he has been WP leader for the COMPLEX and CONTREX IP projects, Project Technical Manager of 2PARMA (ranked as success story by the EU) and currently he is Project Coordinator of the HARPA project. In H2020 he is contributing to the following projects started in 2016: MANGO, Antarex, SafeCop and M2DC. He cooperated for around 20 years with the Technology Transfer Center of POLIMI and in 2013 he created a startup company (IBT Solutions srl) candidate to receive the EIT award in 2016. His main research interests cover multi-many core architectures, NoCs, HPC, low power design, software power estimation, run time resource management, wireless sensor networks, thermal management, and EDA-based design methodologies. He is member of the HiPEAC NoE.

THANKS FOR YOUR ATTENTION

ANY QUESTION ?