EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from ACA – Como exam held on 01/07/2013)

Let us consider a computer with a L1 cache and L2 cache memory hierarchy with the following parameters: Processor Clock Frequency = ***1 GHz*** ; Hit Time $_{L1}$ = 1 clock cycle ; Hit Rate $_{L1}$ = 95%; Hit Time $_{L2}$ = 5 clock cycles; Hit Rate $_{L2}$ = 90% ; Miss Penalty $_{L2}$ = 15 clock cycles; Memory Accesses Per Instruction = 78% ; CPI exec = 3

1. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2}$ =

2. How much is the AMAT?

AMAT =

3. How much is the impact on CPU time of the L2 cache with respect to an IDEAL L2 cache?

CPU_{time} =

$CPU_{time\ IDEAL\ L2}$ =

CPU_{time} / $CPU_{time\ IDEAL\ L2}$ =

Let us assume to introduce an L3 cache with Hit time $_{L3}$ = 8 clock cycles and Hit Rate $_{L3}$ = 92%.

4. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2\,L3}$ =

Being L3 the Last Level Cache, we can assume that now Miss Penalty $_{L3}$ = 15 clock cycles (as the previous case where the L2 cache was the LLC and Miss Penalty $_{L2}$ was 15 clock cycles)

5. How much is Miss Penalty $_{L2}$?

Miss Penalty $_{L2}$ =

6. How much is Miss Penalty $_{L1}$?

Miss $Penalty_{L1}$ =

7. How much is the AMAT?

AMAT =

EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from ACA – Como 12/09/2013)

Let us consider a computer with a L1, L2 and L3 cache memory hierarchy with the following parameters: Processor Clock Frequency = ***1 GHz*** ;
Hit Time $_{L1}$ = 1 clock cycle ; Hit Rate $_{L1}$ = 95%;
Hit Time $_{L2}$ = 4 clock cycles; Hit Rate $_{L2}$ = 92% ;
Hit Time $_{L3}$ = 8 clock cycles; Hit Rate $_{L3}$ = 90% ; Miss Penalty $_{L3}$ = 15 clock cycles;

1. How much is the Global Miss Rate for Last Level Cache?

Miss Rate $_{L1\,L2\,L3}$ =

2. How much is Miss Penalty $_{L2}$?

Miss Penalty $_{L2}$ =

3. How much is Miss Penalty $_{L1}$?

Miss Penalty$_{L1}$ =

4. How much is the AMAT?

AMAT =

5. Given Memory Accesses Per Instruction = 78% ; CPI exec = 3, how much is the impact on CPU time of the L1 and L2 cache when considering an IDEAL L3 cache ?

CPU$_{time\ IDEAL\ L3}$ =

EXERCISE on MEMORY HIERARCHY (5 points)
(Ex. taken from HP book 5th Ed. on page B-31)

Let us consider a computer with a L1 cache and L2 cache memory hierarchy. Suppose that in 1000 memory references there are 40 misses in L1 and 20 misses in L2.

1. What are the various miss rates?

Miss Rate $_{L1}$ =

Miss Rate $_{L2}$ =

Global Miss Rate for Last Level Cache:

Miss Rate $_{L1\,L2}$ =

Assume the Hit Time $_{L1}$ = 1 clock cycle ; Hit Time $_{L2}$ = 10 clock cycles; Miss Penalty $_{L2}$ = 200 clock cycles; Memory Accesses Per Instruction = 150%

2. How much is the AMAT?

AMAT =

3. How much is the average memory stall cycles per instruction?

Avg. Memory Stalls per Instr. =