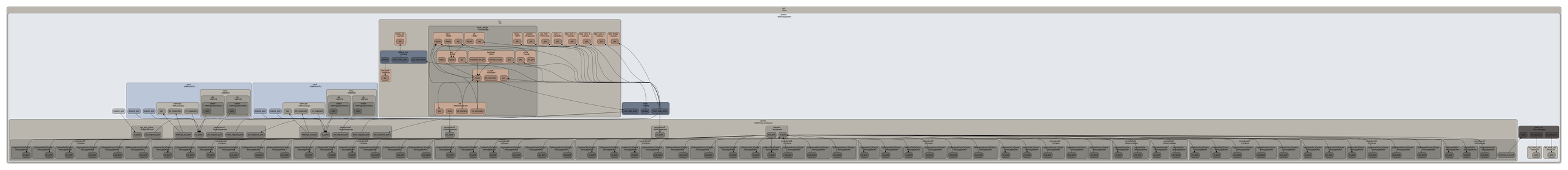

root
: Root

system
: MyRubySystem

pc
: Pc

south_bridge
: SouthBridge

pic1
: I8259

pic2
: I8259

cmos

: Cmos

dma1
: I8237

keyboard
: I8042

pit
: I8254

speaker
: PcSpeaker

io_apic
: I82094AA

ide
: X86IdeController

pci_host
: PcPciHost

com_1
: Uart8250

fake_com_2
: IsaFake

fake_com_3
: IsaFake

fake_com_4
: IsaFake

fake_floppy
: IsaFake

default_bus
: IOXBar

empty_isa
: IsaFake

bad_addr
: BadAddr

iobus
: IOXBar

cpu0
: X86KvmCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

cpu1
: X86KvmCPU

mmu

: X86MMU

itb
: X86TLB

walker
: X86PagetableWalker

dtb
: X86TLB

walker
: X86PagetableWalker

interrupts
: X86LocalApic

mem_ctrl
: PolicyManager

loc_mem_ctrl
: MemCtrl

far_mem_ctrl
: MemCtrl

caches
: MESITwoLevelCache

network
: MyNetwork

controllers00
: L1Cache

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

controllers01
: L1Cache

requestFromL1Cache
: MessageBuffer

responseFromL1Cache
: MessageBuffer

unblockFromL1Cache
: MessageBuffer

requestToL1Cache
: MessageBuffer

responseToL1Cache
: MessageBuffer

controllers02
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers03
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers04
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers05
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers06
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers07
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers08
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers09
: L2Cache

DirRequestFromL2Cache
: MessageBuffer

L1RequestFromL2Cache
: MessageBuffer

responseFromL2Cache
: MessageBuffer

unblockToL2Cache
: MessageBuffer

L1RequestToL2Cache
: MessageBuffer

responseToL2Cache
: MessageBuffer

controllers10
: DirController

requestToDir
: MessageBuffer

responseToDir
: MessageBuffer

responseFromDir
: MessageBuffer

controllers11
: DMAController

responseFromDir
: MessageBuffer

requestToDir
: MessageBuffer

controllers12
: DMAController

responseFromDir
: MessageBuffer

requestToDir
: MessageBuffer

sequencers0
: RubySequencer

sequencers1
: RubySequencer

sequencers2
: DMASequencer

sequencers3
: DMASequencer

sys_port_proxy
: RubyPortProxy

system_port

in_ports

output

inputs

inputs pio

mem_side_ports

inputs output

int_pin

int_primary int_secondary

pio

pio

pio

keyboard_int_pin mouse_int_pin pio

int_pin pio pio

int_requestor

cpu_side_ports

pio

dma

in_ports

pio

pio pio pio pio pio pio

cpu_side_ports

default

default mem_side_ports

pio

pio

pio_request_port pio_request_port mem_request_port pio_response_port pio_request_port mem_request_port pio_response_port in_ports

icache_port

in_ports

dcache_port int_responder int_requestor port port

interrupt_out_port

icache_port pio

in_ports

dcache_port int_responder int_requestor port port

interrupt_out_port

pio

port

memory_out_port

loc_req_port

port

far_req_port

port

in_port

out_port out_port

out_port

in_port in_port