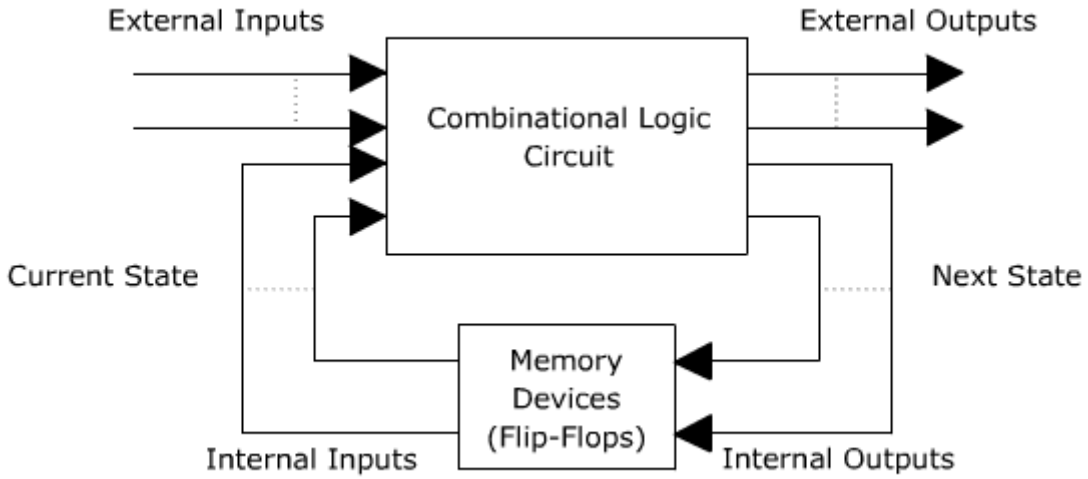
Sequence Detetector

Design a sequence detector to detect a sequence 1101.

Theory:

Sequential Circuits:

Sequential circuits works on a clock cycle which may be synchronous or asynchronous. The figure shows a basic diagram of sequential circuits. Sequential circuits use current inputs and previous inputs by storing the information and putting back into the circuit on the next clock cycle.



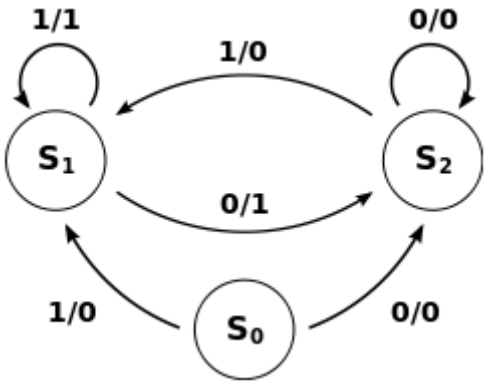
Finite State Machine (FSM):

A FSM is a model used to design sequential logic circuits. It is conceived as an abstract machine that can be in one of a finite number of *states*. The machine is in only one state at a time; the state it is in at any given time is called the *current state*. It can change from one state to another when initiated by a triggering event or condition, this is called a *transition*. A particular FSM is defined by a list of its states, and the triggering condition for each transition. It can be implemented using models like Mealy and Moore machine. For this expt., we will use Mealy model implementation.

Mealy Machine:

In this model of FSM, the output values are determined both by its current state and the current inputs. The state diagram of a mealy machine associates an output value with each transition edge.

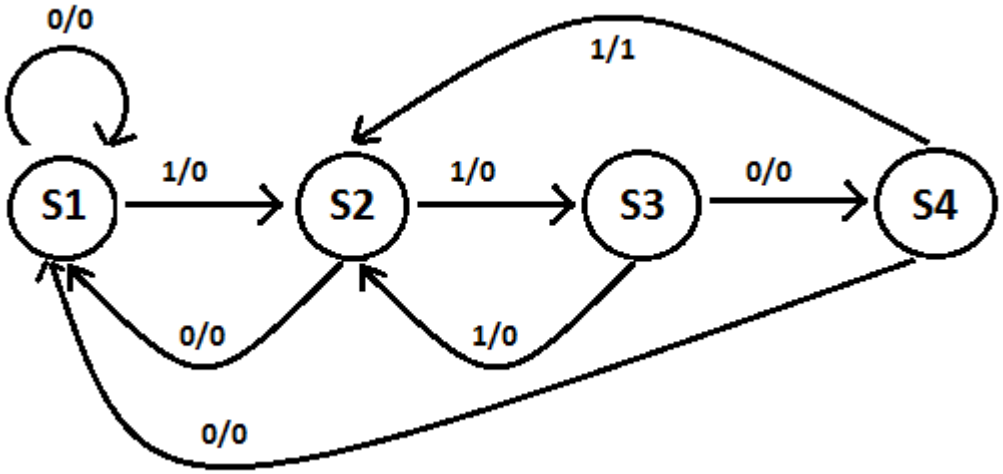
Example:



Here 1/1, 1/0, 0/1, 0/0 represent input/output and S0, S1, S2 represent the states. Consider a part of the state diagram S1 -> S2 where "0/1" is written on the arrow. This can be interpreted as, when the current state of the system is S1 and when input "0" is applied, the system goes into next state - S2 and the output of the system is "1".

Sequence detector:

Suppose a sequence detector is to be designed to detect a sequence 1101.
Then the state diagram will be:



Note that this state diagram is considering overlap i.e. if we have input 1101101 we will have output 0001001.
For same input, non-overlap case will have output 0001000. Either cases are correct but we will consider only overlap case henceforth.

References:

http://www.ee.surrey.ac.uk/Projects/Labview/Sequential/Course/03-Seq_Intro/Intro.html

http://en.wikipedia.org/wiki/Finite-state_machine

http://en.wikipedia.org/wiki/Mealy_machine