Bidirectional Counter

Procedure:

1. Write the verilog code for the experiment.
2. Save this file as updown_counter.v
3. Now visit the e-prayog webpage: http://59.181.142.81/
4. Login on the page if you are registered or sign-up if not registered.
5. Now visit the webpage of Remote Triggered FPGA based Automation system: http://59.181.142.81/fpga/automation.php
6. Click on upload verilog file button and upload your verilog file “updown_counter.v”
7. After the browser specifies “All checks passed”, select the clock pin as “clk”.
8. Give the test inputs for clock instances where the input is changing.
9. Click on “Set input vectors and Execute” - this will compile the design, assign pins according Altera DE2-70 board, synthesize it and execute it on the board with the given test inputs to generate a vcd file output. (this will take about some time from 1-3 mins depending on the design complexity).
10. Download the vcd file which is now available on webpage.
11. Open this vcd file using GTKwave and view the waveform.