

# Sequence Detector

## Tutorial:

1. Write verilog code.

Sample code:

```
module m1101( clk, rst, inp, outp);
    input clk, rst;
    input inp;
    output outp;
    reg [1:0] state=0;
    reg outp=0;

    always @( posedge clk )
    begin
        if( rst )
        begin
            state <= 2'b00;
            outp <= 0;
        end
        else
        begin
            case( {state,inp} )
                3'b000: begin
                    state <= 2'b00;
                    outp <= 0;
                end
                3'b001: begin
                    state <= 2'b01;
                    outp <= 0;
                end
                3'b010: begin
                    state <= 2'b00;
                    outp <= 0;
                end
                3'b011: begin
                    state <= 2'b10;
                    outp <= 0;
                end
                3'b100: begin
                    state <= 2'b11;
                    outp <= 0;
                end
                3'b101: begin
```

```

        state <= 2'b01;
        outp <= 0;
    end
    3'b110: begin
        state <= 2'b00;
        outp <= 0;
    end
    3'b111: begin
        state <= 2'b01;
        outp <= 1;
    end
endcase
end
end
endmodule

```

2. Save this code as seq\_dut.v and save it in a directory.

3. Visit e-prayog webpage: <http://59.181.142.81/>

The screenshot shows the e-Prayog Virtual Labs (Electronics) IIT Bombay website. The header includes the IIT Bombay logo and the e-Prayog title. Below the header is a navigation bar with links to Home, Devices & Circuits, Modern Digital Design, Signal Processing, Image Processing, Microcontrollers, People, Feedback, and Workshop Report. The main content area is divided into two columns. The left column contains a 'Login for e-Prayog' section with username and password fields, and a 'Downloads' section with links to Java Runtime, Labview Runtime, SEQUEL, Scilab, and UrJTAG. The right column contains an 'Introduction' section with a paragraph about the importance of laboratories in engineering education and a list of developed electronics lab courses.

## Introduction

Laboratories play an important role in engineering education. The laboratory work provides them an opportunity to witness classroom-learned theoretical concepts at work; operate instruments used in the experimental set-up; measure different quantities and thereafter analyze the experimental data; and work collaboratively. However, physical distances and the lack of resources make us unable to perform experiments, especially when they involve sophisticated instruments. Also, trained teachers are always a scarce resource. Rapid development and ever increasing use of Information and Communication Technology (ICT) has revolutionized the education system by eliminating limitations in terms of physical distance, time and access, by providing equal opportunity to everyone, irrespective of place and time.

As a part of e-Prayog, the following electronics lab courses have been developed:

- Electronic Devices and Circuits
- Network Analysis
- Linear Integrated Circuits
- Single and Custom...

4. Login on the page if you are registered or sign-up if not registered.



Login for e-Prayog

Username

Password



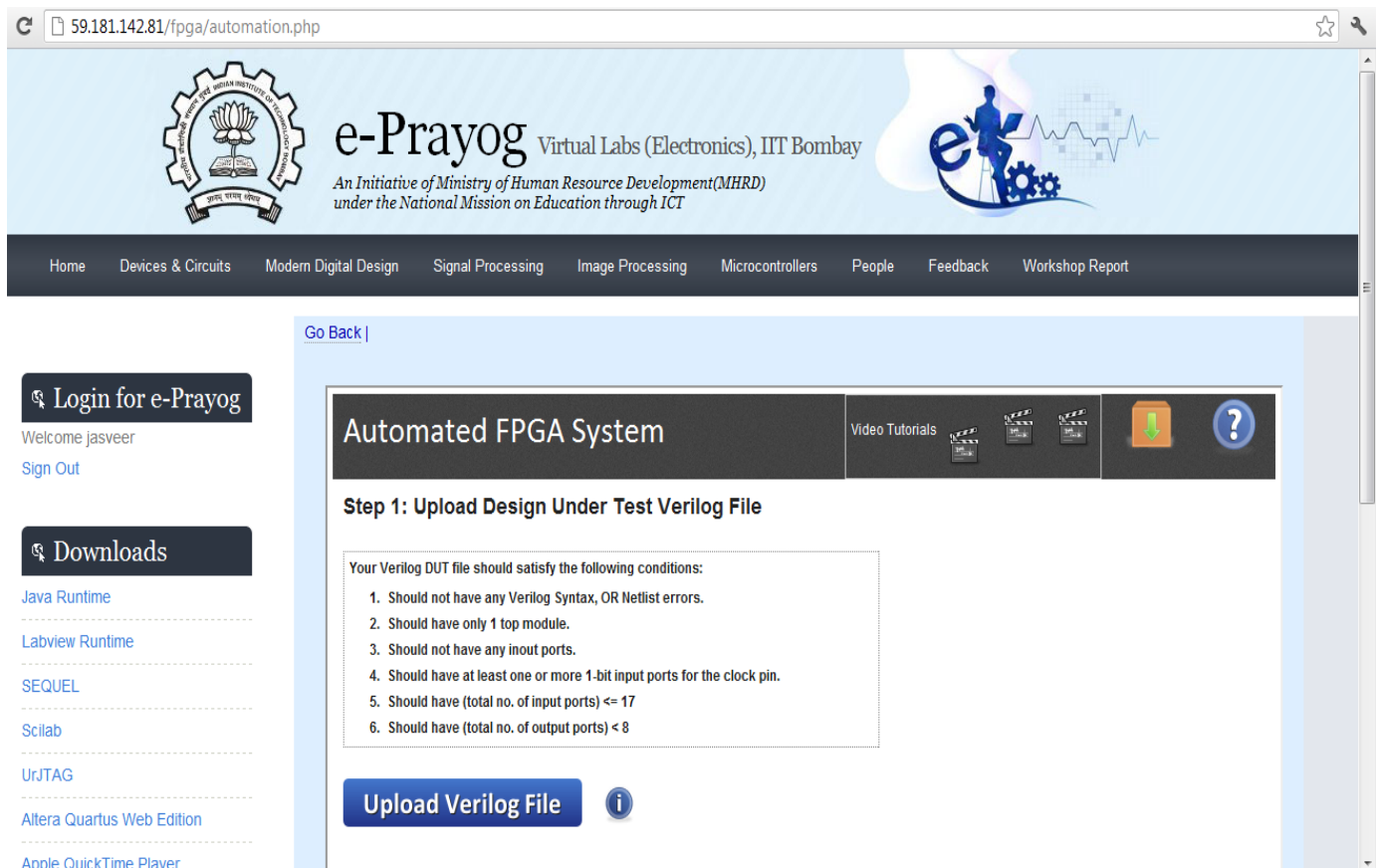
Login for e-Prayog

Welcome jasveer

[Sign Out](#)

5. Now visit the webpage of Remote Triggered FPGA based Automation system:

<http://59.181.142.81/fpga/automation.php>



The screenshot shows a web browser window with the address bar displaying `59.181.142.81/fpga/automation.php`. The page header features the IIT Bombay logo and the text "e-Prayog Virtual Labs (Electronics), IIT Bombay" and "An Initiative of Ministry of Human Resource Development (MHRD) under the National Mission on Education through ICT". A navigation bar includes links: Home, Devices & Circuits, Modern Digital Design, Signal Processing, Image Processing, Microcontrollers, People, Feedback, and Workshop Report.

The main content area is titled "Automated FPGA System" and includes a "Go Back" link. Below the title, it says "Step 1: Upload Design Under Test Verilog File". A box lists conditions for the Verilog DUT file:

1. Should not have any Verilog Syntax, OR Netlist errors.
2. Should have only 1 top module.
3. Should not have any inout ports.
4. Should have at least one or more 1-bit input ports for the clock pin.
5. Should have (total no. of input ports)  $\leq 17$
6. Should have (total no. of output ports)  $\leq 8$

Below the list is a blue button labeled "Upload Verilog File" and an information icon. On the left sidebar, there is a "Login for e-Prayog" section with "Welcome jasveer" and "Sign Out" link, and a "Downloads" section with links: Java Runtime, Labview Runtime, SEQUEL, Scilab, UrJTAG, Altera Quartus Web Edition, and Apple QuickTime Player.



6. Click on upload verilog file button and upload your verilog file "seq\_dut.v"

7. After the browser specifies "All checks passed", select the clock pin as "clk".

8. Give the test inputs for clock instances where the input is changing.

Automated FPGA System

Video Tutorials



Step 3: Provide input vectors & Execute Design

Clock Cycle	rst	inp
0	1	0
1		
2	0	1
3		1
4		0
5		1
6		1
7		0
8		1
9		
10		

Add Row

Delete Row

Set Input Vectors & Execute

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9. Click on “Set input vectors and Execute” - this will compile the design, assign pins according Altera DE2-70 board, synthesize it and execute it on the board with the given test inputs to generate a vcd file output. (this will take about some time from 1-3 mins depending on the design complexity).

10. The log will appear and the output vcd file will be available for download