Bidirectional Counter

Tutorial:

1. Write verilog code:

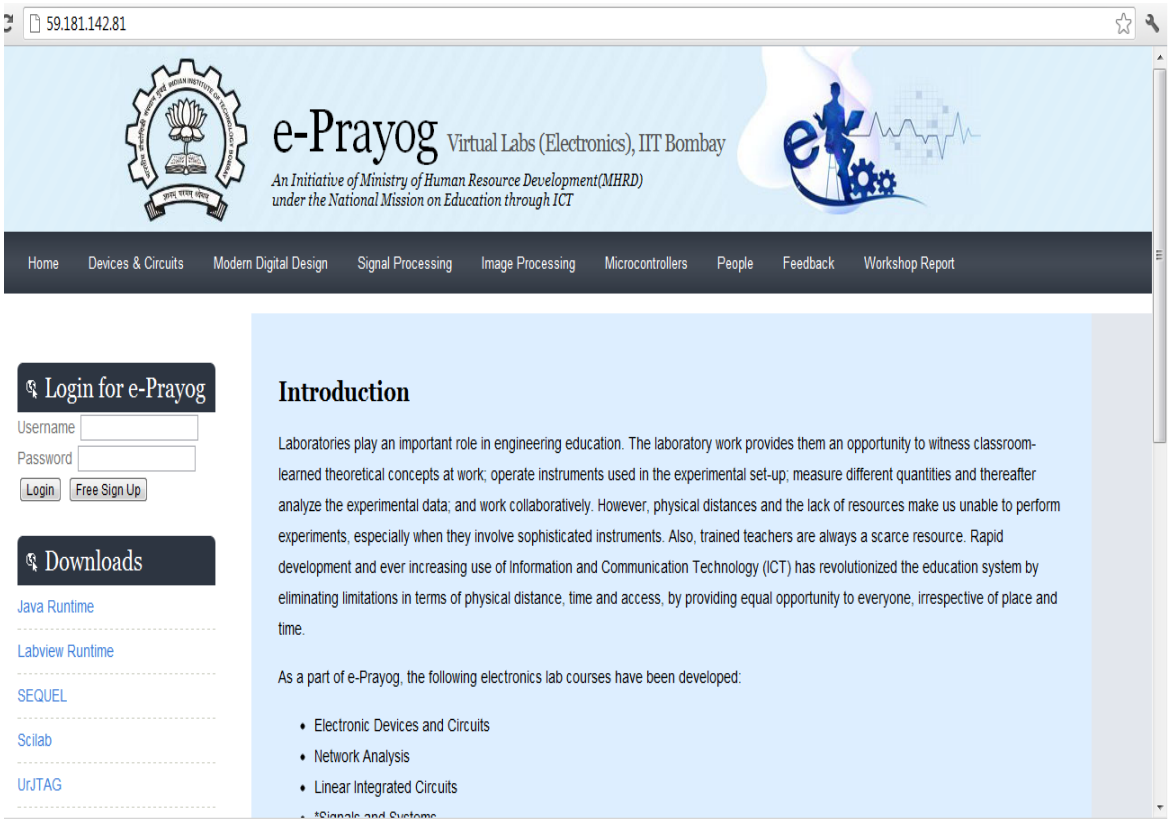
Sample code:

```
module updown_counter(clk, reset, mode, count);
      input clk, reset, mode;
      output [ 7 :0 ] count;
      wire reset, mode;
      reg [ 7 :0] count;

      always @(posedge clk )
      begin
            if(!reset)
                count <= 8'b0100;
            else if (mode == 0)
                count <= count + 1;
           else if (mode == 1)
                count <= count - 1;
      end
endmodule
```

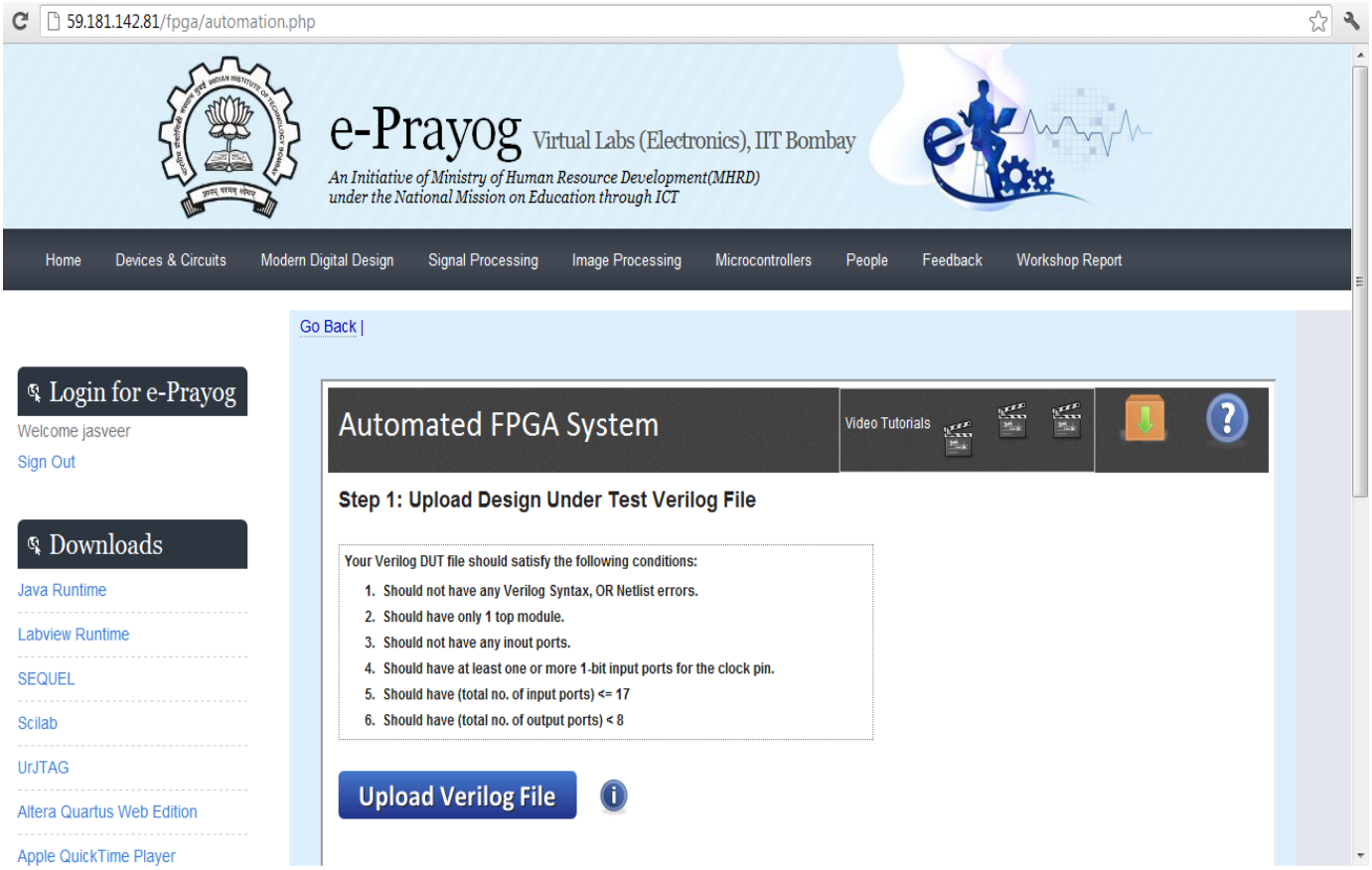
2. Save this code as updown_counter.v and save it in a directory.

3.Visit e-prayog webpage: http://59.181.142.81/

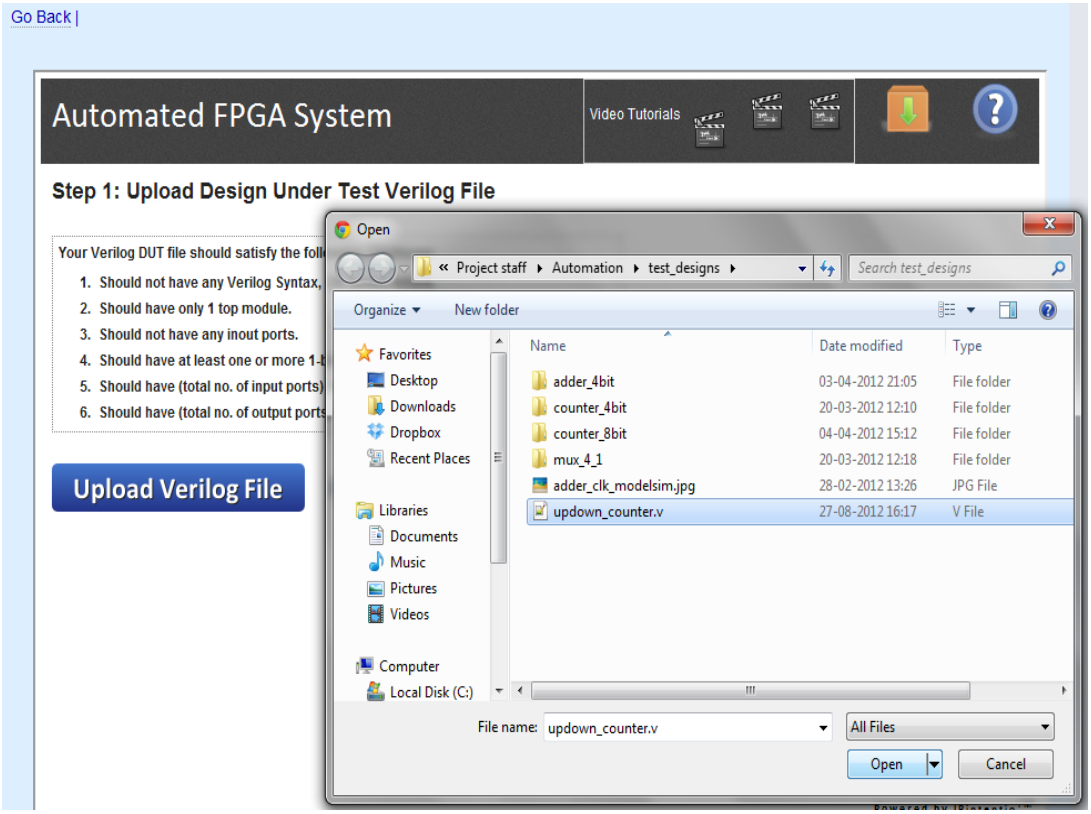


4. Login on the page if you are registered or sign-up if not registered.

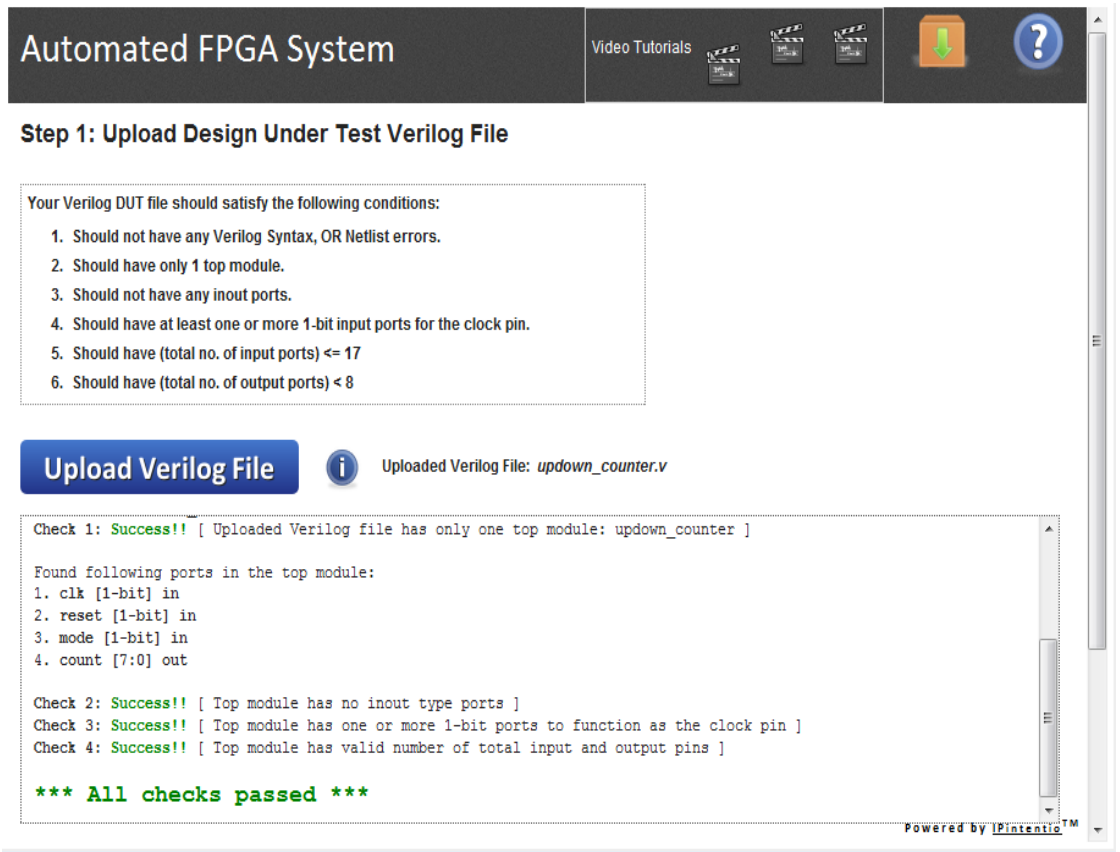
5. Now visit the webpage of Remote Triggered FPGA based Automation system: http://59.181.142.81/fpga/automation.php



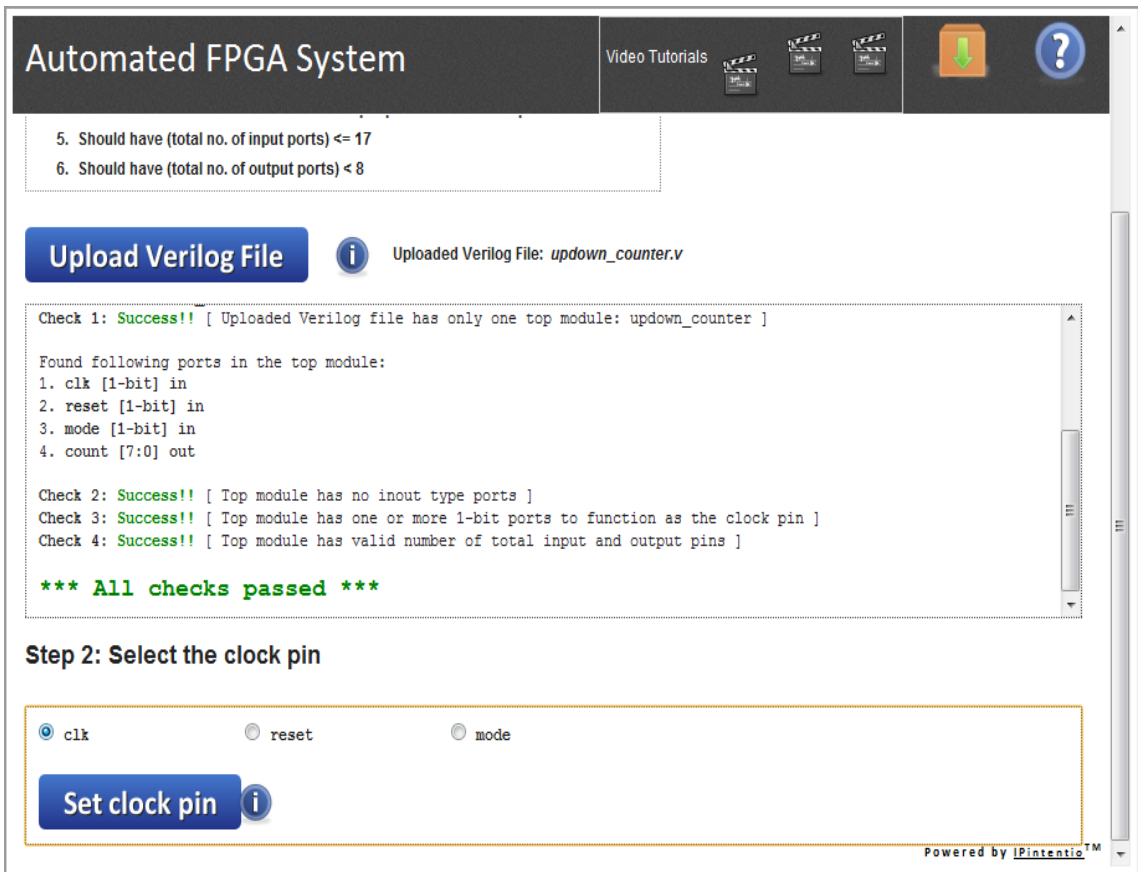
6. Click on upload verilog file button and upload your verilog file “updown_counter.v”



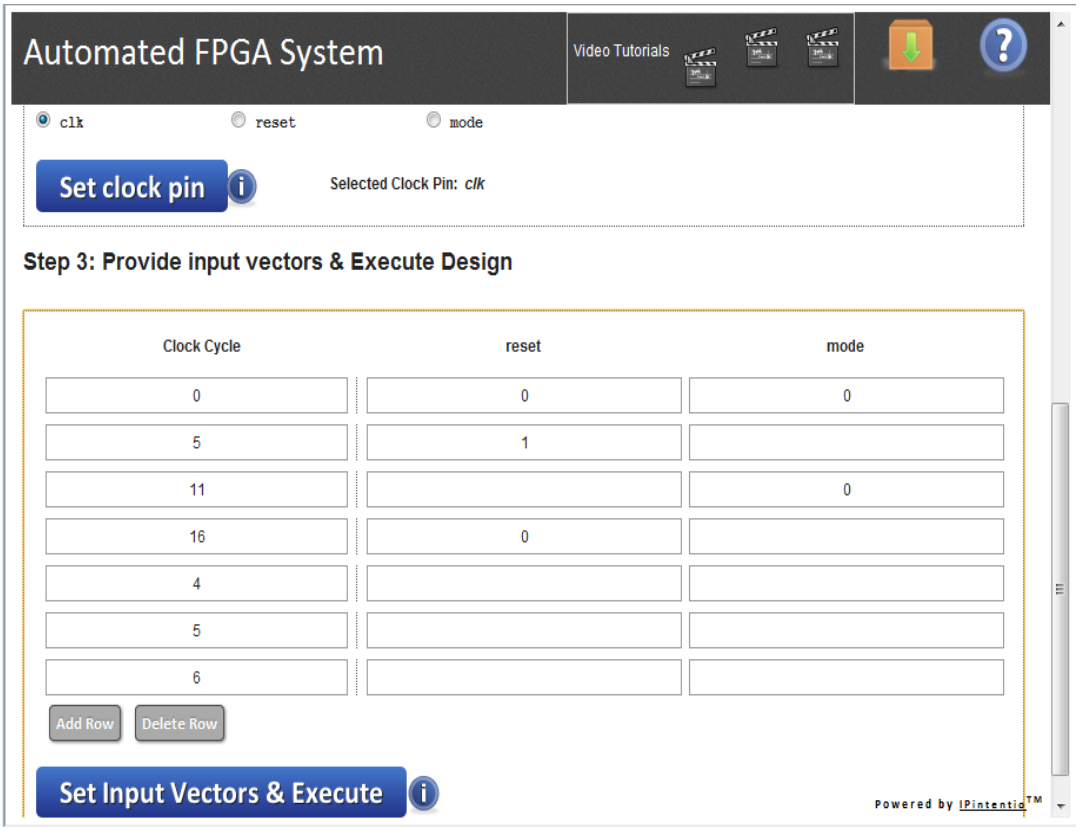
Now click on open:



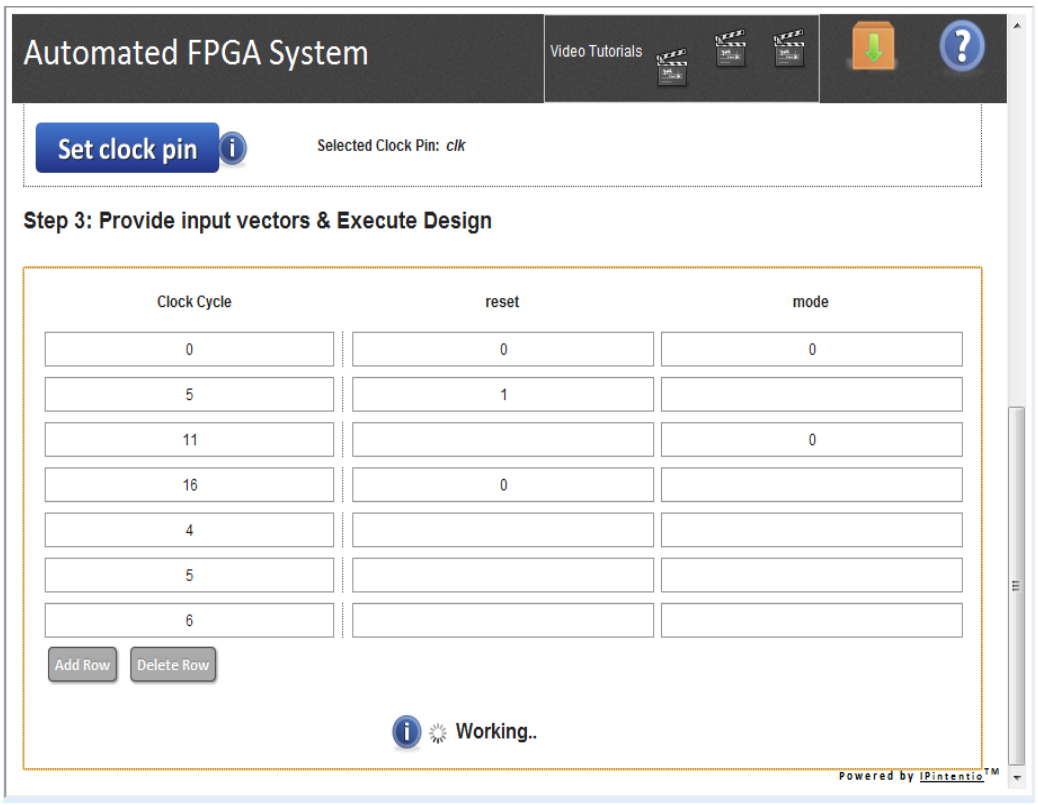
7. After the browser specifies “All checks passed”, select the clock pin as “clk”.



8. Give the test inputs for clock instances where the input is changing.



9. Click on “Set input vectors and Execute” - this will compile the design, assign pins according Altera DE2-70 board, synthesize it and execute it on the board with the given test inputs to generate a vcd file output. (this will take about some time from 1-3 mins depending on the design complexity).



The log will appear and the output vcd file will be available for download: