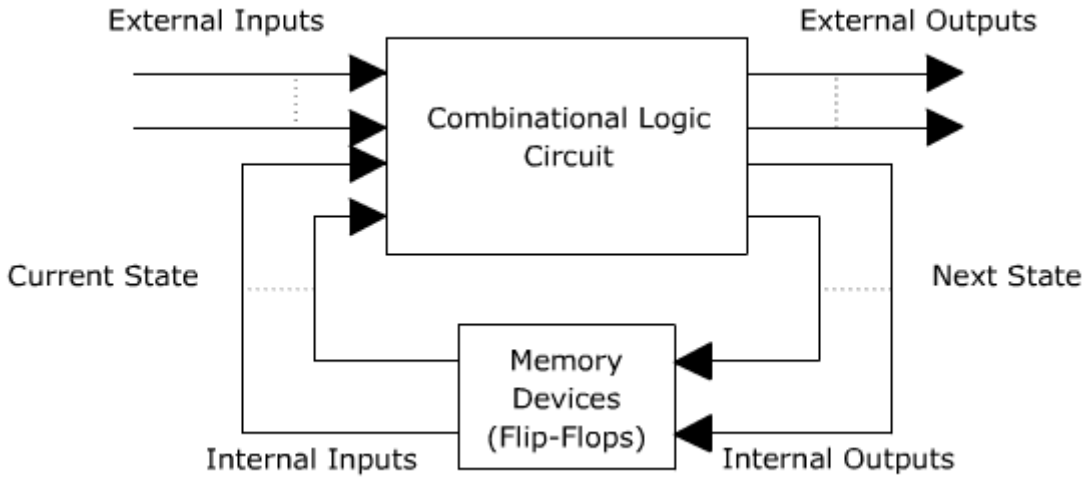
Traffic Light Controller (TLC)

Design a simple traffic light controller.

Theory:

Sequential Circuits:

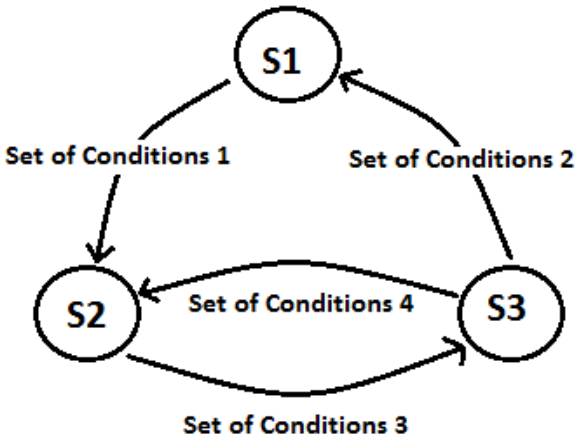
Sequential circuits works on a clock cycle which may be synchronous or asynchronous. The figure shows a basic diagram of sequential circuits. Sequential circuits use current inputs and previous inputs by storing the information and putting back into the circuit on the next clock cycle.



Finite State Machine (FSM):

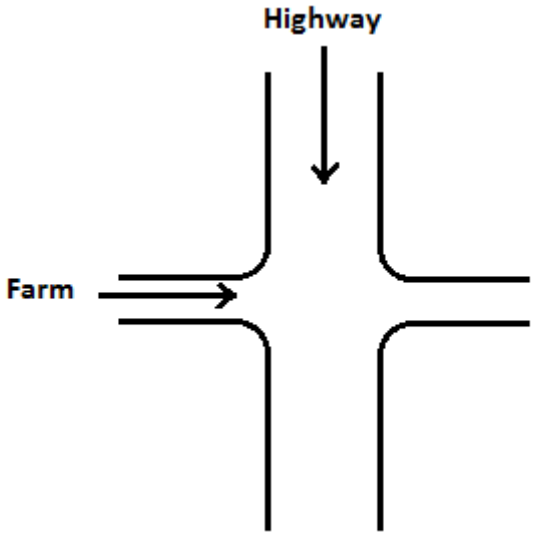
A FSM is a model used to design sequential logic circuits. It is conceived as an abstract machine that can be in one of a finite number of *states*. The machine is in only one state at a time; the state it is in at any given time is called the *current state*. It can change from one state to another when initiated by a triggering event or condition, this is called a *transition*. A particular FSM is defined by a list of its states, and the triggering condition for each transition. This can be shown with the help of a state diagram.

State diagram:

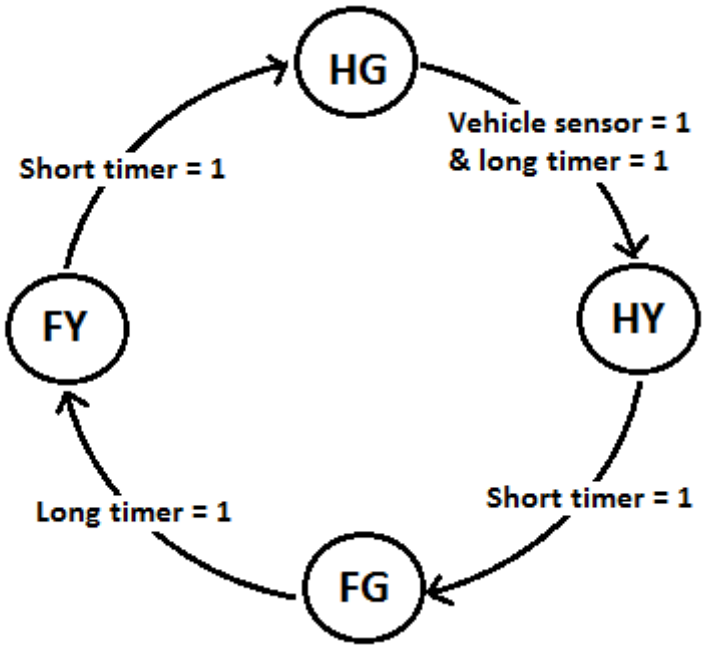


Traffic Light controller:

Suppose we have a cross like this:



There are two timers a long timer for green signal and a short timer for yellow signal.
And assume the state diagram like this:



State diagram Explanation:
State 1: In this state, Highway signal is green, long timer is on and Farm signal is red.
Let this state be called “HG”.
When the vehicle sensor is high and the long timer is out, it goes into state 2 and long timer is reset otherwise the system remains in this state.
State 2: In this state, Highway signal is yellow, short timer is on and Farm signal is red.
Let this state be called “HY”.
When the short timer is out, it goes into state 3 and short timer is reset, otherwise the system remains in this state.

State 3: In this state, Farm signal is green, long timer is on and Highway signal is red.
Let this state be called “FG”.
When the long timer is out, it goes into state 4 and long timer is reset otherwise the system remains in this state.
State 4: In this state, Farm signal is yellow, short timer is on and Highway signal is red.
Let this state be called “FY”.
When the short timer is out, it goes into state 1 and short timer is reset, otherwise the system remains in this state.

References:

http://www.ee.surrey.ac.uk/Projects/Labview/Sequential/Course/03-Seq_Intro/Intro.html

http://en.wikipedia.org/wiki/Finite-state_machine