Sequence Detetector

Tutorial:

1. Write verilog code.

Sample code:

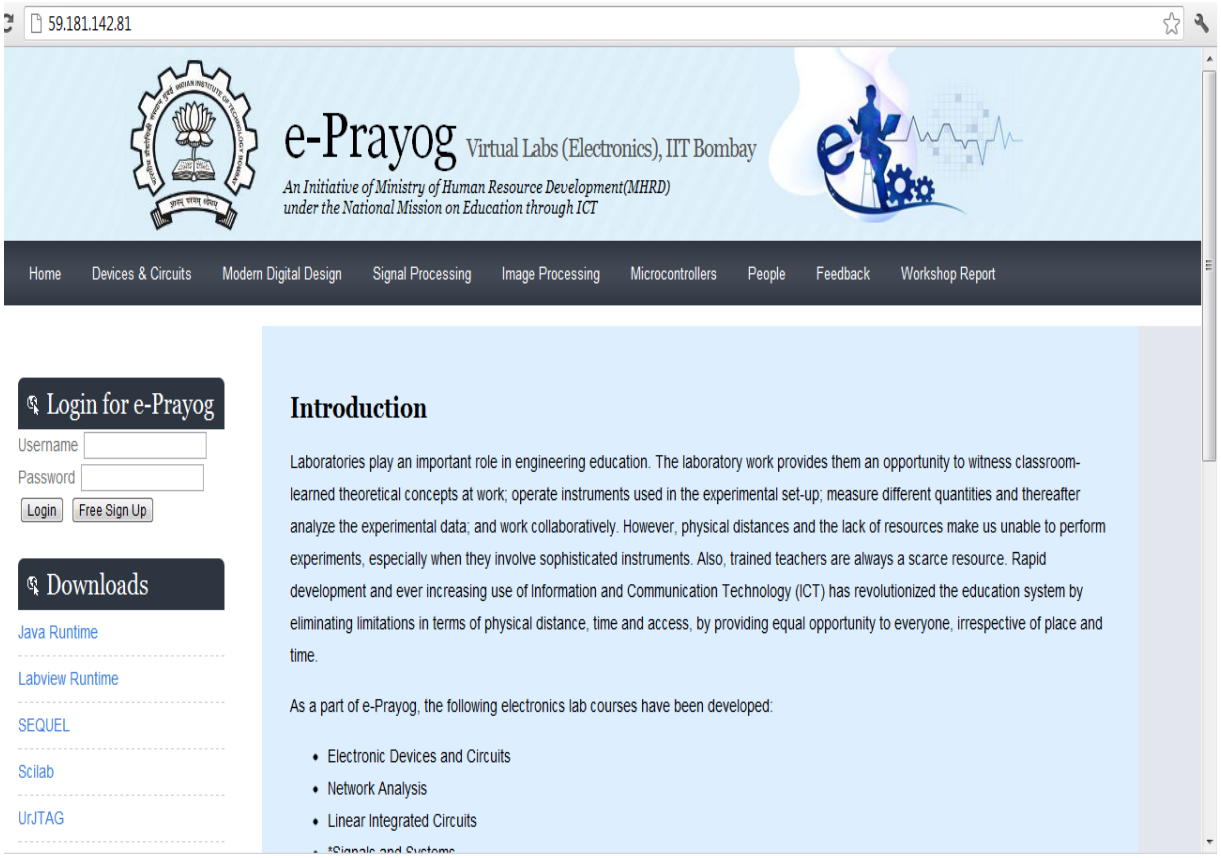
```
module m1101( clk, rst, inp, outp);
   input clk, rst;
   input inp;
   output outp;
   reg [1:0] state=0;
   reg outp=0;

   always @( posedge clk )
   begin
          if( rst )
          begin
               state <= 2'b00;
               outp <= 0;
          end
          else
          begin
          case( {state,inp} )
               3'b000: begin
                    state <= 2'b00;
                    outp <= 0;
               end
               3'b001: begin
                    state <= 2'b01;
                    outp <= 0;
               end
               3'b010: begin
                    state <= 2'b00;
                    outp  <= 0;
               end
               3'b011: begin
                    state <= 2'b10;
                    outp <= 0;
               end
               3'b100: begin
                    state <= 2'b11;
                    outp <= 0;
               end
               3'b101: begin
```

```
                    state <= 2'b01;
                    outp  <= 0;
                end
                3'b110: begin
                    state <= 2'b00;
                    outp <= 0;
                end
                3'b111: begin
                    state <= 2'b01;
                    outp <= 1;
                end
            endcase
            end
        end
endmodule
```

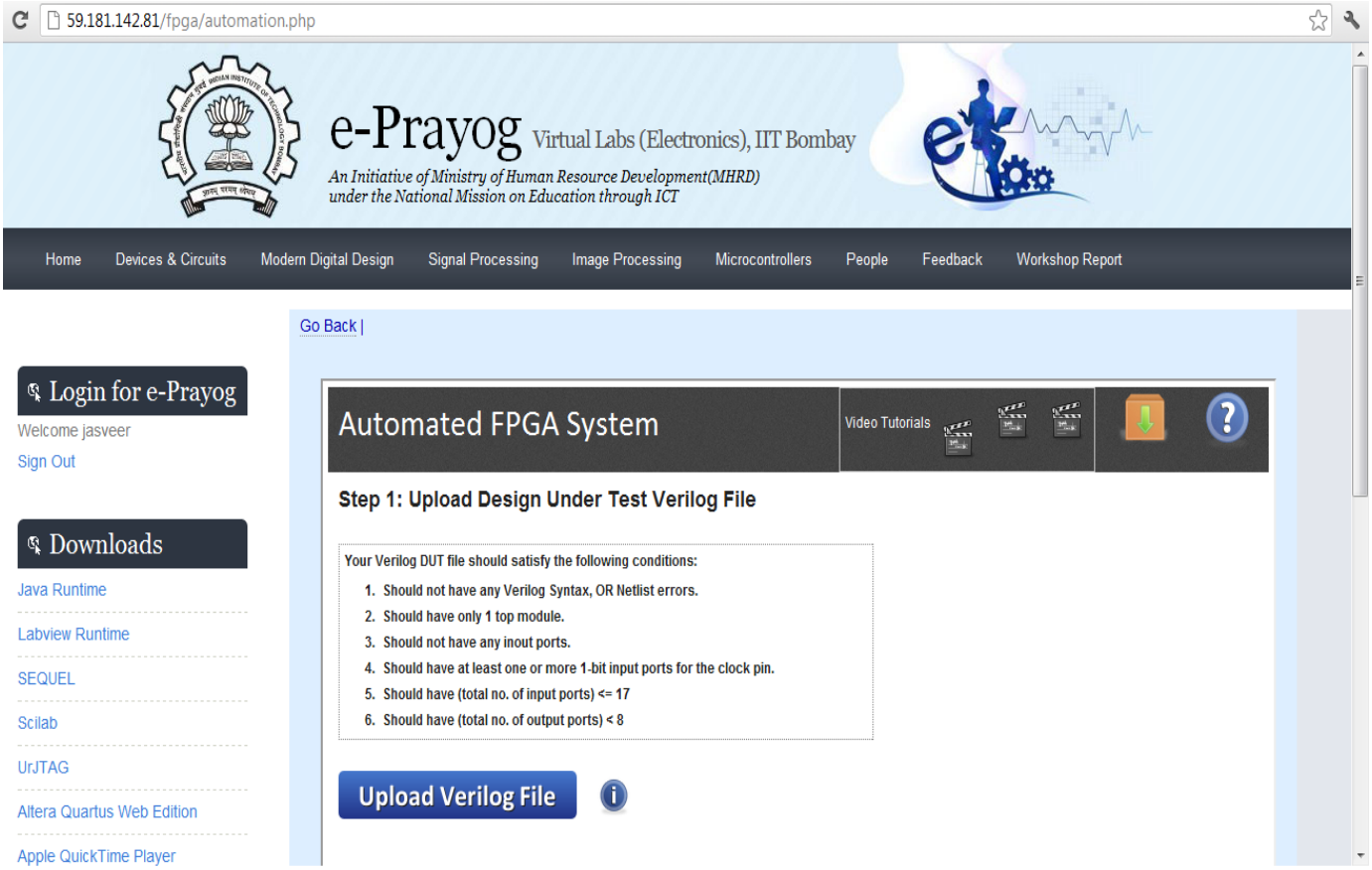
2. Save this code as seq_dut.v and save it in a directory.

3. Visit e-prayog webpage: http://59.181.142.81/



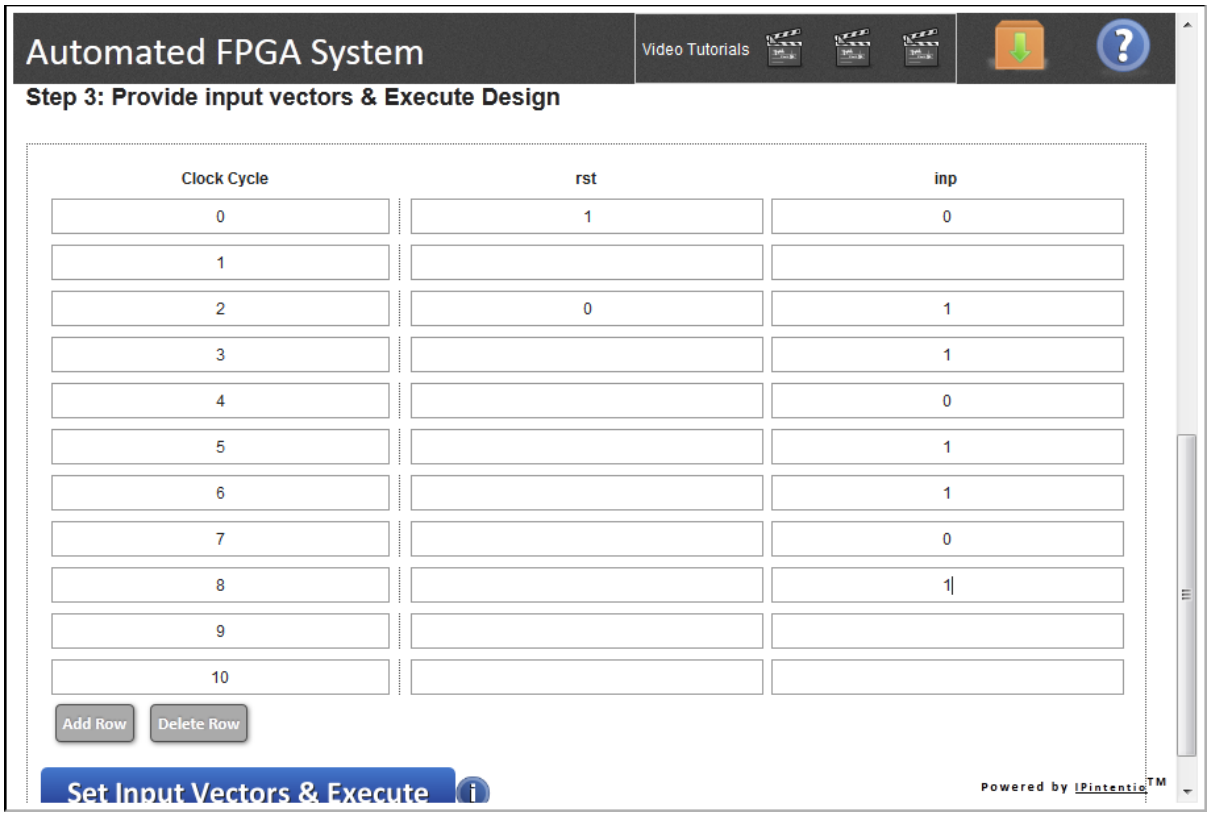
4. Login on the page if you are registered or sign-up if not registered.

5. Now visit the webpage of Remote Triggered FPGA based Automation system: http://59.181.142.81/fpga/automation.php



6. Click on upload verilog file button and upload your verilog file “seq_dut.v”
7. After the browser specifies “All checks passed”, select the clock pin as “clk”.

8. Give the test inputs for clock instances where the input is changing.



9. Click on "Set input vectors and Execute" - this will compile the design, assign pins according Altera DE2-70 board, synthesize it and execute it on the board with the given test inputs to generate a vcd file output. (this will take about some time from 1-3 mins depending on the design complexity).

10. The log will appear and the output vcd file will be available for download