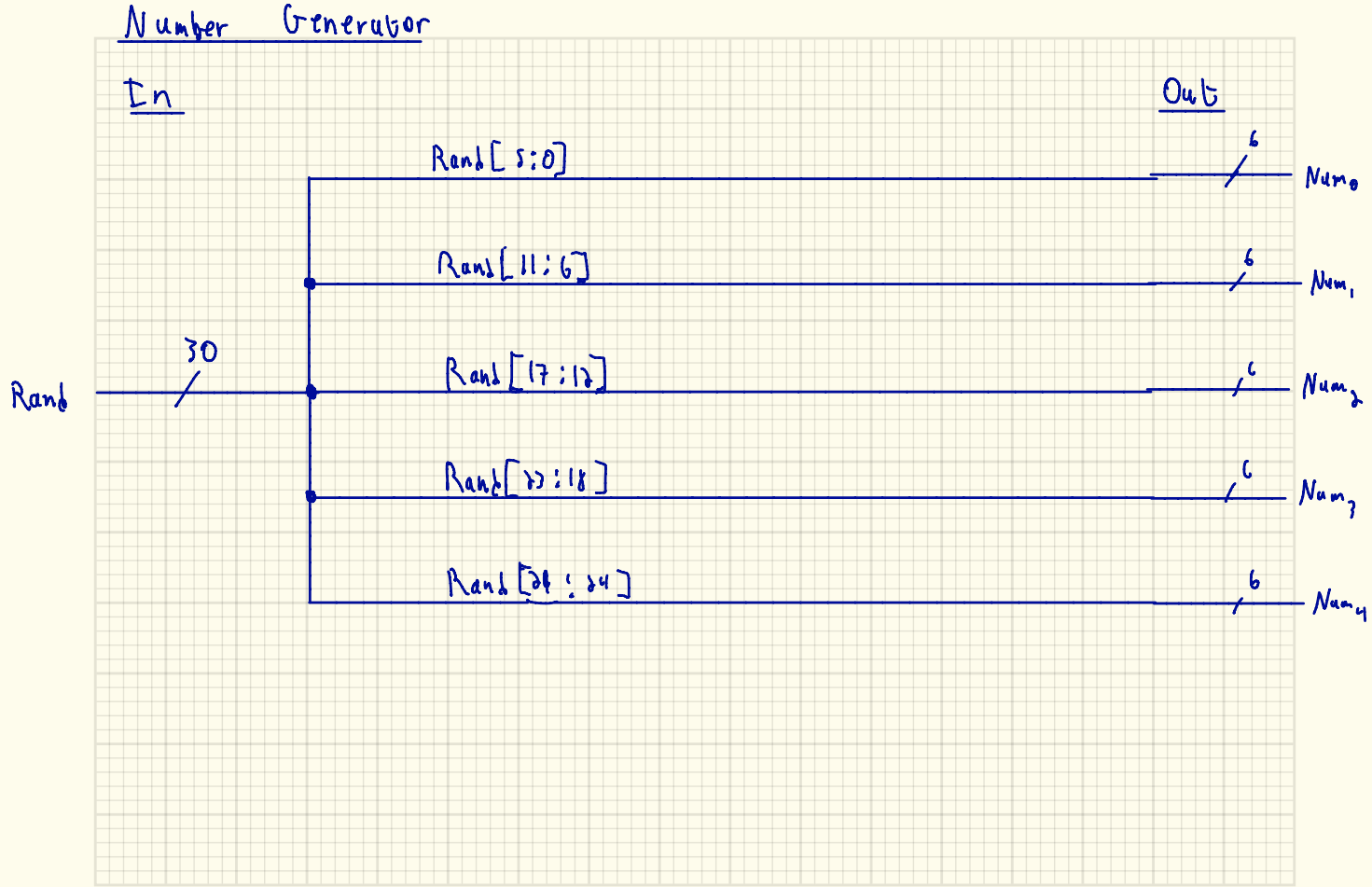
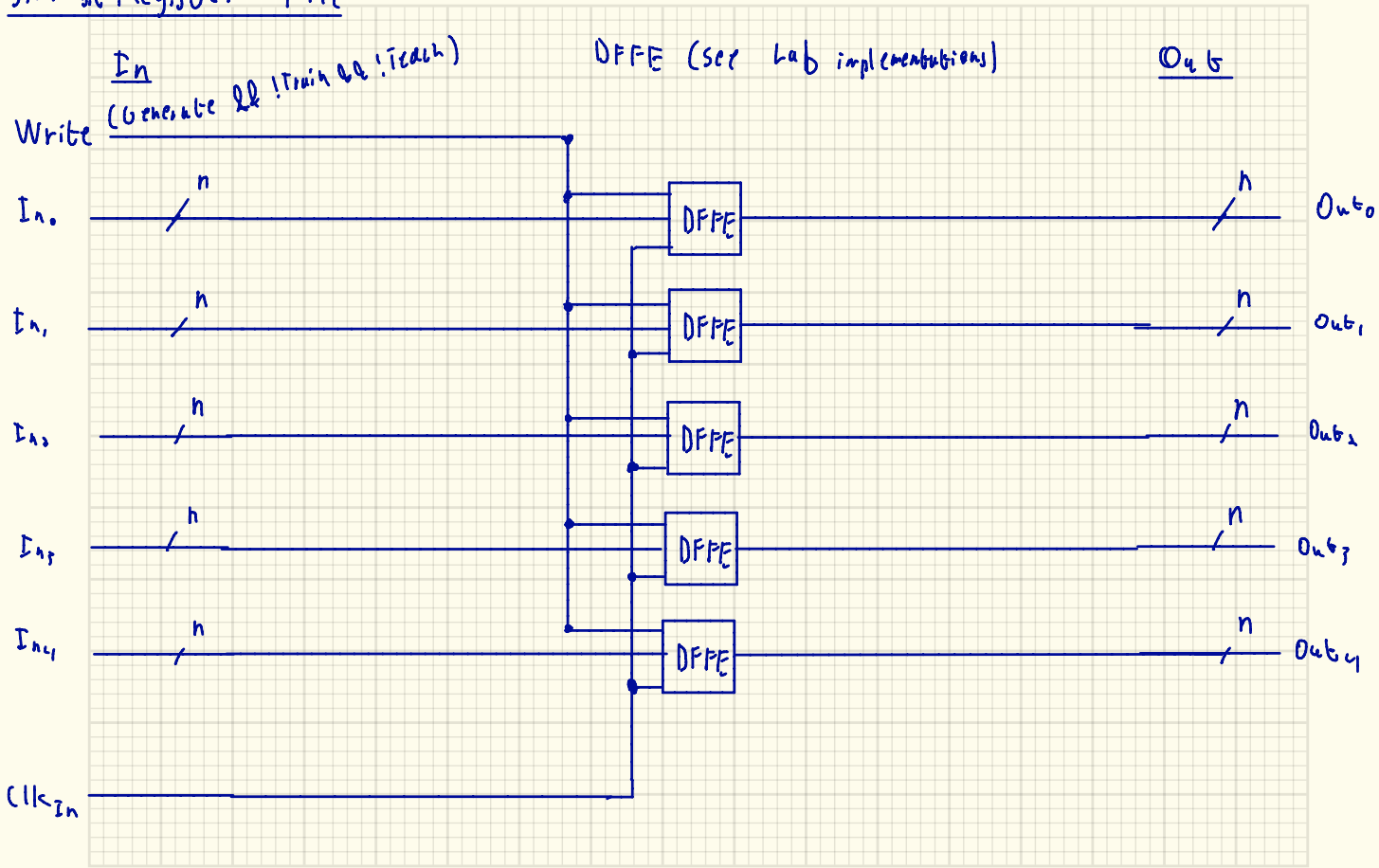
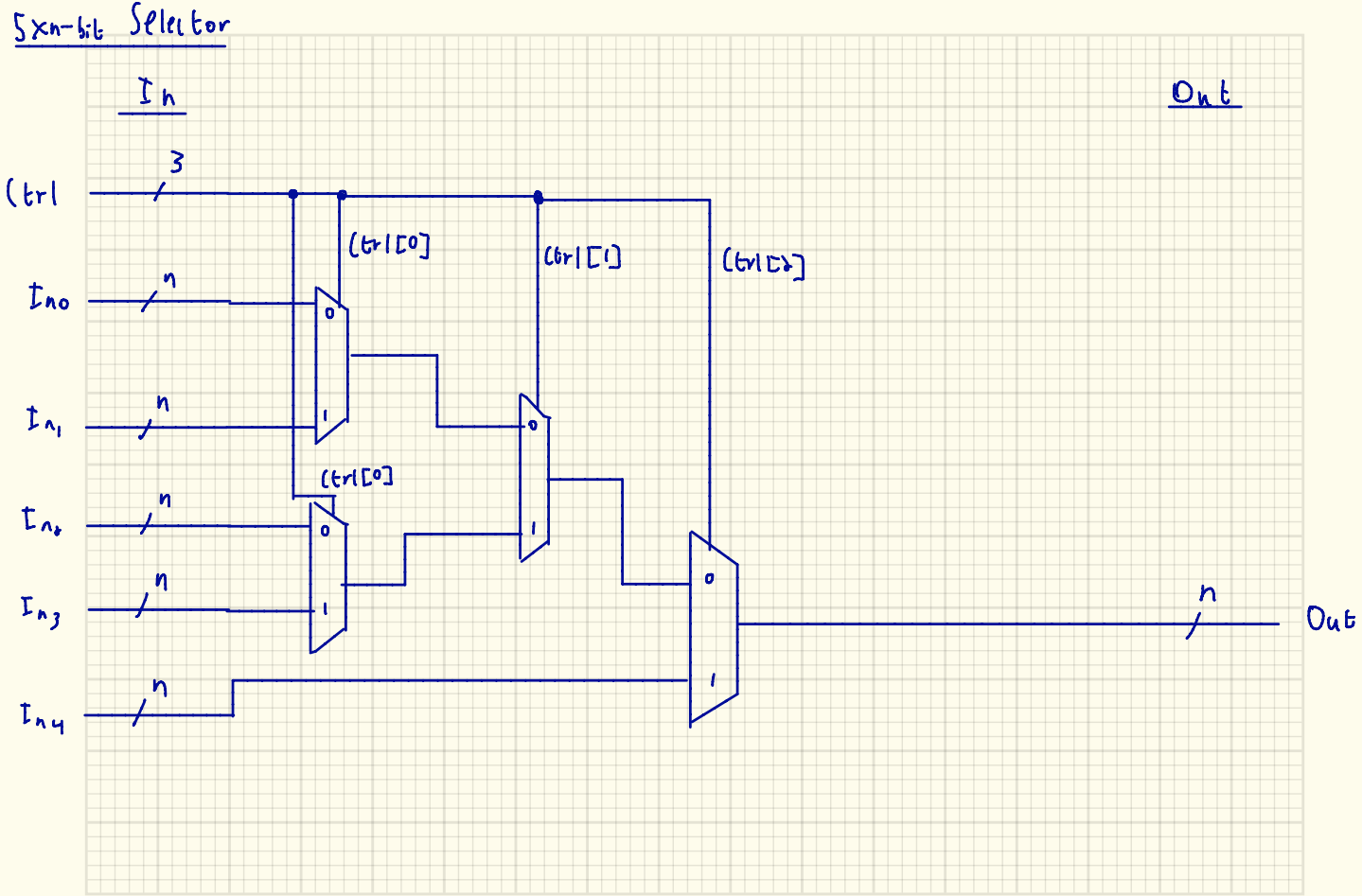

Number Generator
In
Out
Rand
30
Rand[5:0]
Rand[11:6]
Rand[17:12]
Rand[23:18]
Rand[29:24]
6
Num0
Num1
Num2
Num3
Num4

5 x n-bit Register File




5xn-bit Selector
In
Out
3
Ctrl
n
In0
In1
In2
In3
In4
Ctrl[0]
Ctrl[1]
Ctrl[2]
Ctrl[0]
0
1
0
1
0
1
n
Out

Display

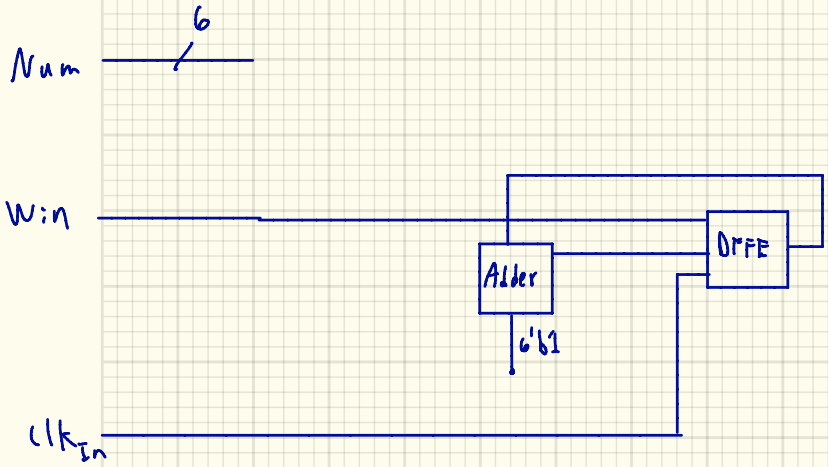
In

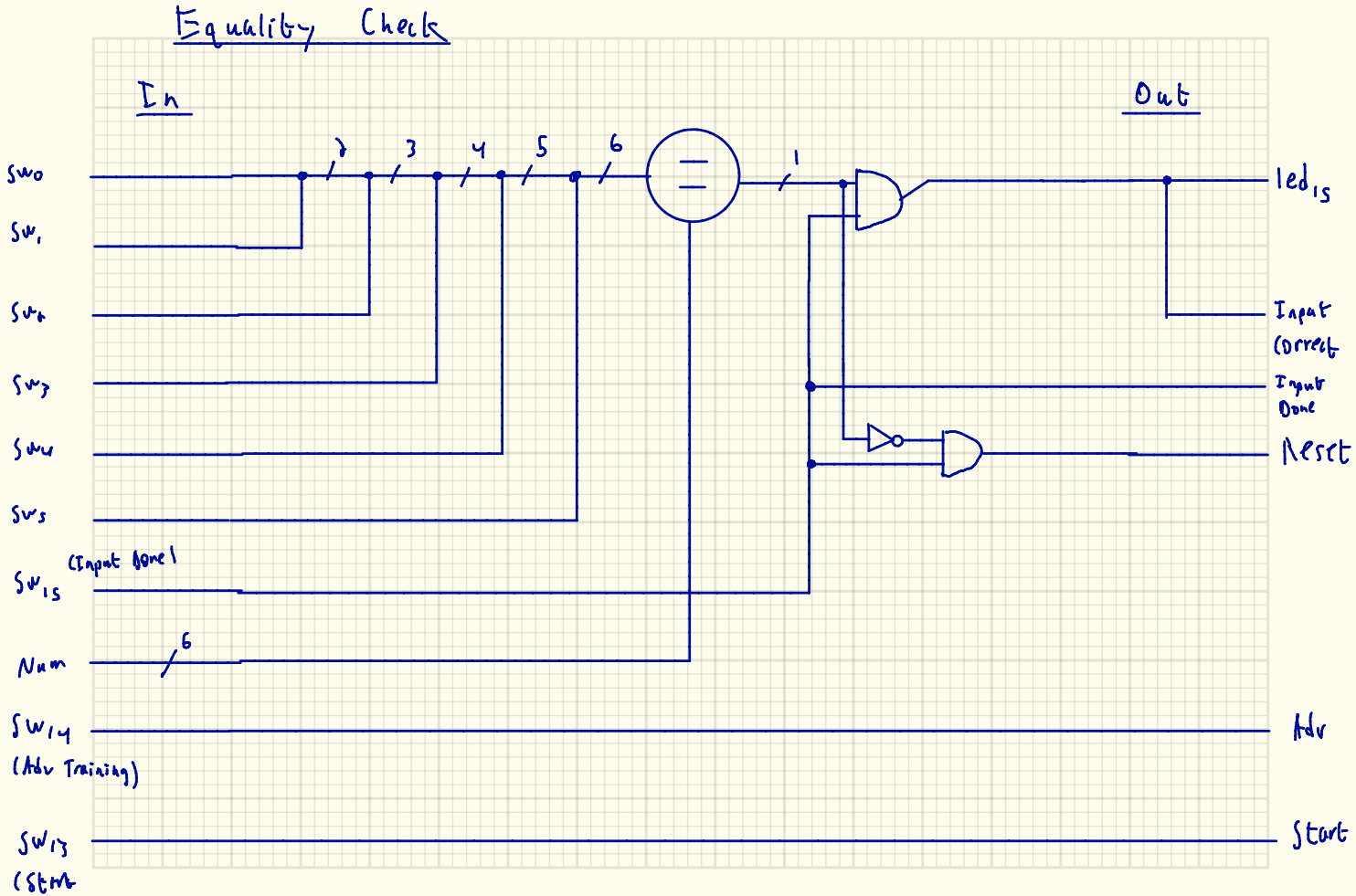
Out

See Implementation in Lab 3

Num is displayed on anode 0, 1

Win count is displayed on anode 2, 3



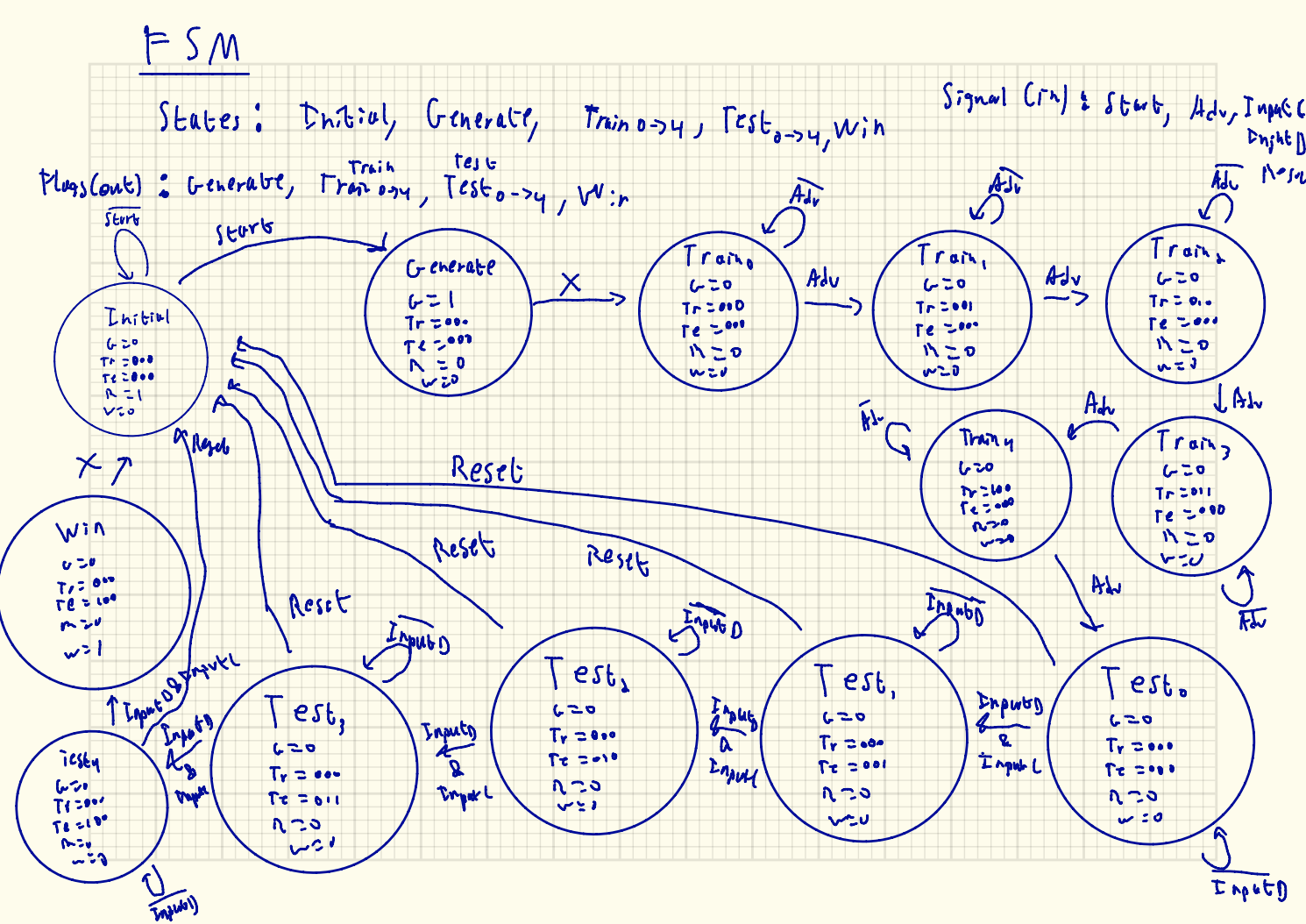

Equality Check
In
Out
Sw0
Sw1
Sw2
Sw3
Sw4
Sw5
Sw15
(Input done)
Num
Sw14
(Adv Training)
Sw13
(Start
1
2
3
4
5
6
6
1
led15
Input
correct
Input
Done
Reset
Adv
Start

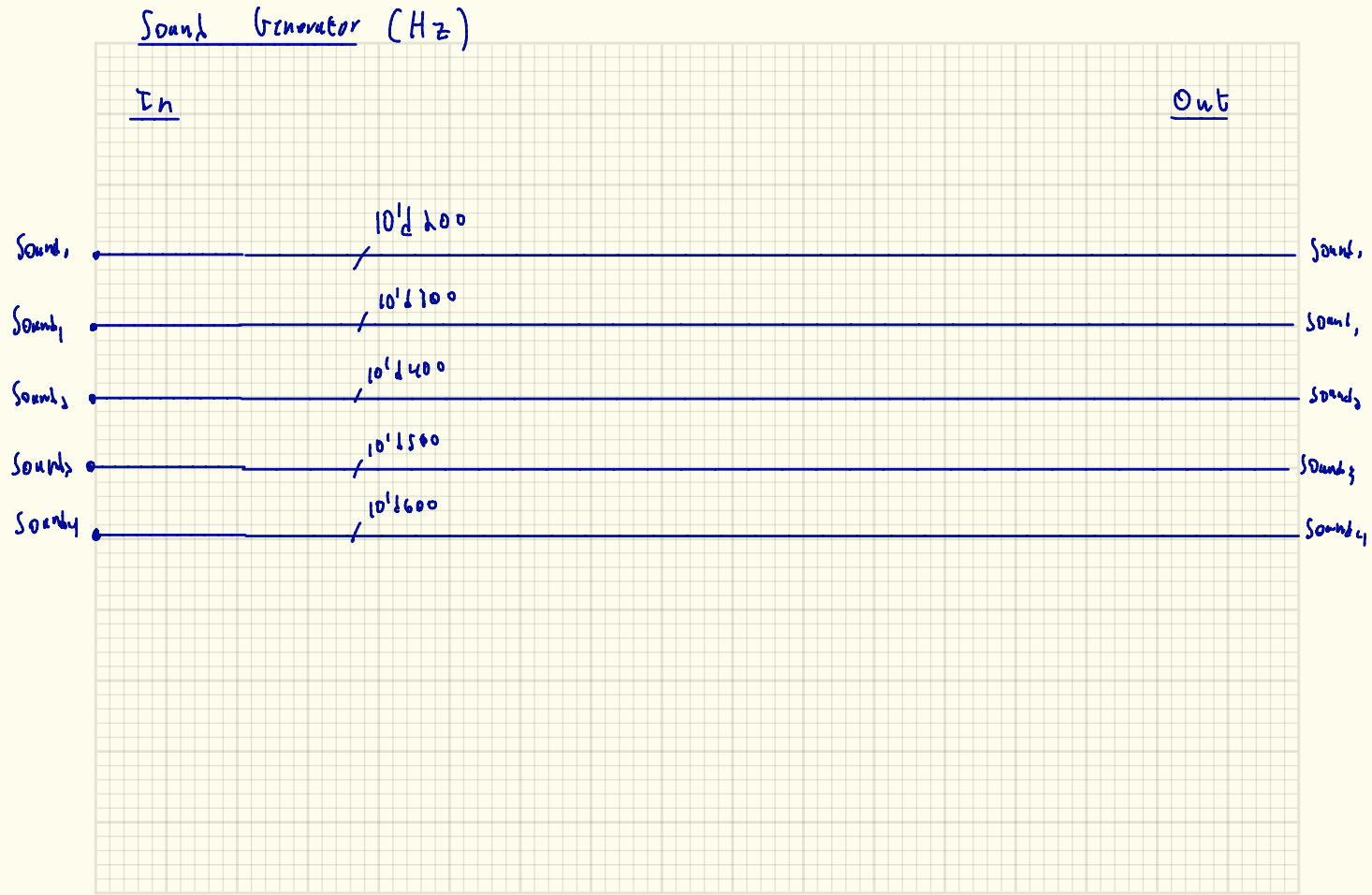
FSM

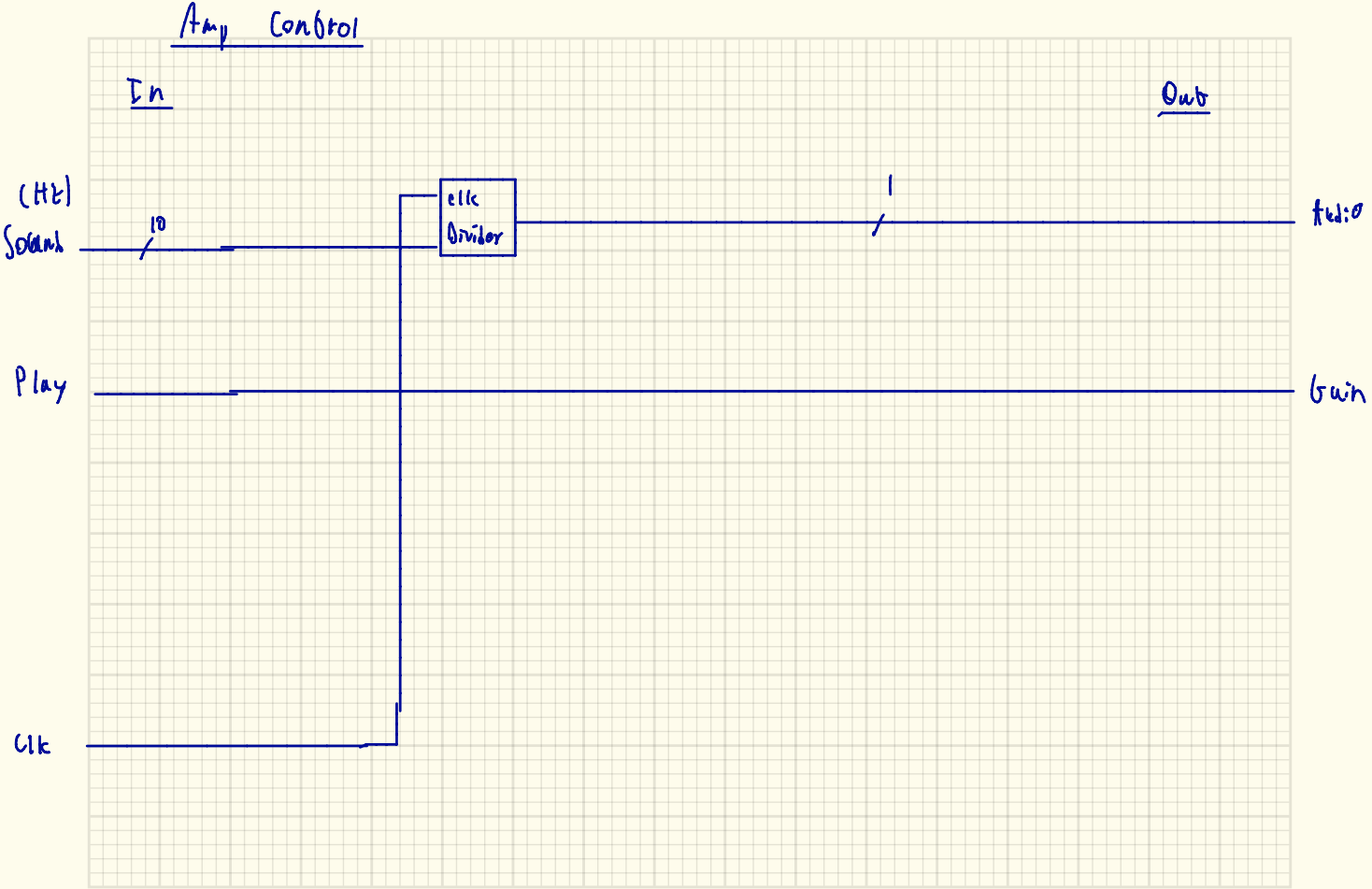
States : Initial, Generate, Train 0->4, Test 0->4, Win

Signal (in) : start, Adv, Input0, Input1

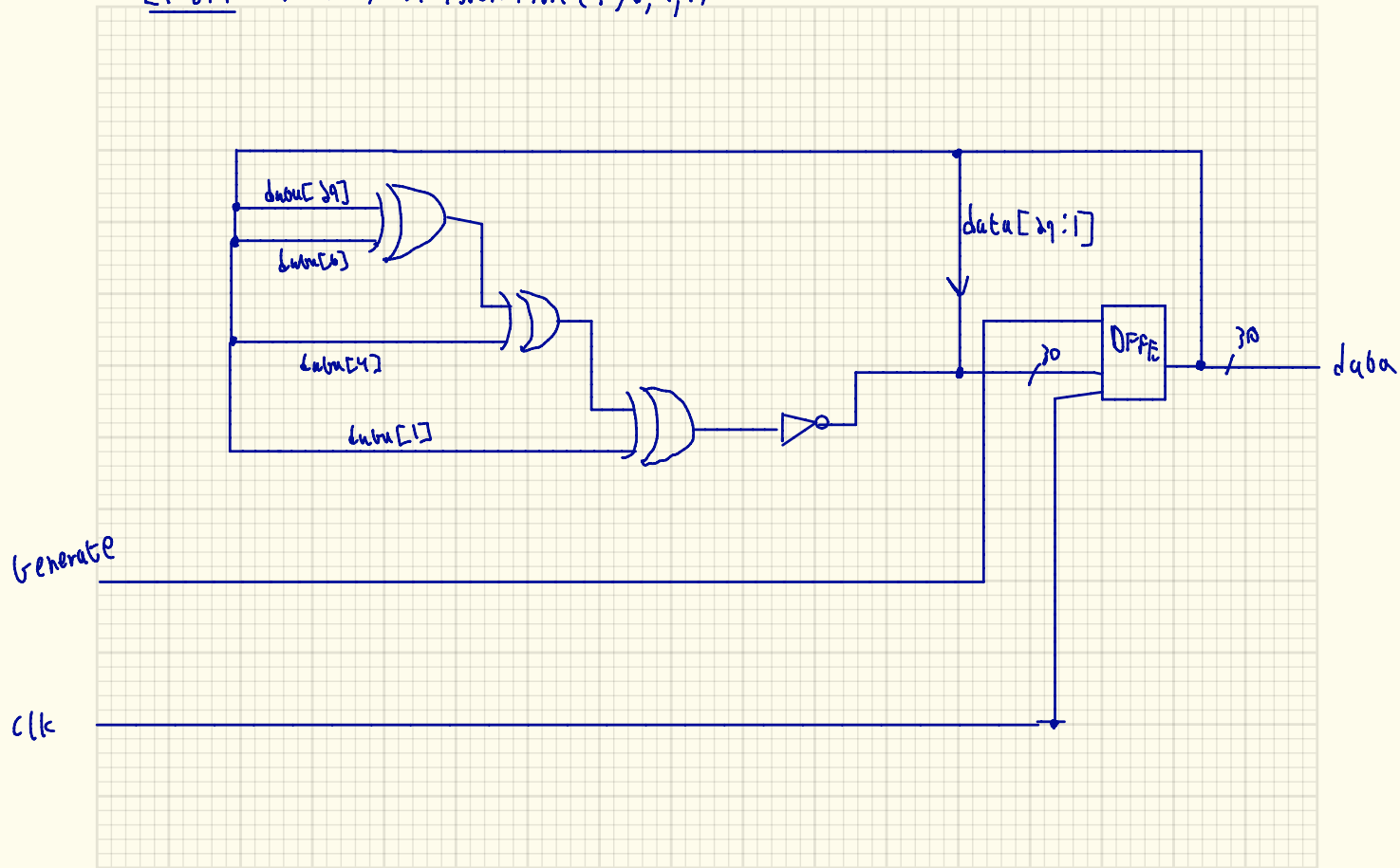
Plugs (out) : Generate, Train 0->4, Test 0->4, Win




Sound Generator (Hz)
In
Out
Sound0
Sound1
Sound2
Sound3
Sound4
10'd200
10'd300
10'd400
10'd500
10'd600
Sound0
Sound1
Sound2
Sound3
Sound4


Amp Control
In
Out
(Hz)
Sound
10
clk
Divider
1
freq
Play
Gain
clk

LFSR (30-bit) ∴ XNOR From (30, 6, 4, 1)



Circuit Diagram