eKT5201

Capacitive Touch Button Controller IC

Data Sheet

DOC. VERSION 1.5

(Applicable to eSenseIDE V1.2.12 & later)

ELAN MICROELECTRONICS CORP.

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Revision History

Doc. Version	Revision Description	Date
1.0	Initial Preliminary Release Version	2011/12/20
1.1	1. update the operating current 2. update the register description and error 3. add the 1Line application circuit	2012/2/14
1.2	Modify the shared ROM/RAM size	2012/6/13
1.3	1. Add the ordering information/Shipping Box Label	2012/08/25
1.4	1. Modify the circuit 2. Add the IDLD mode0 3. Modify the power consumption of Low power	2012/11/25
1.5	1. Add the “Recal” bit of address 0x05 in chap 6.7.5 2. Add the “SGPIO” bit of address 0x12 in chap 6.7.10 3. Modify the TPREQB hold time of I2C address 0x06 register in chap 6.7.6	2014/04/30

1 Introduction

The Capacitive Touch button IC is a microprocessor with 4kx15bit programmable ROM and 432 byte SRAM. It provides details on touch button application solutions based on eKT5201QN24/SO24 microcontroller device. The system application supports up to 16 touch buttons which can be applied to Two-Line type touch sensors. For function applications, the system provides I^2C Slave and Master interface communications with host. You can apply the system protocol to obtain legitimate touch button data from I^2C interface as well as attain complete control of the related peripheral components.

The application supports capacitive touch button with plastic or glass substrate. It can auto-calibrate the parameters for a wide range of capacitance on the touch button sensor.

2 Features

- **CPU Configuration:**
  - 4kx15bits on-chip ROM
  - 432 bytes SRAM
  - 8-level stacks for subroutine nesting
  - 3 programmable Level Voltage Reset
    LVR: 4.0V, 3.5V,&2.7V
  - Four CPU operating mode: Normal, Sleep, Green and IDLE
- **Operating Frequency:**
  - IRC mode**:**
    Main Oscillator**:** 4M/8M/6MHz
    Sub Oscillator**:** 16k/64k
- **Touch Operating Voltage Range:**
  - 2.8~5.5V at -25°C ~ 70°C
- **Peripheral Configuration:**
  - 8-bit real time clock/counter(TCC) with selective signal sources(Fm/Fs)
  - 2-channel Digital-to-Analog Converter for 256 steps
  - I^2C function
- **Touch Button Sensor:**
  - Power-on time: Stable time for operating < 500ms
  - The dependable cover thickness**:**

Type	Min. ~ Max.	Unit
Plastic	1~10	mm
Glass	1~10	mm

Suggestion : under 15x15mm pad size

  - Protocol operation mode support
- **Protocol Mode:**
  - Interface features**:** Standard I^2C @100K bps, Fast @400K bps
  - Up to 16 capacitive sensor buttons (QFN24)
  - Operating current**:** (@ 3.3V 8MHz)

Mode	Description	Power Consumption	Note
Normal	High scan rate without Sleep	3.4mA	@3.3V
Low Power	Idle & Normal modes (alternating)	< 300uA*	Dependent on user's setting
Sleep	Deep Sleep	< 2μA	IC only

* *These parameters are based on the IDLE time*

- **Package Type:**
  - 24 QFN 4x4x0.8mm: eKT5201QN24
  - 24 SOP: eKT5201SO24

NOTE

These are Green Products which do not contain hazardous substances.

3 Pin Assignment for Application

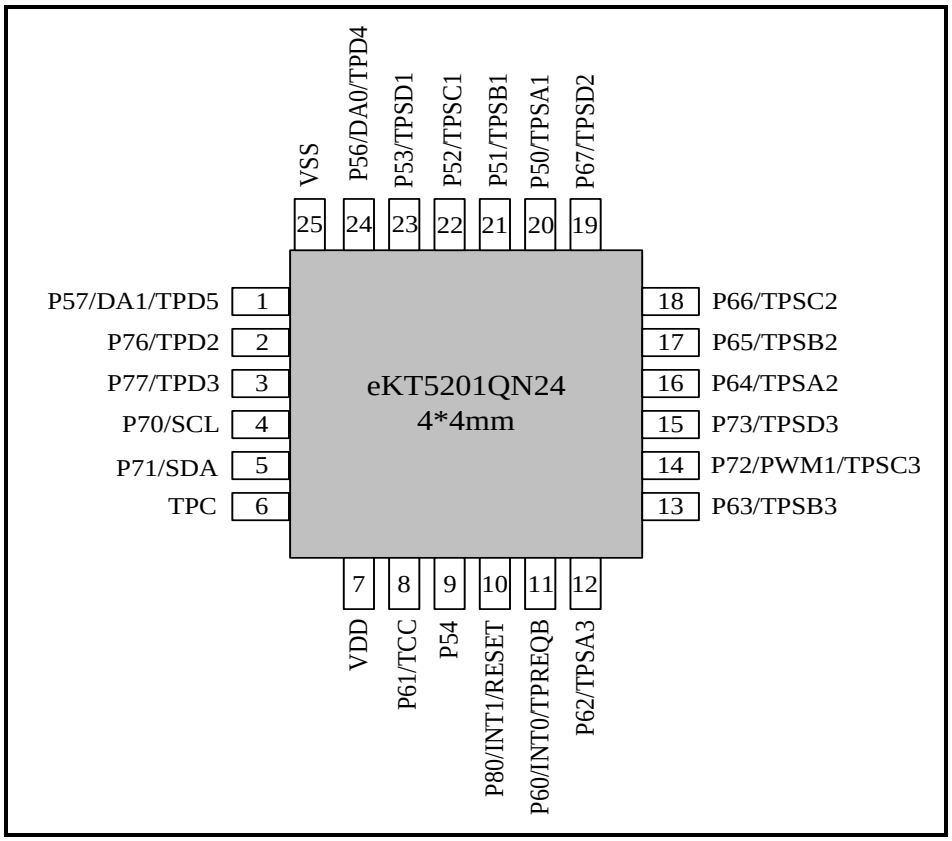

Figure 3-1a eKT5201QFN24 Pin Assignment

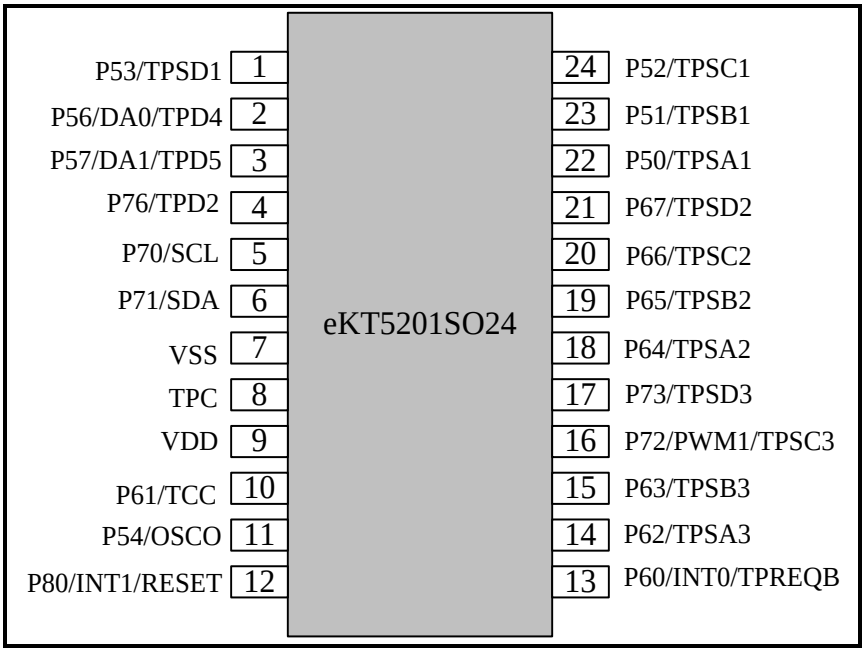

Figure 3-1b eKT5201SO24 Pin Assignment

4 Pin Description

4.1 eKT5201QN24

Symbol	DIR	Pin No.	Function Description
VDD	I	7	Power supply input
TPC	I	6	Touch Button external capacitor (1µf)
VSS	I	BACKSIDE	Ground input
Communication and OUT[n]			
P5x P6x P7x P8x	O	1, 2, 3 8, 9, 10 12 ~ 19 24	Supports a maximum of 16 touch buttons, and 15 of these buttons can be configured with their own output pin function. When one of the touch buttons is triggered, each one of the P5x~P8x becomes active high or active low according to the predefined buttton status. For different composite functions of each P5x~P8x, refer to the eKT5201 Microcontroller Specifications.
SDA, SCL	I/O	5, 4	I^2C communication bus. "Pull high" resistors are required for this bus.
TPREQB	O	11	■ **Power-On Mode:** *W*hen eKT5201 completes power-on initialitzation, TPREQB will shift to low and then returns to high after a few moments. ■ **Normal Mode:** TPREQB performs as Interrupt Signal pin. If TPREQB = **0**, eKT5201 is transmitting data. If TPREQB = **1**, eKT5201 has no data to transmit and is ready to receive command/data from host.
Touch Sensor Pins			
TPD[n]	O	1 ~ 3, 24	TouchKey driver pulse
TPSA[n]	I/O	12, 16, 20	Sensor pin of TouchKey Group A
TPSB[n]	I/O	13, 17, 21	Sensor pin of TouchKey Group B
TPSC[n]	I/O	14, 18, 22	Sensor pin of TouchKey Group C
TPSD[n]	I/O	15, 19, 23	Sensor pin of TouchKey Group D

4.2 eKT5201SO24

Symbol	DIR	Pin No.	Function Description
VDD	I	9	Power supply input
TPC	I	8	Touch Button external capacitor (1µf)
VSS	I	7	Ground input
Communication and OUT[n]			
P5x P6x P7x P8x	O	2 ~ 4, 10 ~ 21	Supports a maximum of 16 touch buttons, and 15 of these buttons can be configured with their own output pin function. When one of the touch buttons is triggered, each one of the P5x~P8x becomes active high or active low according to the predefined buttton status. For different composite functions of each P5x~P8x, refer to the eKT5201 Microcontroller Specifications.
SDA, SCL	I/O	5, 6	I^2C communication bus. "Pull high" resistors are required for this bus.
TPREQB	O	13	■ **Power-On Mode:** *W*hen eKT5201 completes power-on initialitzation, TPREQB will shift to low and then returns to high after a few moments. ■ **Normal Mode:** TPREQB performs as Interrupt Signal pin. If TPREQB = **0**, eKT5201 is transmitting data. If TPREQB = **1**, eKT5201 has no data to transmit and is ready to receive command/data from host.
Touch Sensor Pins			
TPD[n]	O	2 ~ 4	TouchKey driver pulse
TPSA[n]	I/O	14, 18, 22	Sensor pin of TouchKey Group A
TPSB[n]	I/O	15, 19, 23	Sensor pin of TouchKey Group B
TPSC[n]	I/O	16, 20, 24	Sensor pin of TouchKey Group C
TPSD[n]	I/O	17, 21, 1	Sensor pin of TouchKey Group D

5 General Terms Description

5.1 Power Pin

The VDD pin should be connected to the power source through the C1 and C2 capacitors, then to ground. Take note that the ground pin is located at the back side of the package. Hence, no physical GND pin exists on the front side.

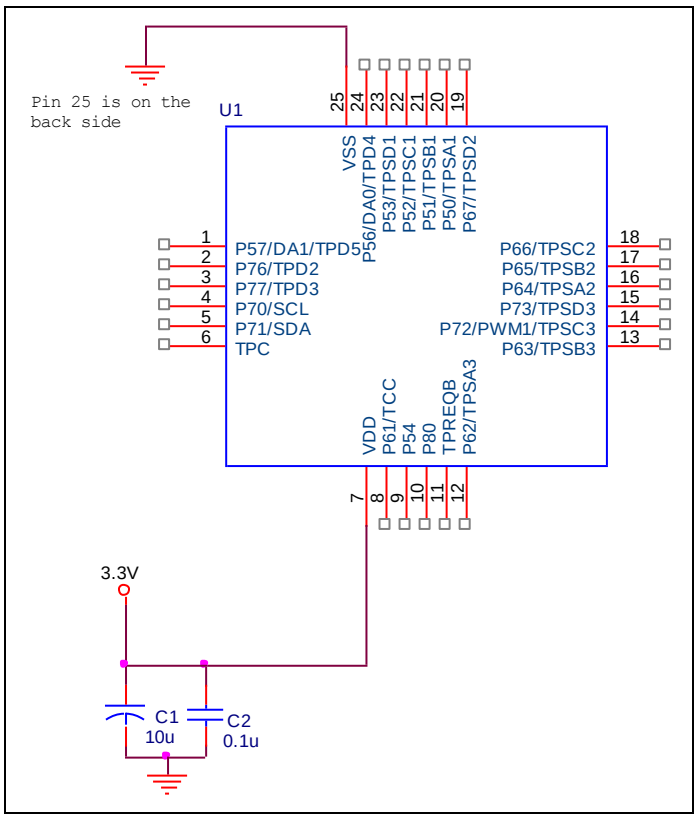

Figure 5-1 Power Pins Connection

5.2 Touch Sensor Pin and Control Pin

5.2.1 Two-Line Type Touch Sensor Pin

The eKT5201 provides up to 16 touch buttons for users application programming. For maximum 16 touch buttons application, 4 driving pins (TPD[n]) and 4 sensor pins (TPSx[n]) are used from eKT5201. Sensor groups from A to D can be activated together. To achieve the maximum 16 touch buttons application only needs 4 times scanning. The scanning sequence for driving pins is always from TPD4, TPD5, TPD2, and TPD3. For sensor group, it is from TPSA1 to TPSD1.

The Figure 5-2 below is a 16-button example which shows TPD2~TPD5 are driving pins and TPSA1~TPSD1 are sensor pins. The sequence should be the TPD4 and TPSA1~TPSD1 are scanned first, followed by TPD5 and TPSA1~TPSD1, then TPD2 and TPSA1~TPSD1 and TPD3 with TPSA1~TPSD1 scanned last. However, when the defined touch buttons are less than 16, the Driving Pins TPD2 and TPD3 are not used. These pins become free I/O's which can be switched as OUT 0/1 and thus, increase the available output pins number.

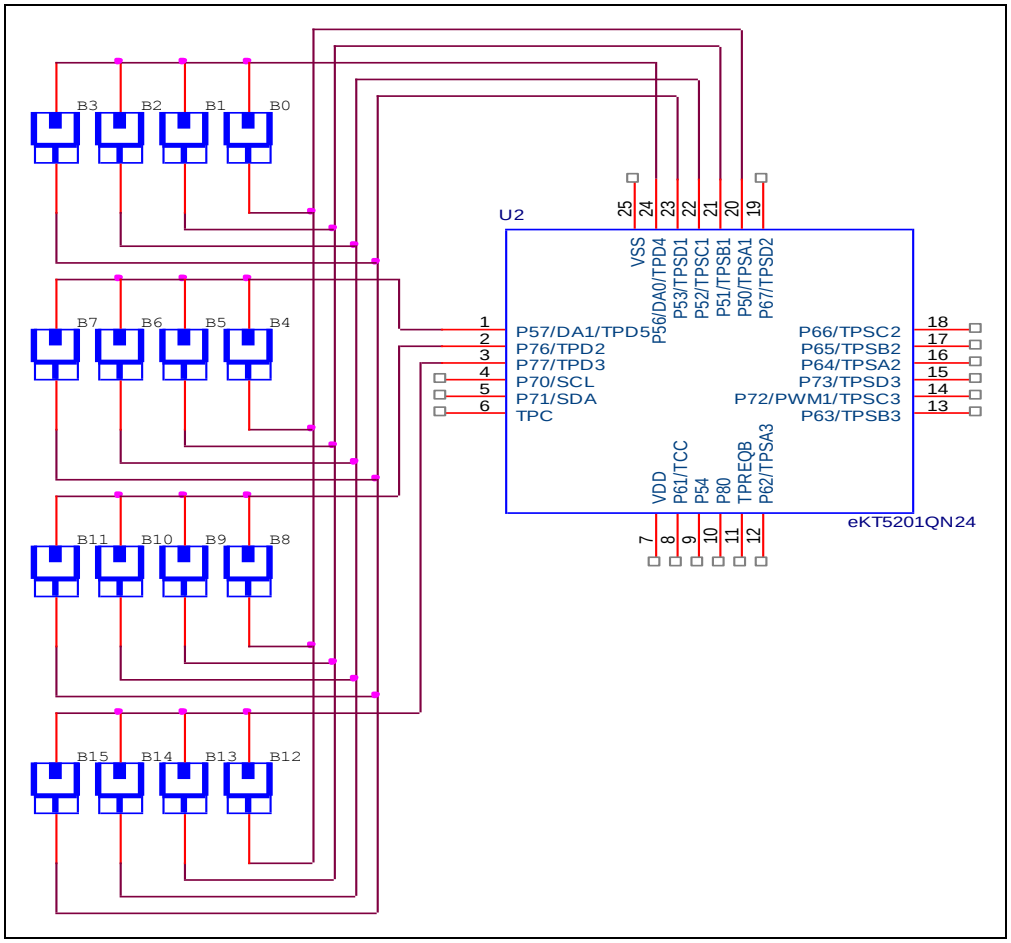

Figure 5-2 Two-Line Type Sensor Group and Driving Pin Connections for 16 Touch Buttons

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5.2.2 One-Line Type Touch Sensor Pin

The eKT5201 also supports One-Line buttons type which provides 12 sensor pins for user's programming application. The following (Figure 5-3) depicts a simple case of 4 touch buttons with Active Shield (AS) function that protects the system against environmental noise. User can activate this function with Register 0x13 (see Section 6.7.11). Either AS pin or GND pin can be used for noise shielding feature, however, both pins (AS and GND pins) cannot be connected together. The scanning sequence for One-Line type sensor group always starts from TPSA1 to TPSD1, then TPSA2 to TPSD2, TPSA3 to TPSD3.

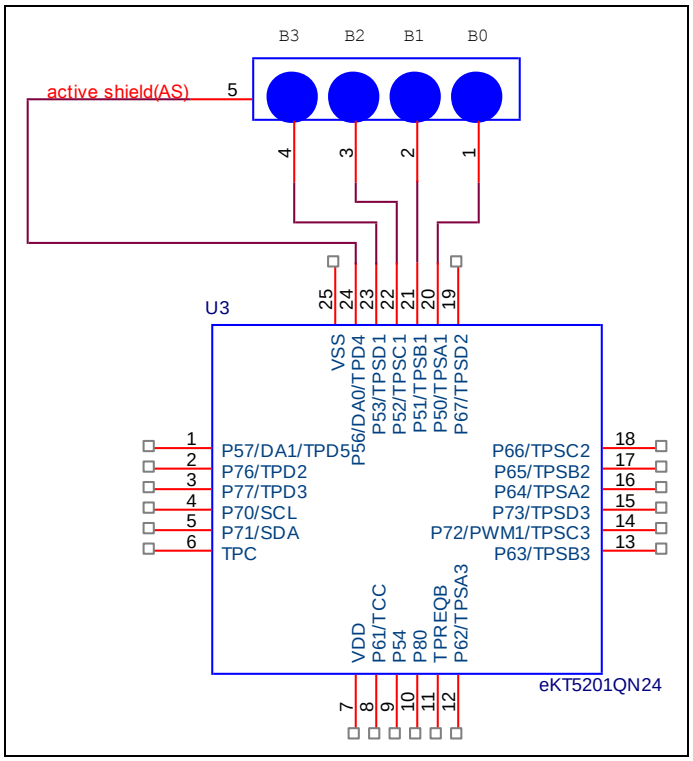


Figure 5-3 One-Line Type Sensor Group Connections for 4 Touch Buttons

5.2.3 Correlation between Touch Buttons and Output Pins

Each of the total 15 port P5x~P8x can be designated with its own output pin after user have configured the I/O's accordingly. User can define the LED display status relative to logic-high or logic-low operation when a finger tip touches or is removed from the touch button. The following figure shows the general usage of the output pins.

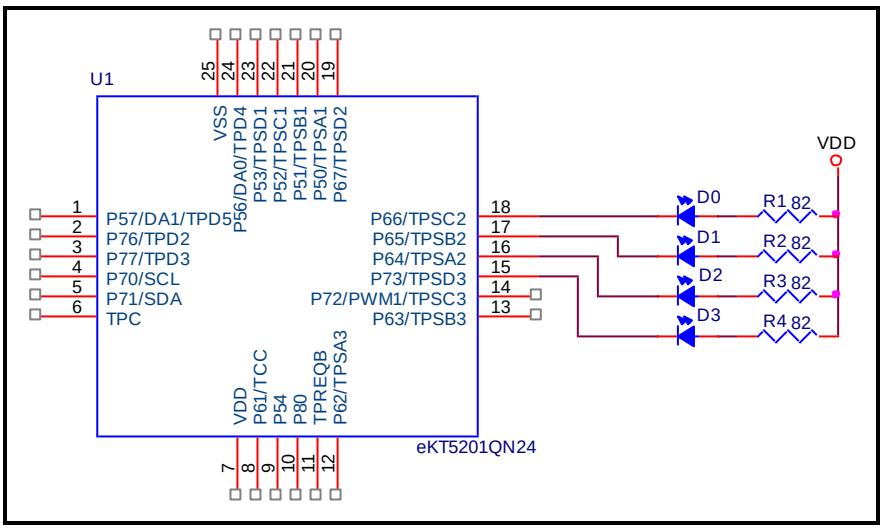


Figure 5-4 Correlation between Touch Buttons and LED display

6 I²C Protocol

The eKT5201 supports standard I²C protocol (SCL, SDA) and a request signal (TPREQB). Figure 6-1 below shows the system block diagram of I²C Slave interface.

The host can read or write eKT5201 via I²C protocol. eKT5201 is always a Slave device. Under I²C Slave interface, the SCL and SDA signals should be pulled high with resistors at the host end. In general, the resistance of the termination Resistors R1 and R2 is from 1kΩ to 10kΩ and appropriate resistance should be selected to accommodate the specified rise times on SCL and SDA. The host processor has to provide a serial clock signal (SCL) to eKT5201. If eKT5201 has a message for the host, TPREQB will send a falling edge signal to indicate transmit request.

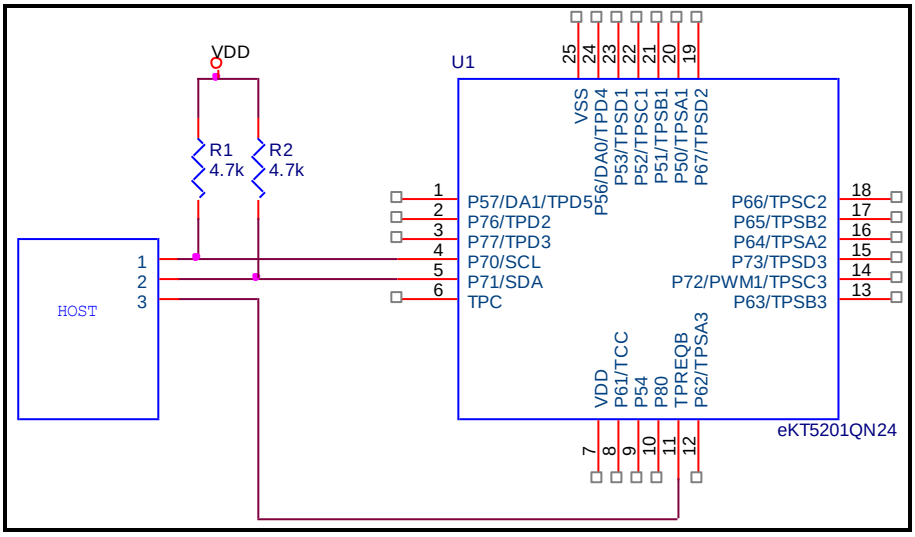


Figure 6-1 eKT5201 Connects to Host through I²C Interface

6.1 I²C Operation

All communications start from a START condition and followed by Slave address packet. The address packet is 9 bits long, consisting of 7 Slave address bits, one READ/WRITE control bit, and an acknowledge bit. When the touch button controller detects that it is being addressed, it will acknowledge by pulling SDA to low in the 9th SCL (ACK) cycle. All data packets are 9 bits long, consisting of one data byte and an acknowledge bit. An Acknowledge (ACK) is initiated by the Receiver by pulling the SDA line to low during the 9th SCL cycle. If the Receiver keeps the SDA line at high, a NACK signal is sent. Each write or read cycle must end with a STOP condition.

Figures 8-2a and 8-2b below illustrate the bit level waveform of I²C Master Write/Read data to/from I²C Slave device with 7-bit addressing mode. When R/$\overline{W}$ bit is set to "**0**", and the Slave address is verified, the I²C Master is able to write data to I²C Slave. On the other hand, when R/$\overline{W}$ bit is set to "**1**" and the Slave address is verified, the I²C Master is able to read data from I²C Slave. If the Slave address verification is in error, I²C Slave will not work.

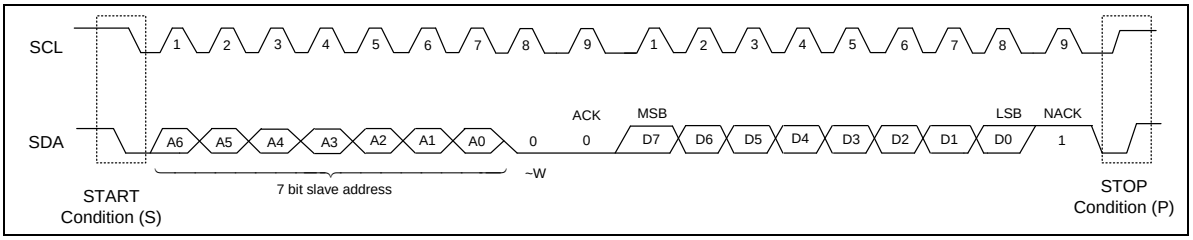


Figure 6-2a I²C Master Writing Data to I²C Slave (R/$\overline{W}$=0) Bit Level Waveform

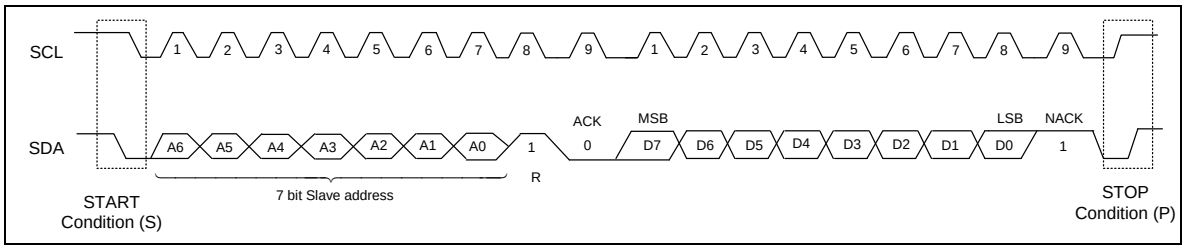


Figure 6-2b I²C Master Reading Data from I²C Slave (R/$\overline{W}$=1) Bit Level Waveform

The I²C bit level waveform shown in the above figures are supported by eKT5201. The eKT5201 touch button controller is defined as a Slave device of I²C while the host is defined as a Master. The touch button controller device address is defined as 7-bit address format.

NOTE

- *The eKT5201 default Slave address is 0110 000.*
- *If to have many masters in I²C system, the masters must support arbitration function.*

6.2 Writing to eKT5201

The eKT5201 supports I²C write protocol. The first byte of a write access is the command code. The next one or "n" bytes, respectively, are the data to be written. The eKT5201 acknowledges each byte, and the entire transaction is completed with a STOP condition.

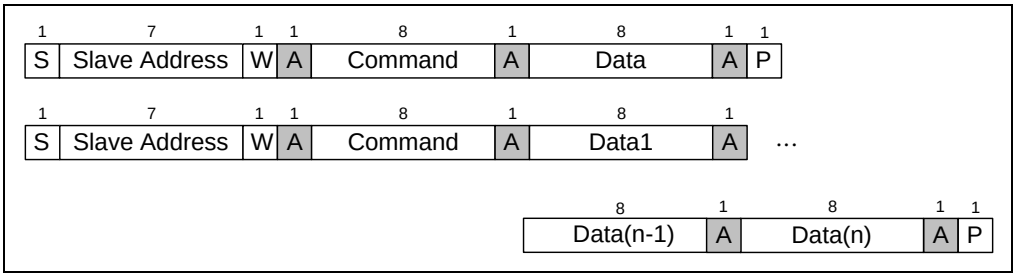


Figure 6-3 Single and Continuing Write Modes

6.3 Reading from eKT5201

Reading data is slightly more complicated than writing data. First the host must write an instruction to the eKT5201. Then, it follows the instruction with a repeated START condition to indicate the host is ready to read from the Slave address. The eKT5201 then, returns one or "n" bytes of data to host. Note that a NACK signifies the end of the read transfer.

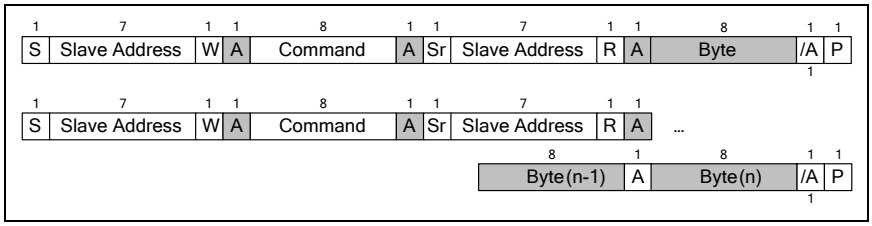


Figure 6-4 Single and Continuing Read Modes

6.4 Timing Conditions

The following figure shows the timing condition and characteristics of the I²C interface. The eKT5201 adopts a bit rate of up to 400k bit/sec.

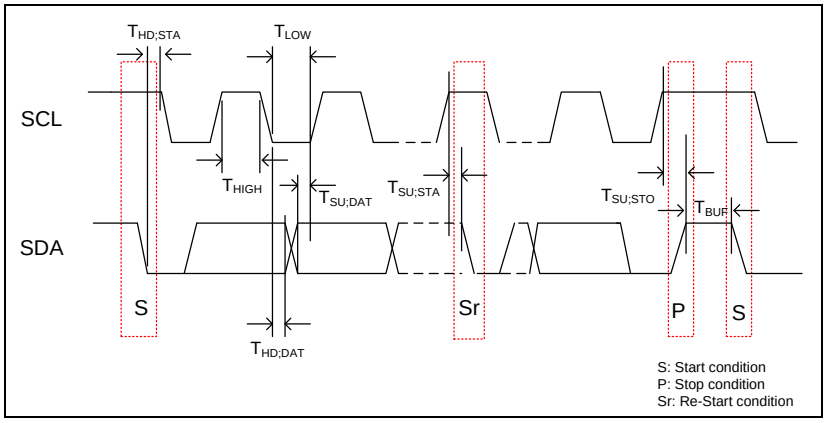


Figure 6-5 I²C Interface Timing Diagram

6.4.1 I²C Interface SDA and SCL Pin Characteristics

Symbol	Description	Standard Mode		Unit
		Min.	Max.	
f_{SCL}	SCL clock frequency	-	100	kHz
$T_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	5	-	µs
T_{LOW}	LOW period of the SCL clock	5	-	µs
T_{HIGH}	HIGH period of the SCL clock	5	-	µs
$T_{SU;STA}$	Set-up time for a repeated START condition	5	-	µs
$T_{HD;DAT}$	Data hold time	5	-	µs
$T_{SU;DAT}$	Data set-up time	3.6	-	µs
$T_{SU;STO}$	Set-up time for STOP condition	6	-	µs
T_{BUF}	Bus free time between a STOP and START condition	5.2	-	µs

Symbol	Description	Standard Mode		Unit
		Min.	Max.	
f_{SCL}	SCL clock frequency	-	400	kHz
$T_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	1	-	µs
T_{LOW}	LOW period of the SCL clock	1.5	-	µs
T_{HIGH}	HIGH period of the SCL clock	1	-	µs
$T_{SU;STA}$	Set-up time for a repeated START condition	1	-	µs
$T_{HD;DAT}$	Data hold time	-	-	µs
$T_{SU;DAT}$	Data set-up time	200	-	ns
$T_{SU;STO}$	Set-up time for STOP condition	1	-	µs
T_{BUF}	Bus free time between a STOP and START condition	1.5	-	µs

6.5 TPREQB Pin

The TPREQB pin is used to automatically alert the host of any changes with any of the button status, thus minimizing the need of unnecessary I^2C communications. After power-on of the touch button controller, the host need not communicate with the device unless the TPREQB pin goes active. The TPREQB will only become inactive again when the host performs a read byte/word. The eKT5201 provides two types of TPREQB operation modes. You can decide which one to use to satisfy the hold-system request.

6.5.1 TPREQB Low-Active Mode:

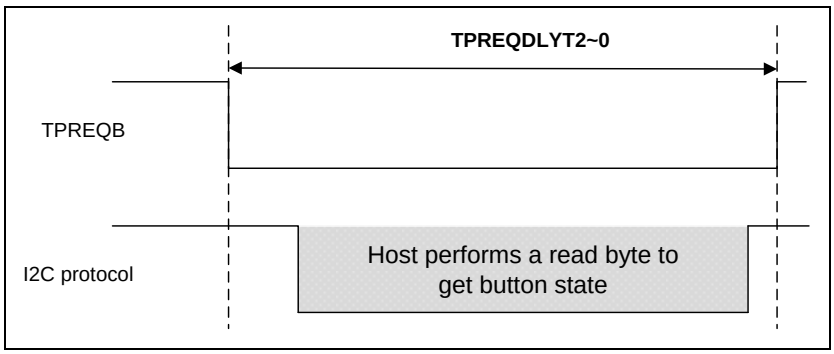


Figure 6-6 TPREQB Signal Recovered underTPREQDLYT2~0

The TPREQB state is Normal High or Normal Low with different settings. For example, if the touch button controller detects any change with the button status (TPREQDLYEN=1), it will pull the TPREQB signal to Low first, and starts the TPREQB timer. TPREQB will then return to High until the TPREQB timer time-out occurs. If TPREQB time duration is set too long, TPREQB will still stay at Low state even if the

I^{2}C communication is already finished. The suitable timing value for TPREQB pin is configured with Bit0 ~ Bit2 of Address 0x06 (see Section 8.7.6) which is very important under TPREQB low-active mode.

6.5.2 TPREQB Waiting Mode:

The TPREQB state is Normal High or Normal Low with different settings. For example, if the touch button controller detects any change with the button status, (TPREQDLYEN=0), it will pull the TPREQB signal to Low first. After the host performs a read byte/word from touch button controller, the touch button controller will pull-high the TPREQB signal again. If the host is not performing read procedure, the TPREQB will always stay at low state.

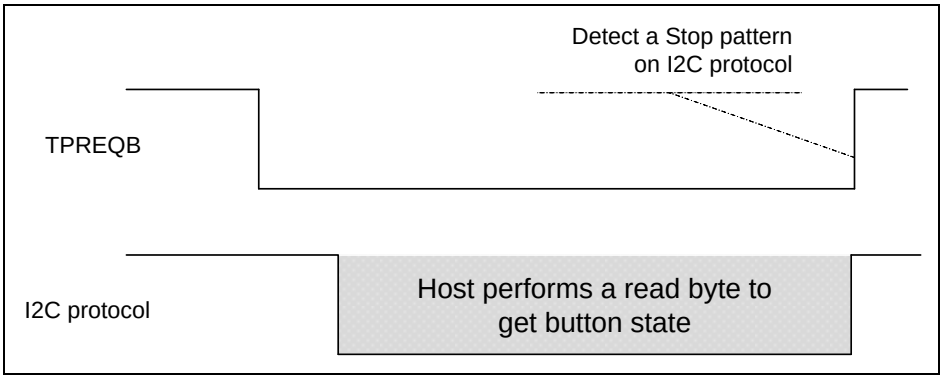


Figure 6-7 TPREQB Signal under TPREQDLYEN=0

6.6 Map Registers Commands Summary

The Host controls the Slave Touch button IC via the following commands**:**

Command (I^2C Address)	Access Direction	Description
0x00	R	Product ID **(PDID)**
0x01	R	BOP Version **(BOPVN)**
0x02	R	Serial Number **(SERNB)**
0x03	R	Firmware Version **(FMVN)**
0x05	R/W	General configure **(GERCON)**
0x06	R/W	TPREQB configure **(TPQCON)**
0x09	R	TPERR bit **(TPERR)**
0x11	R	I^2C Slave address L **(I2CSL)**
0x12	R/W	Touch configure mode **(TPMSMODE)**
0x13	R/W	Touch driver enable bit **(TPIODRV)**
0x14	R/W	Touch sense enable bit **(TPIOSENS)**
0x15	R/W	Touch Sensitivity1 set **(TPSIGAIN1)**
0x16	R/W	Touch Sensitivity2 set **(TPSIGAIN2)**
0x17	R/W	Touch Speed set **(TPSSPEED1)**
0x18	R/W	Touch Speed set **(TPSSPEED2)**
0x19	R/W	Touch button quantity **(TPKEYQUTY)**
0x20	R	Button Status0 **(KEY_MAP0)**
0x21	R	Button Status1 **(KEY_MAP1)**
0x24	R/W	Button operation mode **(KEYOPER)**
0x25	R/W	System operation mode **(SYSOPER)**
0x26	R/W	Button de-bounce **(KEYDEBMS)**
0x30~0x3F	R/W	Trigger level adjustment **(FTN_X)**

6.7 Registers Description

6.7.1 Address 0x00: Product ID

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Product ID							
R-0	R-1	R-0	R-1	R-0	R-0	R-1	R-0

Bit 7~0 (Product ID_0): Product ID is 0x52

6.7.2 Address 0x01: BOP Version

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BOP Version							
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7~0 (Code Version): All 8 bit registers are definable. User may check the BOP version number anytime. Note that the eSense IDE will automatically load the BOP version into the register.

6.7.3 Address 0x02: Serial Number

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Serial Number							
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-1

Bit 7~0 (Serial Number): Serial Number is 0x01

6.7.4 Address 0x03: Firmware Version

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Firmware Code Version							
R	R	R	R	R	R	R	R

Bit 7~0 (Firmware Code Version): All 8 bit registers are definable. User may check the firmware version number anytime.

6.7.5 Address 0x05: General Configuration

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SReset	ReCal	-	ReBuild	-	-	-	-
R/W-0	R/W-0	R-0	R/W-0	R-0	R-0	R-0	R-0

Bit 7 (SReset): Software reset. When this bit is set to "**1**", Reset function is executed immediately and clears the bit to "**0**" after reset is completed.

0: Reset completed

1: Execute reset

Bit 6 (ReCal): This bit is used to recalibrate the sensor basic capacitance to adjust and compensate capacitance shift due to change of environment. If ReCal bit is set from "**0**" to "**1**", it will recalibrate immediately and then return to "**0**" to complete the process.

0: ReCal completed

1: Execute ReCal

Bits 5, 3 ~ 0: Not used bits. Set to "**0**" all the time.

Bit 4 (ReBuild): TouchKey pin assignment and function mode configuration. This bit also includes the Recalibration to adjust sensor basic capacitance change due to environment change as stated above (Bit 6).

When ReBuild bit is set, the TouchKey pin and functions will run according to defined modes. After the host changes the TouchKey configuration contents of Address 0x00~0x1F (by setting ReBuild bit from "**0**" to "**1**"), the TouchKey pin assigned structure will rearrange immediately. Then the ReBuild bit will return to "**0**" when the change is completed.

0: ReBuild completed

1: Execute ReBuild

NOTE
Registers 0x00~0x1F (see Sections 6.7.1 ~ 6.7.19) must rebuild after change.

6.7.6 Address 0x06: TPREQB Pin Configuration

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPREQIO	-	-	-	TPREQDLYEN	TPREQDLYT2	TPREQDLYT1	TPREQDLYT0
R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

If the bits are "**1**", user needs to modify the relevant register to avoid Touch error.

Bit 7 (TPREQBIO): Switch between TPREQB Function and P60. If not to use the TPREQB, the pin can be as GPIO.

0: TPREQB Function

1: P60

Bits 6~4: Not used bits. Set to "**0**" all the time.

Bit 3 (TPREQDLYEN): TPREQB pin delay function control bit

0: Disable

1: Enable

Bit 2 ~ 0 (TPREQDLYT2~0): TPREQB pin status on hold timer

Delay time = $2^{\wedge(N-1)}$*Tbase (where Tbase is 10 msec,

N is TPREQDLYT [2:0].)

TPREQDLYT2	TPREQDLYT1	TPREQDLYT0	Tsec	Note
0	0	0	Tbase/2	Tbase = 10 msec
0	0	1	Tbase*1	-
0	1	0	Tbase*2	-
0	1	1	Tbase*4	-
1	0	0	Tbase*8	-
1	0	1	Tbase*16	-
1	1	0	Tbase*32	-
1	1	1	Tbase*64	-

6.7.7 Address 0x09: TPERR Bit

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	TPTR	TPOV	-
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

If the bits are "**1**", user needs to modify the relevant register to avoid Touch error.

Bits 7~3, 0: Not used bits. Set to "**0**" all the time.

Bit 2 (TPTR): Touch transfer error. Need to increase **Register 0x17, 0x18** Touch transfer time (see Section 6.7.14/6.7.15).

Bit 1 (TPOV): Touch gain overflow. Need to increase fraction factor of **Registers 0x15 & 0x16** Touch Sensitivity (**SST1, SST2_MT, & SST2_FC**). For example; from 1/4 to 1/8 (see Section 6.7.12/6.7.13).

6.7.8 Address 0x11: I²C Slave Address L

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
R-0	R-0	R-1	R-1	R-0	R-0	R-0	R-0

Bits 7(IA7): Reserved bit. Set to "0" all the time.

Bit 6 ~ 0 (IA6~0): eKT5201 Device Slave address. Default is 0x30

6.7.9 Address 0x12: Touch Configuration Mode

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MXM		-	-	-	-	-	SGPIO
R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R/W-0

The register must match with proper button sensor type on PCB.

Bit 7 ~ 6 (MXM): Set eKT5201 button types**:**

MXM	Description	Note
00	Two-Line mode	
01	One-Line mode	
10	Reserve	
11	X	

Bit 5 ~ 1: Not used bits. Set to "**0**" all the time.

Bit 0 (SGPIO): Set the default low status GPIO or skip the default IO setting.

The default GPIO can prevent environmental noise and provide ESD protection. And if the GPIO is not used, the circuit must be connected to GND.

0: Set the default GPIO value from LIB

1: Skip LIB default GPIO setting (user has to set his own default setting)

6.7.10 Address 0x13: Touch Driver Pin Enable Bit

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	DR5EN	DR4EN	DR3EN	DR2EN	-	-
R-0	R-0	WR-0	WR-0	WR-0	WR-0	R-0	R-0

Bit 7 ~ 6: Not used bits. Set to "**0**" all the time.

Bit 5 ~ 2 (DR5EN ~ DR2EN): Touch driver pin enable bits. If disabled, the pin functions as GPIO.

MXM	Bit	QN24 Description		SOP24 Description	
10/11	DR4EN=x	Pin24 = P56/DA0		Pin2 = P56/DA0	
	DR5EN=x	Pin1 = P57/DA1		Pin3 = P57/DA1	
	DR2EN=x	Pin2 = P76		Pin4 = P76	
	DR3EN=x	Pin3 = P77		-	
		X=1	X=0	X=1	X=0
00	DR4EN=x	Pin24 = TPD4	Pin24 = P56/DA0	Pin2 = TPD4	Pin2 =P56/DA0
	DR5EN=x	Pin1 = TPD5	Pin1 = P57/DA1	Pin3 = TPD5	Pin3 = P57/DA1
	DR2EN=x	Pin2 = TPD2	Pin2 = P76	Pin4 = TPD2	Pin4 = P76
	DR3EN=x	Pin3 = TPD3	Pin3 = P77	-	-
01	DR4EN=x	Pin24 = AS1	Pin24 = P56/DA0	Pin2 = AS1	Pin2 = P56/DA0
	DR5EN=x	Pin1 = AS2	Pin1 = P57/DA1	Pin3 = AS2	Pin3 = P57/DA1
	DR2EN=x	Pin2 = AS3	Pin2 = P76	Pin4 = AS3	Pin4 = P76
	DR3EN=x	No used	Pin3 = P77	-	-

NOTE

The MXM is the Address 0x12 TP mode

Bit 1 ~ 0: Not used bits. Set to "**0**" all the time.

6.7.11 Address 0x14: Touch Sense Pin Enable Bit

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEN3EN	SEN2EN	SEN1EN	-	-	-	-	-
R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0

Bit 7 (SEN3EN): TPSA3~TPSD3 enable control bits. If disabled, the pin functions as GPIO.

0: Disable

1: Enable TPSA3 ~ TPSD3

SEN3EN	QN24 Pin Description	SO24 Pin Description
0	Pin12 = P62	Pin14 =P62
	Pin13 = P63	Pin15 = P63
	Pin14 = P72	Pin16 = P72
	Pin15 = P73	Pin17 = P73
1	Pin12 = TPSA3	Pin14 = TPSA3
	Pin13 = TPSB3	Pin15 = TPSB3
	Pin14 = TPSC3	Pin16 = TPSC3
	Pin15 = TPSD3	Pin17 = TPSD3

Bit 6 (SEN2EN): TPSA2~TPSD2 enable control bits. If disabled, the pin functions as GPIO.

0: Disable

1: Enable TPSA2~TPSD2

SEN2EN	QN24 Pin Description	SO24 Pin Description
0	Pin16 = P64	Pin18 = P64
	Pin17 = P65	Pin19 = P65
	Pin18 = P66	Pin20 = P66
	Pin19 = P67	Pin21 = P67
1	Pin16 = TPSA2	Pin18 = TPSA2
	Pin17 = TPSB2	Pin19 = TPSB2
	Pin18 = TPSC2	Pin20 = TPSC2
	Pin19 = TPSD2	Pin21 = TPSD2

Bit 5 (SEN1EN): TPSA1~TPSD1 enable control bits. If disabled, the pin functions as GPIO.

0: Disable

1: Enable TPSA1~TPSD1

SEN1EN	QN24 Pin Description	SO24 Pin Description
0	Pin20 = P50	Pin22 = P50
	Piin21 = P51	Piin23 = P51
	Pin22 = P52	Pin24 = P52
	Pin23 = P53	Pin1 = P53
1	Pin20 = TPSA1	Pin22 = TPSA1
	Pin21 = TPSB1	Pin23 = TPSB1
	Pin22 = TPSC1	Pin24 = TPSC1
	Pin23 = TPSD1	Pin1 = TPSD1

Bit 4~0: Not used bits. Set to "**0**" all the time.

6.7.12 Address 0x15: Touch SENSITIVITY1 SET

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SST1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 ~ 0 (SST1): Touch sensitivity level selection; **0** is lowest, and **255** is highest. For instance thick cover needs higher sensitivity level, while thin cover requires lower level. This setting will also impact Touch execution time, i.e., higher SST1 needs longer Touch execution time, hence the button response is slower.

6.7.13 Address 0x16: Touch SENSITIVITY2 SET

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	SST2_MT		-	SST2_FC		
R-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 6: Not used bits. Set to "**0**" all the time.

Bit 5 ~ 4 (SST2_MT): SST2_MT is the magnification of SST1 which is used for rough sensitivity adjustment. It has three levels of magnification as shown below**:**

SST2_MT	Description
00	1
01	2
10	4
11	

Bit 3: Not used bits. Set to "**0**" all the time.

Bit 2 ~ 0 (SST2_FC): Touch sensitivity fraction table select bits with a total of 0~7 levels available selections as shown in the table below. The higher the SST2_FC value, the lower the sensibility will be, while the stability becomes higher. In contrary, the lower the SST2_FC value, the higher is the sensibility will be, while the stability becomes lower. The recommended value is **5** (1/28).

$$SENSITIVITY = (SST1 * SST2\_MT + 20) * SST2\_FC$$

SST2_FC	Description	Sensitivity/Stability Level
0	1/2	Highest sensitivity, Lowest stability
1	1/4	
2	1/8	
3	1/16	
4	1/24	
5	1/28	
6	1/32	
7	1/36	Lowest sensitivity, Highest stability

NOTE
If used with 2-Line configuration, the SST2_FC value of 0~3 is recommended.

6.7.14 Address 0x17: Touch SPEED1 Setting

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPP_SE				SPP11	SPP10	SPP9	SPP8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 ~ 4 (SPP_SE): Touch transfer setup time setting. Each transfer needs an initial setup time, and larger trace (route) requires longer setup time.
A total of 16 levels can be set, "**0**" is the shortest and "**15**" is the longest. The longer the setup time, the better the Touch data can be.

$$SPEED\_Setup = (10\mu s + SPP\_SE * 0.5\mu s)$$

Bit 3 ~ 0 (SP11~8): Touch high speed transfer time; 11 ~ 8bit

6.7.15 Address 0x18: Touch SPEED2 Setting

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPP7	SPP6	SPP5	SPP4	SPP3	SPP2	SPP1	SPP0
W/R-0	W/R-0	W/R-0	W/R-0	W/R-0	W/R-0	W/R-0	W/R-0

Bit 7 ~ 0 (SP7~0): Touch transfer time setting. A total of 12 bits (SP11 ~ 0) range can be set; 0xFFF is longest and 0x000 is shortest. This parameter relates to layout size of the physical PCB trace. Therefore, the larger the PCB trace is, the longer transfer time it needs.

$$SPEED\_Transfer = (200\mu s + SPP * 0.5\mu s)$$

6.7.16 Address 0x19: Touch Button Quantity

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	TPQUTY			
R-0	R-0	R-0	R-0	W/R-0	W/R-0	W/R-0	W/R-0

If the pin status of Address 0x13/0x14 is updated, the Touch button quantity must also simultaneously updated.

Bit 7 ~ 4: Not used bits. Set to "**0**" all the time.

Bit 3 ~ 0 (TPQUTY): Select button quantity.

One-Line mode: Maximum is 12 buttons.

Two-Line mode: Maximum is 16 buttons.

6.7.17 Address 0x20: Button Status 0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Btn7	Btn6	Btn5	Btn4	Btn3	Btn2	Btn1	Btn0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7 ~ 0 (Btn7 ~ Btn0): This register determines whether button status is touched or untouched. A total of 8 bits represent each individual status of Buttons 7~0. By reading the register, user is able to check the button status.

0: Button is untouched

1: Button is touched

6.7.18 Address 0x21: Button Status 1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Btn15	Btn14	Btn13	Btn12	Btn11	Btn10	Btn9	Btn8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7 ~ 0 (Btn15 ~ Btn8): This register determines whether button status is touched or untouched. A total of 8 bits represent each individual status of Buttons 15~8. By reading the register, user is able to check the button status.

0: Button is untouched

1: Button is touched

6.7.19 Address 0x24: Button Operation Mode

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BtM1	BtM0	SBO	-	-	-	-	-
R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0

Bit 7 ~ 6 (BtM1 ~ BtM0): Button mode selection

BtM1	BtM0	Description	Note
0	**0**	Multi-button mode	With serveral buttons enabled, buttons that exceed the set senditivity trigger level (0x30~0x4F); will have their status bit set to "**1**".
0	**1**	First button mode	With several buttons enabled, the first button to surpass the set sensitivity trigger level (0x30~0x3F); will have its status bit set to "**1**".
1	**0**	Strong button mode	With several buttons enabled and a number of buttons surpass the set sensitivity trigger level (0x30~0x3F); the button with the highest sensitivity will have its status bit set to "**1**".
1	**1**	X	Not used

Bit 5 (SBO): This bit selects the Strong button mode options (Strong1/Strong2).

0: Strong1 - If KeyA is already pressed; KeyB is also considered pressed. If the total keys (except KeyB) are **released**, KeyB needs to be pressed hardier.

1: Strong2 - If KeyA is already pressed, KeyB is also considered pressed. If KeyB sensitivity is **higher than** KeyA, KeyB needs to be pressed hardier.

NOTE

The KeyA/KeyB sensitivity must be higher than the trigger level. The KeyA/B represents different key numbers.

Bit 4 ~ 0: Not used bits. Set to "**0**" all the time.

6.7.20 Address 00x25: Power Mode Configure

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	TP_IDLE	TP_PWR_M2	TP_PWR_M1
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0

Bit 7 ~ 3: Not used bits. Set to "**0**" all the time.

Bit 2 ~ 0 (TP_IDLE, TP_PWR_M2~M1): Operation mode selection

TP_IDLE	TP_PWR_M2	TP_PWR_M1	Description	Note
0	**0**	**0**	Touch runs at Normal mode.	
0	**0**	**1**	Sleep once. After wake-up, Touch will runs at Normal mode **(SLEEP MODE1)**.	Under this mode, Touch wake-ups by I^2C protocol
0	**1**	**0**	Touch will scan all button status. If no button is triggered, Touch will go to Sleep mode again and wait for next wake-up signal **(SLEEP MODE2)**.	
0	**1**	**1**	Touch will run at Idle mode for about 500ms, and wake-ups to Normal mode to scan all buttons. If no button is triggered, Touch will return to Idle mode and wait for the next 500ms time out **(IDLE MODE0)**.	Under this mode, Touch wake-ups by Internal timer time out.
1	**0**	**0**	Touch will run at Idle mode for about 250ms, and wake-ups to Normal mode to scan all buttons. If no button is triggered, Touch will return to Idle mode and wait for the next 250ms time out **(IDLE MODE1)**.	
1	**0**	**1**	Touch will run at Idle mode for about 125ms, and wake-ups to Normal mode to scan all buttons. If no button is triggered, Touch will return to Idle mode and wait for the next 125ms time out **(IDLE MODE2)**.	
1	**1**	**0**	Touch will run at Idle mode for about 62.5ms, and wake-ups to Normal mode to scan all buttons. If no button is triggered, Touch will return to Idle mode and wait for the next 62.5ms time out **(IDLE MODE3)**.	
1	**1**	**1**	Touch will run at Idle mode about 32ms, and wake-ups to Normal mode to scan all buttons. If no button is triggered, Touch will return to Idle mode and wait for the next 32ms time out **(IDLE MODE4)**.	

6.7.21 Address 0x26: Button De-Bounce Control

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-				Bounce Set			
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 ~ 4: Not used bits. Set to "**0**" all the time..

Bit 3 ~ 0 (Bounce Set): These bits are the bounce time control for buttons. The bounce time mechanism reduces noise interference on button status. The TouchKey controller provides touch and release de-bounce time control to resist noise effect. The following figure shows an example of detection with bounce Time = 2**;** meaning 2 consecutive samples are necessary to trigger the key detection or 2 consecutive samples are necessary to end detection.

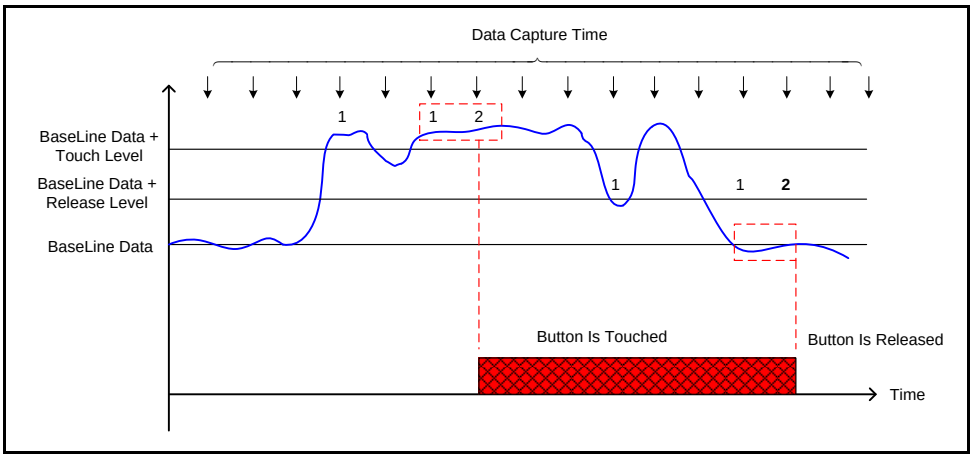


Figure 6-8 An Example of Bounce Time Operation

6.7.22 Address 0x30~0x34F: Trigger Level Adjustment

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FTN_0~FTN_15							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

This register is used to set trigger level and obtain button status. If the sensitivity is higher than the level, the relative bit of the button status will be "**1**".

Bit 7 ~ 0 (FTN_X): Adjustment of 8-bit address value is provided for 32keys & 48keys. 6keys is provided for different applications. The highest setting value is 0xFF, and the lowest is 0x00. The full range value can be adjusted in three stages, i.e., 0x00~0x80 as first stage, 0x81~0xC0 as second stage, and the rest is the third stage. Using the following formula can obtain the correct value to use.

1ST 0x00 ~ 0x80 = $FTN\_X * 2$
2ST 0x81 ~ 0xC0 = $(FTN\_X - 128) * 4 + 256$
3ST 0xC1 ~ 0xFF = $(FTN\_X - 192) * 8 + 512$

6.8 Power-On Reset and Initialization

After the touch button IC is powered on, the eKTF5201 controller will perform initialization. This includes MCU and some parameter initialization. After the initial processing is completed, the TPREQB pin will output low and then returns to high to report the initial Touch state to host. This will tell the host that the touch button IC is ready to start working. The figure below shows the initialization process after power-up. The touch button IC power-on maximum initialization time is 2000ms

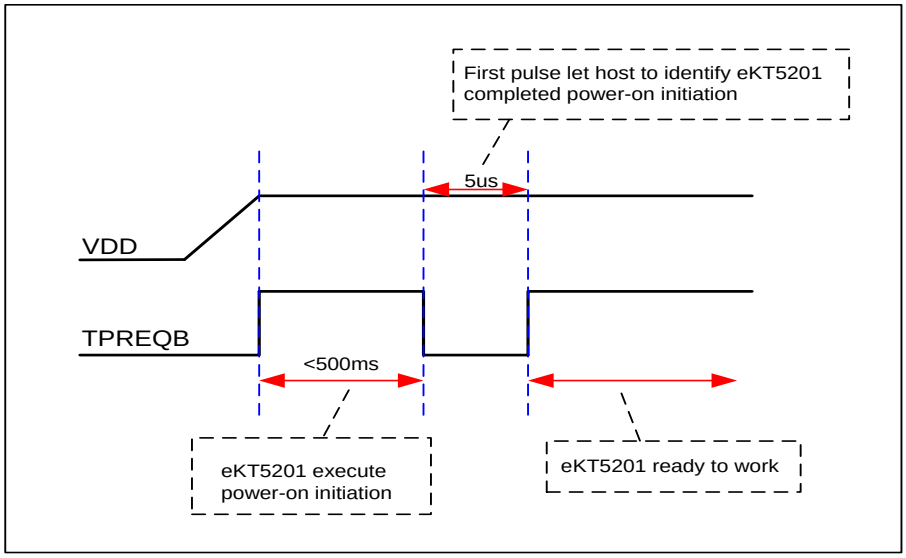


Figure 6-9 Power-on Reset and Initiate Timing Diagram

After eKT5201 has completed the power-on initialization, user can start reading or writing eKT5201 via I^2C protocol.

7 Application Circuits

7.1 1 Line Application Circuit

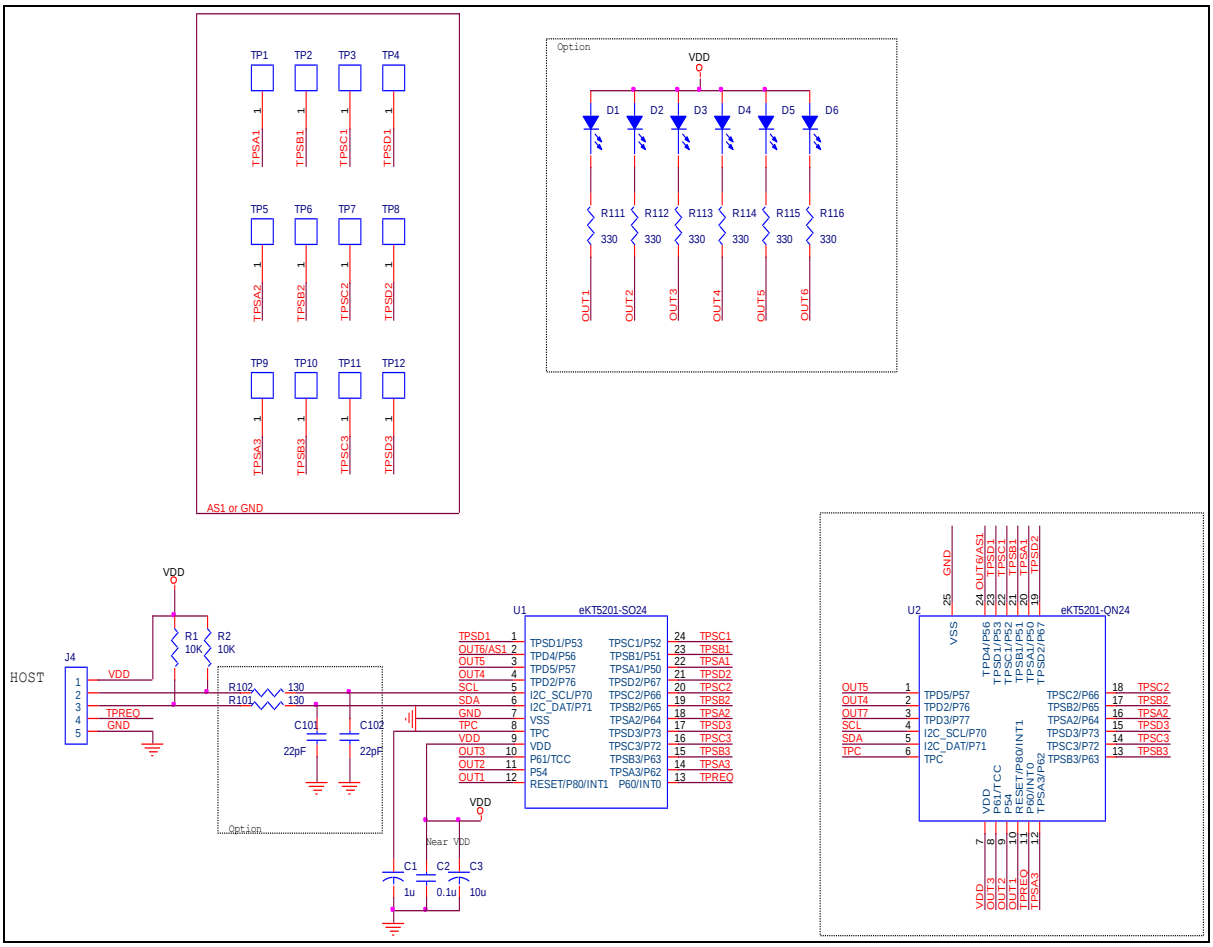


Figure 7-1 eKT5201 1 Line Application Circuits

7.2 2 Line Application Circuit

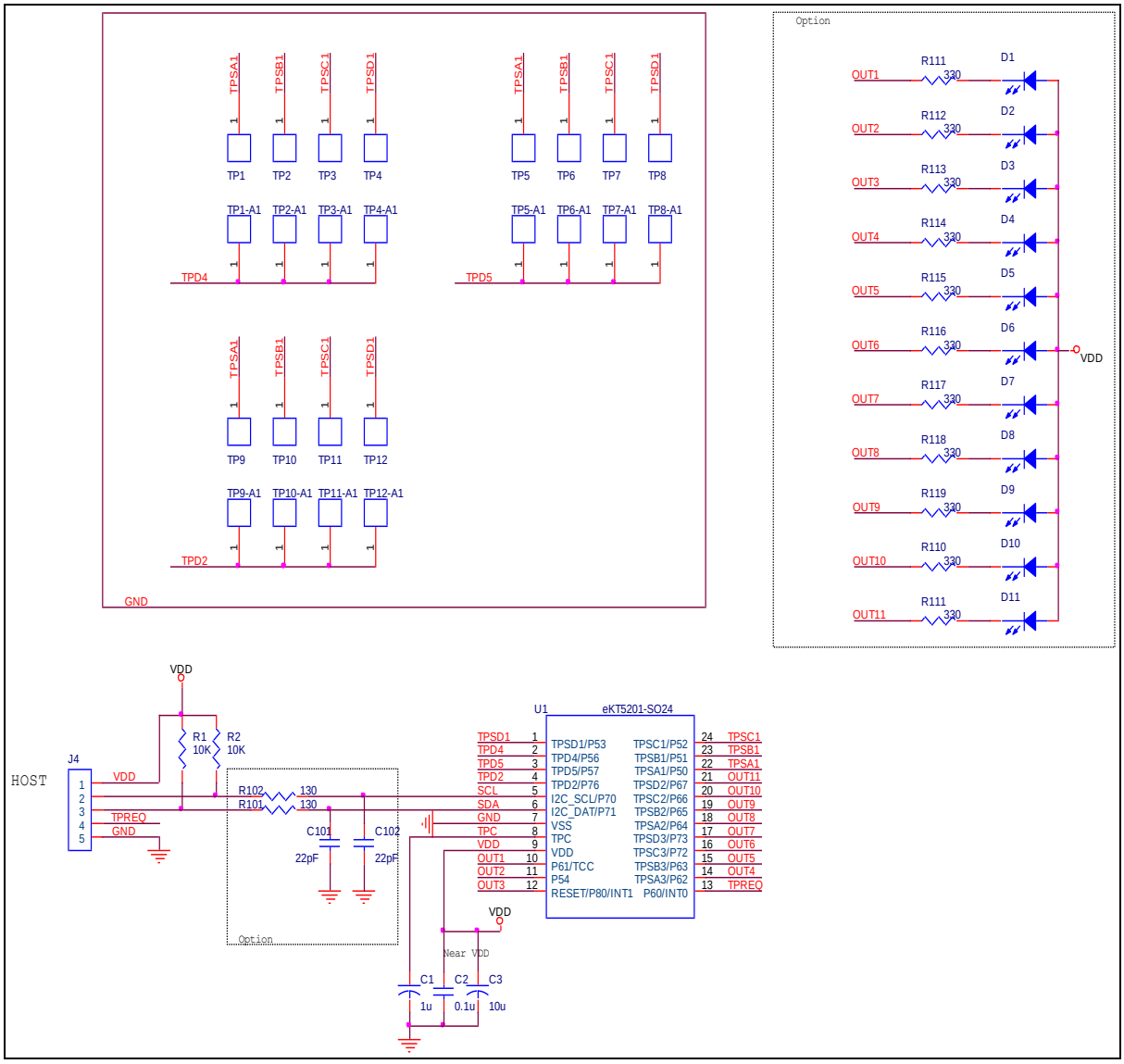
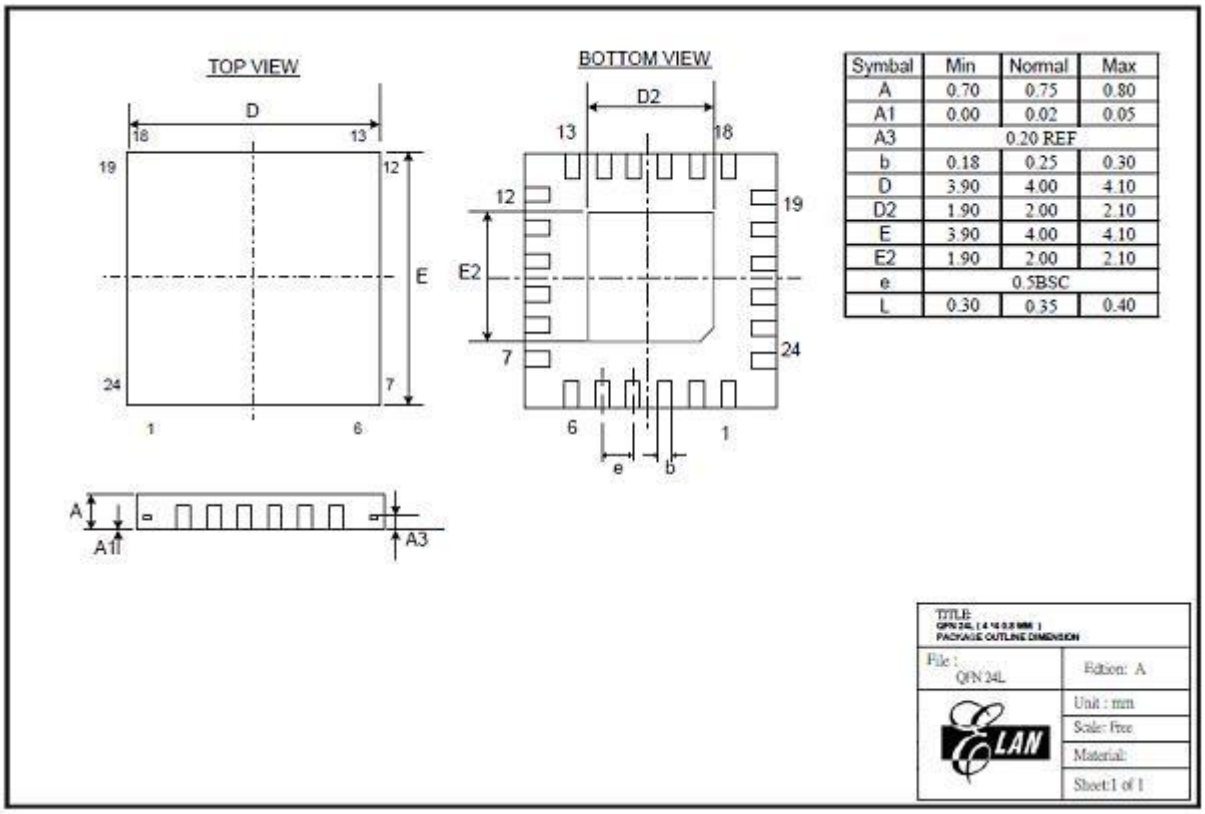


Figure 7-2 eKT5201 2 Line Application Circuits

APPENDIX

A Package Type

A.1 eKT5201QN24

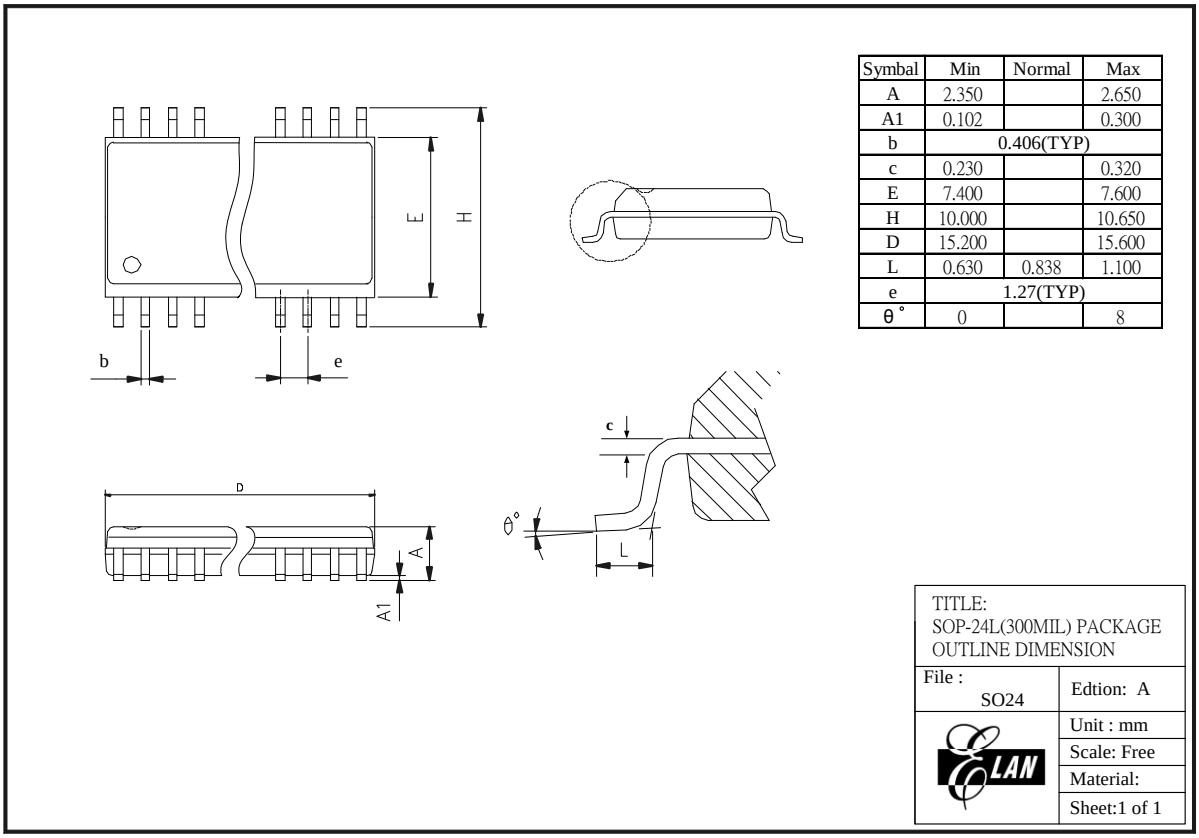


Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e		0.5BSC	
L	0.30	0.35	0.40

TITLE
PACKAGE OUTLINE DIMENSION
File : QFN 24L
Edition: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure A-1 eKT5201 24-Pin QFN Package Type

A.2 eKT5201SO24



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-24L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure A-2 eKT5201 24-pin SOP Package Type

B Ordering Information

IC	Part Number to Order	Package	Marking
eKT5201[*1]	KT5201QN24 x n[*2]	QFN-24pin (4x4x0.8mm)	eKT5201Q xxxxxx yyww n[*3]
eKT5201[*1]	KT5201SO24 x n[*2]	SOP-24pin (300mil)	ELAN eKT5201SO24x[*2] yyww n[*3] xxxxxx

[*1] *The part number 1'st code "**e**" is omitted from the actual order to ELAN as shown at right column.*

[*2] *The code x represents compliance to 1 of the 2 directives on Green product; "**J**" or "**S**". "**J**" complies with the RoHS GP directive, "**S**" complies with the Sony GP directive.*

The code n represents the alphabetical rolling codes used by ELAN for internal identification purposes.

[*3] ***yyww:** data code; **xxxxxx:** batch number (ELAN internal coding)*

The code n represents the alphabetical suffix code used by ELAN for internal identification purposes

NOTE

The internal rolling codes used by ELAN are subject to change without further notice.

B.1 Shipping Box Label

Figure B-1 eKT5201QN Shipping Label

Figure B-2 eKT5201SO Shipping Label

NOTES:

*1 *The code 1 represents compliance to 1 of the 2 directives on Green product; "**J**" or "**S**". "**J**" complies with the RoHS GP directive, "**S**" complies with the Sony GP directive.*

*2 *The code 2 represents ELAN internal rolling code. It is subject to change without further notice.*

*3 *The information on these blocks will vary in accordance with the actual goods being ordered and delivered.*