AN 19.16

Physical Design & Layout Guidelines for Capacitive Sensor Systems

1 Overview

SMSC's RightTouch™[1] capacitive sensor family provides systems with a wide variety of slider, button, and LED driver functionality. This application note describes design and printed circuit board (PCB) layout techniques that can be used to optimize system performance.

Note: Not all RightTouch devices have all features described in this document. Consult the device datasheet for details regarding the specific features offered in each device.

2 Audience

This application note assumes that the reader is familiar with hardware design and the SMSC datasheet for the device of interest.

3 References

The following documents should be referenced when using this application note:

- SMSC RightTouch capacitive touch sensor device datasheets
- SMSC Application Note 18.15, "PCB Design Guidelines for QFN and DQFN Packages" (AN18.15)
- AMKOR Application Note: "Application Notes for Mount Assembly of Amkor's *Micro*LeadFrame (MLF) Packages" (www.amkor.com)

4 Capacitive Touch Sensor Basics

SMSC RightTouch capacitive touch sensor devices detect a finger touch by measuring the capacitance changes on the touch pad. Figure 4.1 gives an overview of a capacitive touch sensor system. In the figure, C_0 is the capacitance value when no object is over the pad (referred to as base capacitance), ΔC is the capacitance change caused by a finger touch (referred to as delta count), and C_t is the total capacitance resulting from a finger touch.

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1. SMSC and the SMSC logo are registered trademarks and RightTouch is a trademark of Standard Microsystems Corporation ("SMSC").
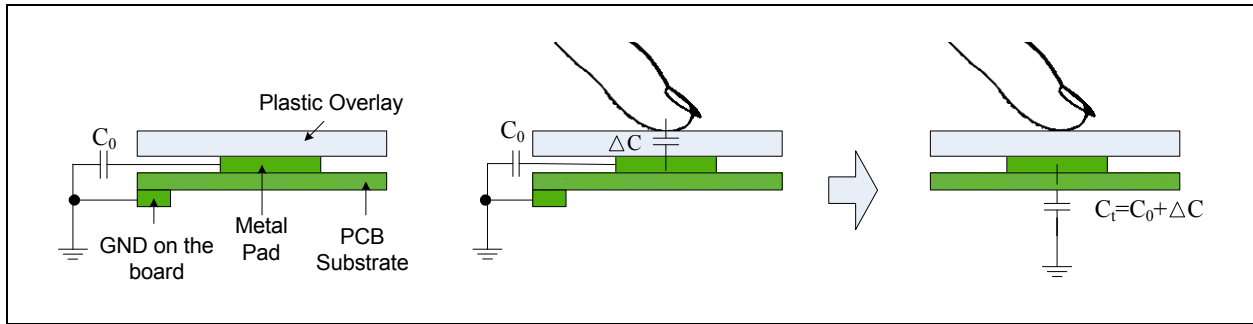
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Figure 4.1 Capacitive Touch Sensor System

The total capacitance of a capacitive touch system can be calculated by the parallel plate Capacitance Equation [1].

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where:

ε_0 = permittivity of space, 8.854 x 10^{-12} F/m

ε_r = relative permittivity of the dielectric material   **[1]**

A = plate area in square meters (m^2)

d = distance between plates in meters (m)

It is important to understand that in real applications the capacitive sensor (CS) system is much more complex than equation [1]. Generally speaking, the system could be considered a group of capacitors, resistors, and even inductors, which are a result of the PCB, the overlay, and the human body. Therefore, it is very difficult to calculate the exact characteristics of a CS system.

The recommendations in this document are based on lab test results and are not absolute conditions. Users can always make their own adjustments based on capacitance equation [1]. For example, use a bigger CS pad when using a thicker overlay.

5 Design Goals

SMSC capacitive touch sensors are designed for a base capacitance (untouched sensor) operating range of 5 to 50pF with a sensitivity for a touch of less than 0.1pF. The device circuitry and logic automatically compensate the measurement to provide a consistent ΔC value over the entire range of base capacitance. This simplifies the system design work and provides the most flexibility for PCB layout, overlay selection, and environmental requirements.

To optimize performance of a capacitive touch sensor system using the SMSC capacitive touch sensors, designs should strive to:

- Achieve a large ΔC relative to noise
- Minimize overlay thickness
- Avoid conductive overlay material

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6 PCB Design Considerations

6.1   PCB General

- Board Material – FR4

- Layer Thickness – No special requirements

- Dielectric Constant Specification (@1MHz) – Typical Value = 4.6, Maximum Value < 5.4

- General recommended 4-layer PCB stack-up:

1. L1: Layer 1 (top) – CS pads.

2. L2: Layer 2 – CS traces.

3. L3: Layer 3 – GND plane. Every effort should be made to keep this ground plane contiguous. This is especially true for the area under the CAPxxxx chip.

4. L4: Layer 4 (bottom) – All components, any LED signal traces, power traces, and communication traces.

- For a PCB with more than 4 layers, always route the CS traces on a layer close to the CS pads layer (L1), and place the GND layer between the CS traces and other signal layers.

- General recommended 2-layer PCB stack-up:

1. L1: Layer 1 (top) – CS pads (and some CS traces if they cannot be routed in layer 2).

2. L2: Layer 2 (bottom) – All components, any LED signal traces, and power traces.

6.2   Ground Shields

Ground fill on L1 (where the CS pads are placed) is recommended, with 0.5 mm (20 mil) or greater distance between the ground and the CS pad edges. There should be a distance of 0.127mm (5 mil) or greater distance between the ground plane and the CS traces. A 15% cross-hatch ground plane fill is recommended.

Keep CS traces shielded by ground at the board edges.

A ground plane on the layer between the CS pads/traces and other components is also recommended. This layer is usually L3 on a 4-layer PCB. This should be a contiguous layer of ground. In extreme circumstances, traces may be routed to the ground plane layer for short distances, but all attempts should be made to avoid this. The ground plane must be left intact under the CAPxxxx device. No traces should be routed on this layer that could divide the ground plane into unconnected segments.

A solid ground plane directly under the CS pads, usually L2 on a 4-layer PCB, should be avoided since it will increase the system base capacitance and may even cause the capacitive touch sensor device to stop working. If ground plane segments are needed to isolate L3 from L1, a 15% cross-hatch should be used. For a 2-layer PCB, a 15% cross-hatch should be used on L2 under the CS pads.

It is also recommended to place ground shields over all unused areas on L4 on a 4-layer PCB.

6.3   PCB Layout

6.3.1   Rules of Layout

The following rules are important to ensure a successful PCB design when using a RightTouch capacitive touch sensor.

- LED output traces must be isolated from CS pads on different layers by a GND plane between them. **NOTE: The same isolation must be observed for the CS pads and traces and any other switching signals on the PCB, including signals generated by sources other than the SMSC RightTouch capacitive touch sensor device.**

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- It is permitted to route CS traces on adjacent layers to CS pads without an isolation GND plane between them

- CS traces cannot be parallel with LED output traces on the same layer or on adjacent layers
  - Minimum distance between LED and CS trace with GND guard trace – 3x trace width
  - Minimum distance between LED and CS trace without GND guard trace – 1.27 mm (50 mil)

- CS minimum trace width – 0.1 mm (4 mil) to 0.2 mm (~8 mil)

- CS minimum trace-to-trace distance – 0.1 mm (4 mil)

- If a CS trace must cross an LED output signal on adjacent layers due to PCB routing constraints, they must cross at a 90 degree angle

- Minimize vias and layer changes in CS traces (this adds parasitic capacitance)

- Unused CS pins and LED pins should be terminated, either with a pull-down resistor or tied directly to GND. **NOTE: Ensure unused LED / GPIO pins shorted to GND are not driven by controlling firmware.**

- Always cover unused areas with a 15% cross-hatch fill GND plane
  - Around CS traces
  - Below CS traces
  - Add vias to GND planes to ensure there are no islands

- Layer specific recommendations:
  - Layer 1 (top) should be limited to capacitive sense touch pads, and touch pad traces if PCB routing density requires it.
  - Layer 2 should have the capacitive sense touch pad traces. If any switching signal traces are routed on Layer 3, ground shield should be placed on Layer 2 to isolate any switching signal traces from the noise sensitive capacitive sense touch pads and traces on Layer 1.
  - Layer 3 should have the ground plane, with all efforts made to keep this uninterrupted. If switching signal traces are placed on this layer due to PCB routing densities, care should be taken keep these as short as possible and the ground shield isolation mentioned for Layer 2 should be used.
  - Layer 4 (bottom) should have the components and switching signal traces, including the LED signal traces and communication signal traces.

6.3.2   Layout Order

1. Mechanical requirements

   - The mechanical requirements / limitations must be known up front. This will include connector placement requirements, PCB shape / size requirements, LED and button pad locations, and any height restrictions in the system. In addition, the overlay material, thickness, and stackup method must be known to correctly design the Cap pad size and dimensions.

2. CAPxxxx location

   - The CAPxxxx placement should take into account decoupling and routing from the initial placement. This would include any height restrictions that will prohibit components such as decoupling capacitors being placed in close proximity to the CAPxxxx.

3. Decoupling capacitor(s)

   - Decoupling capacitor(s) should be placed close to the CAPxxxx V_{DD} power pin, with a short trace between the decoupling capacitor and the CAPxxxx pin, and a short return path for the ground.

   - If vias are used to connect the decoupling capacitor to the ground plane and / or power plane, two vias should be used per capacitor terminal.

   - The power supply traces to the decoupling capacitor must be outside the decoupling current path. The traces between the CAPxxxx and the decoupling capacitors should not extend around the power and ground traces on the board, but should be an enclosed loop from the VDD pin of the chip, to the decoupling capacitor, and back from the capacitor to the ground of the chip.

4. Power distribution

   ■ A bulk capacitor should be located close to the power input connector to the board. Power should be routed directly from the power input connector to this primary input capacitor through a 10mil minimum trace. The ground terminal of the primary input capacitor should have a 10mil minimum trace to the ground of the power input connector. These traces should be kept separate from the power and ground planes of the board.

   ■ Power should be distributed from the primary input capacitor in a star topology, rather than from the power input connector. If a power plane is used on the board, it should be disseminated from the primary input capacitor. The same is true for the board ground plane, it should be disseminated from the primary input capacitor rather than from the power input connector.

5. Route CS traces

   ■ Group CS traces along either the upper or lower edge of the PCB, preferably on L2.

   ■ These traces may be routed under the CS pads if necessary.

   ■ A margin of 5mils minimum should be maintained from the ground plane edge to the CS trace closest to the edge of the board, ensuring there is a good overlap of ground plane completely covering any CS traces.

6. Route LED traces

   ■ Group LED traces along the opposite edge from the CS traces, preferably on L4

   ■ If L3 must be used, insert a GND plane on L2 to isolate the LED traces from the CS pads. Do not route CS traces and LED traces in parallel on adjacent PCB layers.

   ■ If L2 must be used, do not route LED traces under CS pads.

7. Route SMBus signals

8. Route Power, GND and other traces

9. Ground fill all areas. Use vias to link islands together. Peninsulas of ground should not be placed without having vias to connect them to the ground plane.

6.3.3   Layout Checklist

The following checklist is based on SMSC's capacitive touch sensor PCB layout experiments.

1. Verify the bulk input capacitor is placed close to the power input connector, and that the routing is short between the connector and the primary input capacitor. Verify the power and ground is dissimulated from this capacitor rather than from the input connector.

2. Verify the decoupling capacitor(s) is as close as possible to the CAPxxxx, with short, uninterrupted traces between the decoupling capacitor(s) and the CAPxxxx.

3. Verify that all CS traces are on L2. Routing on an adjacent PCB layer underneath CS pads is acceptable.

4. Check CS 1.27 mm (50 mil) isolation from any LED traces and all other traces on L2.

5. Ensure there are no LED traces on L2 under CS Pads or on L1.

6. Verify solid GND on L3, with no breaks in the plane under the CAPxxxx.

7. Verify correct pin 1 connector orientation.

8. Verify mechanical height restrictions.

9. Verify flat flexible cable (FFC) area design and 3 mm (118 mil) keep-out if applicable.

10. Verify all LEDs are in the correct functional location.

11. Ground fill unused areas on L1 and L4, ensure there are no islands.

12. Ensure solder mask is on all CS pads.

13. Verify any dual color LED connections.

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14. Verify SOT-23 pinout.

15. Verify SMSC capacitive touch sensors pin 1 silkscreen is clear.

16. Ensure silkscreen polarity is clear for all LEDs.

17. Make sure the ESD protection planes or guard traces are not solder masked.

18. If off-board cabling is utilized, isolate the communications pins by installing series resistors if needed.

7 Button Pad Design

7.1   Pad Shape and Size

SMSC capacitive touch sensors work well with any CS pad shape, including the most commonly used ones: square, rectangular, round and oval. When designing a rectangular or oval CS pad, a length and breadth ratio of less than 4:1 is recommended.

In general a larger CS pad will have a bigger ΔC (equation [1]) and can provide a more repeatable touch detection. However, since the average adult's fingertip is about 10 mm (~394 mil) in diameter, oversize CS pads will only increase detection sensitivity up to a point.

The CS pad size also depends on the overlay thickness. For thicker overlays, larger CS pads are needed. SMSC capacitive touch sensors can detect a finger touch with a CS pad as small as 16 mm^2 (4 mm x 4 mm) in a system with 2 mm plastic overlay.

For typical applications with a normal thickness (1 - 3 mm) of generic plastic overlay, the recommended pad size is equal or greater than ~29 mm^2. If it is allowed by the board dimensions and CS pad location, a larger pad area is always suggested.

7.2   Pad to Pad Distance

A minimum spacing between two CS pads is ~1.30mm (~51 mil) from edge to edge. However, if two CS pads are placed too close, touching one pad could cause a capacitance change on the other pad. To avoid an unwanted detection, the suggested minimum distance is 10 mm (~394 mil) from edge to edge; however, other factors, such as pad size and the application user's fingertip size, must be considered.

8 Slider Design

Some RightTouch capacitive sensing devices, such as the CAP1114, have the capability to utilize several of the CS inputs as a single slider group.

8.1   Slider Shape and Size

A typical slider shape is shown in Figure 8.1. Similar to the individual CS pad design, the pad size (H x W) needs to be greater than ~ 29 mm^2, and the distance between pads (*d*) should be ~1.3 mm (~51 mil).

Theoretically, any pad shape used for a button pad can also be used for a slider pad. However, the arrow type slider shape shown in Figure 8.1 will provide smoother responses when a finger crosses from one pad to the next. It will also provide a clear direction indicator for schematic design, PCB layout and assembling processes.

Note: During typical operation, SMSC capacitive touch sensors will scan each channel for capacitance change and connect all other channels to ground. Therefore, for the pad to be measured, the two nearby slider pads can be considered as ground planes.
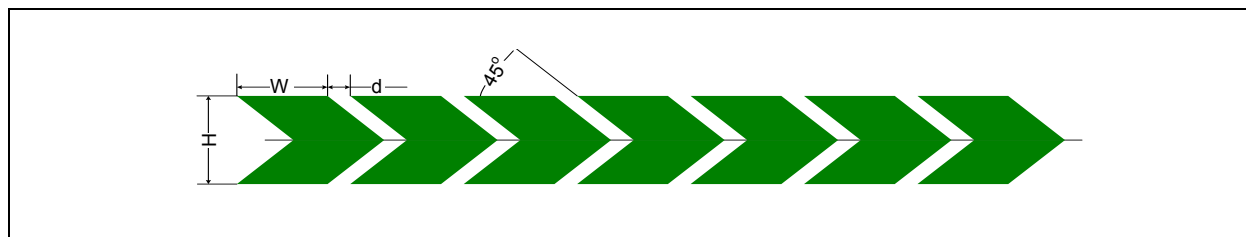
Figure 8.1 Typical Slider Shape

8.2   Slider Design with Different Number of Pads

The 7-pad slider shown in Figure 8.1 will provide good sensitivity as well as enough accuracy for most applications, but a slider with less than 7 pads could also be used for some applications.

In most applications, the width of each pad (W) and the distance between pads (d) usually will be limited by the total length of the slider, and the height of the slider (H) will also be limited by the physical dimensions of the machine. If the pad's size cannot meet the minimum requirement and reduced accuracy is acceptable, the number of pads in the slider can be reduced to 5, 3, or even 2 (up/down control), as shown in Figure 8.2.
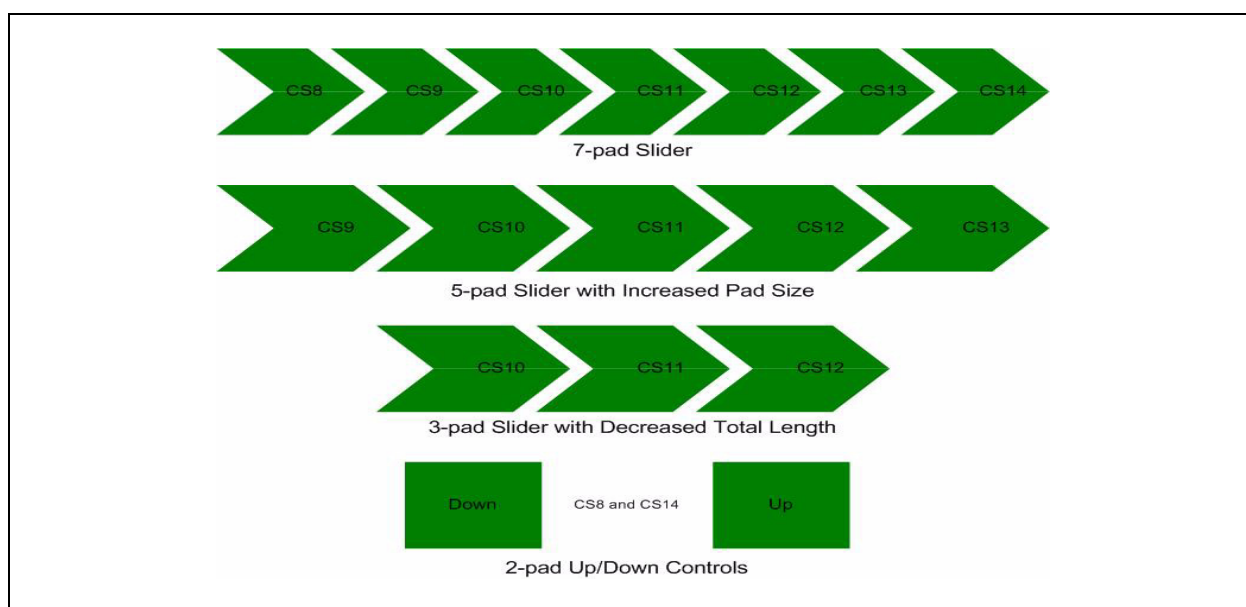
Figure 8.2 Slider with Different Number of CS Pads

9 Electromagnetic Compatibility

SMSC RightTouch capacitive touch sensors are capable of withstanding high levels of electrostatic discharge (ESD) without physical damage. In addition, operational immunity from electromagnetic interference (EMI) and ESD environments is minimized through proprietary techniques. However, excessive environmental conditions can produce false touches, activate internal ESD protective clamps, or affect V_{DD} and ground resulting in device reset. As such, it is important for "electromagnetic compatibility" (EMC) to be considered as early as possible in the system design process.

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ESD typically has two distinct points of entry into a system.

- Transient charge entering through a board-to-board connection. This would require circuit design solutions.
- Transient charge coupling to the PCB. This would require layout and system solutions.

For transient charge entering through a board-to-board connection, there are several approaches that may help resolve this. (See Figure 9.1).

- Increase the impedance to high frequencies using a series resistor, a ferrite bead or a common mode choke on the VCC and GND lines.
- Adding Transient Voltage Suppression Diodes (TVS), also known as avalanche breakdown diodes, between VCC and GND to shunt the ESD current.
- Adding ESD protection devices (series resistors, ferrite beads, etc.) to the communication lines themselves.

Figure 9.1 ESD Protection Solutions

For transient charge coupling to the PCB, there are several approaches that can be used to resolve this.

- The ESD charge point(s) of entry must be determined. These can be visible air gaps in the covering material, areas where two pieces of covering material come together, around the edges of the covering material, etc.
- Specific metal on the PCB may be design as an ESD-Ground (EGND) for conducting the ESD charge. The EGND should be exposed as a metal ring around the outer edge of the PCB to conduct ESD current to the chassis. This EGND should be terminated directly to the system chassis using conductive foam when possible. The EGND ring should be routed on all layers of the PCB.
- Route the signal ground between the EGND and all other traces on the PCB, using a spacing of 20-40 mils.
- Figure 9.2 is an example of an EGND, indicated by the red arrows. This is a strip of metal isolated from the board ground by a spacing of approximately 20 mils, and is AC coupled to the system ground by a 0.1uF capacitor, as shown by the red oval indicator.

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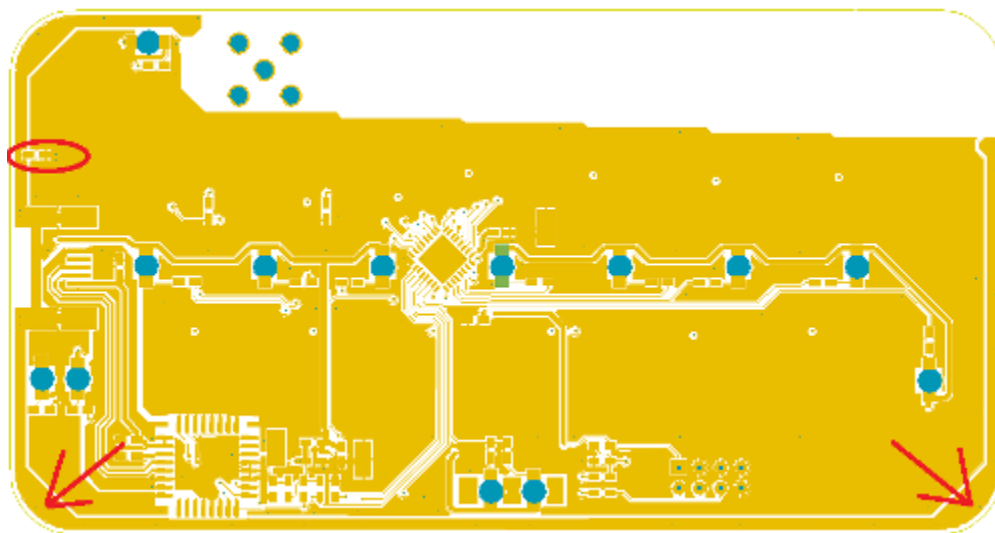
Figure 9.2 EGND Routing Example

There are a couple of additional points to remember:

- Direct coupling of ESD to sensor device pins should be minimized by directing energy to 'safe' areas of the system, such as to chassis ground (via a ground strap or similar means).

- Metal surfaces, such as shown in Figure 9.3, are usually more difficult to protect against ESD than those made only of plastic. As well, plastics may only require "air discharge" ESD compliance (i.e. IEC 61000-4-2) whereas metal covers and buttons can require "direct contact discharge" compliance. Though an explanation of the differences in these two test methods is beyond the scope of this application note, it is generally simpler to provide a safe ESD environment inside a plastic enclosure than one with exposed metal parts.
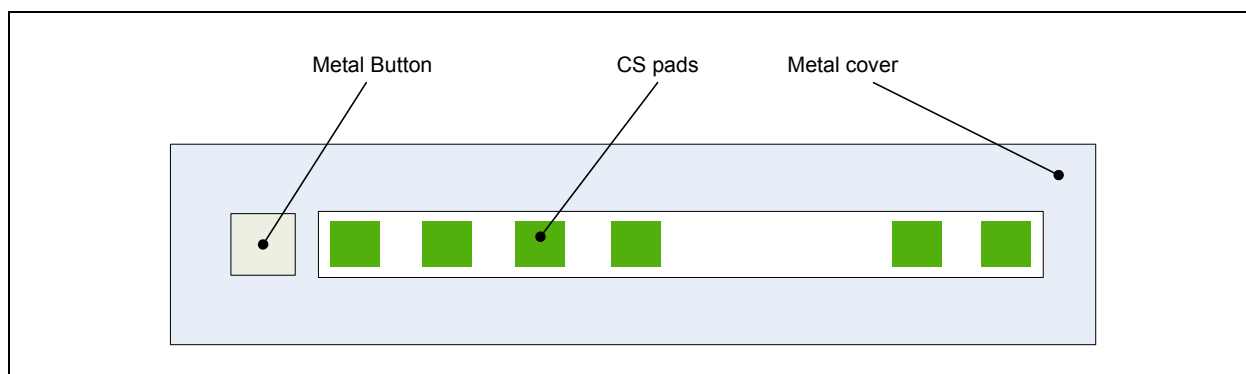
Figure 9.3 Example of Metal Cover with Button

- Other printed circuit boards, in particular ones mounted on the same cover and directly connected to the capacitive sensing PCB, should be considered potential sources of ESD. A typical case is a mechanical power button board.

  - Typically these boards utilize the same V_{DD} as the capacitive sensor PCB. It has been found useful to separate the voltage supply between the two PCBs by a small value resistor (such as 50 ohms).

- Radiation of ESD energy from nearby metal chassis plating should also be considered a possible coupling mechanism. A useful mitigation technique for this type of coupling is to either shield the plate or shield the bottom PCB layer with conductive tape over a thin insulating material.

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- If ESD energy cannot be redirected by mechanical means, a potentially useful risk mitigation can be the use of transient voltage suppression (TVS) diodes connected to V_{DD}, RESET, and long LED traces, especially those going off-board. The voltage rating of these TVS devices should match that of V_{DD} with board placement ideally being in between the ESD source and the RightTouch capacitive sensor device.

- A full layer board grounding and internal conductive coatings on plastic enclosures are among the best mitigation techniques to minimize the effects of EMI.

- Small (5pF-15pF) bypass capacitors can be placed on the CS traces, located as close as possible to the CAPxxxx pins to help shunt excess energy to GND rather than having it enter the CAPxxxx sensor pins.

10 RF Immunity

Some RightTouch capacitive touch sensors are capable of sensing and responding to RF fields. When an RF signal is detected, the response is to disable active sensors to avoid false touches. Once the RF field is removed, the sensors are re-activated. However there are some environments which require additional work to provide immunity to RF signals.

One possible source of problems is the architecture which uses an interface cable to connect the capacitive sensing functions to a main board. An unshielded cable can act as an antenna, and the degree of the interference is a function of the magnitude of exposed RF energy, line impedance, coupled surface area, and the orientation of electromagnetic field from the antenna with respect to the DUT. The right combination of design parameters and RF signals can couple RF frequencies into the pins of the RightTouch capacitive touch sensors. It is always recommended to keep the interface cable as short as possible and to use a shielded cable, One end of the shield should be connected to the chassis GND of the system. In addition, if there is a risk of RF interference, the system firmware should implement SMBus re-entry and an interrupt service routine (ISR) in case of communication failures caused by external EMI.

There are additional methods that can be used to provide robustness to a design with regards to RF signals. Bypass capacitors can be placed on the digital lines, namely ALERT, SMBus_DAT, SMBus_CLK to insulate the communication bus. Since the ALERT line does not have a strict timing requirement, a 0.1uF ground-coupled bypass capacitor may be adequate, placed close to the CAPxxxx pin. However the SMBus_DAT and SMBus_CLK lines require more care due to bus timing and the specification when capacitance is introduced in the line.

As additional bypass capacitors are introduced on the SMBus_DAT and SMBus_CLK lines, the digital RC time constant will be altered and the rising and falling edges of the digital signal lines will be affected. Depending on the baud rate of the SMBus, the added capacitance can cause communication issues in send/receive in an application. In some applications, the SMBus line may require a decreased pull-up resistor value and increased line capacitance to improve the protection against RF interference. The time constant of rising/falling edges are defined in Equation [2] below. Four times the time constant should not exceed the SMBus timing requirement for a given transmission rate.

$$\tau_{\text{time constant}} = R_{\text{pull-up}} \times C_{\text{RF bypass}} \qquad [2]$$

The maximum capacitive load for each bus line is specified at no greater than 400pF. Under RF interferences, the bypass capacitor should behave as a "short" in the AC circuit at the frequency, e.g. 400MHz @4.8W, and decouple the energy directly to chassis and earth ground of the system. Based on lab data, the required impedance of the bypass capacitor in "AC short" condition should be around 20 Ω at the specified RF frequency. The capacitor impedance can be derived from Equation [3] below, where 0.5 is the compensation factor.

$$X_c = 0.5 \times (1/2\pi f_{\text{RF}} C_{\text{RF bypass}}) \qquad [3]$$

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The objectives are to lower the touch sensor's AC line impedance at the specified RF frequency, to redirect the coupled RF energy to earth ground as a short as quickly as possible, and to protect a direct RF exposure at the IC. The introduced bypass capacitor serves the following purposes:

1. NOT to interfere with the SMBus baud rate in communication.

2. Act as an "AC short" and redirect the coupled RF energy to earth ground as quickly as possible.

11 Overlay

In most applications, the CS pads will be covered with an overlay to protect them (Figure 11.1). The material and thickness of the overlay, as well as the adhesive used, will affect the performance of a capacitive sensor system.
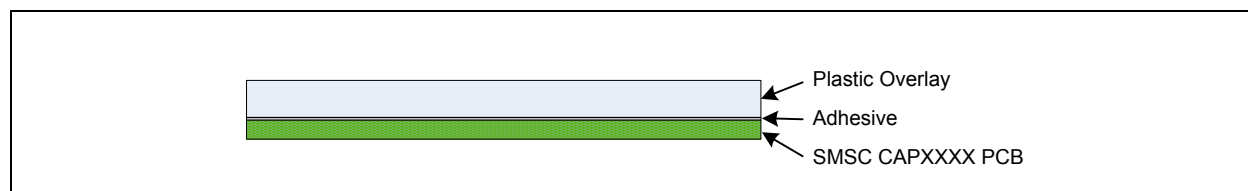
Figure 11.1 Capacitive Touch Sensor PCB and Overlay

11.1   Overlay Materials

The most commonly used overlay materials are plastics which typically have dielectric constants (ε_r) between 2.0 to 3.0. SMSC capacitive touch sensors can accommodate materials with dielectric constants ranging from 2.0 to 8.0.

In selecting an overlay, note that certain contaminants could change the characteristics of the overlay material and possibly affect performance. This information can be found on the specific overlay vendor datasheet.

11.2   Overlay Thickness

SMSC recommends an overlay thickness in the range of 1 - 3 mm (~39 to 118 mil). Due to its advanced architecture and technology, SMSC capacitive touch sensors can work with an even wider range of thicknesses; however, overlay material thickness greater than 3 mm (118 mil) introduces challenges. The sensitivity must be increased to detect changes; this decreases the signal to noise ratio. Thicker plastics also tend to bleed signal from one sensor to another, requiring greater spacing between CS pads.

For thicker overlays, increasing the cap pad size is recommended to achieve the best performance. This relationship is described in equation [1]. For example, a 6 mm x 7 mm pad will generally work well for a 2 mm overlay, while a 12 mm x 7 mm pad is required to achieve the same signal level for a 4 mm overlay.

11.3   Adhesive and Mounting Tapes

SMSC recommends using mounting tapes with 0.05 - 0.15 mm (2 - 6 mil) permanent adhesive, such as 3M Adhesive Transfer Tape 467 which has 0.06 mm (2.4 mil) adhesive or 468 which has 0.130mm (5.1 mil) adhesive.

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11.4   Using Conductive Overlay

In some capacitive sensor applications, the overlay may be conductive due to a conductive coating over the non-conductive plastics or due to filling with carbon to darken the overlay's color.

With conductive material over the CS pads, the resistance of the material will add an equivalent resistor (R) between to the CS inputs (Figure 11.2). When a finger touches a CS pad, capacitance changes on one CS pad will affect other untouched CS pins to a varying degree. The smaller the R, the larger the ΔC on untouched CS pins. If the R is too small, false touch detections will be reported on untouched CS inputs.
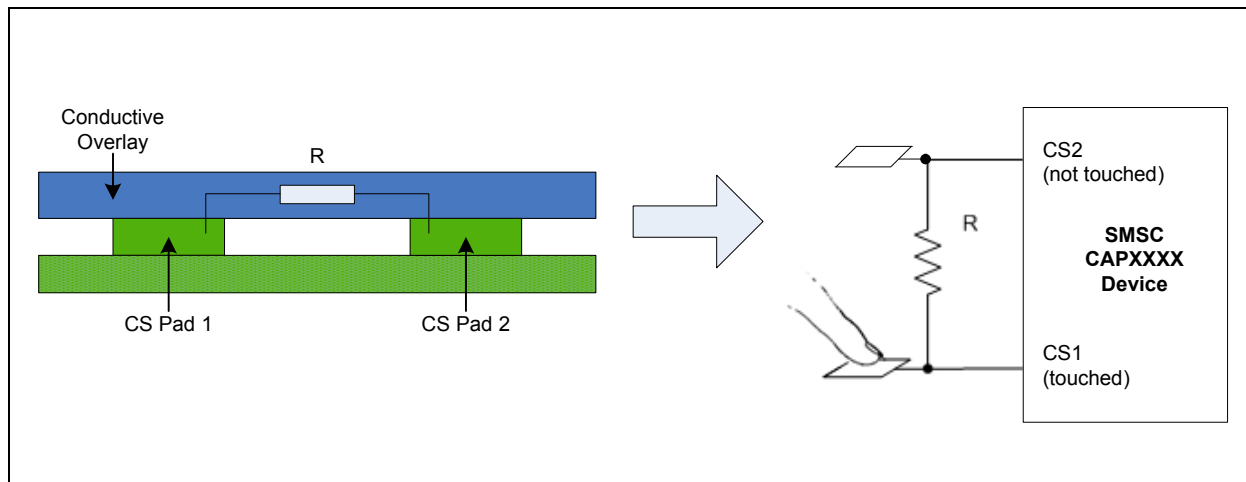
Figure 11.2 Overlay with Conductive Coating

Although the SMSC capacitive touch sensors can handle as low as 50k ohms pad to pad resistance, using a conductive overlay is not recommended. This is because:

- The amount of carbon in the plastic may change and then make the resistance change over time
- The resistance from location to location could be different
- The resistance from different product groups (different date codes) also could be different

Any of the above changes will affect the SMSC capacitive touch sensors input values and cause the device settings (such as Sensitivity and Thresholds) to be incorrect.

If a design must use conductive materials, always test the overlay samples and determine the allowable range of conductivity.

11.5 Air Gaps Between PCB and Overlay

If there are air gaps between the PCB and overlay, a finger press could bend the overlay and cause the distance to change between the overlay and untouched CS pads (Figure 11.3). If the distance changes are big, false touch detections could be reported on adjacent untouched CS pads. The chart of the right side of Figure 11.3 is representative of this type of problem. Ideally there should be only one CS pad responding (number four with value of 127).
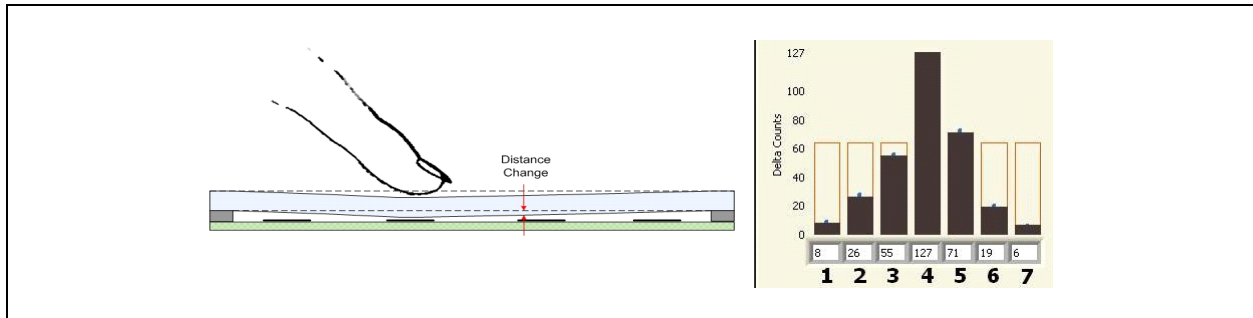
Figure 11.3 Air Gaps

11.6 Mechanical Movement

If both PCB and overlay are very thin, a finger press could bend the overlay and PCB together. If there is no ground shield under the CS pads and traces, the distance between the untouched cap pads and the object under the board will change (Figure 11.4). If the distance changes are big, false touch detections could be reported on pads not being touched.
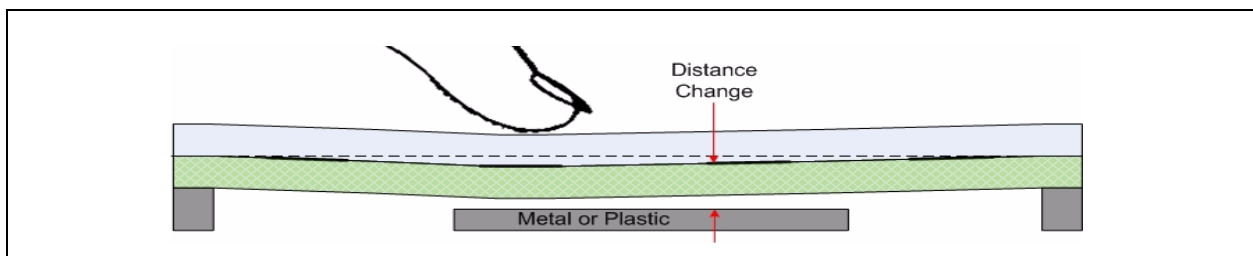
Figure 11.4 Mechanical Movement

To avoid this issue, always provide support under the PCB so it will not bend.

Another recommendation is to add a ground layer on the PCB to shield all CS traces from the bottom, so the distance changes will not cause capacitance changes.

11.7 Metal Shielding Over CS Pads

Some applications may have a metal cover with a window over the cap sensor board. If the window is smaller than the application's CS pads (Figure 11.5), two problems will occur:

■ If a finger touches the metal part, the metal shield will distribute the capacitance change to all CS pads under it and false touch detections will be reported.

■ If a finger touches the inside of the window, the capacitance change (delta count value) could be smaller than expected due to the reduced active sensor pad size; therefore, the desired sensor sensitivity may not be achieved.

It is important to ensure the CS pads are fully exposed if a metal window is used, as shown in Figure 11.6.
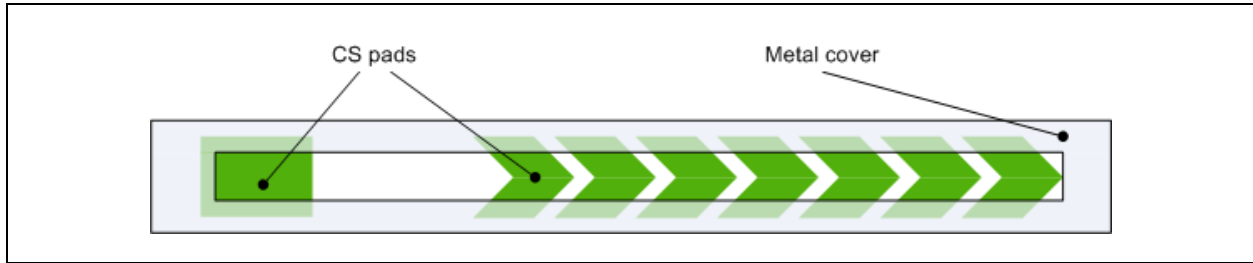
Figure 11.5 Improperly Sized Metal Cover Overlaps CS Pads
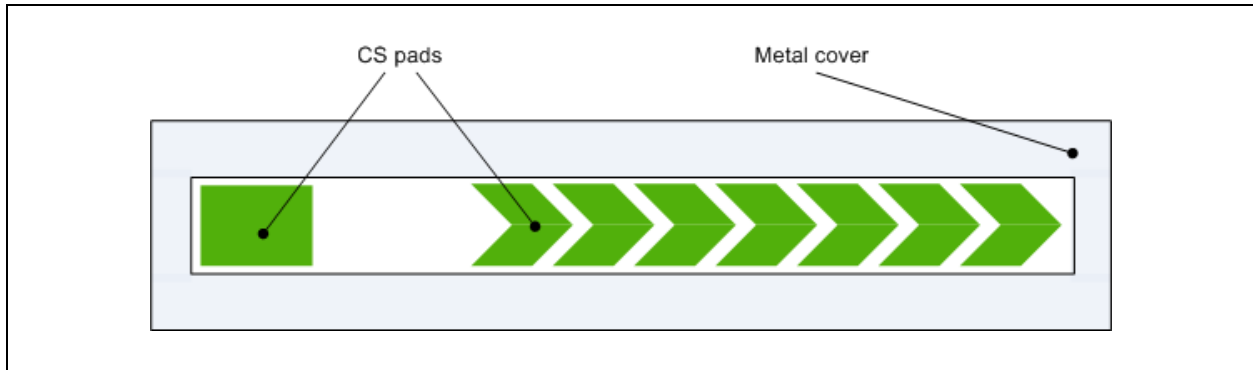
Figure 11.6 Properly Sized Metal Cover - No Overlap

APPLICATION NOTE

Appendix A

A.1 Case Studies - LED Crosstalk With CS Traces

SMSC capacitive touch sensors that include LED drivers use PWM signals to drive the LEDs. The changing impedance of the LED traces can couple to CS traces and interfere with the capacitance sensing circuitry of the device and decrease the signal to noise ratio of the system. False detections may also occur in severe cases.

A.1.1 How the CS Inputs Are Affected by LED Signals

With incorrect PCB layout, LED traces and CS traces could be parallel on the same layer or adjacent layers (Figure A.1). This could result in capacitive coupling between traces.
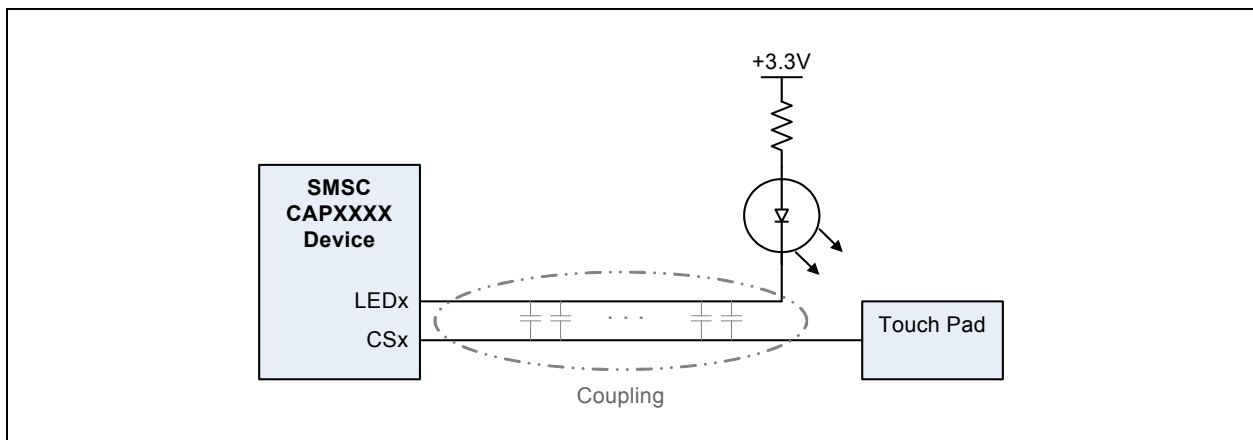
Figure A.1 LED/CS Signal Coupling

When used as an open drain, the LED PWM signal acts as a switch. When it is driven to HIGH, the trace is high impedance. When the LED is driven to LOW, it shorts the trace coupling capacitance to GND for a variable amount of time (depending on the PWM duty cycle), as shown in Figure A.2. This effect is independent of frequency and LED current; in fact, there doesn't even need to be current flowing. The impedance changes will cause the SMSC device to detect a capacitance change which cannot be distinguished from a real touch. This coupling effect is most pronounced when breathing or pulsing LED behaviors are used due to the gradual capacitance change.

It is possible to improve signal to noise ratio by configuring the LED driver as a push-pull output.
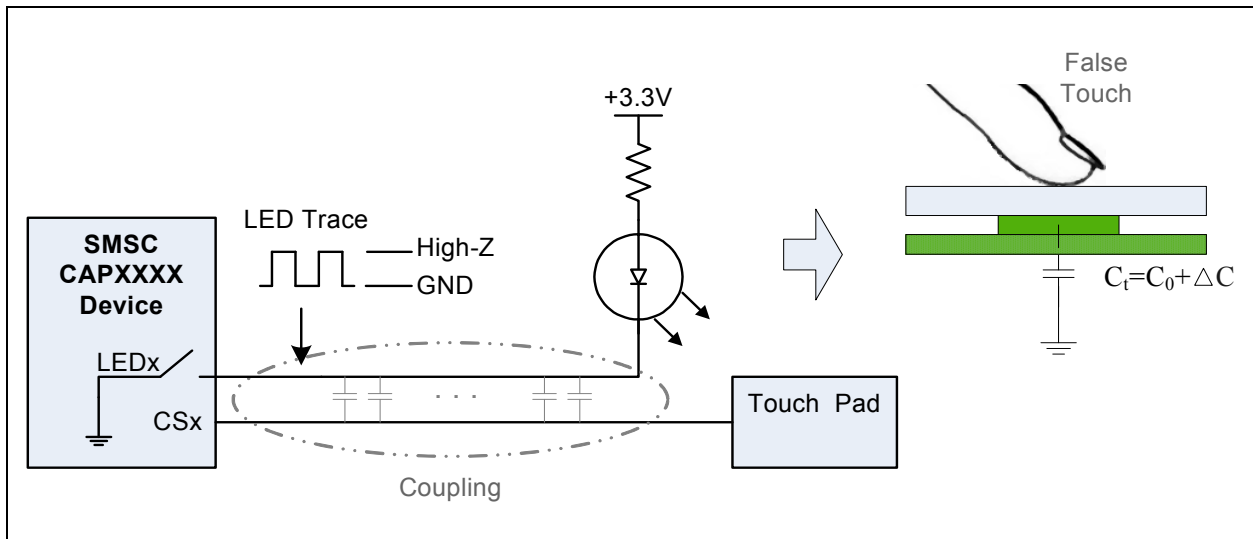
Figure A.2 LED/CS Signal Coupling Equivalent Circuit

A.1.2   Incorrect Layout Example 1

The graphics on the right side of Figure A.3 show the Delta Counts captured by the CAP1014 LabView GUI software. The blue lines indicate the maximum Deltas for each CS channel. A well designed system will have a maximum Delta of 15 counts.

The poor layout using the CAP1014 device, shown on the left side of Figure A.3, exceeds the recommended maximum Delta count. In the layout, when LED4 breathes, it causes nearly every cap sensor to experience crosstalk. In Figure A.3, red arrows on the PCB layout identify the LED4 trace coupling to CS4, 11, 12, 13 and 14.
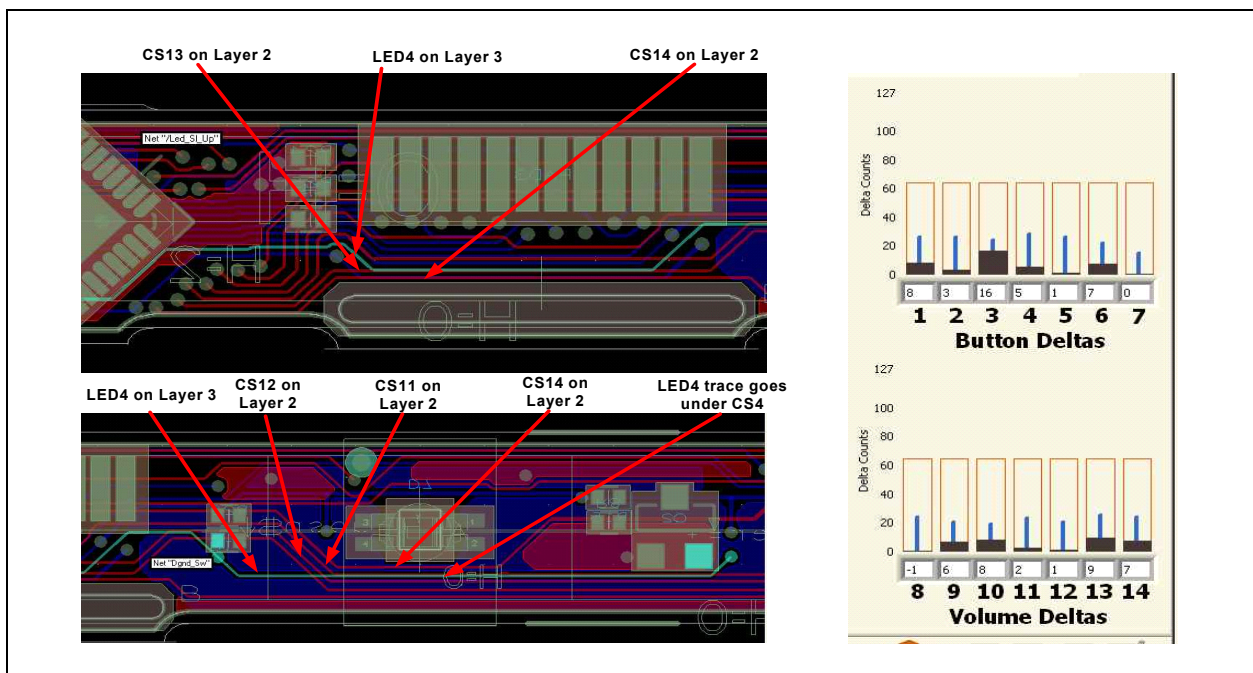
Figure A.3 Incorrect Layout Example 1

APPLICATION NOTE

A.1.3   Incorrect Layout Example 2

The sample 4-layer design using the CAP1014 device, shown in Figure A.4, does NOT incorporate a GND plane to separate LED and CS traces (GND is on the bottom); therefore, driving LED11 to breathe causes moderate to extreme crosstalk in CS1, CS2, CS3 and CS6.

The crosstalk locations can easily be found in the PCB layout (Figure A.4). For most of the PCB length, LED11 signal couples with CS1 and couples with CS3 and CS5 with shorter distances.

Note: LED11 is not actually driving a LED. In this design, it is just an open drain signal line with no pullup resistor.
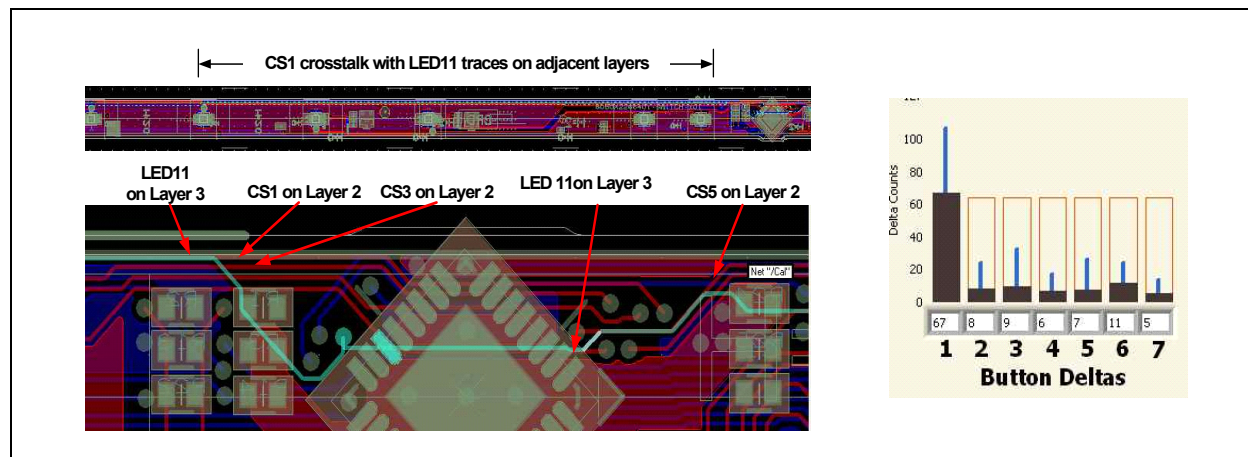
Figure A.4 Incorrect Layout Example 2

A.1.4   Incorrect Layout Example 3

The sample layout using the CAP1014 device, shown in Figure A.5, contains one major and several minor flaws.

- The CS5 trace was routed in parallel with the LED5 for several inches at 0.127 mm (5 mil) spacing. Driving the LED to breathe results in CS5 reporting a false touch. Parallel traces on the same plane appear to be one of the worst offenders.
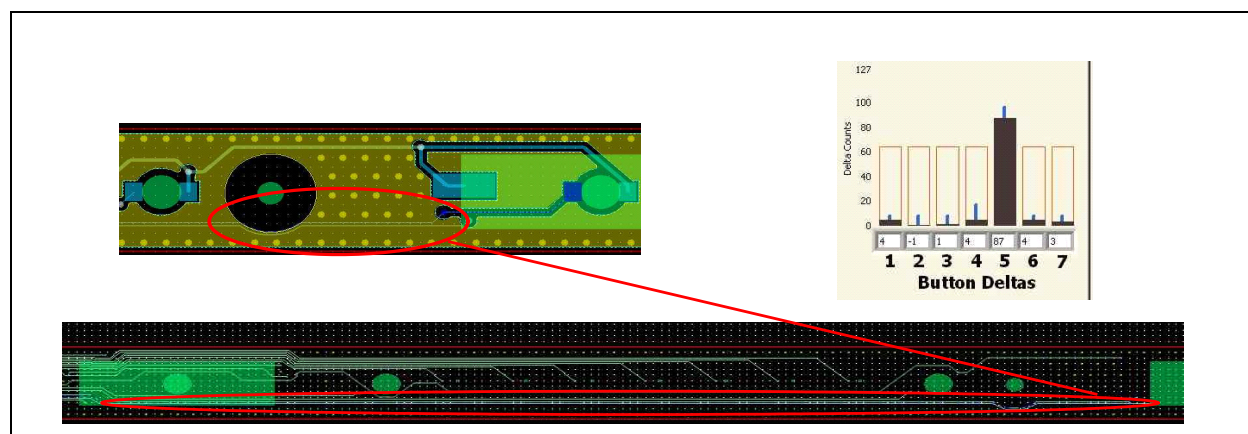
Figure A.5 Incorrect Layout Example 3 - Parallel Traces

- 4 traces (LED4, LED5, LED9 and LED10) were routed under CS4, a 5.5 mm x 16 mm pad. When driving these LED signals, higher Delta counts are observed (Figure A.6).
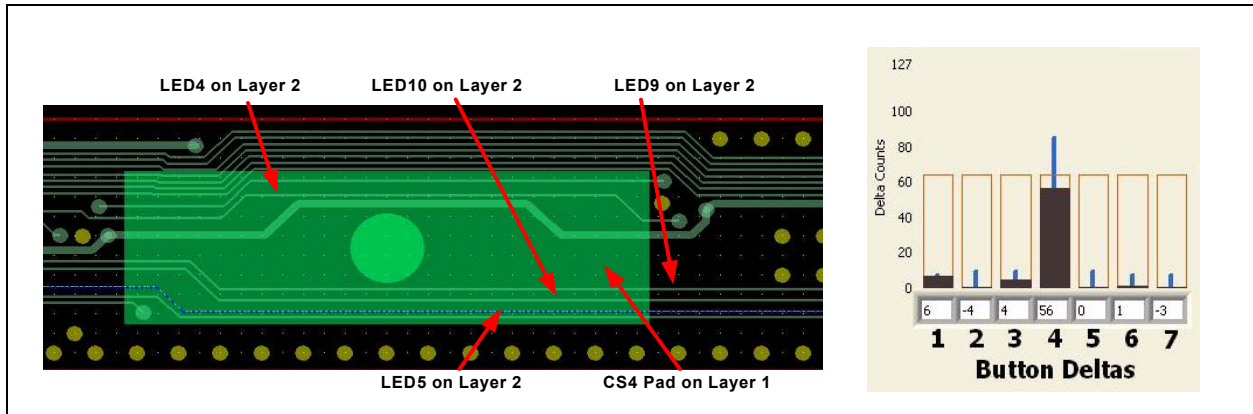
Figure A.6 Incorrect Layout Example 3 - LED Traces Under CS Pad

APPLICATION NOTE

Application Note Revision History

Customer Revision History

REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.2 (06-07-10)	Document	Rearranged sections.
	Section 6, "PCB Design Considerations"	Consolidated PCB recommendations, added additional recommendations, and expanded checklist.
	Section 9, "Electromagnetic Compatibility"	Added.
	Section 10, "RF Immunity"	Added.
Rev. 1.1 (09-04-09)	Figure A.1, "LED/CS Signal Coupling" and Figure A.2, "LED/CS Signal Coupling Equivalent Circuit" and Figure A.6, "Incorrect Layout Example 3 - LED Traces Under CS Pad"	Figures modified.
	Section 1, "Overview"	Added note. Not all features described in this document apply to all devices.
	Section 6.3.3, "Layout Checklist"	Added "no" to item #3 and removed commas. "Ensure there are **no** LED traces on L2 under CS Pads or on L1." LED traces cannot be on L1. If necessary, they can be on L2, but cannot be under any CS Pads. Added item #16: "If off-board cabling is utilized, isolate the communications pins by installing series resistors." em: changed section to 6.3.3
Rev. 1.0 (06-02-09)	Initial release	