

# Operational Amplifier Design

Daniel Raymond

## Design constraints and requirements

- Discrete component design for manufacturing and assembly
- Standard 1% resistor and capacitor values
- Combination of FET and BJT devices
- 50uA bias supply (commercial, off-the-shelf component)
- Split +/-15v power supply

## Component selection

- Ultra low gate charge FETs to increase bandwidth at low bias currents
- BSS84AKQB P-Channel FET
- 2N7002KQB N-Channel FET
- Matched NPN and PNP pair for better biasing and symmetrical gain
- 2N2907 PNP BJT
- 2N2222 NPN BJT

## Spice Models

```
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*****
* Model generated on Feb 28, 13
* MODEL FORMAT: PSpice
.MODEL Q2n2222a npn
+IS=3.88184e-14 BF=929.846 NF=1.10496 VAF=16.5003
+IKF=0.019539 ISE=1.0168e-11 NE=1.94752 BR=48.4545
+NR=1.07004 VAR=40.538 IKR=0.19539 ISC=1.0168e-11
+NC=4 RB=0.1 IRB=0.1 RBM=0.1
+RE=0.0001 RC=0.426673 XTB=0.1 XTI=1
+EG=1.05 CJE=2.23677e-11 VJE=0.582701 MJE=0.63466
+TF=0.06711e-10 XTR=3.92912 VTF=17712.6 ITF=0.4334
+CJC=2.23943e-11 VJC=0.576146 MJC=0.632796 XCJC=1
+FC=0.170253 CJS=0 VJS=0.75 MJS=0.5
+TR=1e-07 PTF=0 KF=0 AF=1
*****
```

```
*****
* NXP BSS84AK
* Polarity P-Channel
* Ratings 50V/4.50E+00OHMS/0.18A
* Date Created Thu Apr 7 07:37:44 2011
*****
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*****
.MODEL MINT NMOS Vto= 1.796 Kp= 663.5m Nfs= 469.8G Eta= 0.000
+ Level= 3 Gamma= 0.000 Phi= 600.0m Is= 1.000E-24 UO= 600.0
+ Js= 0.000 Pb= 800.0m Cj= 0.000 Cjsw= 0.000 Cgso= 0.000 Cgdo=
0.000 Cgbo= 0.000
+ Tox= 100.0n Xj= 0.000
+ Vmax= 1.198K
```

```
.MODEL D_DBDB D Bv= 68 Ibv= 250.0u Rs= 1.000u Is= 3.399f
+ N= 1.000 M= 264.7m VJ= 40.00m Fc= 500.0m Cjo= 5.23p Tt= 18.50n
.ENDS 2N7002AK-Q
```

```
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*****
* Model generated on Mar 1, 13
* MODEL FORMAT: PSpice
.MODEL Q2n2907a pnp
+IS=3.02341e-12 BF=523.064 NF=1.16335 VAF=44.2994
+IKF=0.591421 ISE=3.31443e-11 NE=1.9954 BR=4.8572
+NR=1.18959 VAR=1.33092 IKR=5.91421 ISC=3.31443e-11
+NC=3.81262 RB=2.76209 IRB=0.1 RBM=0.880912
+RE=0.0001 RC=0.857407 XTB=0.119647 XTI=1
+EG=1.05 CJE=3.934e-11 VJE=0.680693 MJE=0.379312
+TF=2.75919e-10 XTR=0.674951 VTF=54426.6
ITF=0.067962
+CJC=2.40198e-11 VJC=0.4 MJC=0.462796 XCJC=1
+FC=0.570446 CJS=0 VJS=0.75 MJS=0.5
+TR=1e-07 PTF=0 KF=0 AF=1
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```

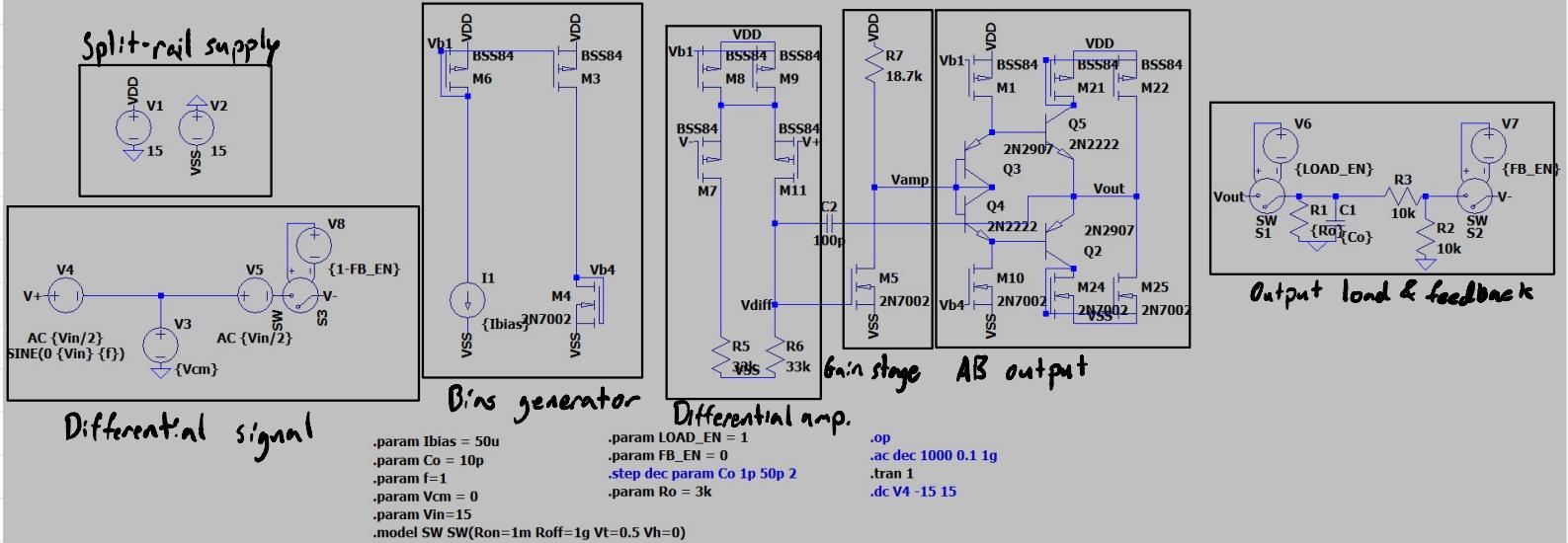
  

```
*****
* NXP BSS84AK
* Polarity P-Channel
* Ratings 50V/4.50E+00OHMS/0.18A
* Date Created Thu Apr 7 07:37:44 2011
*****
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*****
.MODEL MINT PMOS (Vto=-1.66 Kp=1.3807e-01 Nfs=1000000000 Eta=0
+ Level=3 L=1e-4 W=1e-4 Gamma=0 Phi=0.6 Is=1e-24
+ Js=0 Pb=0.8 Cj=0 Cjsw=0 Cgso=0 Cgdo=0 Cgbo=0
+ Tox=1e-07 Xj=0
+ U0=600 Vmax=3000)
++ U0=600 Vmax=1000)
```

```
.MODEL DBD D(Bv=63.00 Ibv=2.00E-06 Rs=1E-6 Is=1.48118796889277e-15
+ N=1 M=0.33 VJ=0.53 Fc=0.5 Cjo=1.144e-11 Tt=1.85e-08)
.ENDS
```

## Schematic



## Hand Analysis

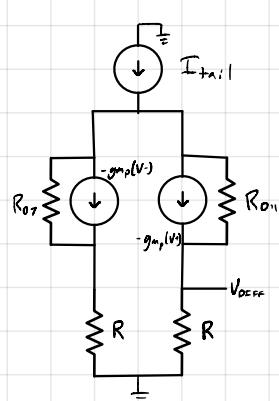
### Bias generator

$$I_{D0} = I_{bias} = 50\mu A \quad V_{b1} = V_{DD} - V_{BSB} = 15 - \left( \sqrt{\frac{2 I_{D0}}{k'_p \frac{w}{L} (1-\lambda V_{AS})}} + V_{th} \right) \approx 15 - \left( \sqrt{\frac{2 I_{D0}}{k'_p \frac{w}{L}}} + V_{th} \right) = 13.313v$$

$$I_{D3} = \frac{k'_p}{2} \frac{w}{L} (V_{DD} - V_{B1} - V_{th})^2 (1-\lambda V_{AS}) \approx \frac{k'_p}{2} \frac{w}{L} (V_{DD} - V_{B1} - V_{th})^2 = 50\mu A \text{ // property of current mirror}$$

$$I_{D4} = I_{D3} = 50\mu A \quad V_{b4} = V_{BS} + V_{BS4} = -15 + \sqrt{\frac{2 I_{D4}}{k'_p \frac{w}{L} (1-\lambda V_{AS})}} + V_{th} \approx -15 + \sqrt{\frac{2 I_{D0}}{k'_p \frac{w}{L}}} + V_{th} = -13.192v$$

### Differential amp.



$$g_{mp} = \sqrt{2 k'_p \frac{w}{L} \frac{I_{D8} + I_{D9}}{2}} = 3.7158mA/V$$

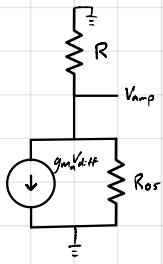
$$\alpha_v = \frac{V_{diff}}{(V_+ - V_-)} = \frac{R(-g_{mp}(V_+) + g_{mp}(V_-))}{(V_+ - V_-)} = \frac{(V_+ - V_-)(-g_{mp})(R)}{V_+ - V_-} = -g_{mp} R$$

$$V_{diff} = V_{b4} \text{ // to bias gain stage}$$

$$R = \frac{V_{diff} - V_{BS}}{I_{D8+D9}/2} = \frac{1.908V}{50\mu A} = 36.16k$$

$$\alpha_v = -134.36 = 42.57dB \angle 180^\circ$$

## Gain stage



$$V_{\text{amp}} = -g_{m1} V_{\text{diff}} (R \parallel R_{05}) \approx -g_{m1} V_{\text{diff}} R$$

Biasing w/ simulation

$$R_5 = R_6 = 33.2 \text{ k}$$

$$I_{D5} = 800 \mu\text{A} // \text{strongly affected by } V_{\text{th}} \text{ & } R_6$$

$$R = \frac{V_{\text{op}}}{I_{D5}} = \frac{15\text{V}}{800 \mu\text{A}} = 18.75 \text{ k} \Rightarrow 18.7 \text{ k}$$

$$a_v = \frac{V_{\text{amp}}}{V_{\text{diff}}} = -g_{m1} R = -\sqrt{2k_n' \times I_{D5}} R = -609.29 = 55.70 \text{ dB } \angle -180^\circ$$

$$R_0 = R \parallel R_{05} \approx R = 18.7 \text{ k}$$

AB output

Voltage follower proof:

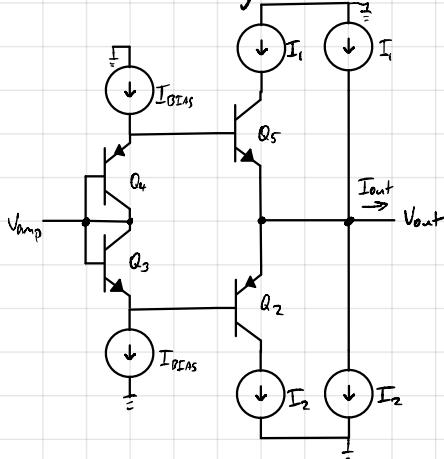
$$V_{B3} = V_{B4} = V_{\text{amp}} \quad V_{E3} = V_{B3} + 0.7 \quad V_{E4} = V_{B4} - 0.7$$

$$V_{E5} = V_{E3} - 0.7 \quad V_{E2} = V_E + 0.7$$

$$V_{E5} = V_{B3} = V_{B4} = V_{E3}$$

$$V_{E5} = V_{E2} = V_{\text{amp}}$$

Current gain:



I<sub>out</sub> < 0

$$i_2 = i_{\text{out}}/2 // \text{current mirror}$$

$$i_{b2} \approx i_2/\beta_p // \beta \text{ assumption}$$

$$i_{b3} \approx i_{b2}/\beta_n // \beta \text{ assumption}$$

$$\frac{i_{\text{out}}}{i_{b3}} = \frac{i_{b3} \cdot \beta_p \beta_n^2}{i_{b3}} = 2 \beta_p \beta_n = 0.97274 \text{ A/}\mu\text{A}$$

I<sub>out</sub> > 0

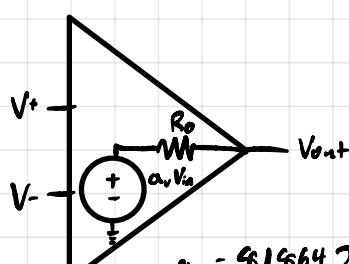
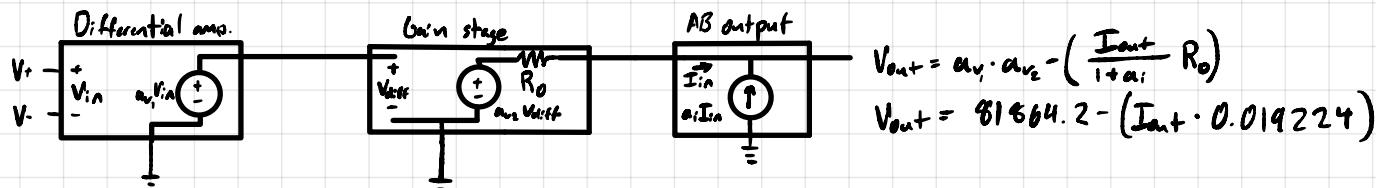
$$i_1 = i_{\text{out}}/2$$

$$i_{b5} = i_1/\beta_n$$

$$i_{b4} = i_{b5}/\beta_p$$

$$\frac{i_{\text{out}}}{i_{b4}} = 2 \beta_n \beta_p = 0.97274 \text{ A/}\mu\text{A}$$

Small signal block diagram



$$a_v = 81864.2 \text{ V/V} = 95.262 \text{ dB}$$

$$R_o = 0.019224 \Omega$$

# Simulation

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## Operating point

--- Operating Point ---

```
V(vb1): 13.0383 voltage
V(vss): -15 voltage
V(vdd): 15 voltage
V(n002): 1.96169 voltage
V(n011): 0 voltage
V(v+): 0 voltage
V(n010): -13.499 voltage
V(n009): -2.53932 voltage
V(vout): -1.95025 voltage
V(vamp): -1.96196 voltage
V(n005): -1.3845 voltage
V(n001): -13.0563 voltage
V(n006): -5.8566e-06 voltage
V(n007): -0.975123 voltage
V(vb4): -13.5293 voltage
V(p001): 0 voltage
V(vdiff): -13.34 voltage
V(n012): -13.34 voltage
V(v-): -9.76098e-13 voltage
V(n003): 0 voltage
V(n004): 0 voltage
V(n008): 1 voltage
```

Ic(Q2):	-8.48159e-05 device_current	I(C1):	-5.8566e-29 device_current
Ib(Q2):	-3.10942e-07 device_current	I(C2):	1.13897e-21 device_current
Ie(Q2):	8.51268e-05 device_current	I(I1):	5e-05 device_current
Ic(Q3):	-4.96435e-05 device_current	I(R1):	-1.9522e-09 device_current
Ib(Q3):	-1.98608e-07 device_current	I(R2):	-9.75123e-05 device_current
Ie(Q4):	4.98422e-05 device_current	I(R3):	9.75132e-05 device_current
Ic(Q4):	4.94419e-05 device_current	I(R5):	5e-05 device_current
Ib(Q4):	2.47251e-07 device_current	I(R6):	5e-05 device_current
Ie(Q4):	-4.96891e-05 device_current	I(R7):	0.000907057 device_current
Ic(Q5):	3.61348e-05 device_current	I(S1):	-1.9522e-09 device_current
Ib(Q5):	1.57878e-07 device_current	I(S2):	-9.76098e-10 device_current
Ie(Q5):	-3.62927e-05 device_current	I(S3):	9.76098e-10 device_current
Id(M6):	-5e-05 device_current	I(V1):	-0.00122933 device_current
Ig(M6):	-2.48314e-11 device_current	I(V2):	-0.00132684 device_current
Is(M6):	5e-05 device_current	I(V3):	-9.76098e-10 device_current
Id(M8):	-5e-05 device_current	I(V4):	0 device_current
Ig(M8):	-2.36595e-12 device_current	I(V5):	9.76098e-10 device_current
Is(M8):	5e-05 device_current	I(V6):	0 device_current
Id(M9):	-5e-05 device_current	I(V7):	0 device_current
Ig(M9):	-2.36595e-12 device_current	I(V8):	0 device_current
Is(M9):	5e-05 device_current		
Id(M21):	-3.61348e-05 device_current		
Ig(M21):	-2.48309e-11 device_current		
Is(M21):	3.61348e-05 device_current		
Id(M22):	-3.61348e-05 device_current		
Ig(M22):	-2.00943e-12 device_current		
Is(M22):	3.61348e-05 device_current		
Id(M3):	-5e-05 device_current		
Ig(M3):	-1.57075e-12 device_current		
Is(M3):	5e-05 device_current		
Id(M1):	-5e-05 device_current		
Ig(M1):	-2.05016e-12 device_current		
Is(M1):	5e-05 device_current		
Id(M7):	-5e-05 device_current		
Ig(M7):	-2.1351e-12 device_current		
Is(M7):	5e-05 device_current		
Id(M11):	-5e-05 device_current		
Ig(M11):	-2.1351e-12 device_current		
Is(M11):	5e-05 device_current		
Id(M24):	8.48159e-05 device_current		
Ig(M24):	-5.35491e-11 device_current		
Is(M24):	-8.48159e-05 device_current		
Id(M25):	8.48159e-05 device_current		
Ig(M25):	-1.42847e-11 device_current		
Is(M25):	-8.48159e-05 device_current		
Id(M4):	5.00001e-05 device_current		
Ig(M4):	-5.35491e-11 device_current		
Is(M4):	-5.00001e-05 device_current		
Id(M10):	5.00001e-05 device_current		
Ig(M10):	-1.44002e-11 device_current		
Is(M10):	-5.00001e-05 device_current		
Id(M5):	0.00090721 device_current		
Ig(M5):	-1.43188e-11 device_current		
Is(M5):	-0.00090721 device_current		

## AC Gain and Bandwidth

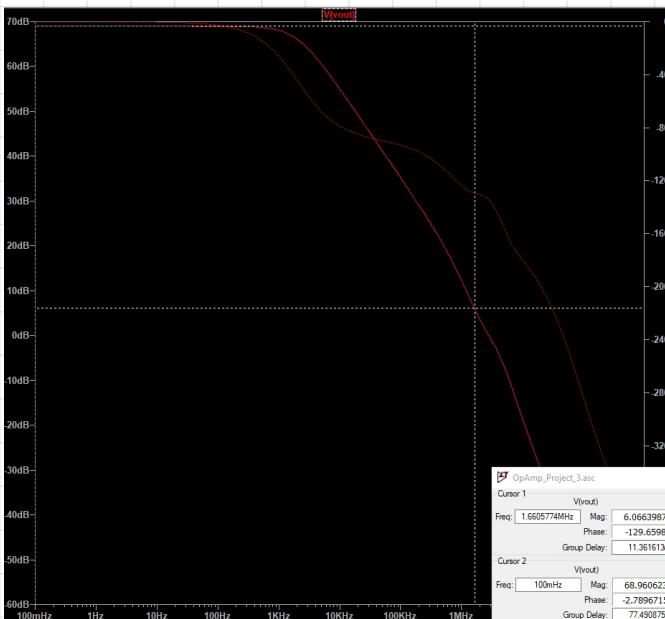
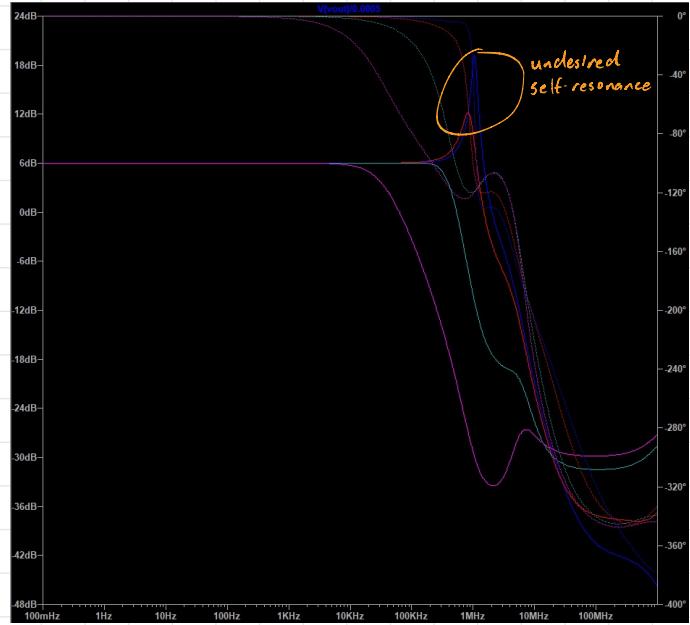
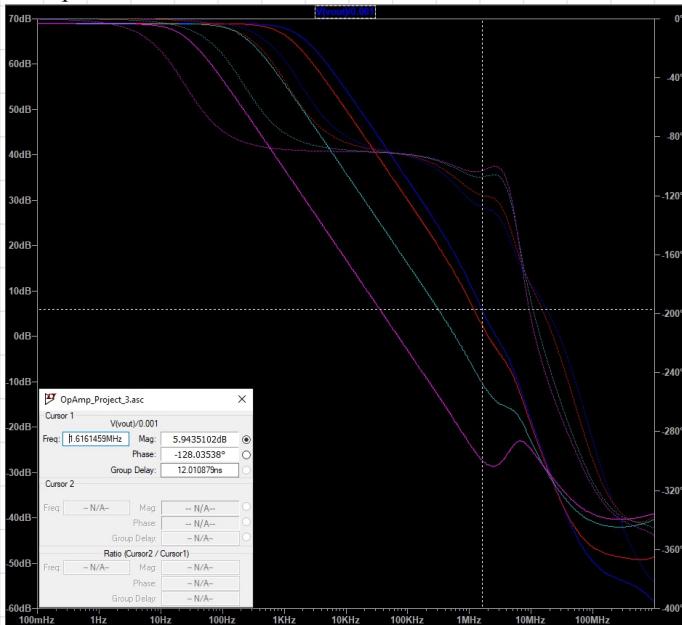


Fig 1: Open loop gain without compensation

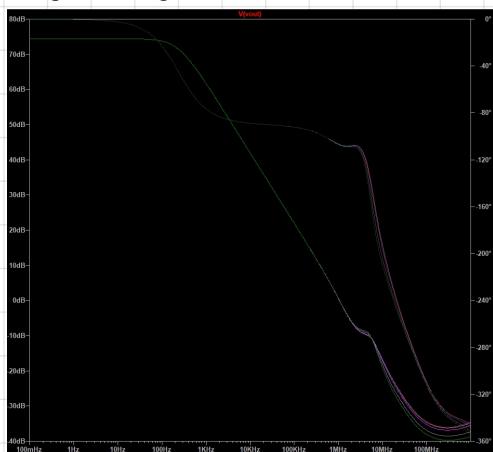
lower gain than expected because of differential stage parasitics. The parasitics in the first stage play the largest role because of small bias current and large output impedance. That lead the design decision to minimize active components in the gain stages. The gain-bandwidth product of  $\approx 3.23$  MHz seems to be an intrinsic property of the components available. Given the limitations of components, the design was used despite not meeting the expected bandwidth.

## Compensation



Compensation capacitor stepped  $1\text{pF}$ ,  $10\text{pF}$ ,  $100\text{pF}$ ,  $1\text{nF}$ . Bandwidth decreased, but loop stability improved.  $100\text{pF}$  selected for moderate bandwidth, and clean pole near unity gain.

## Output loading



$$C_L = 1\text{p}, 5\text{p}, 10\text{p}, 50\text{p}$$

Minimal effect on gain/phase

Fig 4: Effects of load capacitance

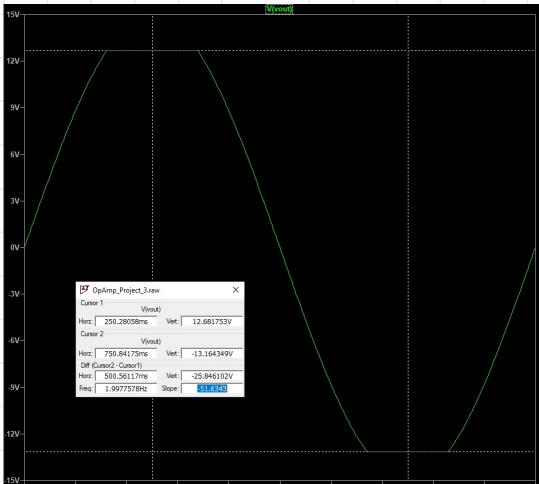


Fig 5: Voltage swing with  $3\text{k}\Omega$  load

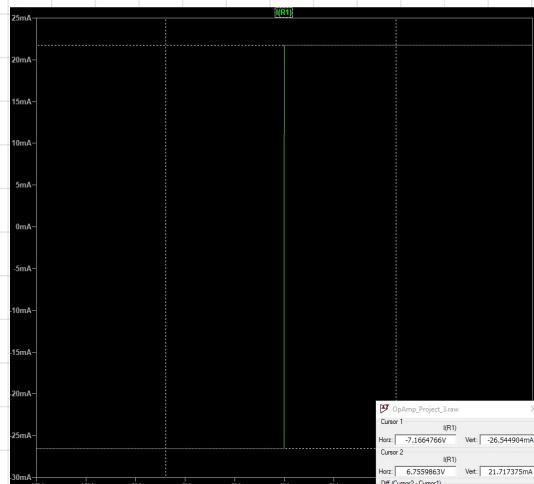
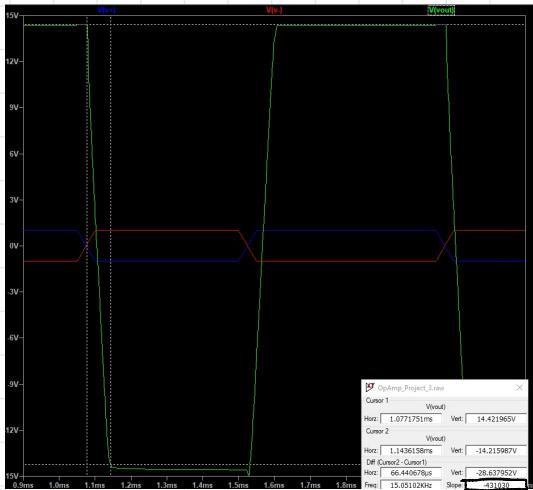
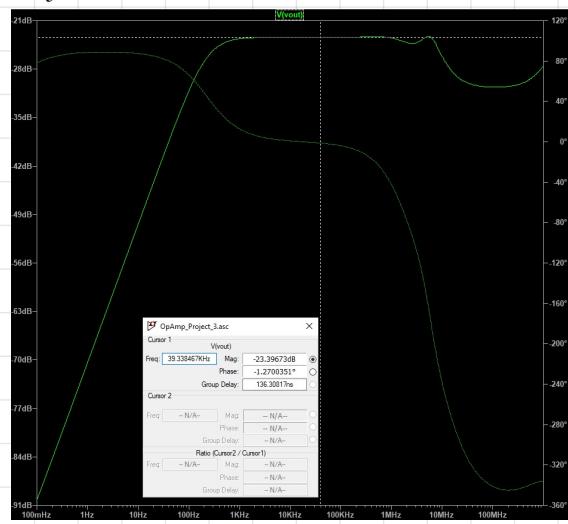


Fig 6: Current output into short circuit

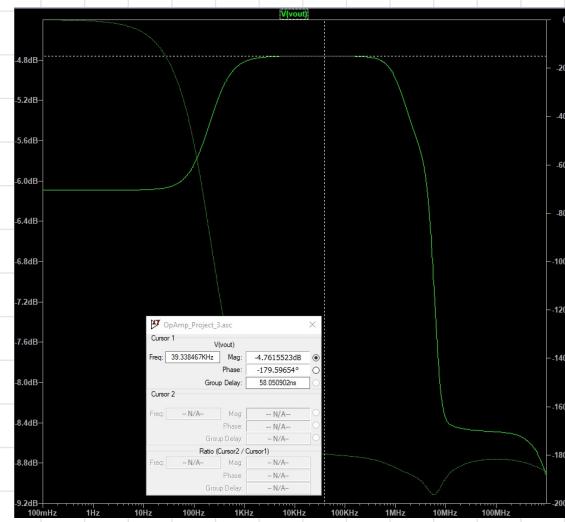
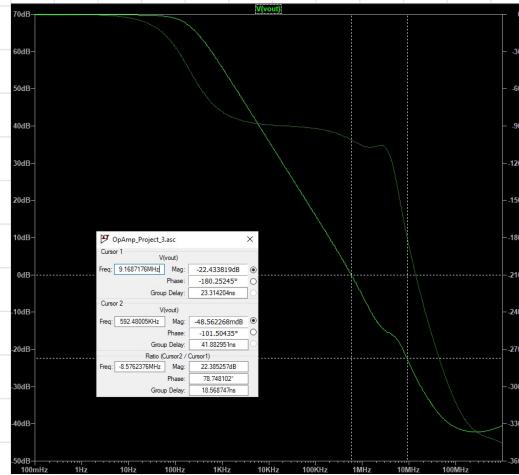
## Frequency Response



Rejection ratios



$$CMRR = \frac{a_v}{a_{cm}} = 68.96 - (-23.40) = 92.36 \text{ dB}$$



## Table of Properties

Minimum closed-loop gain	$6 \text{ dB}$
Dual power supply	$\pm 15 \text{ V}$
Quiescent power dissipation	$38.34 \text{ mW}$
Output current (source and sink)	$21.71 \text{ mA}, -26.5^{\circ}\text{mA}$
Slew rate	$0.4310 \text{ V}/\mu\text{s}$
Input bias current	$0 \text{ A}$
Positive output voltage swing	$12.68 \text{ V}$
Negative output voltage swing	$-13.16 \text{ V}$
Maximum capacitive load	$> 50 \text{ pF}$
Minimum resistive load	$< 3 \text{ k}\Omega$
Open loop gain	$68.96 \text{ dB}$
Phase margin	$49^{\circ}$
Gain margin	$22.43 \text{ dB}$
Closed loop bandwidth	$0.4279 \text{ MHz}$