CETT1429 **Name _____**
Semester Project Amplifier **Date _____**

Object:

- Design, build, and test a multistage transistor amplifier. The amplifier final design must meet the specifications listed below.

Specifications:

Supply voltage:	V_{CC}	≤	15 Volts DC
Supply current:	I_S	≤	200 mA at maximum output
Input impedance:	Z_{IN}	≥	20 kilohms (measured @ 1 KHz)
Voltage Gain:	A_V	=	100 +/- 5 from 100 Hz to 15 kHz
Load Resistance:	R_L	=	1 kohm +/- 5% (AC coupled)
Active devices:	no more than three transistors		
Passive devices:	resistors and capacitors must be standard values available in lab		
Output voltage:	must be capable of a 6 volt peak-to-peak sine wave with no visible distortion when viewed on an oscilloscope		

- **Your completed final report is due on or before date:_____ and will not be accepted after that date.**

- Reports will be graded primarily on the completeness of the design, the reporting AND analysis of each change made in the circuit from the initial design to the final working version. All measurements and every change made from the original version in Step #2 should be carefully documented. Record why each change was made and how it changed the operation of the circuit. This is to be the basis for your grade.

Procedure:

Step #1: Make decisions on

- Number of stages
- Gain of each stage
- Power supply voltage

- Begin working on design of the amplifier starting from the last stage. After the last stage design is completed, use the input impedance of the last stage as a load for the previous stage, and design that stage. You will probably have to rework your design several times to get the gain and input impedance correct, since changing the gain or input impedance of a stage will cause changes in all preceding stages.

Step #2: Submit first draft of complete design for instructor's approval at the beginning of the lab period. Draw each stage on one sheet. Show all calculations for each stage on the same sheet.

ALTERNATE APPROACH: Design the amplifier, construct the amplifier in Multisim, and print the Multisim schematics to attach to your calculation sheets.

- Your design sheet will be copied and returned to you immediately for use in the steps listed below.
- Construct last stage and check Q-point voltage only. Record the Q-point voltage measured from your unchanged design on the lab data sheet. Then redesign to get a better Q-point, if necessary.
- Construct middle stage (if used) and check Q-point only, recording the voltage and then redesigning, if necessary.
- Construct first stage and check Q-point only, as in the previous stages.

Step #3: After correcting Q-points (if necessary), connect stages, recheck Q-points, and input a 1 KHz, 0.06 volt peak-to-peak sine wave. A voltage divider may be needed to reduce the signal generator output to 0.06 volt p-p. Measure and record the input and output voltage of each stage, and calculate the voltage gain of each stage, and of the overall amplifier.

Step #4: Make final corrections to voltage gain. Measure Z_{IN}. Check frequency response. Set up circuit for instructor evaluation with AC input.

Step #5: Submit final drawing, calculations, and measured data as recorded on the final data sheet.

Include a schematic or copy + paste one here.

Step #1 Data Sheet **Name _____**
CETT1429 Semester Project Amplifier **Date _____**

Number of stages _____

Stage 1 gain _____

Stage 2 gain _____

Stage 3 gain _____

Include a schematic or copy + paste one here.

Step #2 Data Sheet **Name _____**
CETT1429 Semester Project Amplifier **Date _____**

	STAGE 1	STAGE 2	STAGE 3	
❑ List the Q-points of each stage as originally designed.				
V_{CQ} (measured)	_____	_____	_____	volts DC
V_B (measured)	_____	_____	_____	volts DC
❑ List changes made to correct Q-points or gain. Include original value of resistors, and the **actual** value used in lab.				
R_1 (original)	_____	_____	_____	
R_1 (final design)	_____	_____	_____	
R_2 (original)	_____	_____	_____	
R_2 (final design)	_____	_____	_____	
❑ List the final design values for the Q-points of each stage.				
	STAGE 1	STAGE 2	STAGE 3	
V_{CQ} (measured)	_____	_____	_____	volts DC
V_{BQ} (measured)	_____	_____	_____	volts DC

Step #3 Data Sheet **Name _____**
CETT1429 Semester Project Amplifier **Date _____**

- Before measuring any AC voltages, connect an oscilloscope to the input, and with the input connected to the signal generator and the amplifier power on, adjust the signal generator so that the input to the amplifier output is 0.06 v p-p @ 1 KHz (sinewave). Do not change this setting.
- Note that the signal generator output can be more easily adjusted if you use a 100:1 voltage divider on the output of the generator. This will reduce a 6 Vp-p signal generator output to 0.06 Vp-p

Note: Base the A_V(theory) on the **actual resistors** used.

A_V (theory)	_____	_____	_____	
V_{IN}	0.06	_____	_____	V p-p
V_{OUT}	_____	_____	_____	V p-p
Av (V_{OUT}/V_{IN})	_____	_____	_____	

- Explain why you think the voltage gains you have measured are not the same as the theoretical gain calculated for each stage. Explain what you intend to do to correct the gain.

This sheet is to be completed by the laboratory instructor. Set up and test the complete amplifier, and then tell the laboratory instructor that you are ready for final check.

FINAL DATA SHEET
CETT1429 Semester Project Amplifier

Name _____
Date _____

- ❑ All measurements recorded below should be made with the laboratory oscilloscopes.
- ❑ Before measuring any voltages, connect an oscilloscope to the final load resistor and to the input, and with the input connected to the signal generator and the amplifier power on, adjust the signal generator so that the amplifier output is 6 V p-p (2.12 V RMS) @ 1 KHz (sinewave).
- ❑ If your circuit is not capable of 6 V p-p output, reduce the input until the output is undistorted, record V_{OUT}, and proceed with the measurements, substituting your output voltage for 6 V.

	STAGE 1	STAGE 2	STAGE 3	
A_V (theory)	_____	_____	_____	
V_{IN}	0.06	_____	_____	V p-p
V_{OUT}	_____	_____	_____	V p-p
A_V (V_{OUT}/V_{IN})	_____	_____	_____	

- ❑ Measure Z_{IN} by placing a 22 K resistor in series with the input, readjusting the signal generator to produce 6 V p-p at the output, and calculating Z_{IN} using Ohm's Law.

  Z_{IN} (theory) _____

  Z_{IN} (measured) _____

- ❑ Measure the voltage gain at the minimum and maximum frequencies specified at the beginning of this laboratory.

  A_V (overall) @ 1KHz = Av (V_{OUT3}/V_{IN1}) = _____ (from data above)

  ❑

  A_V (overall) @ 100 Hz = _____

  A_V (overall) @ 15 KHz = _____

  ❑

- ❑ Attach LTSpice simulation and plot printouts

  ❑

- ❑ Attach Fritzing or other CAD drawings

  ❑

- ❑ Attach or email waveforms from oscilloscope indicating that the amplifier meets specifications.

  ❑

- ❑ Bonus: Attach a PCB design from Fritzing or some other CAD package

  ❑