7.1.6 Power supply scheme

 $V_{DD33USB}$ $V_{DD50USB}$ USB V_{SS} IOs USB V_{DDLDO} V_{SS} regulator Core domain (V_{CORE}) Voltage regulator Power switch D3 domain (System Level shifter D1 domain logic, (CPU, peripherals, EXTI, D2 domain 10 IOs Peripherals, RAM) (peripherals, logic RAM) RAM) Flash V_{DD} VDD domain HSI, LSI, CSI, HSI48, HSE, PLLs **VBAT** Backup domain charging Backup V_{BAT} regulator 1.2 to 3.6\ Power switch LSE, RTC, Wakeup logic, Backup backup RAM BKUP Ю registers, IOs logic Reset V_{REF} V_{DDA} Vss Analog domain REF_BUF ADC, DAC nF + 1 × 1 µF OPAMP, V_{REF+} Comparator V_{REF} 8 MSv46116V5

Figure 68. Power supply scheme

- 1. N corresponds to the number of VDD pins available on the package.
- 2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Caution:

Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the

4