Chapter 6

Two-Level Voltage Source Inverter

6.1 INTRODUCTION

The primary function of a voltage source inverter (VSI) is to convert a fixed dc voltage to a three-phase ac voltage with variable magnitude and frequency. A simplified circuit diagram for a two-level voltage source inverter for high-power medium-voltage applications is shown in Fig. 6.1-1. The inverter is composed of six group of active switches, $S_1 \sim S_6$, with a free-wheeling diode in parallel with each switch. Depending on the dc operating voltage of the inverter, each switch group consists of two or more IGBT or GCT switching devices connected in series.

This chapter focuses on **pulse width modulation** (PWM) schemes for the high-power two-level inverter, where the device switching frequency is normally below 1 kHz. A carrier-based sinusoidal PWM (SPWM) scheme is reviewed, followed by a detailed analysis on **space vector modulation** (SVM) algorithms. The conventional SVM scheme usually generates both even- and odd-order harmonics voltages. The mechanism of even-order harmonic generation is analyzed, and a modified SVM scheme for even-order harmonic elimination is presented.

6.2 SINUSOIDAL PWM

6.2.1 Modulation Scheme

The principle of the sinusoidal PWM scheme for the two-level inverter is illustrated in Fig. 6.2-1, where v_{mA}, v_{mB}, and v_{mC} are the three-phase sinusoidal **modulating waves** and v_{cr} is the triangular **carrier wave**. The fundamental-frequency component in the inverter output voltage can be controlled by **amplitude modulation index**

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{6.2-1}$$

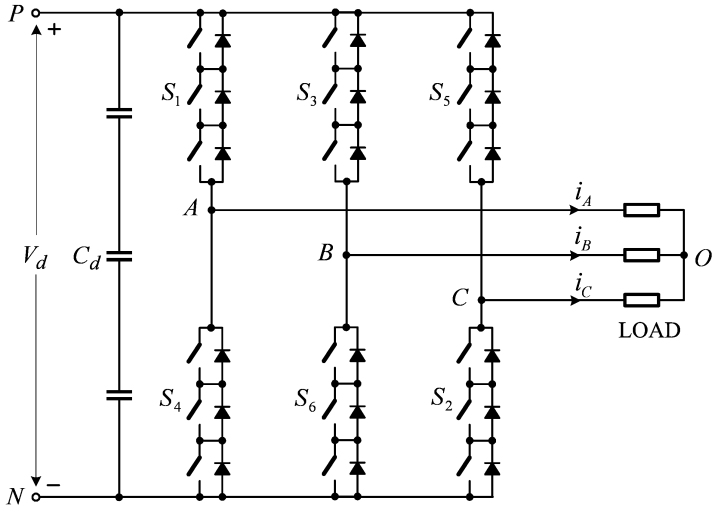


Figure 6.1-1 Simplified two-level inverter for high-power applications.

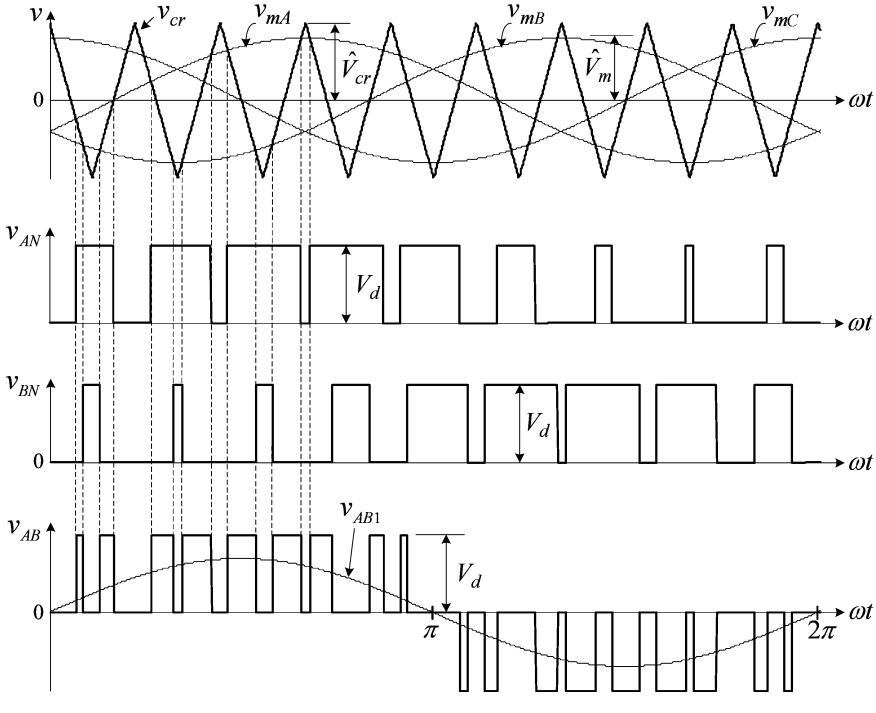


Figure 6.2-1 Sinusoidal pulse-width modulation (SPWM).

where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak values of the modulating and carrier waves, respectively. The amplitude modulation index m_a is usually adjusted by varying $\hat{V}_m$ while keeping $\hat{V}_{cr}$ fixed. The **frequency modulation index** is defined by

$$m_f = \frac{f_{cr}}{f_m} \tag{6.2-2}$$

where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively.

The operation of switches S_1 to S_6 is determined by comparing the modulating waves with the carrier wave. When $v_{mA} \geq v_{cr}$, the upper switch S_1 in inverter leg A is turned on. The lower switch S_4 operates in a complementary manner and thus is switched off. The resultant **inverter terminal voltage** v_{AN}, which is the voltage at the phase A terminal with respect to the negative dc bus N, is equal to the dc voltage V_d. When $v_{mA} < v_{cr}$, S_4 is on and S_1 is off, leading to $v_{AN} = 0$ as shown in Fig. 6.2-1. Since the waveform of v_{AN} has only two levels, V_d and 0, the inverter is known as a **two-level inverter**. It should be noted that to avoid possible short circuit during switching transients of the upper and lower devices in an inverter leg, a **blanking time** should be implemented, during which both switches are turned off.

The inverter line-to-line voltage v_{AB} can be determined by $v_{AB} = v_{AN} - v_{BN}$. The waveform of its fundamental-frequency component v_{AB1} is also given in the figure. The magnitude and frequency of v_{AB1} can be independently controlled by m_a and f_m, respectively.

The **switching frequency** of the active switches in the two-level inverter can be found from $f_{sw} = f_{cr} = f_m \times m_f$. For instance, v_{AN} in Fig. 6.2-1 contains nine pulses per cycle of the fundamental frequency. Each pulse is produced by turning S_1 on and off once. With the fundamental frequency of 60 Hz, the resultant switching frequency for S_1 is $f_{sw} = 60 \times 9 = 540$ Hz, which is also the carrier frequency f_{cr}. It is worth noting that the device switching frequency may not always be equal to the carrier frequency in multilevel inverters. This issue will be addressed in the later chapters.

When the carrier wave is synchronized with the modulating wave (m_f is an integer), the modulation scheme is known as **synchronous PWM**, in contrast to **asynchronous PWM** whose carrier frequency f_{cr} is usually fixed and independent of f_m. The asynchronous PWM features a fixed switching frequency and easy implementation with analog circuits. However, it may generate **noncharacteristic harmonics**, whose frequency is not a multiple of the fundamental frequency. The synchronous PWM scheme is more suitable for implementation with a digital processor.

6.2.2 Harmonic Content

Figure 6.2-2 shows a set of simulated waveforms for the two-level inverter, where v_{AB} is the inverter line-to-line voltage, v_{AO} is the **load phase voltage** and i_A is the load current. The inverter operates under the condition of $m_a = 0.8$, $m_f = 15$, $f_m = 60$ Hz, and $f_{sw} = 900$ Hz with a rated three-phase inductive load. The load power factor is 0.9 per phase. We can observe the following:

- All the harmonics in v_{AB} with the order lower than $(m_f - 2)$ are eliminated.
- The harmonics are centered around m_f and its multiples such as $2m_f$ and $3m_f$.

The above statements are valid for $m_f \geq 9$ provided that m_f is a multiple of 3 [1].

The waveform of the load current i_A is close to sinusoidal with a THD of 7.73%. The low amount of harmonic distortion is due to the elimination of low-order harmonics by the modulation scheme and the filtering effect of the load inductance.

Figure 6.2-3 shows the harmonic content of the inverter line-to-line voltage v_{AB} normalized to its dc voltage V_d as a function of m_a, where V_{ABn} is the nth-order harmonic voltage (rms). The fundamental-frequency component V_{AB1} increases linearly with m_a, whose maximum value can be found from

$$V_{AB1,\max} = 0.612 V_d \qquad \text{for } m_a = 1 \tag{6.2-3}$$

The THD curve for v_{AB} is also given in the figure.

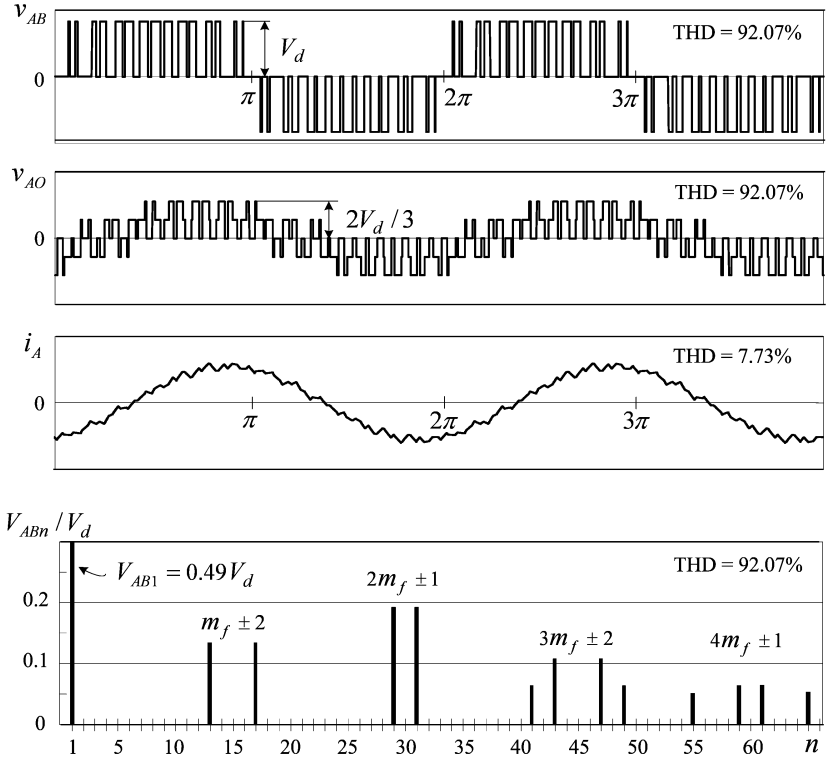


Figure 6.2-2 Simulated waveforms for the two-level inverter operating at $m_a = 0.8$, $m_f = 15$, $f_m = 60$ Hz, and $f_{sw} = 900$ Hz.

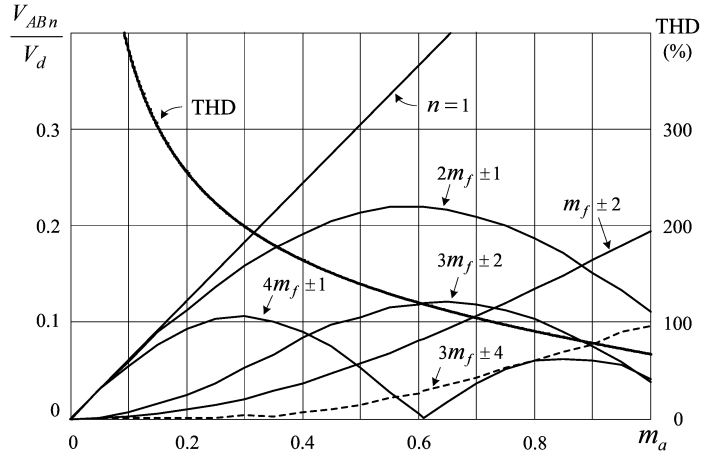


Figure 6.2-3 Harmonic content of v_{AB} in Fig. 6.2-2.

6.2.3 Overmodulation

Overmodulation occurs when the amplitude modulation index m_a is greater than unity. Figure 6.2-4 shows such a case with $m_a = 2$. The overmodulation causes a reduction in number of pulses in the line-to-line voltage waveform, leading to the emergence of low-order harmonics such as the 5th and 11th. However, the fundamental voltage V_{AB1} is boosted to $0.744V_d$, which represents a 22% increase in comparison with $0.612V_d$ at $m_a = 1$. With m_a further increased to 3.24, v_{AB} becomes a square wave, whose fundamental voltage is $V_{AB1} = 0.78V_d$, which is the highest possible value produced by the two-level VSI. The overmodulation is seldom used in practice due to the difficulties to filter out the low-order harmonics and the nonlinear relationship between V_{AB1} and m_a.

6.2.4 Third Harmonic Injection PWM

The inverter fundamental voltage V_{AB1} can also be increased by adding a third harmonic component to the three-phase sinusoidal modulating wave without causing overmodulation. This modulation technique is known as **third harmonic injection** PWM.

Figure 6.2-5 illustrates the principle of this PWM scheme, where the modulating wave v_{mA} is composed of a fundamental component v_{m1} and a third harmonic component v_{m3}, making v_{mA} somewhat flattened on the top. As a result, the peak fundamental component $\hat{V}_{m1}$ can be higher than the peak triangular carrier wave $\hat{V}_{cr}$, which boosts the fundamental voltage v_{AB1}. In the meantime the peak modulating wave $\hat{V}_{mA}$ can be kept lower than $\hat{V}_{cr}$, avoiding the problems caused by overmodulation. The maximum amount of v_{AB1} that can be increased by this scheme is 15.5% [2, 3].

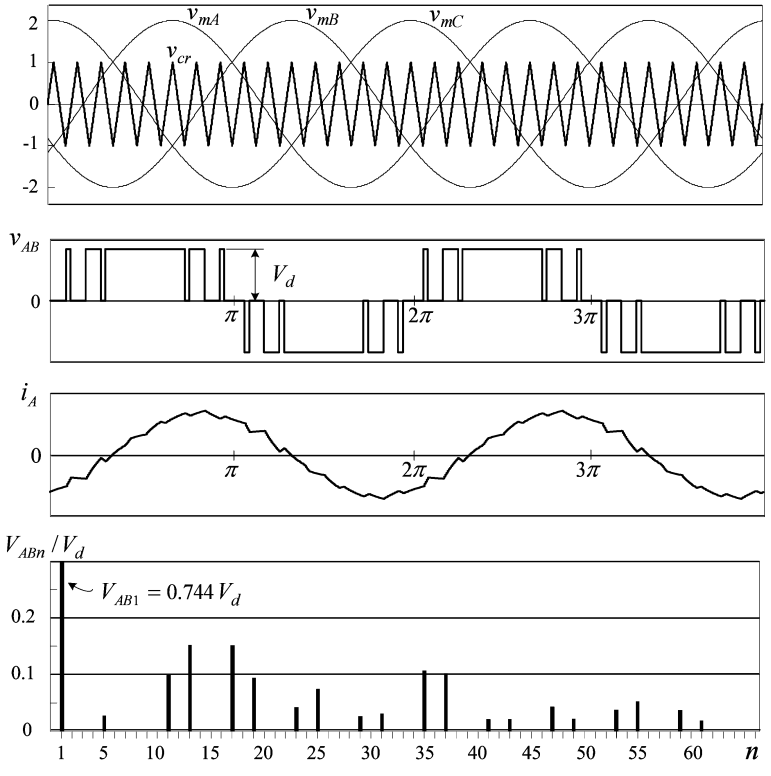


Figure 6.2-4 Overmodulation (m_a = 2.0, m_f = 15, and f_m = 60 Hz).

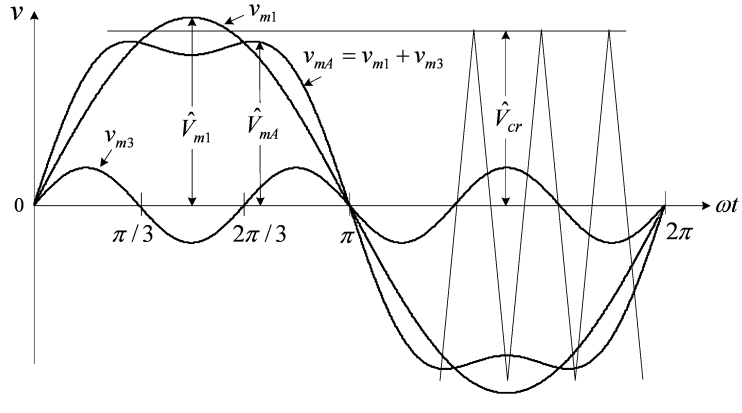


Figure 6.2-5 Modulating wave v_{mA} with third harmonic injection.

The injected third harmonic component v_{m3} will not increase the harmonic distortion for v_{AB}. Although it appears in each of the inverter terminal voltages v_{AN}, v_{BN} and v_{CN}, the third-order harmonic voltage does not exist in the line-to-line voltage v_{AB}. This is because the line-to-line voltage is given by $v_{AB} = v_{AN} - v_{BN}$, where the third-order harmonics in v_{AN} and v_{BN} are of zero sequence with the same magnitude and phase displacement and thus cancel each other.

6.3 SPACE VECTOR MODULATION

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters [3, 4]. This section presents the principle and implementation of the space vector modulation for the two-level inverter.

6.3.1 Switching States

The operating status of the switches in the two-level inverter in Fig. 6.1-1 can be represented by **switching states**. As indicated in Table 6.3-1, switching state 'P' denotes that the upper switch in an inverter leg is on and the inverter terminal voltage (v_{AN}, v_{BN}, or v_{CN}) is positive ($+V_d$) while 'O' indicates that the inverter terminal voltage is zero due to the conduction of the lower switch.

There are eight possible combinations of switching states in the two-level inverter as listed in Table 6.3-2. The switching state [POO], for example, corresponds to the conduction of S_1, S_6, and S_2 in the inverter legs A, B, and C, respectively. Among the eight switching states, [PPP] and [OOO] are **zero states** and the others are **active states**.

6.3.2 Space Vectors

The active and zero switching states can be represented by active and zero **space vectors**, respectively. A typical space vector diagram for the two-level inverter is shown in Fig. 6.3-1, where the six **active vectors** $\vec{V}_1$ to $\vec{V}_6$ form a regular hexagon with six equal sectors (I to VI). The **zero vector** $\vec{V}_0$ lies on the center of the hexagon.

Table 6.3-1 Definition of Switching States

Switching State	Leg A			Leg B			Leg C		
	S_1	S_4	v_{AN}	S_3	S_6	v_{BN}	S_5	S_2	v_{CN}
P	On	Off	V_d	On	Off	V_d	On	Off	V_d
O	Off	On	0	Off	On	0	Off	On	0

Table 6.3-2 Space Vectors, Switching States, and On-State Switches

Space Vector		Switching State (Three Phases)	On-State Switch	Vector Definition
Zero Vector	$\vec{V}_0$	[PPP] [OOO]	S_1, S_3, S_5 S_4, S_6, S_2	$\vec{V}_0 = 0$
Active Vector	$\vec{V}_1$	[POO]	S_1, S_6, S_2	$\vec{V}_1 = \frac{2}{3} V_d e^{j0}$
	$\vec{V}_2$	[PPO]	S_1, S_3, S_2	$\vec{V}_2 = \frac{2}{3} V_d e^{j\frac{\pi}{3}}$
	$\vec{V}_3$	[OPO]	S_4, S_3, S_2	$\vec{V}_3 = \frac{2}{3} V_d e^{j\frac{2\pi}{3}}$
	$\vec{V}_4$	[OPP]	S_4, S_3, S_5	$\vec{V}_4 = \frac{2}{3} V_d e^{j\frac{3\pi}{3}}$
	$\vec{V}_5$	[OOP]	S_4, S_6, S_5	$\vec{V}_5 = \frac{2}{3} V_d e^{j\frac{4\pi}{3}}$
	$\vec{V}_6$	[POP]	S_1, S_6, S_5	$\vec{V}_6 = \frac{2}{3} V_d e^{j\frac{5\pi}{3}}$

To derive the relationship between the space vectors and switching states, refer to the two-level inverter in Fig. 6.1-1. Assuming that the operation of the inverter is three-phase balanced, we have

$$v_{AO}(t) + v_{BO}(t) + v_{CO}(t) = 0 \tag{6.3-1}$$

where v_{AO}, v_{BO}, and v_{CO} are the instantaneous load phase voltages. From mathematical point of view, one of the phase voltages is redundant since given any two phase

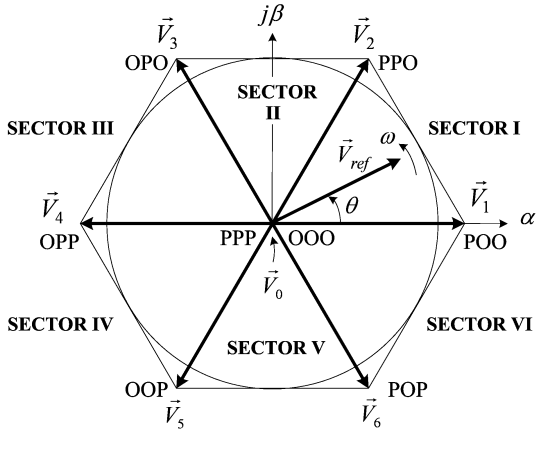


Figure 6.3-1 Space vector diagram for the two-level inverter.

voltages, the third one can be readily calculated. Therefore, it is possible to transform the three-phase variables to equivalent two-phase variables [5]:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{AO}(t) \\ v_{BO}(t) \\ v_{CO}(t) \end{bmatrix} \tag{6.3-2}$$

The coefficient 2/3 is somewhat arbitrarily chosen. The commonly used value is 2/3 or $\sqrt{2/3}$. The main advantage of using 2/3 is that the magnitude of the two-phase voltages will be equal to that of the three-phase voltages after the transformation. A space vector can be generally expressed in terms of the two-phase voltages in the α–β plane

$$\vec{V}(t) = v_\alpha(t) + jv_\beta(t) \tag{6.3-3}$$

Substituting (6.3-2) into (6.3-3), we have

$$\vec{V}(t) = \frac{2}{3}[v_{AO}(t)e^{j0} + v_{BO}(t)e^{j2\pi/3} + v_{CO}(t)e^{j4\pi/3}] \tag{6.3-4}$$

where $e^{jx} = \cos x + j\sin x$ and $x = 0$, $2\pi/3$ or $4\pi/3$. For active switching state [POO], the generated load phase voltages are

$$v_{AO}(t) = \frac{2}{3}V_d, \qquad v_{BO}(t) = -\frac{1}{3}V_d, \qquad \text{and} \qquad v_{CO}(t) = -\frac{1}{3}V_d \tag{6.3-5}$$

The corresponding space vector, denoted as $\vec{V}_1$, can be obtained by substituting (6.3-5) into (6.3-4):

$$\vec{V}_1 = \frac{2}{3}\, V_d e^{j0} \tag{6.3-6}$$

Following the same procedure, all six active vectors can be derived

$$\vec{V}_k = \frac{2}{3}\, V_d e^{j(k-1)\frac{\pi}{3}}, \qquad k = 1, 2, \ldots, 6 \tag{6.3-7}$$

The zero vector $\vec{V}_0$ has two switching states [PPP] and [OOO], one of which seems redundant. As will be seen later, the **redundant switching state** can be utilized to minimize the switching frequency of the inverter or perform other useful functions. The relationship between the space vectors and their corresponding switching states is given in Table 6.3-2.

Note that the zero and active vectors do not move in space, and thus they are referred to as **stationary vectors**. On the contrary, the **reference vector** $\vec{V}_{ref}$ in Fig. 6.3-1 rotates in space at an angular velocity

$$\omega = 2\pi f_1 \tag{6.3-8}$$

where f_1 is the fundamental frequency of the inverter output voltage. The angular displacement between $\vec{V}_{ref}$ and the α-axis of the α–β plane can be obtained by

$$\theta(t) = \int_0^t \omega(t)dt + \theta(0) \tag{6.3-9}$$

For a given magnitude (length) and position, $\vec{V}_{ref}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\vec{V}_{ref}$ passes through sectors one by one, different sets of switches will be turned on or off. As a result, when $\vec{V}_{ref}$ rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of $\vec{V}_{ref}$, while its output voltage can be adjusted by the magnitude of $\vec{V}_{ref}$.

6.3.3 Dwell Time Calculation

As mentioned earlier, the reference $\vec{V}_{ref}$ can be synthesized by three stationary vectors. The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a **sampling period** T_s of the modulation scheme. The dwell time calculation is based on '**volt-second balancing**' principle, that is, the product of the reference voltage $\vec{V}_{ref}$ and sampling period T_s equals the sum of the voltage multiplied by the time interval of chosen space vectors.

Assuming that the sampling period T_s is sufficiently small, the reference vector $\vec{V}_{ref}$ can be considered constant during T_s. Under this assumption, $\vec{V}_{ref}$ can be approximated by two adjacent active vectors and one zero vector. For example, when $\vec{V}_{ref}$

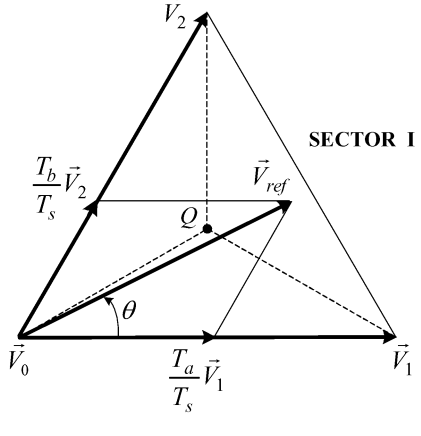


Figure 6.3-2 $\vec{V}_{ref}$ synthesized by $\vec{V}_1, \vec{V}_2$ and $\vec{V}_0$.

falls into sector I as shown in Fig. 6.3-2, it can be synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$. The volt-second balancing equation is

$$\begin{aligned} \vec{V}_{ref}T_s &= \vec{V}_1T_a + \vec{V}_2T_b + \vec{V}_0T_0 \\ T_s &= T_a + T_b + T_0 \end{aligned} \tag{6.3-10}$$

where T_a, T_b, and T_0 are the **dwell times** for the vectors $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_0$, respectively. The space vectors in (6.3-10) can be expressed as

$$\vec{V}_{ref} = \vec{V}_{ref}e^{j\theta}, \qquad \vec{V}_1 = \frac{2}{3}V_d, \qquad \vec{V}_2 = \frac{2}{3}V_d e^{j\frac{\pi}{3}}, \qquad \text{and} \qquad \vec{V}_0 = 0 \tag{6.3-11}$$

Substituting (6.3-11) into (6.3-10) and then splitting the resultant equation into the real (β-axis) and imaginary (β-axis) components in the α–β plane, we have

$$\begin{aligned} &\text{Re:} \quad V_{ref}(\cos\theta)T_s = \frac{2}{3}V_dT_a + \frac{1}{3}V_dT_b \\ &\text{Im:} \quad V_{ref}(\sin\theta)T_s = \frac{1}{\sqrt{3}}V_dT_b \end{aligned} \tag{6.3-12}$$

Solving (6.3-12) together with $T_s = T_a + T_b + T_0$ yields

$$\begin{aligned} T_a &= \frac{\sqrt{3}T_s\,V_{ref}}{V_d}\sin\left(\frac{\pi}{3} - \theta\right) \\ T_b &= \frac{\sqrt{3}T_s\,V_{ref}}{V_d}\sin\theta \qquad\qquad \text{for } 0 \le \theta < \pi/3 \\ T_0 &= T_s - T_a - T_b \end{aligned} \tag{6.3-13}$$

To visualize the relationship between the location of $\vec{V}_{ref}$ and the dwell times, let us examine some special cases. If $\vec{V}_{ref}$ lies exactly in the middle between $\vec{V}_1$ and $\vec{V}_2$ (i.e., $\theta = \pi/6$), the dwell time T_a for $\vec{V}_1$ will be equal to T_b for $\vec{V}_2$. When $\vec{V}_{ref}$ is closer to $\vec{V}_2$ than $\vec{V}_1$, T_b will be greater than T_a. If $\vec{V}_{ref}$ is coincident with $\vec{V}_2$, T_a will be zero. With the head of $\vec{V}_{ref}$ located right on the central point Q in figure 6.3-2, $T_a = T_b = T_0$. The relationship between the $\vec{V}_{ref}$ location and dwell times is summarized in Table 6.3-3.

Note that although Eq. (6.3-13) is derived when $\vec{V}_{ref}$ is in sector I, it can also be used when $\vec{V}_{ref}$ is in other sectors provided that a multiple of $\pi/3$ is subtracted from the actual angular displacement θ such that the modified angle θ' falls into the range between zero and $\pi/3$ for use in the equation, that is,

$$\theta' = \theta - (k-1)\pi/3 \qquad \text{for } 0 \le \theta' < \pi/3 \tag{6.3-14}$$

where $k = 1, 2, \ldots, 6$ for sectors I, II, . . . , VI, respectively. For example, when $\vec{V}_{ref}$ is in sector II, the calculated dwell times T_a, T_b, and T_0 based on (6.3-13) and (6.3-14) are for vectors $\vec{V}_2$, $\vec{V}_3$, and $\vec{V}_0$, respectively.

Table 6.3-3 $\vec{V}_{ref}$ Location and Dwell Times

$\vec{V}_{ref}$ **Location:**	$\theta = 0$	$0 < \theta < \frac{\pi}{6}$	$\theta = \frac{\pi}{6}$	$\frac{\pi}{6} < \theta < \frac{\pi}{3}$	$\theta = \frac{\pi}{3}$
Dwell Times:	$T_a > 0$ $T_b = 0$	$T_a > T_b$	$T_a = T_b$	$T_a < T_b$	$T_a = 0$ $T_b > 0$

6.3.4 Modulation Index

Equation (6.3-13) can be also expressed in terms of **modulation index** m_a

$$\begin{aligned} T_a &= T_s m_a \sin\left(\frac{\pi}{3} - \theta\right) \\ T_b &= T_s m_a \sin\theta \\ T_0 &= T_s - T_a - T_b \end{aligned} \tag{6.3-15}$$

where

$$m_a = \frac{\sqrt{3} V_{ref}}{V_d} \tag{6.3-16}$$

The maximum magnitude of the reference vector, $V_{ref,\max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon shown in Fig. 6.3-1. Since the hexagon is formed by six active vectors having a length of $2V_d/3$, $V_{ref,\max}$ can be found from

$$V_{ref,\max} = \frac{2}{3} V_d \times \frac{\sqrt{3}}{2} = \frac{V_d}{\sqrt{3}} \tag{6.3-17}$$

Substituting (6.3-17) into (6.3-16) gives the maximum modulation index:

$$m_{a,\max} = 1$$

from which the modulation index for the SVM scheme is in the range of

$$0 \le m_a \le 1 \tag{6.3-18}$$

The maximum fundamental line-to-line voltage (rms) produced by the SVM scheme can be calculated by

$$V_{\max,SVM} = \sqrt{3}\,(V_{ref,\max}/\sqrt{2}) = 0.707 V_d \tag{6.3-19}$$

where $V_{ref,\max}/\sqrt{2}$ is the maximum rms value of the fundamental phase voltage of the inverter.

With the inverter controlled by the SPWM scheme, the maximum fundamental line-to-line voltage is

$$V_{\max,SPWM} = 0.612 V_d \tag{6.3-20}$$

from which

$$\frac{V_{\max,SVM}}{V_{\max,SPWM}} = 1.155 \tag{6.3-21}$$

Equation (6.3-21) indicates that for a given dc bus voltage the maximum inverter line-to-line voltage generated by the SVM scheme is 15.5% higher than that by the SPWM scheme. However, the use of third harmonic injection SPWM scheme can also boost the inverter output voltage by 15.5%. Therefore, the two schemes have essentially the same **dc bus voltage utilization**.

6.3.5 Switching Sequence

With the space vectors selected and their dwell times calculated, the next step is to arrange switching sequence. In general, the switching sequence design for a given $\vec{V}_{ref}$ is not unique, but it should satisfy the following two requirements for the minimization of the device switching frequency:

(a) The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off.
(b) The transition for $\vec{V}_{ref}$ moving from one sector in the space vector diagram to the next requires no or minimum number of switchings.

Figure 6.3-3 shows a typical **seven-segment** switching sequence and inverter output voltage waveforms for $\vec{V}_{ref}$ in sector I, where $\vec{V}_{ref}$ is synthesized by $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_0$. The sampling period T_s is divided into seven segments for the selected vectors. The following can be observed:

- The dwell times for the seven segments add up to the sampling period ($T_s = T_a + T_b + T_0$).
- Design requirement (a) is satisfied. For instance, the transition from [OOO] to [POO] is accomplished by turning S_1 on and S_4 off, which involves only two switches.
- The redundant switching sates for $\vec{V}_0$ are utilized to reduce the number of switchings per sampling period. For the $T_0/4$ segment in the center of the sampling period, the switching state [PPP] is selected, whereas for the $T_0/4$ segments on both sides, the state [OOO] is used.
- Each of the switches in the inverter turns on and off once per sampling period. The **switching frequency** f_{sw} of the devices is thus equal to the **sampling frequency** f_{sp}, that is, $f_{sw} = f_{sp} = 1/T_s$.

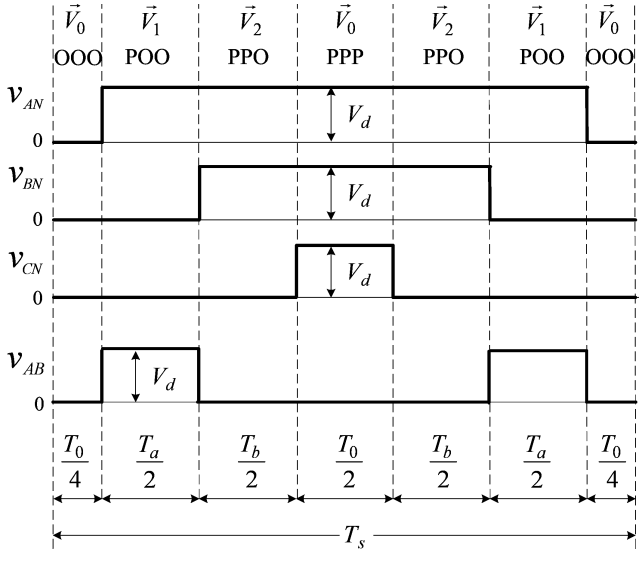


Figure 6.3-3 Seven-segment switching sequence for $\vec{V}_{ref}$ in sector I.

Let us now examine a case given in Fig. 6.3-4, where the vectors $\vec{V}_1$ and $\vec{V}_2$ in Fig. 6.3-3 are swapped. Some switching state transitions, such as the transition from [OOO] to [PPO], are accomplished by turning on and off four switches in two inverter legs simultaneously. As a consequence, the total number of switchings during the sampling period increases from six in the previous case to ten. Obviously, this switching sequence does not satisfy the design requirement and thus should not be adopted.

It is interesting to note that the waveforms of v_{AB} in Figs. 6.3-3 and 6.3-4 produced by two different switching sequences seem different, but they are essentially the same. If these two waveforms are drawn for two or more consecutive sampling periods, we will notice that they are identical except for a small time delay (T_s/2). Since T_s is much shorter than the period of the inverter fundamental frequency, the effect caused by the time delay is negligible.

Table 6.3-4 gives the seven-segment switching sequences for $\vec{V}_{ref}$ residing in all six sectors. Note that all the switching sequences start and end with switching state [OOO], which indicates that the transition for $\vec{V}_{ref}$ moving from one sector to the next does not require any switchings. The switching sequence design requirement (b) is satisfied.

6.3.6 Spectrum Analysis

The simulated waveforms for the inverter output voltages and load current are shown in Fig. 6.3-5. The inverter operates under the condition of f_1 = 60 Hz, T_s = 1/720 s, f_{sw} = 720 Hz, and m_a = 0.8 with a rated three-phase inductive load. The load power factor is 0.9 per phase. It can be observed that the waveform of the in-

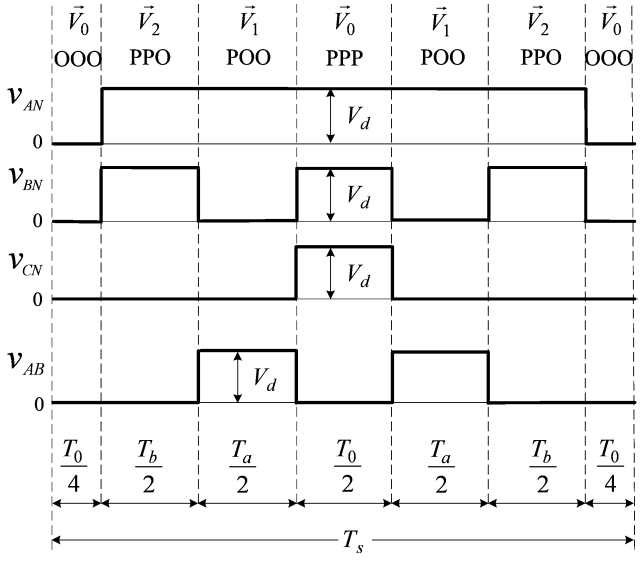


Figure 6.3-4 Undesirable seven-segment switching sequence.

verter line-to-line voltage v_{AB} is not **half-wave symmetrical**, that is, to $v_{AB}(\omega t) \neq -v_{AB}(\omega t + \pi)$. Therefore, it contains even-order harmonics, such as 2nd, 4th, 8th, and 10th, in addition to odd-order harmonics. The THD of v_{AB} and i_A is 80.2% and 8.37%, respectively.

Figure 6.3-6 shows waveforms measured from a laboratory two-level inverter operating under the same conditions as those given in Fig. 6.3-5. The top and bottom traces in Fig. 6.3-6a are the inverter line-to-line voltage v_{AB} and load phase

Table 6.3-4 Seven-Segment Switching Sequence

	Switching Segment						
Sector	1	2	3	4	5	6	7
I	$\vec{V}_0$ OOO	$\vec{V}_1$ POO	$\vec{V}_2$ PPO	$\vec{V}_0$ PPP	$\vec{V}_2$ PPO	$\vec{V}_1$ POO	$\vec{V}_0$ OOO
II	$\vec{V}_0$ OOO	$\vec{V}_3$ OPO	$\vec{V}_2$ PPO	$\vec{V}_0$ PPP	$\vec{V}_2$ PPO	$\vec{V}_3$ OPO	$\vec{V}_0$ OOO
III	$\vec{V}_0$ OOO	$\vec{V}_3$ OPO	$\vec{V}_4$ OPP	$\vec{V}_0$ PPP	$\vec{V}_4$ OPP	$\vec{V}_3$ OPO	$\vec{V}_0$ OOO
IV	$\vec{V}_0$ OOO	$\vec{V}_5$ OOP	$\vec{V}_4$ OPP	$\vec{V}_0$ PPP	$\vec{V}_4$ OPP	$\vec{V}_5$ OOP	$\vec{V}_0$ OOO
V	$\vec{V}_0$ OOO	$\vec{V}_5$ OOP	$\vec{V}_6$ POP	$\vec{V}_0$ PPP	$\vec{V}_6$ POP	$\vec{V}_5$ OOP	$\vec{V}_0$ OOO
VI	$\vec{V}_0$ OOO	$\vec{V}_1$ POO	$\vec{V}_6$ POP	$\vec{V}_0$ PPP	$\vec{V}_6$ POP	$\vec{V}_1$ POO	$\vec{V}_0$ OOO

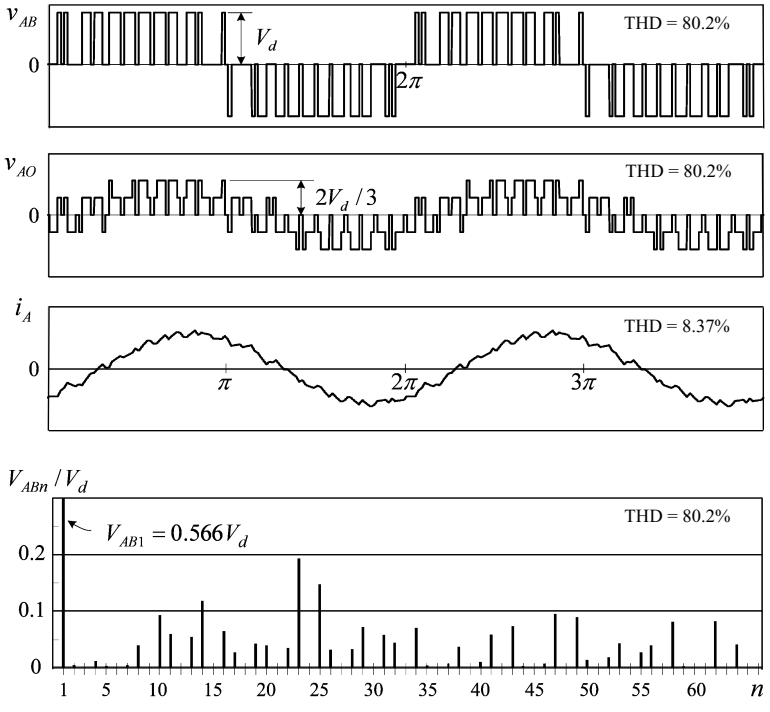
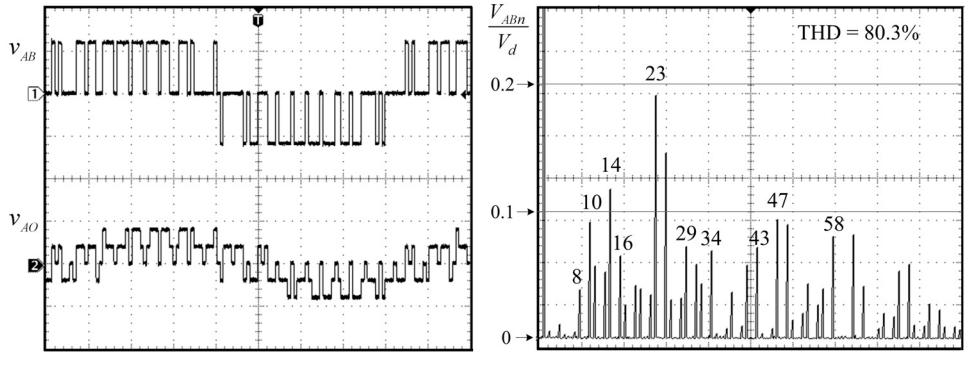


Figure 6.3-5 Inverter output waveforms produced by SVM scheme with f_1 = 60 Hz, f_{sw} = 720 Hz, and m_a = 0.8.



(a) Waveforms 2 ms/div (b) Spectrum (500 Hz/div)

Figure 6.3-6 Measured inverter voltage waveforms and harmonic spectrum for the verification of simulated waveforms in Fig. 6.3-5.

voltage v_{AO}, and the spectrum of v_{AB} is given in Fig. 6.3-6b. The experimental results match with the simulation very well.

Figure 6.3-7 shows the harmonic content of v_{AB} for the inverter operating at f_1 = 60 Hz and f_{sw} = 720 Hz. Although the low-order harmonics, such as 2nd, 4th, 5th, and 7th, are not eliminated, they have very low magnitudes. The maximum fundamental line-to-line voltage (rms) occurs at $m_a = 1$ and can be found from

$$V_{AB1,\max} = 0.707 V_d \qquad \text{for } m_a = 1 \tag{6.3-22}$$

which is around 15.5% higher than that given in (6.2-3) for the SPWM scheme without using the third harmonic injection technique.

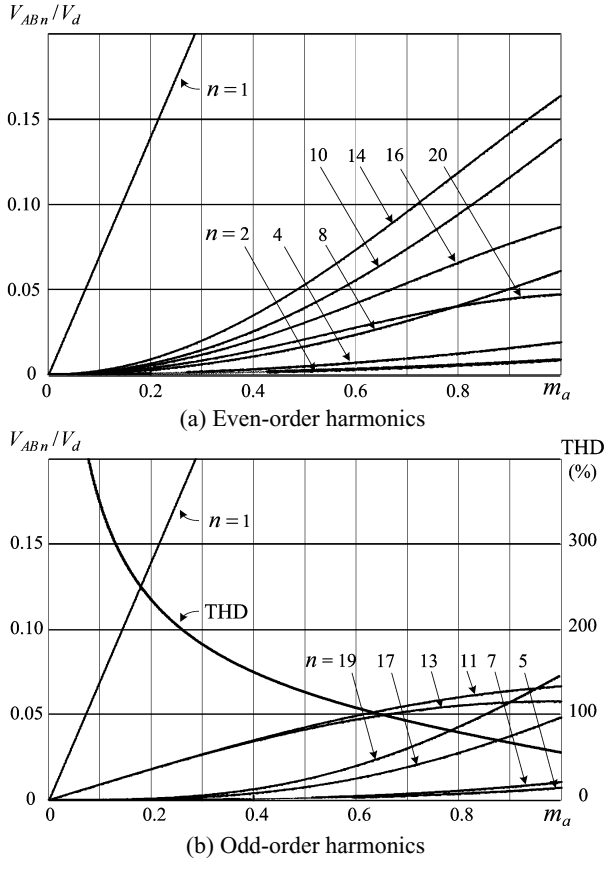
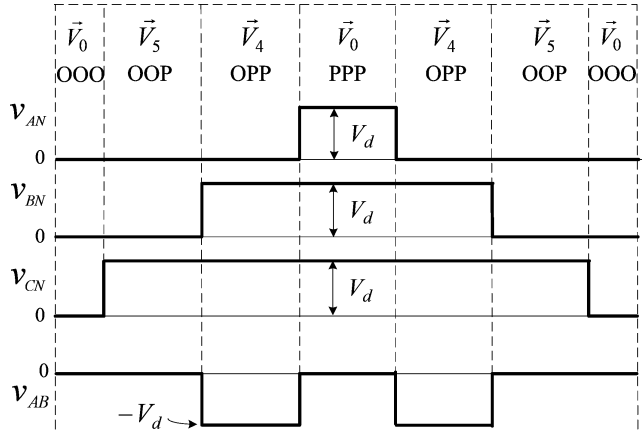


Figure 6.3-7 Harmonic content of v_{AB} with f_1 = 60 Hz and f_{sw} = 720 Hz.

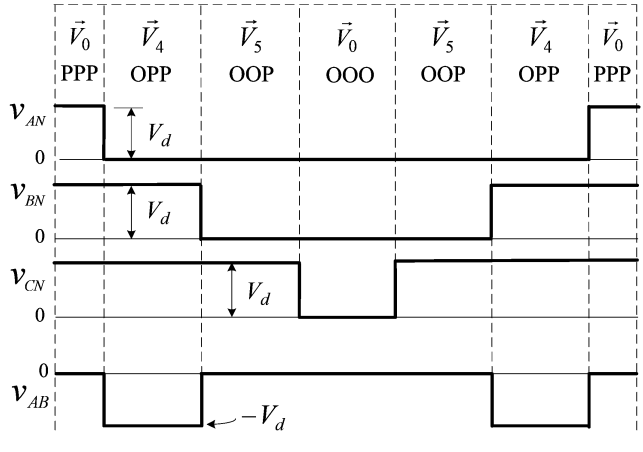
6.3.7 Even-Order Harmonic Elimination

As indicated earlier, the line-to-line voltage waveform produced by the SVM inverter contains even-order harmonics. In the inverter-fed medium-voltage drives, these harmonics may not have a significant impact on the operation of the motor. However, when the two-level converter is used as a rectifier, its line current THD should comply with harmonic standards such as IEEE 519-1992. Since most standards have more stringent requirements on even-order harmonics than on odd-order ones, this section presents a modified SVM scheme with even-order harmonic elimination.

To investigate the mechanism of even-order harmonic generation, consider a case where the reference vector $\vec{V}_{ref}$ falls into sector IV. Based on the switching se-



(a) Type-A sequence (starts and ends with [OOO])



(b) Type-B sequence (starts and ends with [PPP])

Figure 6.3-8 Two valid switching sequences for $\vec{V}_{ref}$ in sector IV.

quence given in Table 6.3-4, the waveform of inverter line-to-line voltage v_{AB} in a sampling period is illustrated in Fig. 6.3-8a. The waveform does not have a mirror image (not symmetrical about the horizontal axis) in comparison with that in Fig. 6.3-3, where $\vec{V}_{ref}$ is in a sector 180° apart from sector IV. This implies that the waveform generated by the SVM scheme is not half-wave symmetrical, leading to the generation of even-order harmonics.

Let's now consider type-B switching sequence shown in Fig. 6.3-8b, which is also a valid switching sequence that satisfies the design requirement (a) stated earlier. By comparing the waveform of v_{AB} with that in Fig. 6.3-3, it is clear that the use of this switching sequence would lead to $v_{AB}(\omega t) = -v_{AB}(\omega t + \pi)$. As a result, the waveform of v_{AB} would not contain any ever-order harmonics.

Examining the two switching sequences in Fig. 6.3-8, we can find out that the type-A sequence starts and ends with [OOO] while the type-B sequence commences and finishes with [PPP]. The waveforms of v_{AB} generated by both sequences seem different. However, they are essentially the same except for a small time delay ($T_s/2$), which can be clearly observed if these two waveforms are drawn for two or more consecutive sampling periods.

To make the three-phase line-to-line voltage half-wave symmetrical, type-A and type-B switching sequences can be alternatively used. In addition, each sector in the space vector diagram is divided into two regions as shown in Fig. 6.3-9. Type-A sequence is used in the nonshaded regions, while type-B sequence is employed in the shaded regions. The detailed switching sequence arrangements are given in Table 6.3-5.

It can be observed from the table that the transition for $\vec{V}_{ref}$ moving from region a to b causes additional switchings. This implies that the even-order harmonic elimination is achieved at the expense of an increase in switching frequency. The amount of switching frequency increase can be determined by

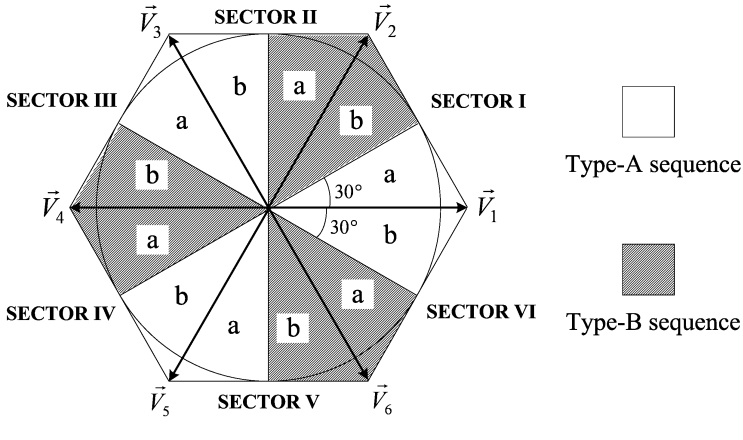


Figure 6.3-9 Alternative use of two switching sequences for even-order harmonic elimination.

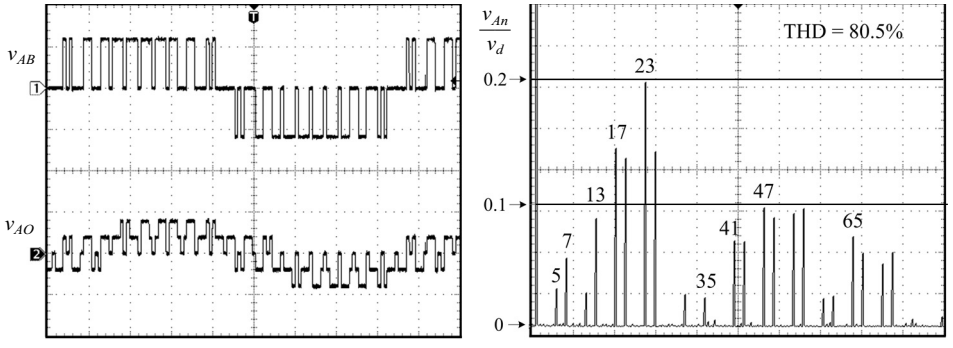
Table 6.3-5 Switching Sequence of the Modified SVM for Even-Order Harmonic Elimination

Sector	Switching Sequence						
I-a	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_2$	$\vec{V}_0$	$\vec{V}_2$	$\vec{V}_1$	$\vec{V}_0$
	OOO	POO	PPO	PPP	PPO	POO	OOO
I-b	$\vec{V}_0$	$\vec{V}_2$	$\vec{V}_1$	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_2$	$\vec{V}_0$
	PPP	PPO	POO	OOO	POO	PPO	PPP
II-a	$\vec{V}_0$	$\vec{V}_2$	$\vec{V}_3$	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_2$	$\vec{V}_0$
	PPP	PPO	OPO	OOO	OPO	PPO	PPP
II-b	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_2$	$\vec{V}_0$	$\vec{V}_2$	$\vec{V}_3$	$\vec{V}_0$
	OOO	OPO	PPO	PPP	PPO	OPO	OOO
III-a	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_4$	$\vec{V}_0$	$\vec{V}_4$	$\vec{V}_3$	$\vec{V}_0$
	OOO	OPO	OPP	PPP	OPP	OPO	OOO
III-b	$\vec{V}_0$	$\vec{V}_4$	$\vec{V}_3$	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_4$	$\vec{V}_0$
	PPP	OPP	OPO	OOO	OPO	OPP	PPP
IV-a	$\vec{V}_0$	$\vec{V}_4$	$\vec{V}_5$	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_4$	$\vec{V}_0$
	PPP	OPP	OOP	OOO	OOP	OPP	PPP
IV-b	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_4$	$\vec{V}_0$	$\vec{V}_4$	$\vec{V}_5$	$\vec{V}_0$
	OOO	OOP	OPP	PPP	OPP	OOP	OOO
V-a	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_6$	$\vec{V}_0$	$\vec{V}_6$	$\vec{V}_5$	$\vec{V}_0$
	OOO	OOP	POP	PPP	POP	OOP	OOO
V-b	$\vec{V}_0$	$\vec{V}_6$	$\vec{V}_5$	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_6$	$\vec{V}_0$
	PPP	POP	OOP	OOO	OOP	POP	PPP
VI-a	$\vec{V}_0$	$\vec{V}_6$	$\vec{V}_1$	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_6$	$\vec{V}_0$
	PPP	POP	POO	OOO	POO	POP	PPP
VI-b	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_6$	$\vec{V}_0$	$\vec{V}_6$	$\vec{V}_1$	$\vec{V}_0$
	OOO	POO	POP	PPP	POP	POO	OOO

$$\Delta f_{sw} = 3f_1 \tag{6.3-23}$$

where f_1 is the fundamental frequency of the inverter output voltage.

The inverter output waveforms measured from a laboratory two-level inverter with modified SVM scheme are shown in Fig. 6.3-10. The inverter operates under the condition of f_1 = 60 Hz, T_s = 1/720 s, and m_a = 0.8. The waveforms of the inverter line-to-line voltage v_{AB} and load phase voltage v_{AO} are of half-wave symme-



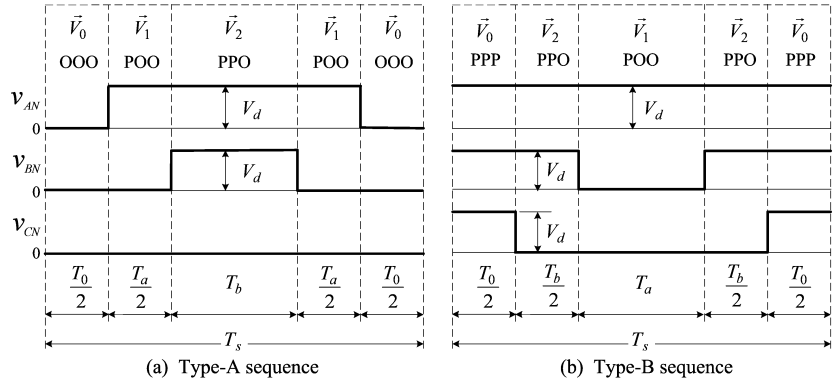
(a) Waveforms 2 ms/div (b) Spectrum (500 Hz/div)

Figure 6.3-10 Measured waveforms produced by the modified SVM with even-order harmonic elimination (f_1 = 60 Hz, T_s = 1/720 s, and m_a = 0.8).

try, containing no even-order harmonics. Compared with the harmonic spectrum given in Fig. 6.3-6, the magnitude of the 5th and 7th harmonics in v_{AB} is increased while the THD essentially remains the same (refer to Appendix at the end of the book for details).

6.3.8 Discontinuous Space Vector Modulation

As pointed out earlier, the switching sequence design is not unique for a given set of stationary vectors and dwell times. Figure 6.3-11 shows two **five-segment** switching sequences and generated inverter terminal voltages for $\vec{V}_{ref}$ in sector I. For type-A sequence, the zero switching sate [OOO] is assigned for $\vec{V}_0$ while type-B sequence utilizes [PPP] for $\vec{V}_0$.



(a) Type-A sequence (b) Type-B sequence

Figure 6.3-11 Five-segment switching sequence.

In the five-segment sequence, one of the three inverter output terminals is clamped to either the positive or negative dc bus without any switchings during the sampling period T_s. Furthermore, the switching sequence can be arranged such that the switching in an inverter leg is continuously suppressed for a period of $2\pi/3$ per cycle of the fundamental frequency. For instance, the inverter terminal voltage v_{CN} can be clamped to the negative dc bus continuously in sectors I and II as shown in Table 6.3-6. Due to the switching discontinuity, the five-segment scheme is also known as **discontinuous space vector modulation** [4].

The use of type-A sequence alone will make the conduction angle of the lower switch in an inverter leg longer than that of the upper switch, causing unbalanced power and thermal distributions. The problem can be mitigated by swapping the two types of the switching sequences periodically. The switching frequency of the inverter will increase accordingly.

Figure 6.3-12 shows the simulated waveforms for v_{AB} and i_A when the inverter operates at f_1 = 60 Hz, f_{sw} = 600 Hz, T_s = 1/900 s, and m_a = 0.8 with a rated three-phase inductive load. The load power factor is 0.9 per phase. Since the gate signals for S_1, S_3 and S_5 are suppressed continuously for a period of $2\pi/3$ per cycle of the fundamental frequency, the switching frequency of the five-segment sequence is reduced by 1/3 compared with the seven-segment sequence with the same sampling period. The waveform of v_{AB} is not half-wave symmetrical, containing large amount of even-order harmonics. The THDs of v_{AB} and i_A are 91.8% and 12.1%, respectively, which are higher than those in the seven-segment sequence. This is mainly caused by the reduction of switching frequencies.

Table 6.3-6 Five-Segment Switching Sequence

Sector	Switching Sequence (Type A)					
I	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_2$	$\vec{V}_1$	$\vec{V}_0$	$v_{CN} = 0$
	OOO	POO	PPO	POO	OOO	
II	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_2$	$\vec{V}_3$	$\vec{V}_0$	$v_{CN} = 0$
	OOO	OPO	PPO	OPO	OOO	
III	$\vec{V}_0$	$\vec{V}_3$	$\vec{V}_4$	$\vec{V}_3$	$\vec{V}_0$	$v_{AN} = 0$
	OOO	OPO	OPP	OPO	OOO	
IV	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_4$	$\vec{V}_5$	$\vec{V}_0$	$v_{AN} = 0$
	OOO	OOP	OPP	OOP	OOO	
V	$\vec{V}_0$	$\vec{V}_5$	$\vec{V}_6$	$\vec{V}_5$	$\vec{V}_0$	$v_{BN} = 0$
	OOO	OOP	POP	OOP	OOO	
VI	$\vec{V}_0$	$\vec{V}_1$	$\vec{V}_6$	$\vec{V}_1$	$\vec{V}_0$	$v_{BN} = 0$
	OOO	POO	POP	POO	OOO	

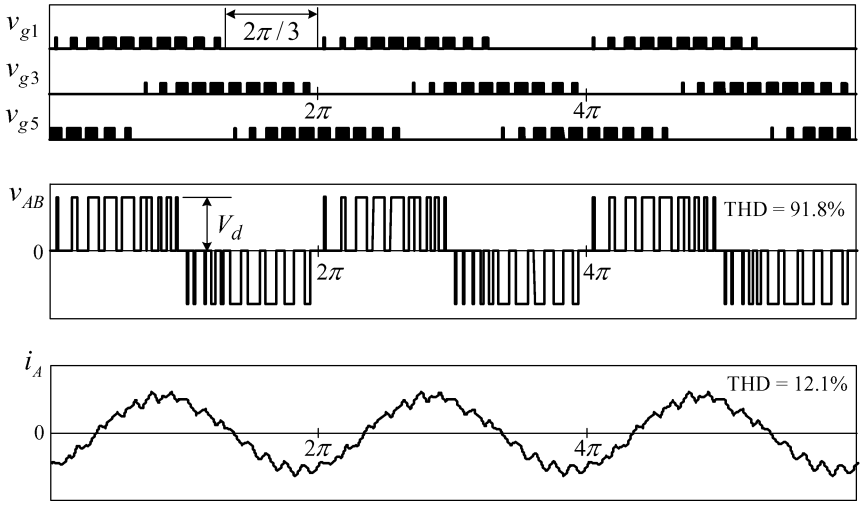


Figure 6.3-12 Waveforms produced by five-segment SVM with $f_1 = 60$ Hz, $f_{sw} = 600$ Hz, $T_s = 1/900$ s and $m_a = 0.8$.

6.4 SUMMARY

This chapter focuses on pulse-width modulation schemes for the two-level voltage source inverter. The switching frequency of the inverter is usually limited to a few hundred hertz for high-power medium-voltage (MV) drives. A carrier-based sinusoidal pulse-width modulation (SPWM) scheme is reviewed, followed by a detailed analysis on space vector modulation (SVM) algorithms, including derivation of space vectors, calculation of dwell times, design of switching sequence, and analysis of harmonic spectrum and THD.

The SVM schemes usually generate both odd- and even-order harmonics in the inverter output voltages. The even-order harmonics may not have a significantly impact on the operation of the motor. However, they are strictly regulated by harmonic guidelines such as IEEE Standard 519-1992 when the two-level converter is used as a rectifier in the MV drive. Since the two-level voltage source rectifier is not separately discussed in the book, the mechanism of even-order harmonic generation is analyzed and a modified SVM scheme for even-order harmonic eliminations presented.

The two-level inverter has a number of features, including simple converter topology and PWM scheme. However, the inverter produces high dv/dt and THD in its output voltage, and therefore often requires a large-size LC filter installed at its output terminals. Other advantages and drawbacks of the two-level inverter for use in the MV drive will be elaborated in Chapter 12.

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