MOSFET

OptiMOS^{TM} Power-MOSFET, 30 V

Features

- Optimized for high performance SMPS
- Integrated monolithic Schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
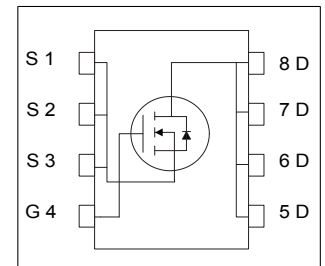- Halogen-free according to IEC61249-2-21

SuperSO8

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	1.1	mΩ
I_D	100	A
Q_{OSS}	45	nC
Q_G(0V..10V)	68	nC

S 1		8 D
S 2		7 D
S 3		6 D
G 4		5 D

Type / Ordering Code	Package	Marking	Related Links
BSC011N03LSI	PG-TDSON-8	011N03LI	-

[1] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - - -	- - - - -	100 100 100 100 37	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	400	A	T_C=25 °C
Avalanche current, single pulse[3]	I_{AS}	-	-	50	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	100	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	96 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[1]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.3	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[1]	R_{thJA}	-	-	50	K/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=10 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	I_D=10 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- 3	0.5 -	mA	V_{DS}=24 V, V_{GS}=0 V, T_j=25 °C V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.2 0.9	1.5 1.1	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	0.3	0.6	1.2	Ω	-
Transconductance	g_{fs}	80	160	-	S	$\lvert V_{DS}\rvert$>2$\lvert I_D\rvert R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	4300	5719	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	1600	2128	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	220	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	9.2	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	35	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	6.2	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

[1] Defined by design. Not subject to production test

Table 6 Gate charge characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[2]	Q_{gs}	-	10.1	13.4	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	6.8	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge[2]	Q_{gd}	-	10.6	14	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	13.9	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	34	45	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	68	90	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	27	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[2]	Q_{oss}	-	45	60	nC	V_{DD}=15 V, V_{GS}=0 V

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	96	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	400	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.56	0.7	V	V_{GS}=0 V, I_F=12 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	5	-	nC	V_R=15 V, I_F=12 A, di_F/dt=400 A/µs

[1] See ″Gate charge waveforms″ for parameter definition
[2] Defined by design. Not subject to production test
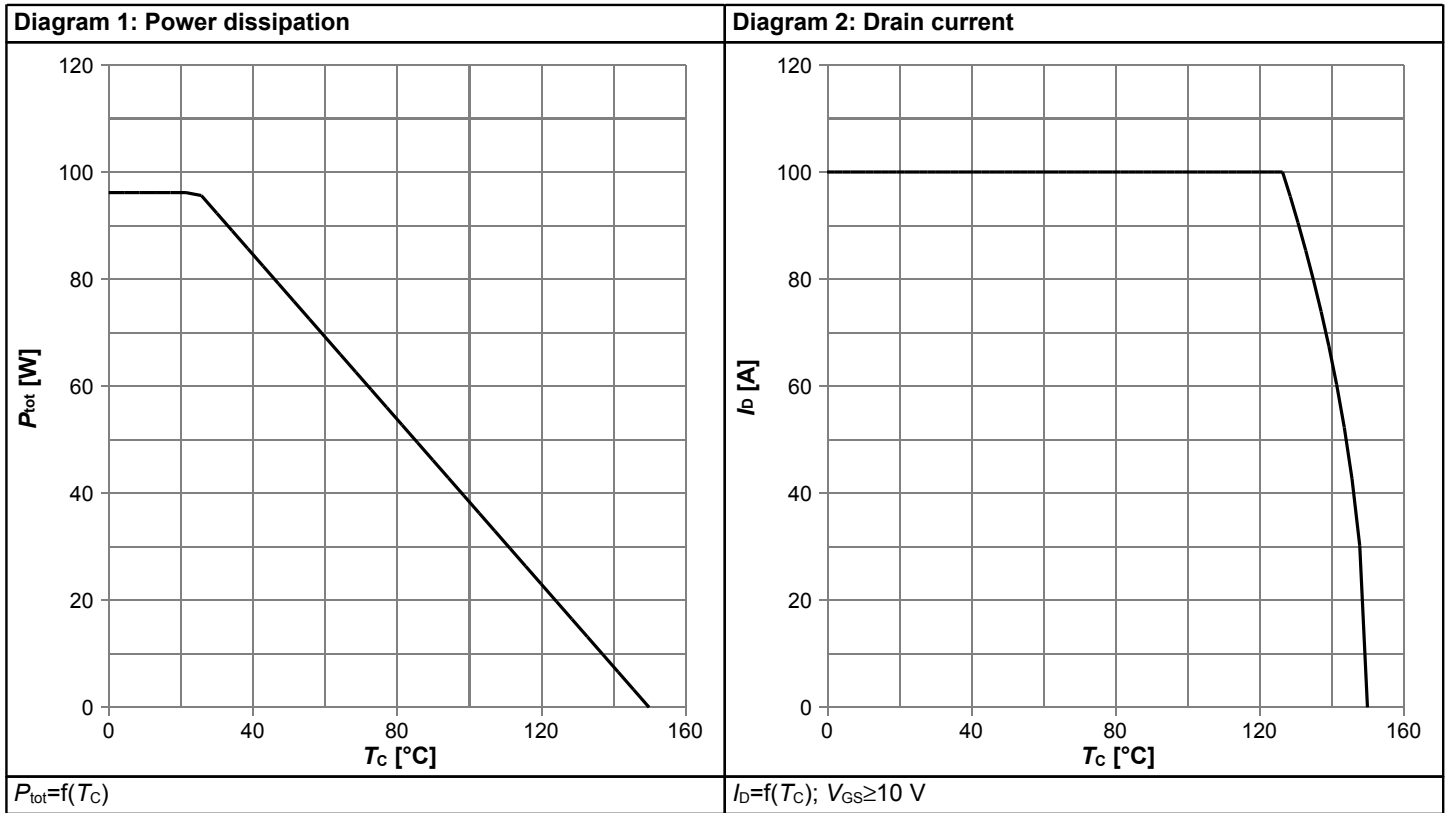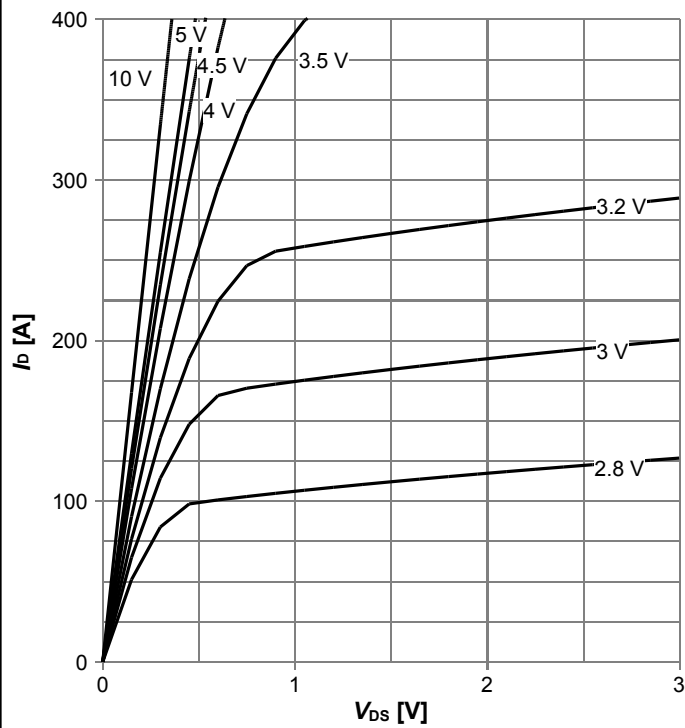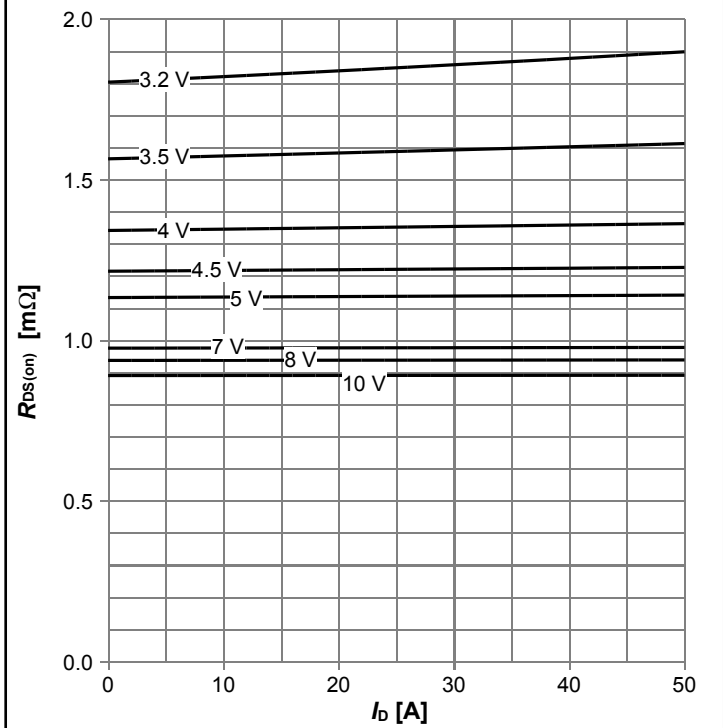
4 Electrical characteristics diagrams

Diagram 1: Power dissipation	Diagram 2: Drain current

P_{tot}=f(T_C)

I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Z_{thJC}=f(t_p); parameter: D=t_p/T
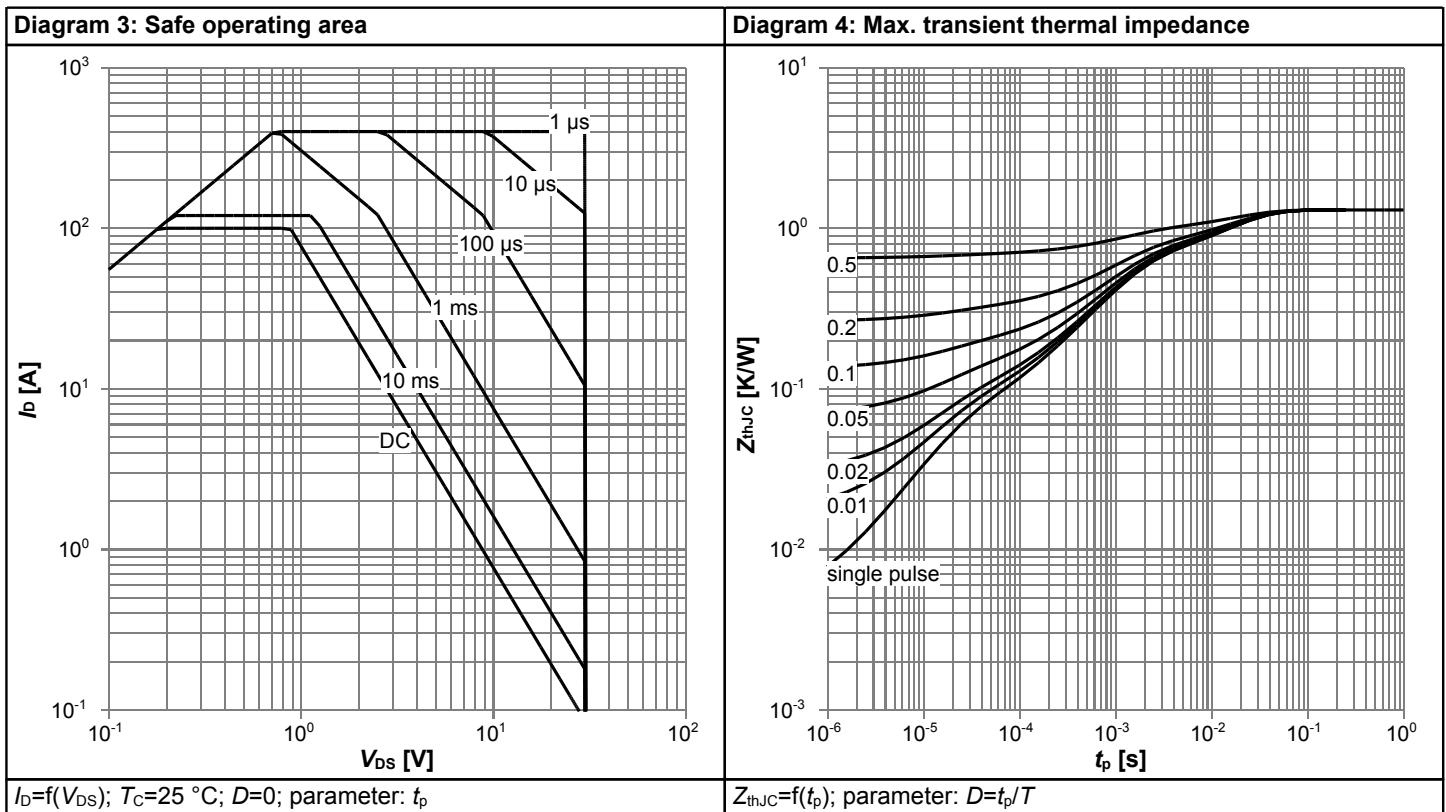
Diagram 5: Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
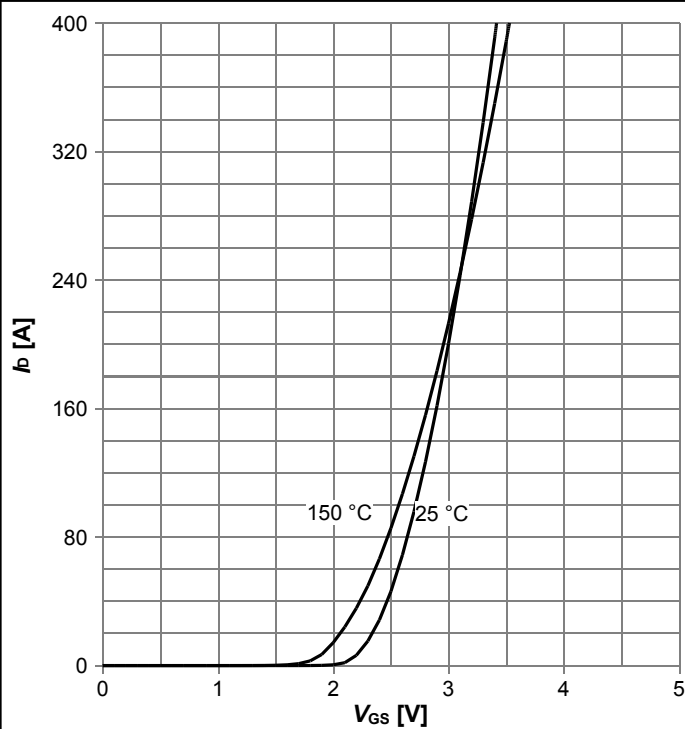
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance
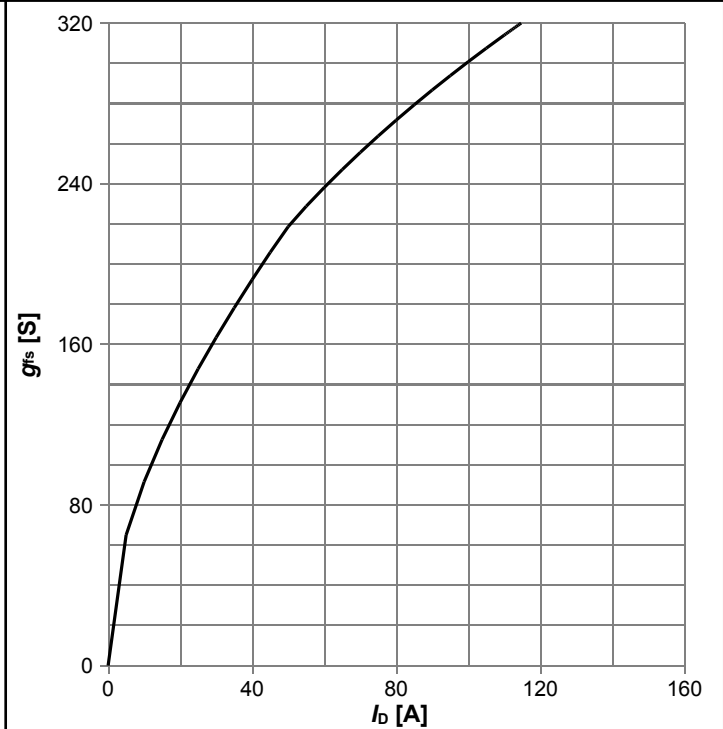
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance
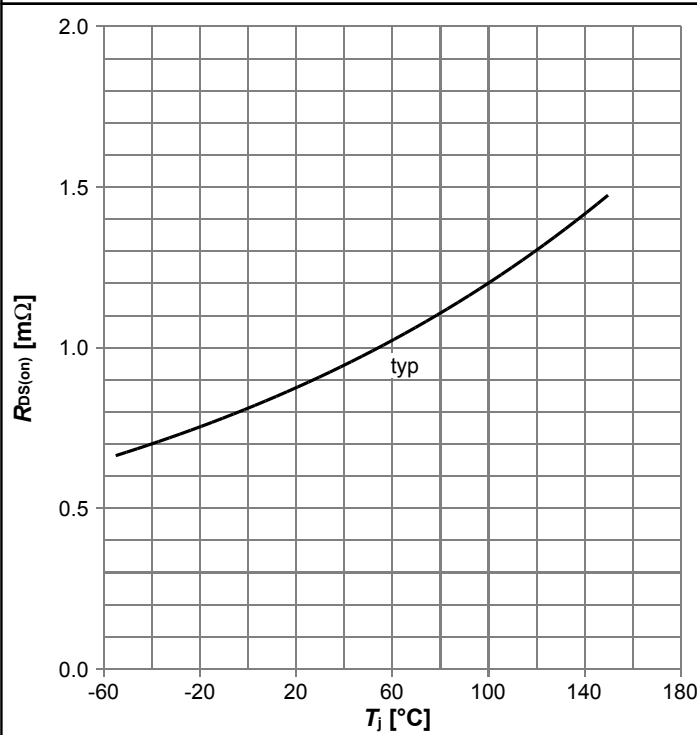
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
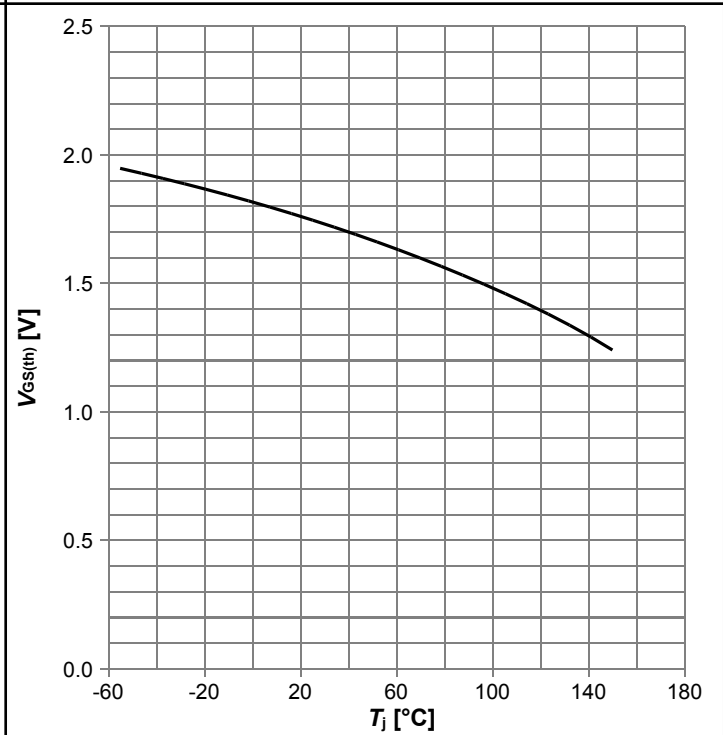
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=10 mA

Diagram 11: Typ. capacitances
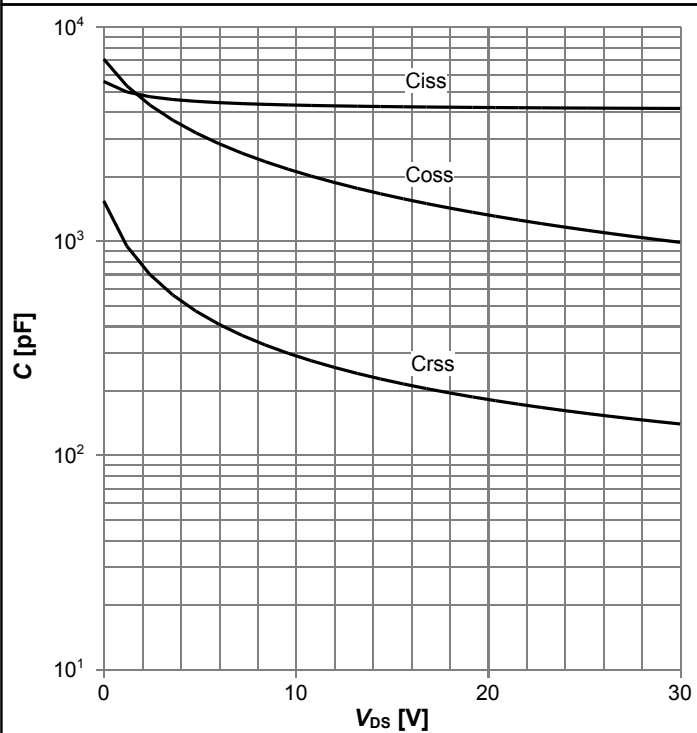
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
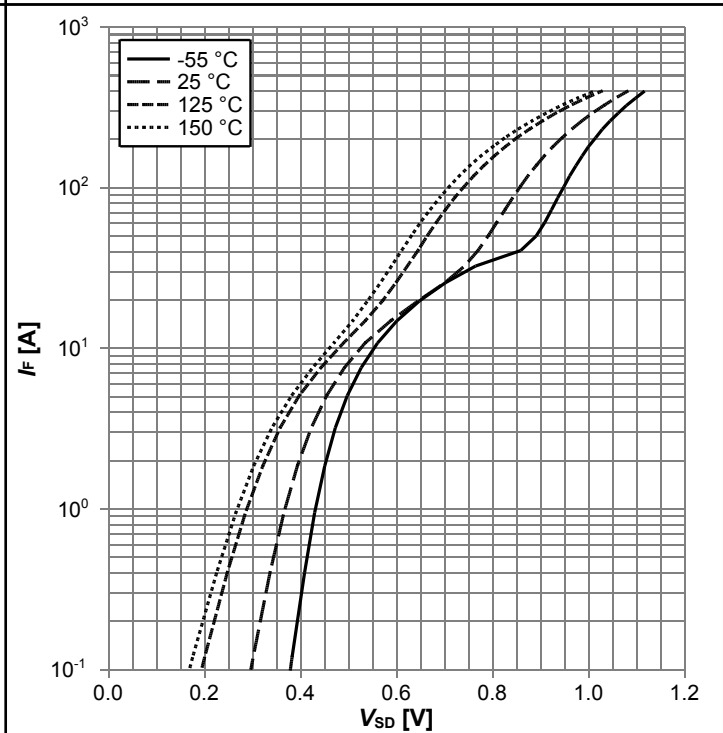
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics

Plot of I_{AV} [A] (y-axis, logarithmic from 10^0 to 10^2) versus t_{AV} [µs] (x-axis, logarithmic from 10^0 to 10^3), with curves labeled 25 °C, 100 °C, and 125 °C.
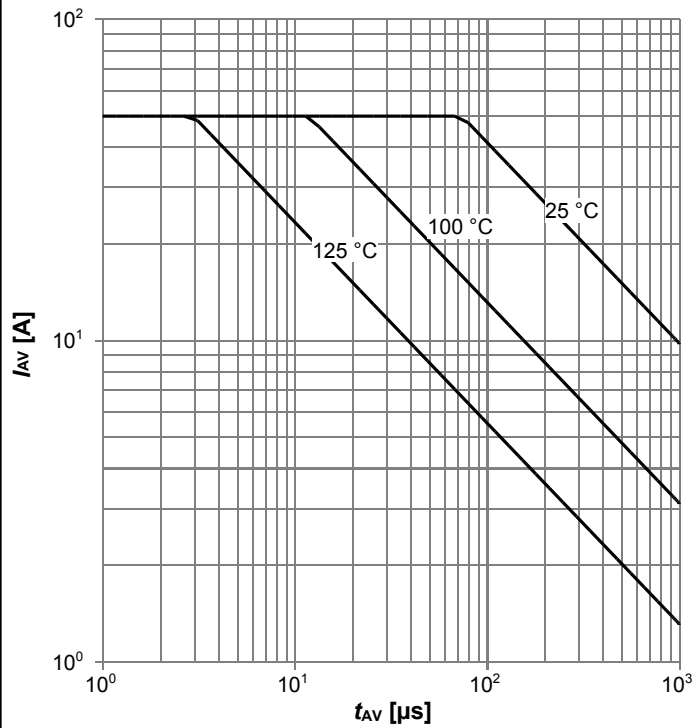
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge

Plot of V_{GS} [V] (y-axis from 0 to 12) versus Q_{gate} [nC] (x-axis from 0 to 80), with curves labeled 6 V, 15 V, and 24 V.
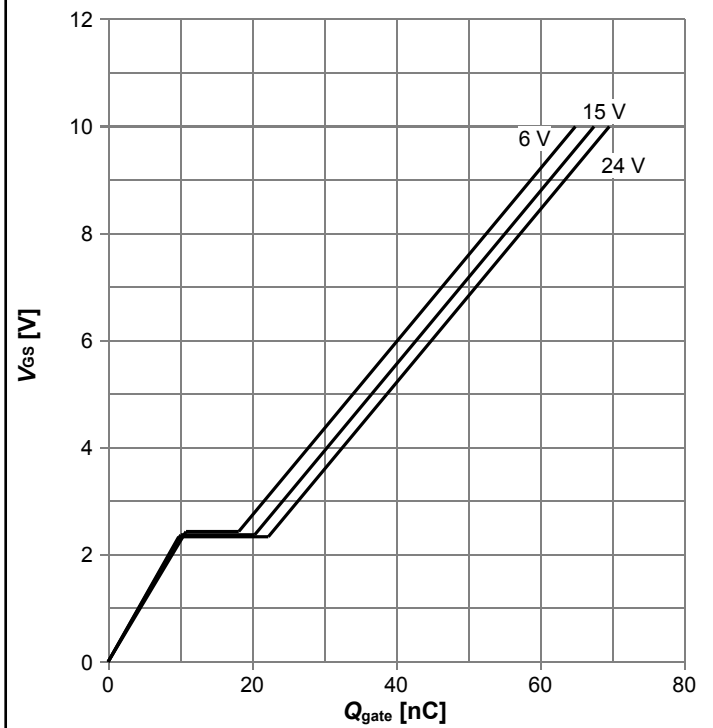
$V_{GS}=f(Q_{gate})$; $I_D=30$ A pulsed; parameter: V_{DD}

Diagram 15: Typ. drain-source leakage current

Plot of I_{DSS} [A] (y-axis, logarithmic from 10^{-6} to 10^{-2}) versus V_{DS} [V] (x-axis from 0 to 25), with curves labeled 125 °C, 100 °C, 75 °C, and 25 °C.
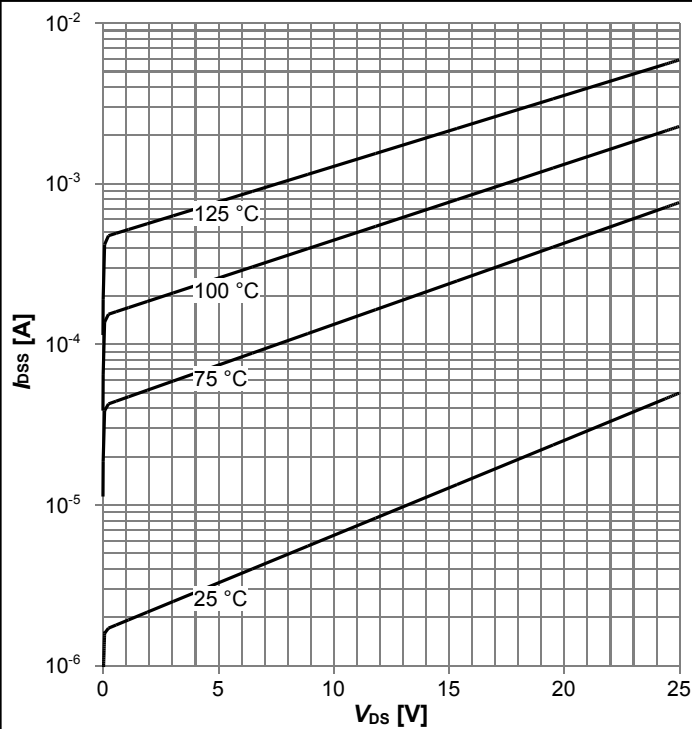
$I_{DSS}=f(V_{DS})$; $V_{GS}=0$ V; parameter: T_j

Diagram Gate charge waveforms

Waveform diagram of V_{GS} versus Q_{gate} showing $V_{gs(th)}$, $Q_{g(th)}$, Q_{gs}, Q_{sw}, Q_{gd}, and Q_g.

OptiMOS^{TM} Power-MOSFET, 30 V
BSC011N03LSI
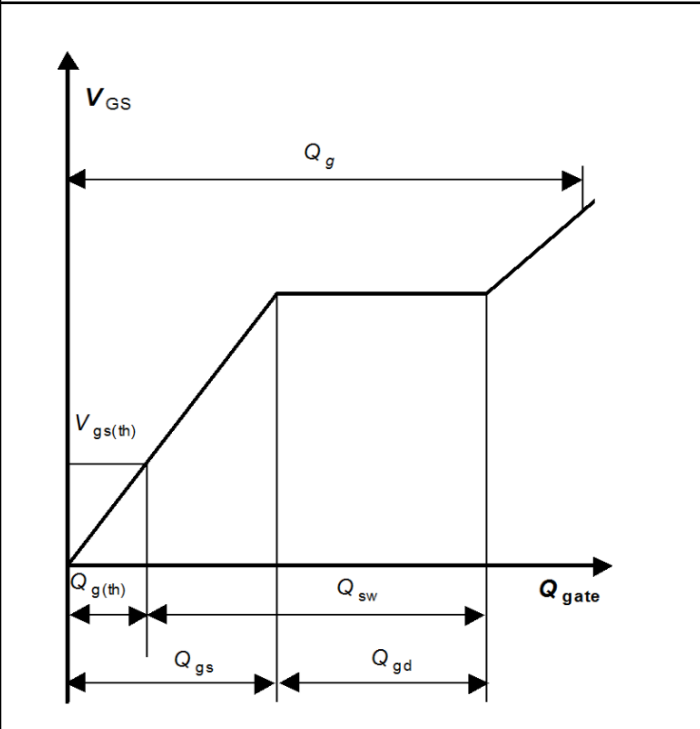
5   Package Outlines

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.
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REVISION
07
SCALE   10:1
0   1   2   3mm
EUROPEAN PROJECTION
ISSUE DATE
06.06.2019

Figure 1   Outline PG-TDSON-8, dimensions in mm

PG-TDSON-8: Recommenåd Boardpads & Apertures
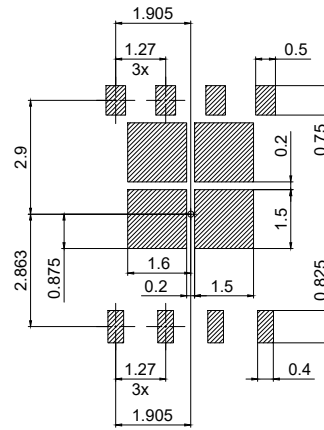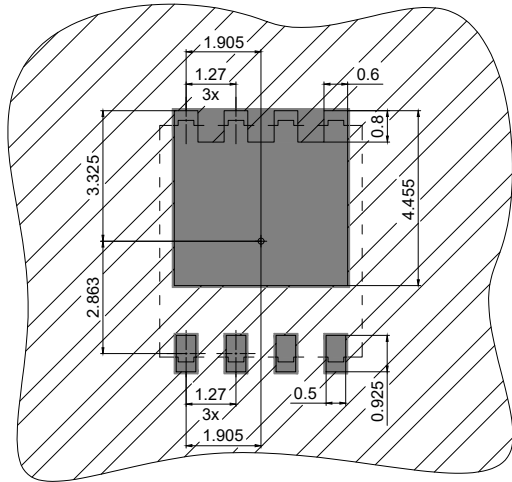
Figure 2   Outline Boardpads (TDSON-8), dimensions in mm

Dimension in mm

Figure 3   Outline Tape (TDSON-8)

Revision History

BSC011N03LSI

Revision: 2020-02-19, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2020-02-19	Update package drawings and footnotes

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