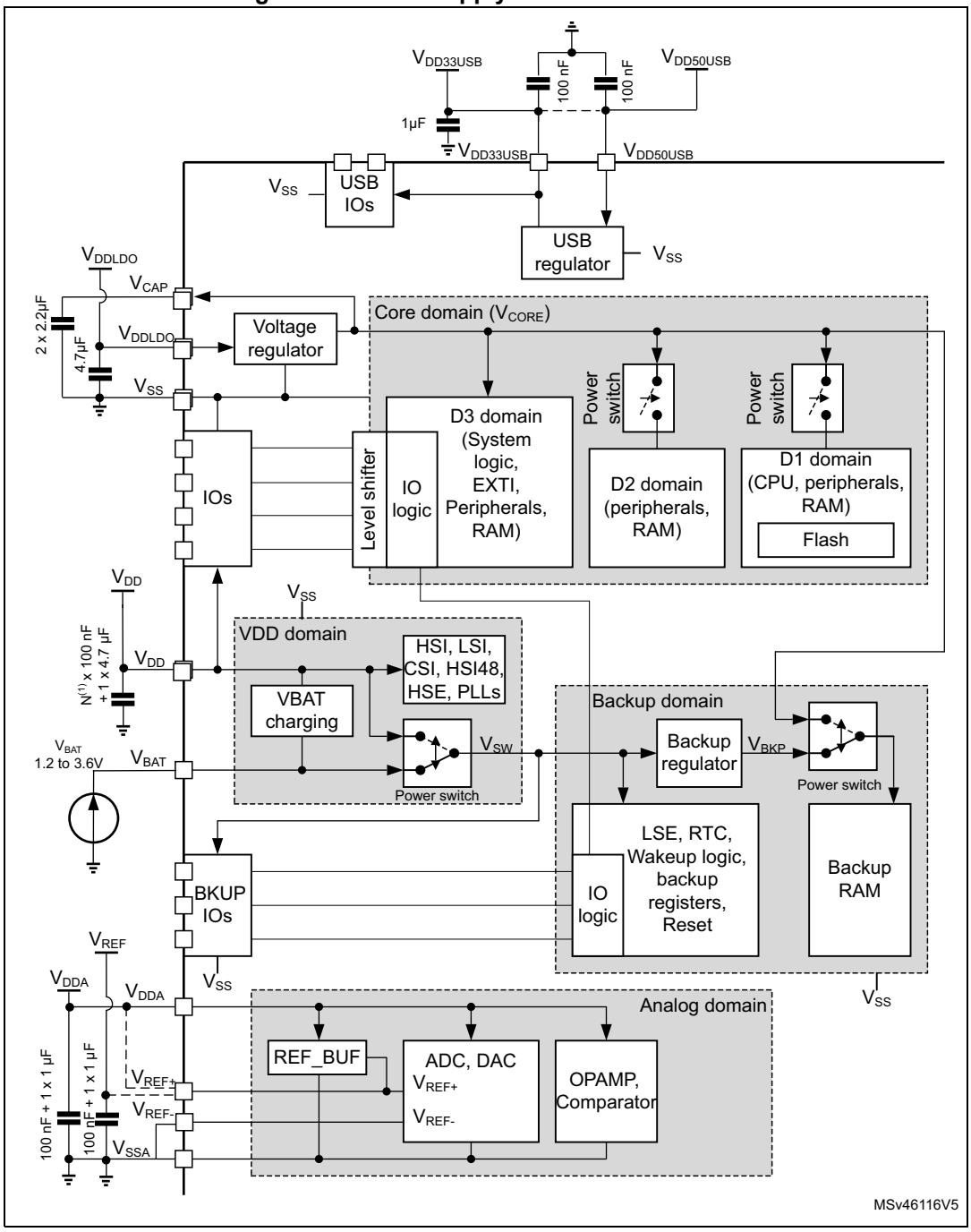
### 7.1.6 Power supply scheme

**Figure 68. Power supply scheme**




1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the