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**Faculty of Electrical Engineering
Department of Measurement**

Bachelor's Thesis

On-board computer for PC104 format CubeSats

Filip Geib
Cybernetics and Robotics

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<https://github.com/visionspacetec/VST104>
Supervisor: Ing. Vojtěch Petrucha, Ph.D.

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Abstrakt / Abstract

Klúčové slová: CubeSat; PC104; OBC; hardvér; PCB dizajn; schémy.

Preklad titulu: Palubný počítač pre CubeSaty formátu PC104

Keywords: CubeSat; PC104; OBC; hardware; PCB design; schematics.

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[chap:intro]

Chapter 1

Introduction

Chapter 2

VST104 project

2.1 CubeSat background

2.1.1 CubeSat concept

CubeSats are modular spacecraft from a picosatellite class, usually constructed of similar components and limited to specific dimensions and materials. CubeSats are being developed in several sizes, which are based on a standard 1U unit [1]. This unit is defined as being $100.0 \pm 0.1[\text{mm}]$ wide and $113.5 \pm 0.1[\text{mm}]$ tall, with a limited mass of $1.33[\text{kg}]$ [2]. Numerous CubeSats also include deployable subsystems, such as antennas, probes, or solar panels that exceed the normative dimensions when deployed [3]. For illustration, some of the already launched CubeSats are shown in figure 2.1.



[img:cubesats]

Figure 2.1. Photos of already launched CubeSats of various sizes. 1U SkCube (left), 2U Asgardia-1 (center), 3U EnduroSat platform (right). Sources: TASR, Asgardia, SmallSat.

“CubeSats are very popular among universities and other non-commercials groups globally. Larger space companies are developing CubeSat missions in-house to train new employees and assess the possibilities of new technologies” [4]. “Several types of CubeSats have been developed and deployed for a specific mission, such as research and development satellites, earth remote sensing satellites, and space tethers satellites” [5].

“A CubeSat must conform to specific criteria that control factors such as its shape, size, and weight. The standardized aspects of CubeSats make it possible for companies to mass-produce components and offer off-the-shelf parts. As a result, the engineering and development of CubeSats become less costly than highly customized small satellites. The standardized shape and size also reduces costs associated with transporting them to, and deploying them into, space” [1]. Some of the standards were introduced by the concept’s originators in the CubeSat Design Specification [2]. A team from the JPL has compiled the CubeSat principles in The CubeSat Approach to Space Access [6].

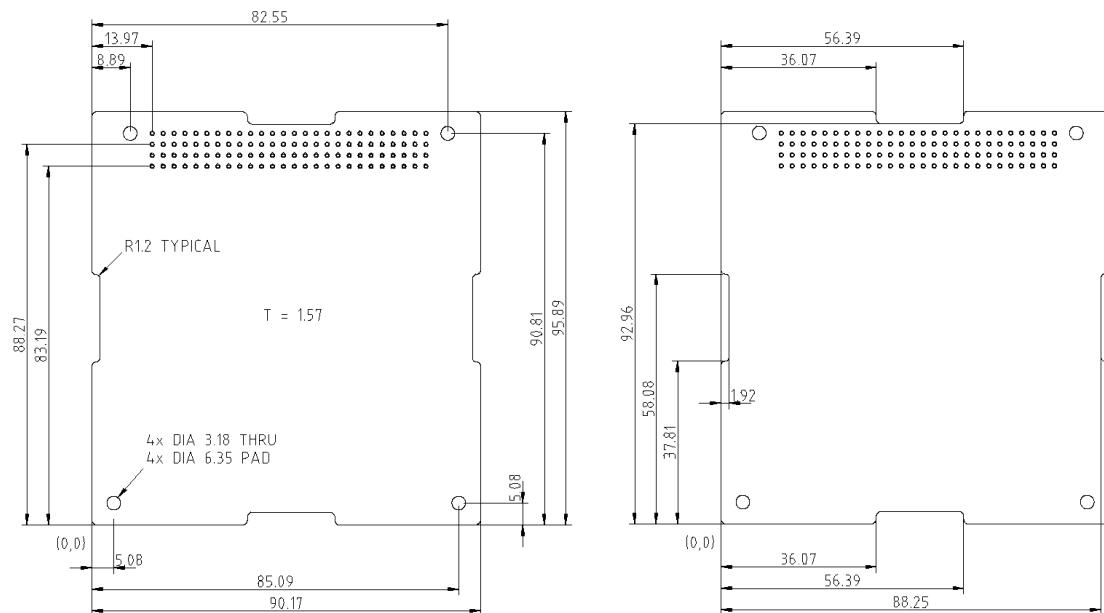
[chap:PC104standard]

2.1.2 PC/104 standard

The CubeSat industry has adopted the PC/104 specifications [7] as a de-facto standard for electronic boards. Moreover, such specifications provide mechanical and electrical benefits towards CubeSat fabrication beyond the compatibility with different structure and electronics suppliers. Following the PC/104 specifications, all electronic boards must measure 90.17 x 95.89[mm], and the electric bus must allocate four rows with 26 contacts of standard 2.54[mm] spacing through-hole (THT) headers” [8].

The PC/104 boards are meant to be stacked on top of each other, forming a rigid structure. The 104 pin headers provide a electrical connection between the individual boards, creating one electrical system. Excluding the headers, the PC/104 boards are firmly attached together with M3 standoffs placed in the corner mounting holes. This combination of the shared electrical bus and M3 bolts improves the stiffness provided by the CubeSat’s structure and simplifies the internal harnessing [8].

As the PC/104 standard allows some freedom for changes, a slightly modified PC/104 board template was used in this project. The template was designed by the LibreCube initiative [9] and its drawings are shown in figure 2.2. The only modification done to the original PC/104 board are 1.9 x 20.3[mm] cutouts located on the board’s four edges. These cutouts are designed to accommodate CubeSat’s auxiliary cables.



[img:PC104]

Figure 2.2. Technical drawings of the LibreCube PC/104 board. Overall geometry (left) and edge cutouts (right). All dimensions are in [mm]. Source: LibreCube.

2.1.3 On Board Computer

The three main design parameters of the electronic systems of small satellites are power consumption, physical dimensions and radiation environment behavior. [10]

[chap:existingOBCmodules]

2.1.4 Existing OBC modules

[11–19]

2.2 Project motivation

Despite growing interest from industry in CubeSats as proper means of technology demonstration, such platforms are still primarily considered as an educational tool. [8]

It is possible to start programming the satellite at the beginning of the project. However, some software developing practices, such as Test-driven Development (TDD), recommend testing the software while it is being developed. Therefore, in practice, software should be directly programmed on the target computer. [8]

2.2.1 Board Sierra

2.2.2 Board Delta

2.2.3 Element Foxtrot

[chap:openSource]

2.2.4 Open source

2.3 Project workflow

2.3.1 Main header pinout

In addition, the allocation and distribution topology for power are not taken over, nor standardized for CubeSats, leading to compatibility issues [6]. Therefore, when PC/104 is mentioned as standard in relation to CubeSats, this refers to a fixed physical wiring harness and the mechanical layout and not the data bus or pin allocation [20].

2.3.2 Components footprints

Every electronic component needs to be properly attached to the PCB's surface. An arrangement of pads required to solder the component on the PCB is called a footprint. Components with different standardized packages require corresponding footprints. These footprints are usually available for download on various websites or are included in the KiCad official libraries. Although it is comfortable to use these pre-made footprints, this approach brings inconsistency and dependency to the PCB design. Therefore we decided to create each of the used footprints by ourselves, following reference designs in components' datasheets and KiCad library conventions [21].

It is a common feature in modern PCB design software such as KiCad to support a 3D visualization. Besides pads, copper traces or

2.3.3 Bills of materials

2.3.4 PCB assembly

Chapter 3

Board Sierra

In this chapter, we are addressing the design process and overall characteristics of the Board Sierra. Design challenges, development decisions, and final features are explained in detail. Particular attention is given to the onboard computer, from now referred to as the OBC. A detailed description of its subsystems is listed in chapter 4.

3.1 OBC characteristics

An OBC of a CubeSat is a complex subsystem combining various features. Reviewing technical documentation of already existing OBCs (chapter 2.1.4) showed that some features are shared among most OBCs, whereas some are unique. In this section, we list all of the features we decided to implement, both typical and VST104 related.

[chap:radiationAndRedundancy]

3.1.1 Radiation and redundancy

Occasionally traveling through weaker parts of the Earth's magnetic field and not shielded by the Earth's atmosphere, the CubeSats have to operate in an environment full of radiation. A direct hit of a high-energy particle might have serious consequences for OBC functionality. These include transistor gate ruptures, memory bit flips, software upsets, or latch-ups [22–24]. Proper measures have to be taken to increase the OBC durability and ability to handle errors, resulting in maximizing a mission lifetime. This process is known as radiation hardening and can be achieved by two different techniques.

A physical approach, also known as a radiation hardening by design, relies on special radiation-hardened components. Hardened ICs are manufactured on insulating substrates (rather than typical semiconductor wafers) or use some of the many dedicated design principles [22]. Implementation of this strategy is typical for professional and more expensive satellites than the CubeSats. These components are usually bigger, costly, and have reduced performance and functionality compared to ordinary ones.

Considering the size and budget requirements of our OBC, we chose to implement another option. Instead of the previously mentioned physical hardening technique, a logical one was realized. The OBC hosts multiple schematic design features ensuring the proper handling of any radiation-related event. These include: i) over-current sensing power management, ii) separate peripheral isolators, iii) full high-impedance mode requested by the higher logic, iv) triple-redundant memories, or v) multiple onboard temperature sensors. A fully double-redundant OBC is presented in chapter 5.

[chap:capabilitiesAndFeatures]

3.1.2 Capabilities and features

Having in mind the expectations of the VST supervisors, features common for OBCs by different manufacturers (chapter 2.1.4), and design requirements implied by the radiation (chapter 3.1.1), we set and implemented the following OBC's features:

- **Microcontroller:** An ultra-low-power STM32L496 ARM Cortex-M4 core microcontroller drives the OBC. This MCU can run up to 78[MHz], is equipped with a 1[MB]

flash memory and 320[kB] RAM, and provides a wide external connectivity. A user can program and debug this MCU using a separate SWI or UART connection.

- **External clock sources:** The MCU is equipped with two external clock sources for improved and more reliable clock generation and timing. Low-speed external 32.768[kHz] oscillator and high-speed external 26[MHz] oscillator. This oscillator can be temporarily disabled by the MCU to achieve better power consumption.
- **Robust power management:** Two separate power lines with 3.3[V] and 5[V] ratings supply the OBC. A robust power management circuitry is present separately on these lines, providing tunable over and under-voltage protection, over-current protection, amplified current monitoring output, kill switching, and simultaneous power down.
- **Isolation of the peripherals:** The OBC can communicate with other CubeSat modules using a 2x CAN bus, 3x I²C, 4x UART, 2x SPI, 22 GPIO pins, and 5 maintenance signals. All the peripherals are 5[V] tolerant and connected to the PC104 main header thru separate analog switches. These isolators are independently controlled by the MCU and provide a complete or selected disconnection from the rest of the CubeSat.
- **Redundant external memory:** Two subsystems of triple redundant external memories are available for MCU's additional data storage. This triple redundancy ensures data validity in the radiation-rich environment, although the single-mode is also supported. The first memory subsystem is a 3x 32[MB] Flash connected via the Quad-SPI interface, while the second one is a 3x 2[Mb] F-ram using the SPI.
- **CAN bus peripherals:** Two CAN transceivers provide the OBC's support of a high-speed CAN bus. These transceivers ensure a voltage level conversion (3.3[V] for the MCU, 5[V] for the CubeSat) and support communication speeds up to 250[kB s⁻¹].
- **Temperature monitoring:** Seven I²C temperature sensors are spread over the entire OBC. These sensors monitor the temperature of essential submodules, 2x MCU, 2x power management, 2x CAN bus drivers, and 1x external memories. The MCU can power on or off these sensors to save some power or resolve a latch-up even.
- **Maximal payload sector:** The PCB surface occupied by the OBC circuitry is shrink to the minimal size possible. The remaining area is considered as a payload sector that can accommodate any user-defined modules. In our case, we decided to place a universal soldering array with exposed power lines all over this sector.

[chap:componentsSelection]

3.2 Electronic components

Electronic components are the building stones of each electronic hardware. Big commercial, military, or research spacecrafts use specialized components designed, modified, or particularly selected for space applications. CubeSats, on the other hand, use in most cases commercial off-the-shelf (COTS) components that are not specifically designed for application within the space environment [3]. The use of COTS components is certainly an attractive option for the development team of small satellite projects. Lead times are short, and recent developments in personal computing equipment and consumer electronic allow for high performance [25]. In the VST104 project, we also decided to follow this trend and to use COTS components. In this section, we describe various requirements applied to these components and the criteria of their selection.

[chap:componentsCertification]

3.2.1 Components certification

Spacecrafts are exposed to a harsh environment and its effects during their lifetime. This problem needs to be also addressed on the electronic components level by selecting

components with adequate parameters. The two essential criteria that need to be watched are operational temperature range and mechanical stress resistance.

“The temperature range that electronic components can encounter in orbit is quite large as the thermal control options are limited” [4]. “The most crucial impact on the temperatures of a spacecraft is caused by the external radiation from Sun and Earth, as well as internal heat dissipation throughout electronic devices” [3]. Typical operational temperature for CubeSat components is in the range of -40 to $+85[^\circ\text{C}]$ [3–4], usually referred to as an industrial temperature range. As we wanted to be on the safe side, we decided to add a safety margin by extending the range. We chose the automotive range of -40 to $+125[^\circ\text{C}]$ as a requirement for electronic components in our design.

“During the launch, a spacecraft is subjected to various external loads resulting from vibroacoustic noise, booster ignition and burn out, propulsion system engine vibration, steady-state booster acceleration, and much more” [5]. Hence, various measures are applied to increase the robustness of the spacecraft. Regarding the OBC design, it was necessary to select only the electronic components meeting the AEC-Q100 and AEC-Q200 standards. “Components meeting these specifications are suitable for the harsh automotive environment without additional component-level qualification testing” [26].

To sum it up, all of the electronic components used in the Sierra Board i) are rated for the automotive temperature range of -40 to $+125[^\circ\text{C}]$, and ii) obtained the AEC-Q100 or AEC-Q200 qualification. The only exception is the MCU with no AEC qualification.

Some of the OBC’s potential applications may not require temperature and automotive certification of the electronics components. In such a case, some components may be replaced by their uncertified variants to save a bit of the financial budget. All of the electronics components with an official uncertified version are listed in table 8.2. Furthermore, the potential user is encouraged to replace all passive components (resistors, capacitors, ferrite beads, inductors) with unqualified parts of the same parameters. A replacement of oscillators Y[1,2] is possible, although this change is non-negligible.

[chap:powerConsumption]

3.2.2 Power consumption

CubeSat’s power budget is a closely monitored thing. Such a small spacecraft has a limited means of generating and storing electric power. Solar arrays are usually bound in their active surface and lack advanced tools of positioning. Similarly, battery storage systems are restricted by the available space and means of temperature control. It is crucial to minimize the power requirements of the CubeSat, including the OBC.

Reasonable power consumption of the OBC can be achieved on the level of electronic components selection by prioritizing the low-power components. A downfall of this approach is usually an implied decrease in their performance, speed, or frequency. Therefore, we preferred components with similar parameters but lower power consumption. This affected mostly the selection process in cases of the MCU and memory ICs.

Not only a component’s power consumption but also its efficiency is an important parameter. While choosing switching components such as electronic fuses, hot-side switches, or analog switches, a low on-resistance was preferred. Power losses on pull-down/pull-up resistors had to be also taken into consideration. A single $10[\text{k}\Omega]$ pull-down resistor connected to a $3.3[\text{V}]$ signal drains a constant current of $330[\mu\text{A}]$, creating a power loss of approximately $1.1[\text{mW}]$. During the schematic design, we aimed more at a subsystem’s robustness rather than avoiding this particular type of power loss. Therefore, some of the pull-down/pull-up resistors may be left unpopulated and their functionality compensated by programmable resistors integrated inside the MCU.

The summary of power consumption of the specific electronics components is listed in table 8.1. Overall power consumption of specific OBC's submodules is listed in table 3.1. It sums power consumptions of all ICs and losses on pull-down/pull-up resistors in the particular subsystem. For the computation, two assumptions were made: i) full functionality of the subsystem, ii) input voltage range as described in table 4.2.

Subsystem	3.3[V] current [mA]			5[V] current [mA]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Processing unit	-	-	-	-	-	-
Power management	-	-	-	-	-	-
Header isolation	-	-	-	-	-	-
Flash memories	-	-	-	-	-	-
F-ram memories	-	-	-	-	-	-
Dual CAN bus	-	-	-	-	-	-
Temp. monitoring	-	-	-	-	-	-

[\[bsystemConsumption\]](#)

Table 3.1. A rough estimation of particular subsystems' power consumption. Legend: min. - subsystem in standby mode, typ. - subsystem in typical operation, max. - subsystem peak performance. This table should be used for orientation purposes only. A potential user is encouraged to conduct a proper measurement for each Board Sierra application.

[\[chap:additionalParams\]](#)

3.2.3 Additional parameters

A selection of particular electronic components is a vital part of designing circuitry. Usually, various electronic components share the same functionality and are available from different manufacturers. After filtering the available components by specific functionality (with respect to 3.2.1 and 3.2.2), it was common to find various suitable candidates. Therefore, additional criteriums had to be set to resolve the selection:

- **Price:** As this OBC is not primarily designed for an actual space flight (as explained in ??), an individual component's price is not negligible. With a lower overall cost of the OBC, a broader project expansion in the LibreCube community can be achieved. Thus components with sufficient attributes but lower price were favored.
- **Footprint:** As a result of maximizing the PC104 payload sector, the actual OBC area was significantly decreased. Therefore components of smaller dimensions available in fine-pitch packages (e.g. SSOP or QFN) were preferred. The same logic applies to passive components such as resistors and capacitors, resulting in a 0201 package (0603 in metric) being the most widely used in this design. After researching the technical capabilities and related costs of PCB manufacturers, we decided not to use the BGA-packaged components. Their significantly smaller footprints would require more precise fanout, resulting in increased manufacturing difficulty and price.
- **Distributor:** We considered it important to use only typically stocked components available from the global distributors. In our case, Mouser electronic¹. This rule should repeal any future problems in components sourcing or logistics. Therefore, the availability of a specific component in this distributor was a selection factor.

3.3 PCB features and design

Designing the Board Sierra's PCB was probably the most demanding part of the VST104 project. Restricted surface available for the complex OBC's circuitry, compact

¹ <http://www.mouser.com/>

footprint of the PC104 main header with a not ideal location, and limited capabilities of the considered PCBs manufacturers made the routing and fanout challenging. Visualization of the designed module rendered in KiCad is shown in figures 8.2 and 8.3.

3.3.1 PCB requirements

The benefit of the Board Sierra's lower price regarding the particular electronic components was described in chapter 3.2.3. The same logic applies to the decision-making during the PCB design. It is a common feature between PCBs manufacturers that the less advanced design, the cheaper PCB. This includes many parameters such as copper layer count, presence of buried vias and their size, copper clearances, tracks widths, and much more. On the other hand, fine features such as buried vias simplify the process of PCB design and allow more compact layouts. Therefore, it was crucial to find a balance between the manufacturing price and complexity of the OBC's layout and routing.

Although, following the proper design rules and standards created for automotive and especially space applications is much more important than lowering the PCB's manufacturing price. We addressed various requirements and suggestions listed in ECSS standards ECSS-Q-ST-70-12C [27] and ECSS-Q-ST-70-60C [28]. Other precious recommendations were found and implemented from the TEC-ED IoD Board Specification [29]. These specifications refer, for example, to track width and spacing, pad design, copper planes, or thermal rules. However, these documents are aimed at state-of-the-art spacecrafts designed and operated by the ESA. Thus a punctual following of all of the requirements and suggestions was not necessary for our CubeSat application.

[chap:payloadSector]

3.3.2 OBC and payload sector

As mentioned in chapter 3.1.2, a high ratio between the payload sector area and OBC area was set as one of the Board Sierra's key features. This requirement substantially affected the OBC's circuitry layout and fanout. After multiple iterations of components' placements and alignments, we have significantly reduced the required OBC area. The payload sector covers roughly three-fourths of the available PC104 module surface, leaving only one-fourth to accommodate the OBC. Visual perception can be obtained from the Board Sierra 3D renders in figures 8.2 and 8.3. The OBC sector is situated at the northwest quartal of the PC104 module, surrounded by the payload sector.

3.3.3 PCB characteristics

The PCB's dimensions, geometry, and layout of the main connector and mounting holes are fully specified by the PC104 standard, as described in chapter 2.1.2. The only modification added to this template are $1.9 \times 20.3[\text{mm}]$ cutouts on the module's four edges. These cutouts were introduced in the LibreCube board specification and are designed to accommodate CubeSat's auxiliary power and data cables [9].

Regarding the manufacturing price and complexity, the PCB would ideally be a four-layer one. This means two copper layers for signal traces, a power distribution layer, and a ground plane. Unfortunately, the two signal layers would not be enough to accommodate complex OBC's circuitry. Therefore, we had to choose a six-layer PCB with the following setup: i) signal layers: top, second inner, bottom; ii) ground plane layers: first inner, fourth inner; iii) power distribution layers: third inner. "An additional benefit of the added layers is improved thermal dissipation, as adding a layer of copper to the circuit board can significantly decrease the resulting temperatures" [3].

Additional parameters of the PCB manufacturing such as material, isolation and copper thickness, surface finish and solder mask types are not specified in this thesis

nor the VST104 project. It is the responsibility of the potential user to customize these parameters accordingly to the requirements of the specific application. In such a case, we encourage the user to follow relevant sections of the ECSS standard [27].

3.3.4 Traces, vias and routing

Electronic components are placed on both sides of the PCB due to the restricted OBC area. Corresponding top and bottom copper layers cover as much routing as possible. The second inside layer accommodates traces that do not fit into the two surface layers. The general width of a signal trace is 0.2[mm], respectively 0.173[mm] for traces near the main PC104 header. Clearance between traces themselves and other copper planes is set to 0.127[mm]. All of these parameters satisfy the minimal specifications in the ECSS standard [27]. No blind, buried or micro vias are used in the design. The diameter of general via is 0.45[mm] with a 0.24[mm] drill. This parameters result in a 6.7 aspect ratio for a standard 1.6[mm] thick PCB, which recognizes the ECSS ≤ 7 rule [27].

The first and fourth inner layers are ground plane layers. Their purpose is to connect all of the component's GND pins, provide shielding against the EMI and act as heatsink dissipating components heat. Despite the ECSS suggestion, both the ground planes have a solid fill instead of additional openings in a grid format [27]. The reason is, the current fifth version of KiCad does not support this option. This design flaw will be improved shortly as the checked fill option is included in the upcoming KiCad v6.

A copper plane with a solid fill is also located in the third inside layer. This plane is attached to a 3.3[V] power source, and its task is to connect all required components to this power bus. This layer also accommodates a 5[V] power distribution routing. Its traces are 0.45[mm] wide with multiple vias to minimize the potential voltage drop.

The final PCB routing highlighted by the particular OBC's subsystems is shown throughout multiple figures in chapter 4. General principles of good routing were implemented throughout the PCB design. These include steep turns avoiding, differential pairs matching, or sliver and peelable prevention [28]. If available, fanout and routing suggestions included in electronic components datasheets were followed. As suggested by the ECSS [27], a teardrop finish was applied to all of the pads using the KiCad Teardrops extension listed in chapter 2.2.4. It is important to mention that the current KiCad v5 does not support advanced design settings common for professional software such as Altium Designer or CadSoft EAGLE. Our approach to handling this problem was adding extra margins to the few parameters listed in KiCad, which increased the overall tolerance. The final PCB design passed a design rule check (DRC) with various parameters set according to manufacturers' standards and ECSS suggestions [28].

Chapter 4

Board Sierra - submodules

In this chapter, we are addressing each of the OBC's submodules as listed in chapter 3.1.2. The motivation, requirements, development decisions, functionality, schematic design, and PCB design of each submodule are explained in detail. These descriptions are illustrated by functional diagrams, schematic diagrams, and PCB fanouts.

4.1 Microcontroller

The processing unit is the most important part of the OBC. Professional designs use MCUs with a wide variety of different instruction set architectures [11, 13, 15–16, 19]. However, the ARM architecture seems to be the most popular [12, 14, 17–18]. This architecture is known for its good multiprocessing support, low power consumption, affordable pricing, and existing applications in various fields. Considering these benefits and influenced by the LibreCube initiative, existing TUDSaT's project, and most importantly the VST supervisors, we decided to pick an STM32 microprocessor.

Our task was to choose a particular model of this 32-bit, Arm and Cortex-M based MCU. Aiming rather for a low-power than high-performance characteristics, we decided to select an L series. Particularly the L4 series as it combines the largest flash memory size with the highest number of general-purpose input/output pins (GPIOs) [30]. Although, only one device from the L4 series is equipped with two CAN bus channels. As the presence of a second bus is crucial for our double-redundant approach, the STM32L496xx option was selected. This family comes in six different packages. Avoiding all of the BGA-like ones (as described in section 3.2.3) narrows the selection to Zx, Vx, and Rx variants. The Zx is the most capable one in terms of flash size and GPIO count. Therefore the STM32L469ZG (where G stands for extended operating temperature range) was our final choice [31]. From now on, we will refer to this particular device as the MCU. Some of its key characteristics are listed in table 4.1.

Max. frequency	80 [MHz]	SPI	3
Flash memory	1 [MB]	I ² C	4
Static RAM	320 [kB]	UART	5
Comparators	2	CAN	2
Op. amplifiers	2	GPIO	115
Operation temp.	−40 to 125 [°C]	DAC	2

Table 4.1. Highlighted characteristics of the STM32L469ZG microcontroller [31].

4.1.1 Schematic design

The MCU pin assignment was continuously changing during the entire process of OBC schematic and PCB design. Its final state is presented in figure 8.4. We attempted to maximize the number of user-free GPIOs with added functionalities such as ADC

or PWM while keeping the fanout manageable. A significant help during this process was the CubeMX tool of the STM32CubeIDE, visualizing all of the pinout combinations with a specific functionality. Each of the 3.3[V] tolerant pins was used only for the internal circuitry, resulting in a fully 5[V] tolerant main PC104 header connection.

A significant number of filtering and reservoir capacitors is needed to ensure the proper MCU functionality. The assignment of correct capacitors to required MCU pins was pretty straightforward, following the device datasheet [31] and STM32L4 hardware development application note [32]. Furthermore, a 10[μ H] choke and 120[Ω] at 100[MHz] ferrite bead were placed in series with the analog power input. This LC filter supported by the bead should effectively eliminate both low and high-frequency interference.

The clock and data lines of both I²C busses are equipped with standard 4.7[k Ω] resistors. Multiple 22[Ω] resistors were placed in series with high-speed clock signals of the SPI interface. Two 0[Ω] resistors are present on *FAULT* and *MODE* lines to facilitate an optional hardware isolation. A 10[k Ω] resistor at *PH3* is suggested by [32].

4.1.2 PCB design

Location and fanout of the MCU are shown in figure 4.1. The MCU is placed on the PCB top side, covering most of the non-payload area. This big footprint of a LQFP144 package (approximately 2 x 2[cm]) is a consequence of avoiding the BGA packages while still trying to keep the pin count high. All of the capacitors were placed as close to their assigned pins as possible. In some cases, it was necessary to use the bottom side of the PCB. The same approach was applied to all of the resistors. A hole of 1.2[mm] diameter is placed roughly at the middle of the MCU footprint. The diameter was set to fit a 19 gauge needle attached to a syringe with epoxy. This epoxy glue should be filled through this hole into the void space between the PCB and the MCU. This procedure is typical for space applications. Its purpose is to add some mechanical robustness to the LQFP device and create a thermal bridge between the PCB and the devices.

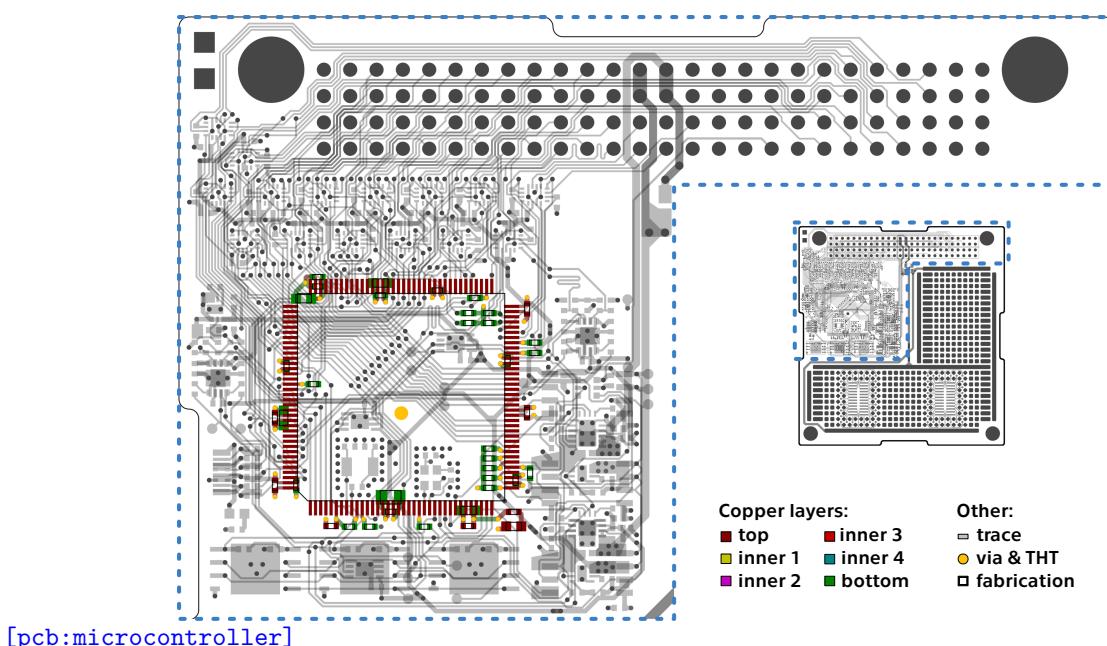


Figure 4.1. Highlighted location of microcontroller circuitry.

4.2 External clock sources

Proper timing and synchronization are the key features while dealing with high-speed data busses, ADCs, or other precise applications. The MCU is equipped with two internal RC oscillators that can be used to drive a master system clock and other auxiliary clocks [31]. These internal oscillators generally have a significantly lower frequency stability, a higher temperature dependency, and smaller overall accuracy than their external equivalents [33]. Therefore, to increase the clock precision and reliability in the harsh space environment, we had to implement external clock sources.

A 4 – 48[MHz] high speed external oscillator (HSE) can drive the system clock. Supported types are crystal, ceramic resonator, or silicone oscillator [31]. The last option seems to be the best as it is insensitive to electromagnetic interference (EMI) and vibration. The only downside is its slightly lower temperature rejection [34]. We chose the SiT8924B, a 26[MHz] silicon microelectromechanical system (MEMS) oscillator [35]. Accordingly to the clock configuration tool of the stm32cube software, we can reach various system clock and auxiliary clocks frequencies up to 78[MHz] (maximum is 80[MHz] [31]). This is done using the phase-locked loop (PLL) clock generation.

A 32.768[kHz] low speed external oscillator (LSE) can drive the real time clock (RTC), hardware auto calibration, or other timing functions [31]. Table 7 in [36] recommends individual crystal resonators for combination with STM32 MCUs. After a consideration of these options, we decided to pick the ABS07AIG ceramic base crystal [37].

4.2.1 Schematic design

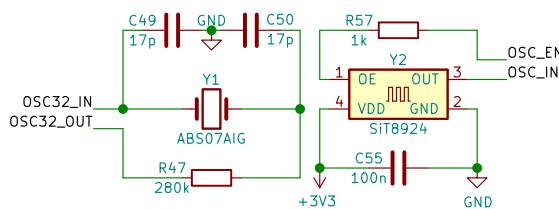
The HSE circuitry follows the oscillator datasheet [35] and is shown on the right side of figure 4.2. Only a decoupling capacitor and a terminator resistor are required. The clock output *OSE_IN* can be enabled or disabled by the binary *OSC_EN* signal.

The LSE circuitry is based on a reference design in the oscillator design guide [36]. To achieve a stable frequency of this Pierce oscillator, it is required to find the values of load capacitors C_{L1} , C_{L2} and external resistor R_E . This can be done using equations

$$C_L = \frac{C_{L1}C_{L2}}{C_{L1} + C_{L2}} + C_S \quad \wedge \quad C_{L1} = C_{L2}, \quad (1)$$

$$R_E = \frac{1}{2\pi f C_{L2}}, \quad (2)$$

where C_L is the crystal load capacitance, f is the crystal oscillation frequency and C_S is the stray capacitance [36]. Values of C_L and f are listed in the crystal datasheet [37]. We can assume as a rule of thumb, that $C_S = 4[\text{pF}]$. The final LSE circuitry with computed values of the components is shown on the left side of figure 4.2.



[sch:clockSources]

Figure 4.2. Schematic diagram of external clock sources.

4.2.2 PCB design

Location and fanout of the external clock circuitry are shown in figure 4.3. All of the components are placed on the bottom side of the PCB. The circuitry layout follows multiple tips presented in the oscillator design guide [36]. Separate GND planes are assigned to both the HSE and LSE circuitry. These planes are bounded by guard rings, formed by series of vias. Each of the planes is connected to a common GND only at one point. This approach provides proper EMI shielding while reducing a ground loop effect. We also minimized the distance between the MCU pins and both oscillators. All these measures combined should improve the clock generation stability and robustness.

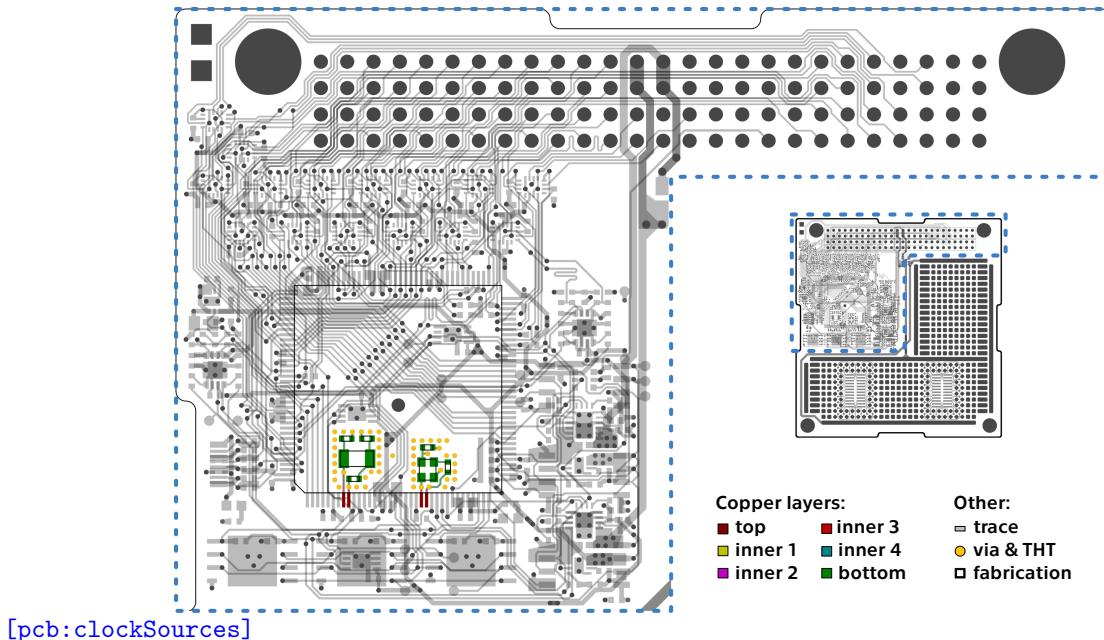


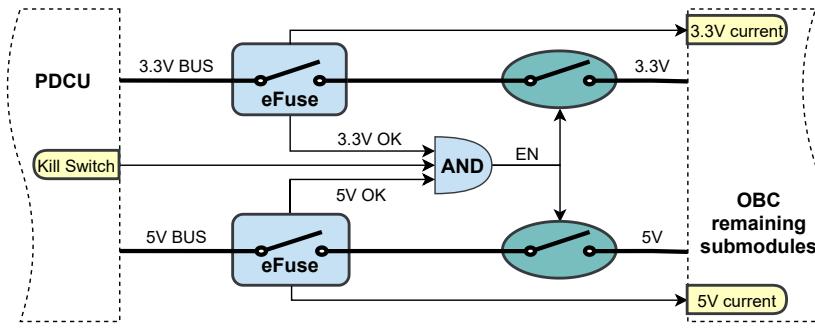
Figure 4.3. Highlighted location of external clock sources circuitry.

4.3 Power management

The electric power subsystem (EPS) is known to be the most vital subsystem of a spacecraft. Its reliability and error handling should be ensured by the power control and distribution unit (PDCU). However, it is a good practice by professional manufacturers to include an additional power monitoring and control to their OBC module designs [11–19]. We have to implement circuitry that can sense a power bus malfunction and, as a response, power down the OBC. This feature is also important for some of the OBC on-earth user cases. During a hardware development or a system presentation, the user might misconnect the power line or use an unsupported power source by a mistake.

A functional diagram of the implemented power management is shown in figure 4.4. To increase the overall efficiency and decrease complexity, we decided to avoid any voltage conversion independent from the PDCU. Therefore, our OBC requires two separate inputs from the main power buss (3.3[V] and 5[V]). The OBC is connected to each of these inputs through an electronic fuse (eFuse). This device continuously monitors the bus for events of under-voltage, over-voltage, and over-current¹. As a response to such an event, the eFuse will switch into high impedance and pull down

¹ This is a crucial feature in handling and resolving a latch-up event.



[dia:powerManagement]

Figure 4.4. Functional diagram of power management circuitry.

specific input of an AND logic gate. This gate simultaneously controls two load switches, one for each power line. This approach ensures that a fault on one power bus will result in a high impedance of both OBC power inputs. It also eliminates the risk of a death loop, in which a reset of eFuses is not possible as they are switching each other off. Added benefits of this design are an inbuild current measurement and a Kill Switch integration into the logic gate. A summary of the final power management rating is listed in table 4.2. These values were chosen considering the power requirements of the remaining OBC components and are a subject of change by a future user.

Power input	Parameter	Min	Typ	Max	Unit
3.3[V] BUS	voltage	2.9	3.3	3.5	V
	current	0.0	-	1.2	A
5[V] BUS	voltage	4.6	5.0	5.4	V
	current	0.0	-	1.2	A

[tab:powerManagement]

Table 4.2. OBC power rating. Value out of range will cause a protective shutdown.

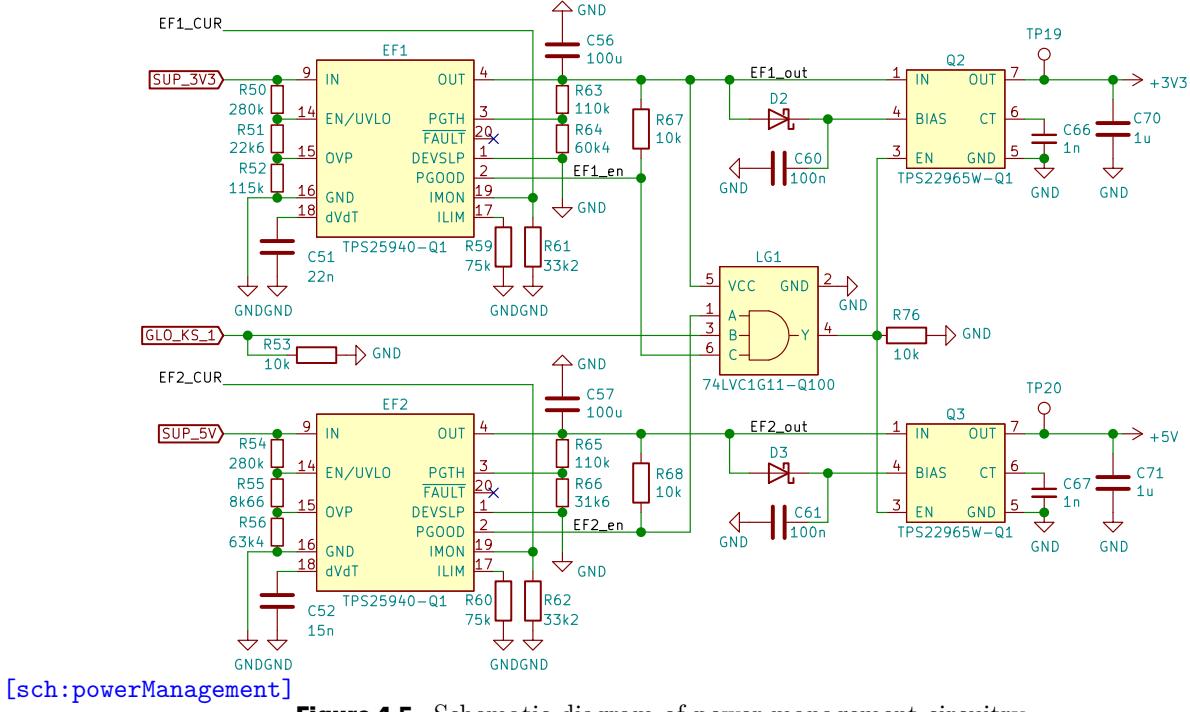
[secc:powerManagementSch]

4.3.1 Schematic design

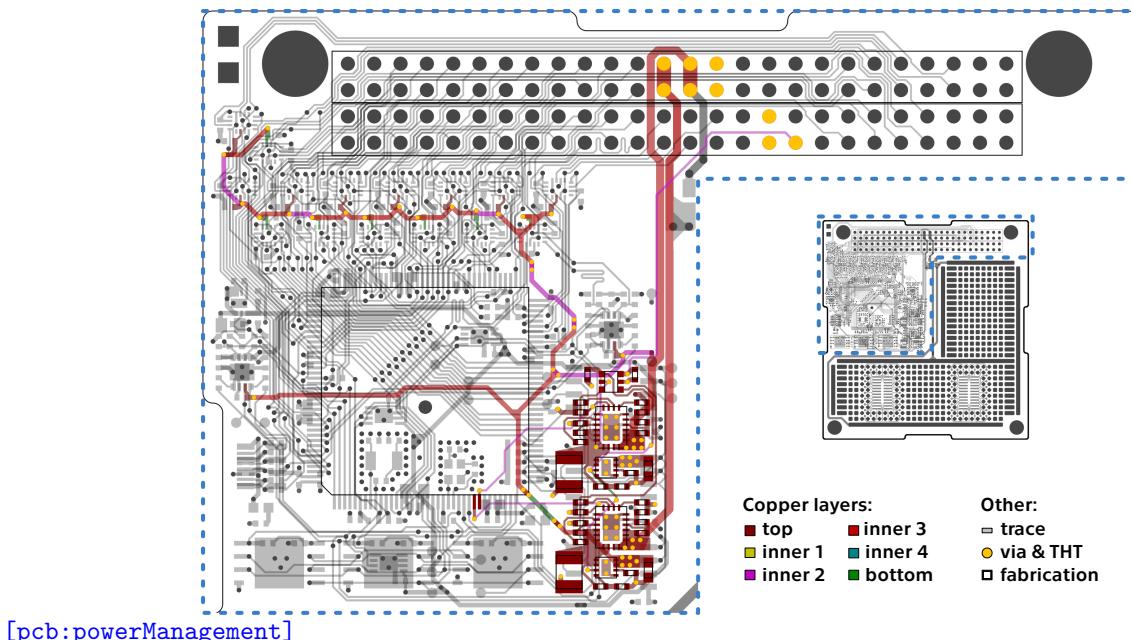
An actual schematic diagram of power management circuitry is shown in figure 4.5. The most important part of this design is the eFuse, as it covers all of the power control features. We decided to use the TPS25940-Q1 device [38]. Custom threshold values can be set following the typical application schematic in the datasheet [38]. This is done by connecting specific resistors, with values calculated using the TPS2594x design calculation tool [39]. As the logic AND gate, we chose the 74LVC1G11-Q100 [40]. This device is designed to operate in a mixed logic level environment, what corresponds with our application. The last important component is the load switch. In our case, the TPS22965W-Q1 with an inbuilt output discharge function [41]. For a correct operation of the switch, the *VBIAS* pin should stay saturated for a while after disconnecting the *VIN* voltage. We achieved this behavior by charging a capacitor connected to the *VBIAS* from the *VIN* through a Schottky diode. Four reservoir capacitors are placed on both sides of the load switches, following the suggestions in both datasheets [38, 41]. Nominal logic values of all switching signals are set by pull-up or pull-down resistors.

4.3.2 PCB design

Location and fanout of the power management circuitry are shown in figure 4.6. All of the power management components are placed on the top side of the PCB. Similarly, all of the power tracks are on the top copper layer. Only a few signal traces are running

**Figure 4.5.** Schematic diagram of power management circuitry.

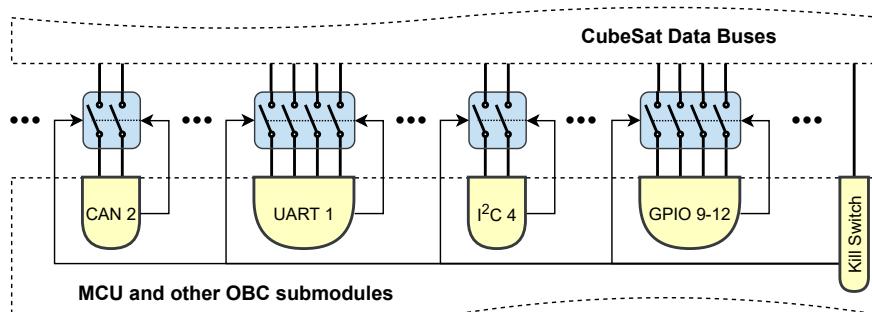
within the second or the bottom layer. Both the 3.3[V] and 5[V] control circuitry share the same layout and tracing regarding recommendations presented in the eFuse and load switch datasheets [38, 41]. The 3.3[V] part is situated closer to the main PC104 header, while the 5[V] part is right below it. Both eFuses are connected to the main PC104 header power pins through strengthened 0.77[mm] traces in the third copper layer. Considering a standard copper thickness of 35[μ m], each of the input traces is rated to deliver up to 2[A] of current. The logic gate with associated pull-down resistors is located above all of the remaining circuitry, closest to the main PC104 header.

**Figure 4.6.** Highlighted location of power management circuitry.

4.4 Peripheral isolators

The spacecraft OBC is connected to many data buses shared among all other CubeSat submodules. In some scenarios, the OBC must be able to isolate itself from a specific or multiple data buses. For example, to switch between OBCs in a redundant configuration, to handle a failure on a data bus, or to prevent unintentional interference. Standard approaches to address this feature are based on using analog switches [42], optocouplers [43], or FPGAs [11]. Furthermore, these isolators should also guarantee that all data lines are in a high impedance state when the OBC is powered off.

After a brief survey, we decided to implement the design using robust analog switches. This approach is more straightforward, less expensive, and requires a smaller PCB area than the optocoupler or the FPGA-based ones. A functional diagram of the implemented circuitry is shown in figure 4.7. All of the OBC data lines are connected to the rest of the spacecraft through a series of analog switches. These data lines are grouped by particular data buses and are assigned to a separate switch. The OBC can enable or disable a specific switch and therefore isolate a particular data bus from the remaining spacecraft subsystems. Pulling low the Kill Switch will result in high impedance of all switches and completely isolating the OBC data lines.

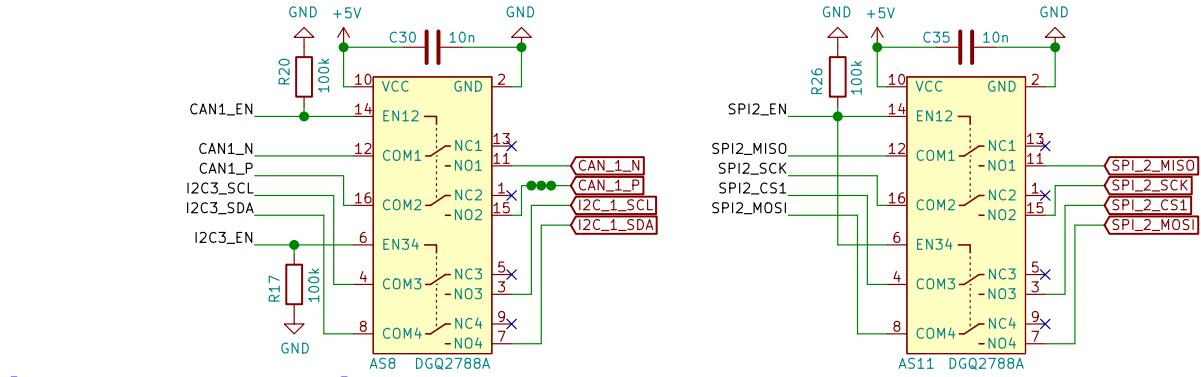


[dia:peripheralIsolators]

Figure 4.7. Functional diagram of peripheral isolators circuitry.

4.4.1 Schematic design

Schematic diagrams of two isolators are shown in figure 4.8. We decided to use the DGQ2788A device [44]. The OBC hosts fifteen of these analog switches in a dual double pole double throw (DPDT) configuration. The OBC data lines are connected to common terminals (*COM*). Normally closed terminals (*NC*) are left floating, whereas normally open terminals (*NO*) are connected to the spacecraft data lines. The important Kill Switch functionality is implemented using the device's power down protection. If the switch loses power, it will enter the normal state. This approach simplifies the circuitry a lot as it substitutes an otherwise necessary system of multiple logic gates. Other beneficial features of this analog switch are a high latch-up current of 300[mA] and inbuild signal clamping. The device will clamp all of the signals exceeding its supply voltage by internal diodes. As the MCU pins connected to these analog switches are 5[V] tolerant, we chose to power the switches from the 5[V] power bus. A malfunction could be caused by the switch's enable terminals (*EN*), as they do not include internal pull-up or pull-down resistors. We decided to use external pull-down ones to avoid the enable signals' floating state and avoid unintentional device switching. The decoupling capacitors were placed accordingly to the device datasheet.



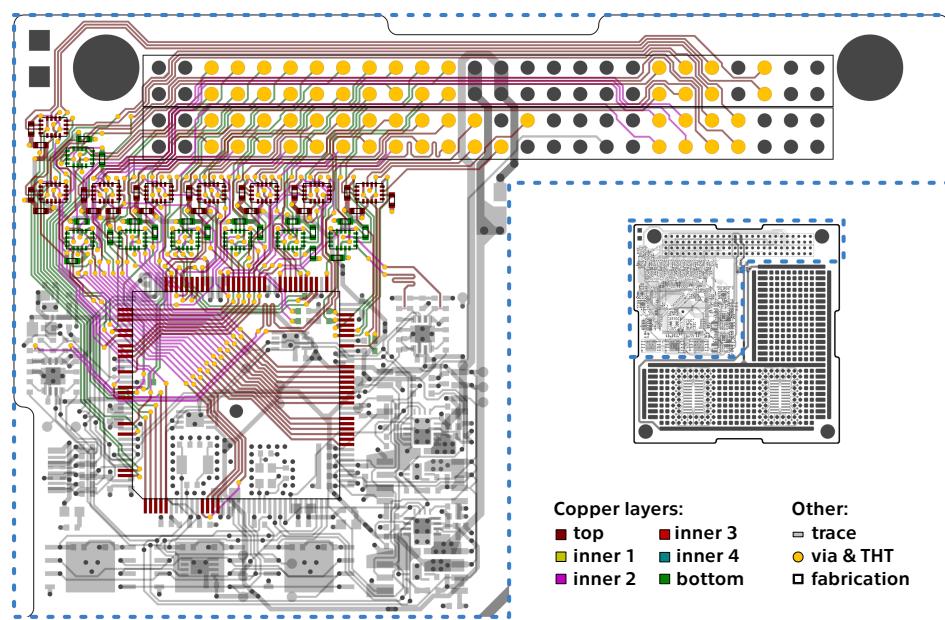
[sch:peripheralIsolators]

Figure 4.8. Schematic diagram of two peripheral isolators.

:peripheralIsolatorsPCBDesign]

4.4.2 PCB design

Location and fanout of the isolators circuitry are shown in figure 4.9. Sixty separate signals are running from the MCU pins through analog switches up to assigned pins in the PC104 header. Hence this part of the PCB was the most challenging to design. The switches are placed in two main rows, each on one side of the PCB (only two switches are not aligned). The position of every switch was determined by its assigned MCU and PC104 header pins. It took several iterations to find out the current layout. The routing network is quite dense, using all three copper signal layers. To accommodate all of the signal traces, the standard signal trace width was decreased from 200[μm] to 173[μm]. This new value was acquired as a maximal width possible to squeeze three traces between two pins of the PC104 header. To ensure CAN buses signal integrity, we addressed a length matching of its differential pairs. As a finishing step of the routing, lengths of separate CAN traces were measured and tuned with serpentine patterns.



[pcb:peripheralIsolators]

Figure 4.9. Highlighted location of peripheral isolators circuitry.

4.5 External memory

One of the OBC's important tasks is collecting and processing data from other sub-modules present in the spacecraft. As this payload and housekeeping communication might generate a wide data flow, external memory storage is usually dedicated to the MCU [11–19]. This secondary memory should be writable, preferably fast, and non-volatile (can retain the stored information after power off) to support quick buffering and permanent data storage. Commonly used semiconductor memory technologies matching the criteria are EPROM, EEPROM, FLASH, and various NVRAMs.

A great threat to memory storage is space radiation, as presented in chapter [45]. In a single event upset (SEU), the storage node charge in memory is upset due to particle strike and change its logic level [22]. This effect results in random bit-flips throughout the memory address space, corrupting the stored information. Approaches handling this damage are based on i) more durable or even rad-hard memory ICs, ii) triple modular redundancy, and iii) error detecting and correcting codes. As the last approach is a software implementation, only the first two could be used in our design.

The EPROM and EEPROM memories are not a good candidate for the OBC, as they proved to be more sensitive to gamma radiation [24]. The same applies to MRAM, as these memories are generally sensitive to single event effects (SEE) [46]. On the other hand, the cell of fairly popular FLASH devices proved to be robust against SEU because more energy is required to change the state of a bit. FLASH memories are more tolerant to radiation and are a good candidate for vital data and code [10]. F-RAM is a technology that combines the best of Flash and SRAM. It offers faster writes, high read-write cycle endurance, and very low power consumption [47]. Moreover, the F-RAM memories have excellent tolerance to radiation [10]. Considering the listed aspects of radiation effects rejection, together with speed and power consumption, we decided to include both FLASH and F-RAM memories in our OBC design. The final parameters of the external memory subsystems are listed in table 4.3.

Subsystem	Size	Max. clock	SPI connection
FLASH	3x 32[MB]	133[MHz]	SIO, DIO, QIO, QPI
F-RAM	3x 2[Mb]	25[MHz]	SIO, QIO

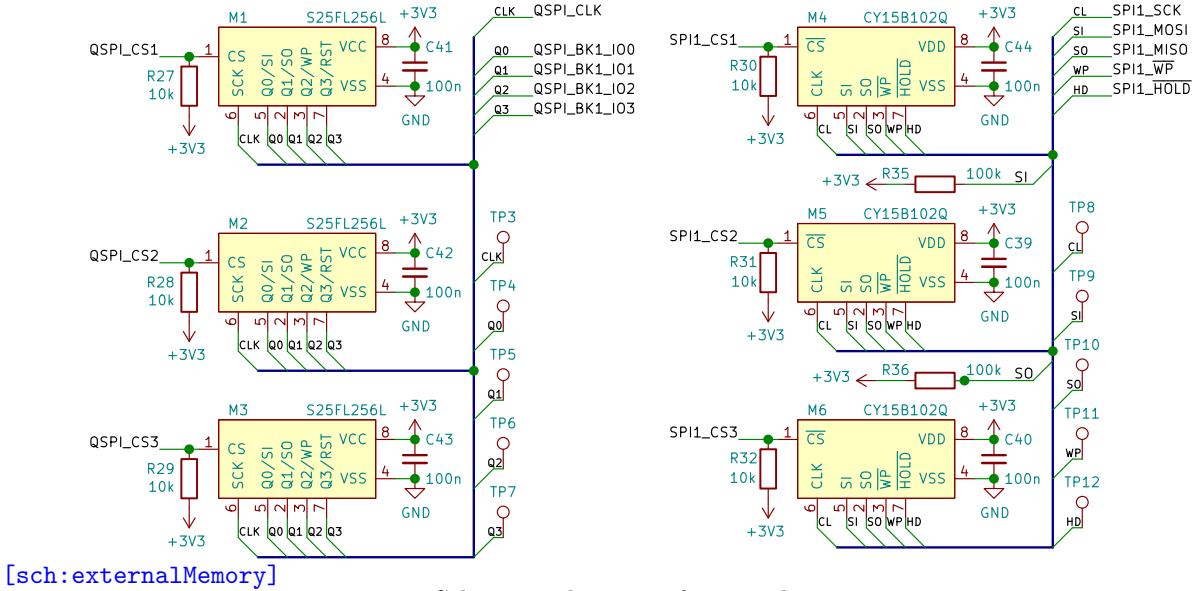
[tab:externalMemory]

Table 4.3. Parameters of the external memory subsystems.

4.5.1 Schematic design

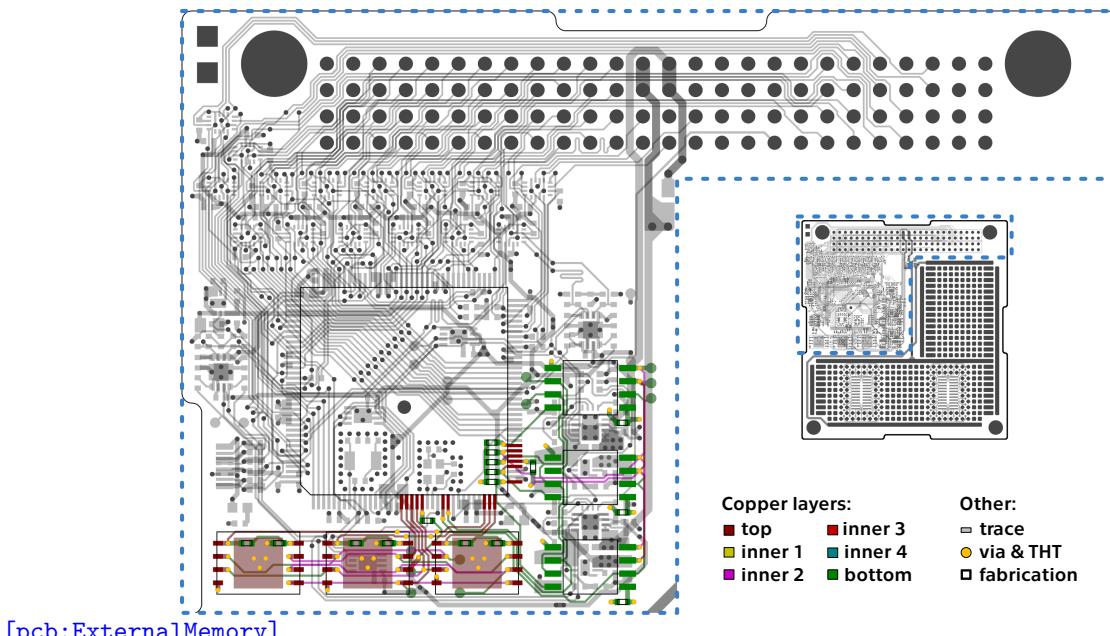
Schematic diagrams of FLASH (left) and F-RAM (right) memory subsystems are shown in figure 4.10. Triple modular redundancy is achieved in both of them by connecting three of the same memory ICs to one shared data bus. The MCU can separately enable or disable a particular IC through its chip select (*CS*) pin. External pull-up resistors added to these selection lines set the disable mode as a default one.

As a FLASH memory, the S25FL256L device was selected [48]. The SPI interface of this 32[MB] NOR memory (also available in 16[MB] version) can operate in single, dual, or four-bit wide signal lines and also supports the quad peripheral interface (QPI) commands. For the F-RAM device, we chose the CY15B102Q [49]. This 2[Mb] memory supports a dual or four-bit wide SPI interface. The 100[nF] decoupling capacitors connected to the power inputs of the memory ICs were suggested by both devices datasheets. Additionally, a test point was placed on each signal line of both SPI data buses. This addition may improve the potential debugging of these subsystems.

**Figure 4.10.** Schematic diagram of external memory circuitry.

4.5.2 PCB design

Locations and fanout of external memory circuitry are shown in figure 4.11. Devices of the FLASH subsystem are located at the top side of the PCB, below the MCU. Devices of the F-RAM subsystem are located at the bottom side of the PCB, right from the MCU. This device is the only one in the entire OBC design with a non-fine pitch package. All of the SPI test pads are placed from the bottom side of the PCB.

**Figure 4.11.** Highlighted location of external memory circuitry.

4.6 CAN bus drivers

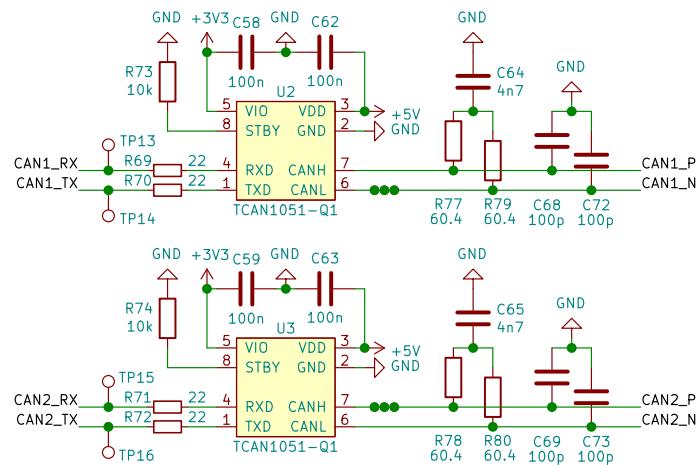
The high-speed SpaceCAN is considered a primary control and monitoring bus of a LibreCube spacecraft. Therefore it was required to ensure its full support by the

OBC. An external CAN transceiver is usually added to a microcontroller, as its internal physical layer has only limited properties or does not even exist. The separate transceiver provides a stable and reliable physical environment. In our case, the MCU's BxCAN is compatible with both 2.0A and 2.0B CAN specifications with a bit rate up to $1[\text{MB s}^{-1}]$ [31]. As the MCU's CAN drivers are equipped with the 2nd network layer only, an external transceiver implementation to our design was required.

4.6.1 Schematic design

A schematic diagram of implemented CAN driving circuitry is shown in figure 4.12. As the MCU supports two independent CAN busses, we had to accommodate each of them. For the CAN transceiver, we decided to use a TCAN1051V-Q1 device [50]. The Rx/Tx lines of the MCU are connected to the device with a $22[\Omega]$ terminating resistors. A test point is also present on each of these lines to assist potential debugging. This version of the device comes with a level shifting feature. Different voltage levels on CAN and Rx/Tx sides are supported. Since the SpaceCAN is a $5[\text{V}]$ bus and the MCU operates at $3.3[\text{V}]$, we set the device's power levels accordingly. As recommended in the device datasheet, decoupling capacitors were added to power pins. Considering the CAN bus's importance, we expect it to stay active straight from powering on the OBC. To save some complexity and MCU pins, we decided to ignore the option of controlling the device standby mode. A pull-down resistor on the *STBY* pin forces an active mode.

A well-designed CAN network usually contains a terminating resistor, filtering, and a transient & ESD protection. To correctly implement these optional features, we followed application reports [51–52]. Instead of a simple $120[\Omega]$ terminating resistor, we chose a more advanced terminating node. A difference is in added filtering as the node consists of two $60[\Omega]$ series resistors connected to a GND through a $4.7[\text{nF}]$ capacitor. Furthermore, $100[\text{pF}]$ filtering capacitors were added to signal lines. Recognizing the suggestions in the reports, we did not include any common-mode chokes or ESD protection in our design. Since our OBC is not intended to operate near heavy machinery, no extra improvement of susceptibility to electromagnetic disturbance or EMC is required.



[sch:canBusDrivers]

Figure 4.12. Schematic diagram of CAN bus driving circuitry.

4.6.2 PCB design

Location and fanout of the CAN bus driving circuitry are shown in figure 4.13. The transceivers are placed on the PCB top side in two different locations. Prioritizing the

PCB surface's optimal usage, we were unable to keep the devices in a mutual area. The transceiver circuitry layout follows suggestions in the datasheet [50] and the application report [51]. This layout is the same for both devices. As mentioned in section 4.4.2, serpentine patterns were used to match trace lengths of particular differential pairs.

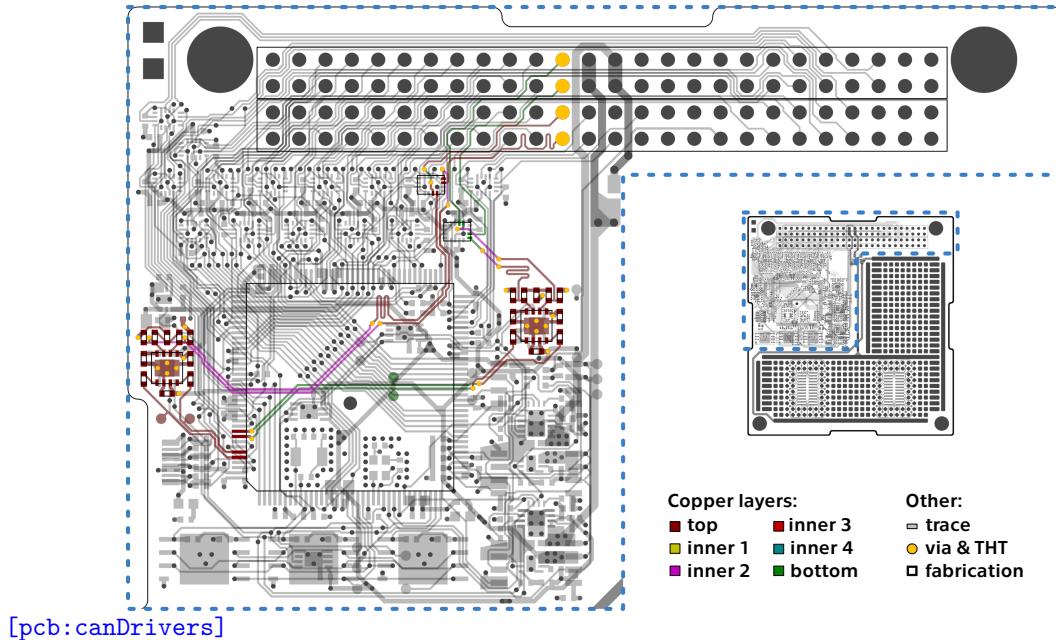


Figure 4.13. Highlighted location of CAN bus drivers circuitry.

4.7 Temperature monitoring

Temperature is a critical parameter in the space environment, and all electronic components are sensitive to its variation. Any increase in temperature may reduce their lifespan and even result in irreversible damage. Such a temperature increase can be evoked by an ambient temperature or by the component's activity. Most electronic components are designed to dissipate heat into the ambient air. This is problematic in the space due to its lack of an atmosphere. Instead, a component transfers heat into the PCB's thermal capacity.² This conduction can produce temperature gradients throughout the PCB and influence other components. Furthermore, a change in a component's temperature can indicate its malfunction. Sudden temperature increase is a common sign of a latch-up event [23]. Accordingly, the OBC temperature is a valuable part of a spacecraft telemetry and worthy of monitoring. Professional OBC manufacturers have also included temperature sensors into their designs [11–13, 16].

Standard temperature sensor technologies include integrated circuit (IC) sensors, thermistors, resistance temperature detectors (RTDs), and thermocouples. Their key features are compared in the guide to temperature sensing [53]. The IC sensors appeared to be the best choice for our design challenge. These sensors are typical for their good accuracy, small footprint, easy complexity, and excellent linearity. A processing unit can usually communicate with the IC sensors using one shared data bus and receive ready-to-use temperature data. In contrast, the implementation of the other sensor technologies requires extra analog components and circuitry. For example, amplifiers and ADCs for thermistors and thermocouples or precise current sources and ADCs

² And then dissipated into the spacecraft environment by the thermal radiation [3].

for RTDs. These non-IC technologies would also use multiple MCU pins and require additional calibration and shielding. As our goal was to design a compact PCB and a simple system, we decided to implement the IC sensors approach.

4.7.1 Schematic design

A schematic diagram of a temperature sensor network is shown in figure 4.14. After a brief survey, we selected a MCP9804 device [54]. This temperature sensor has an accuracy of $\pm 0.25[^\circ\text{C}]$ and communicates through an I²C interface. The device offers eight different I²C addresses, selected by different logic levels on three slave address pins (A_0 - A_2). Thanks to this feature, we were able to use only one I²C bus for all of the devices. The final address assignment to particular sensors is listed in table 4.4. As the temperature monitoring is continuous, we decided not to use the device's inbuild alter function. Placement of a decoupling capacitor and 10[k Ω] pull-up resistors on I²C lines were suggested by the device datasheet. It is worth mentioning that this sensor supports a low-power standby mode, accessible through a special register.

Designator	Targeted component		Slave addr.	I ² C addr.
TS1	M2	- Flash memory	000	0x18
TS2	U1	- MCU, central west	100	0x1C
TS3	EF2	- 5[V] eFuse	001	0x19
TS4	U1	- MCU, north east	110	0x1E
TS5	U3	- CAN2 driver	010	0x1A
TS6	EF1	- 3.3[V] eFuse	011	0x1B
TS7	U2	- CAN1 driver	111	0x1F

[tab:temperatureMonitoring]

Table 4.4. List of temperature sensors location and addresses.

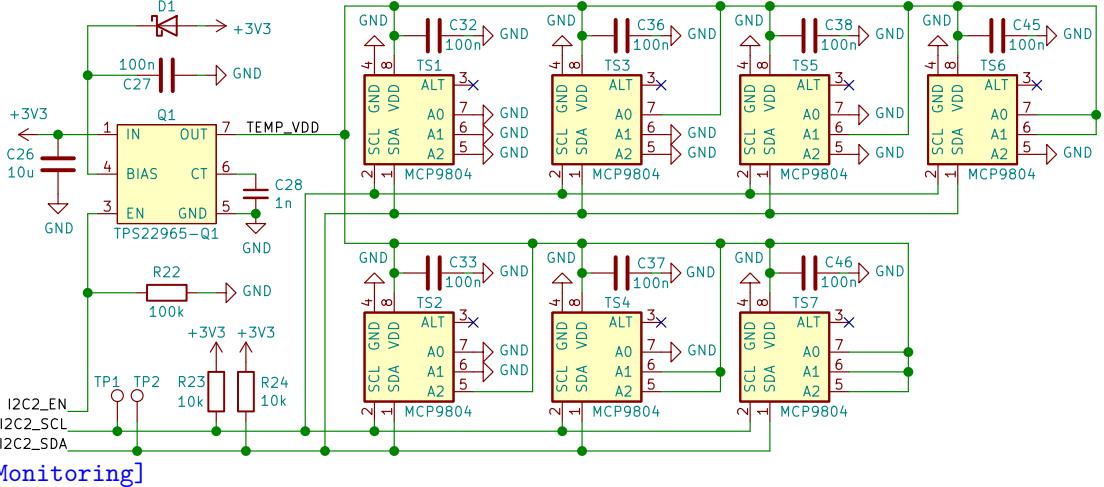
Accordingly to the survey on CubeSat electrical bus reliability [20], the I²C interface is the most likely to fail. Over half of investigated spacecrafts experienced at least one I²C lockup³. Hence it was essential to apply measures assuring the proper functionality of our I²C based temperature monitoring network. We had to implement a mechanism that can either prevent the lockup from occurring or is capable of resolving it. We chose the second option, as we consider it as a more robust and reliable. A simple but efficient approach to resolve an I²C lockup is to reset the power of all its slave devices. For this purpose, we implemented the TPS22965W-Q1 load switch in the very same configuration as we have used in the power management circuitry (subsection 4.3.1).

4.7.2 PCB design

The layout of the temperature monitoring circuitry is dependent on the other subsystems. Therefore, it had to be implemented as the very last one. Each of the IC sensors was assigned to monitor a temperature of a particular device from another subsystem. These monitored devices were carefully chosen to cover all of the OBC's most critical components. These are various ICs used in the other subsystems as they execute multiple tasks, produce most of the heat, and are vulnerable to latch-up events. A listing of the monitored devices and their assigned temperature sensors is stated in table 4.4.

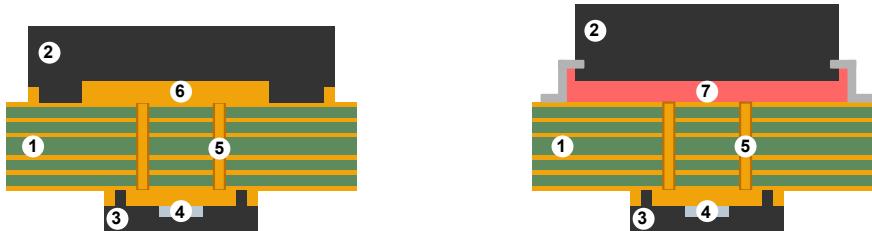
As we cannot exceed a total number of eight IC temperature sensors (MCP9804 devices) at one I²C bus, we decided to monitor only one of the three FLASH devices.

³ A continuous busy state of the I²C bus, where is the master prevented from starting a new transaction.

**Figure 4.14.** Schematic diagram of temperature monitoring circuitry.

We selected the one in the middle as a good approximation of the two remaining FLASH devices. None of the three F-ram devices is monitored directly as the opposite side of the PCB in their location contains a dense layout of the power management circuitry. However, the F-ram devices are neighbored by three temperature sensors: TS5, TS6, and TS3. Measurements obtained from these sensors should be sufficient to monitor the F-ram devices. The MCU contains an inbuilt temperature sensor suitable only for applications that detect temperature changes only [31]. We decided to monitor the MCU with a pair of IC sensors as we prefer to measure the absolute temperature.

To ensure correct temperature measurement, we have to create a sufficient thermal bridge between the temperature sensor and its targeted device. A common approach is to place the sensor on the other side of the PCB, right opposite the device. A thermal bridge is then created using a set of PCB vias. This method is recommended and described in the temperature sensors guideline for SMDs [55]. Its illustration for our use case is shown in figure 4.15. It is worth mentioning that the added vias help dissipate the heat into the PCB and are usually required by the device's datasheet.

**Figure 4.15.** Illustration of a thermal bridge between the temperature sensor and WSON package (left) or LQFP package (right). Legend: ① PCB, ② targeted device, ③ IC temperature sensor, ④ measurement die, ⑤ PCB via, ⑥ thermal pad, ⑦ epoxy resin.

Location and fanout of the temperature monitoring circuitry are shown in figure 4.16. All IC sensors are placed at the bottom side of the PCB, directly under their targeted devices. The load switch is located at the PCB's west-central part. The switch itself and most of its auxiliary components are placed on the top side of the PCB. The I²C bus signal traces and separate power bus runs between all of the sensors.

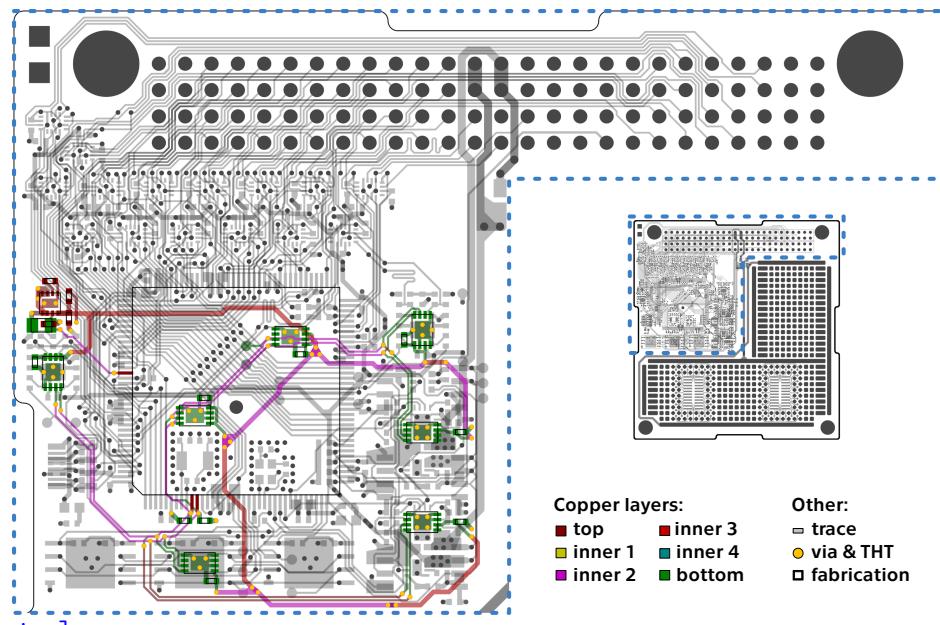


Figure 4.16. Highlighted location of temperature monitoring circuitry.

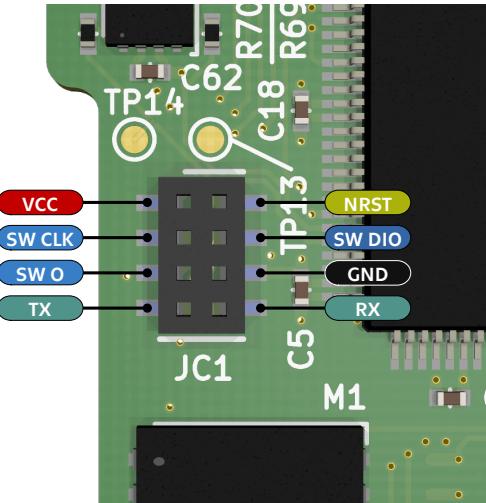
4.8 Debug connector

A host/target interface is required to program or debug the MCU. This interface is made of three components. A hardware debug tool, an SWJ connector and a cable connecting the host to the debug tool [32]. As the SWJ connector is a part of the target board, we had to implement it into our PCB design. The MCU has an embedded SWJ-DP interface that enables either a serial wire debug (SWD) or a JTAG probe to be connected to the target [31]. Considering that the SWD is required by the ST-LINK, is performed using two pins (five needed for the JTAG), and is the preferred debug port [56], we decided to implement the SWD only. This decision slightly decreased the PCB complexity and freed some MCU pins for further usage. Also, the Sierra Board was not created with a mass production intent, the primary use case of the JTAG debug.

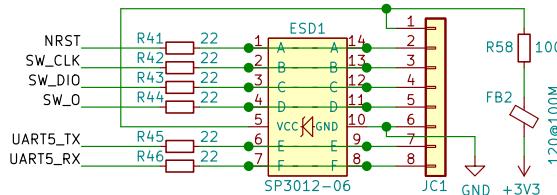
The implemented SWD connector includes not only the two mandatory SWDIO and SWCLK pins. An NRST signal is also presented, enabling a connection under reset. This signal is required to take back the control of the board when it is not responding [56]. Also, a serial wire output (SWO) is available, providing an asynchronous serial communication channel. It has to be used in combination with a serial wire viewer (SWV) [56]. Additionally, one UART channel is also presented, providing a convenient communication option for the development and testing process. Pin assignment of the ST-LINK compatible connector of the Board Sierra is shown in figure 4.17.

4.8.1 Schematic design

The programming connector is intended to be in direct touch with external hardware and human manipulation. As suggested in the application report [23], we decided to protect the associated signals against the ESD. A TVS diode array SP3012-06 [57] was selected, as it provides the exact pin count as needed. All of the debugging MCU signals were routed through this low-capacitance ESD protection device. A schematic diagram of the circuitry is shown in picture 4.18. Additionally, a $22[\Omega]$ terminating resistor is connected in series to each signal. A $100[\Omega]$ resistor and a ferrite bead are connected to



[mod:programPort]

Figure 4.17. Debug connector pinout.

[sch:programPort]

Figure 4.18. Schematic diagram of debug connector circuitry.

the connector's power pin. Their purpose is to limit the transient current and suppresses high-frequency electronic noise that may affect the OBC from an attached debugger.

4.8.2 PCB design

Location and fanout of the debug connector circuitry are shown in figure 4.19. A small 4x2 female header with a 1.27[mm] pitch was selected as a debug connector. Its placement near the edge of the PCB in a cutout area should improve its accessibility and cable management. This SMD connector is located on the PCB's top side, while the remaining electronics parts are placed below it, from the bottom side of the PCB.

4.9 Payload sector

As mentioned in section 3.3.2, only one-fourth of the entire PCB surface is occupied by the OBC circuitry. The remaining space is meant to be used as a user-defined payload sector. After discussing with the VST supervisors, we utilized this sector as a universal prototyping board. We implemented this feature to illustrate the purpose of this sector - to accommodate any user-specific circuitry. We expect that a future user of the Board Sierra would replace the universal board with his mission-specific circuitry.

The design of the universal prototyping board is visible in figures 8.2 and 8.3. Its main feature is a grid of 0.85[mm] wide THT holes with a plating utilized for an SMD soldering. This THT array is surrounded and divided by power bus rails, providing 5[V], 3.3[V], and GND connections. This power delivery is sourced directly from the main PC104 header, bypassing the power management circuitry. However, each of the rails is fused by a 1206 packaged ceramic fuse. In the lower part of the prototyping board,

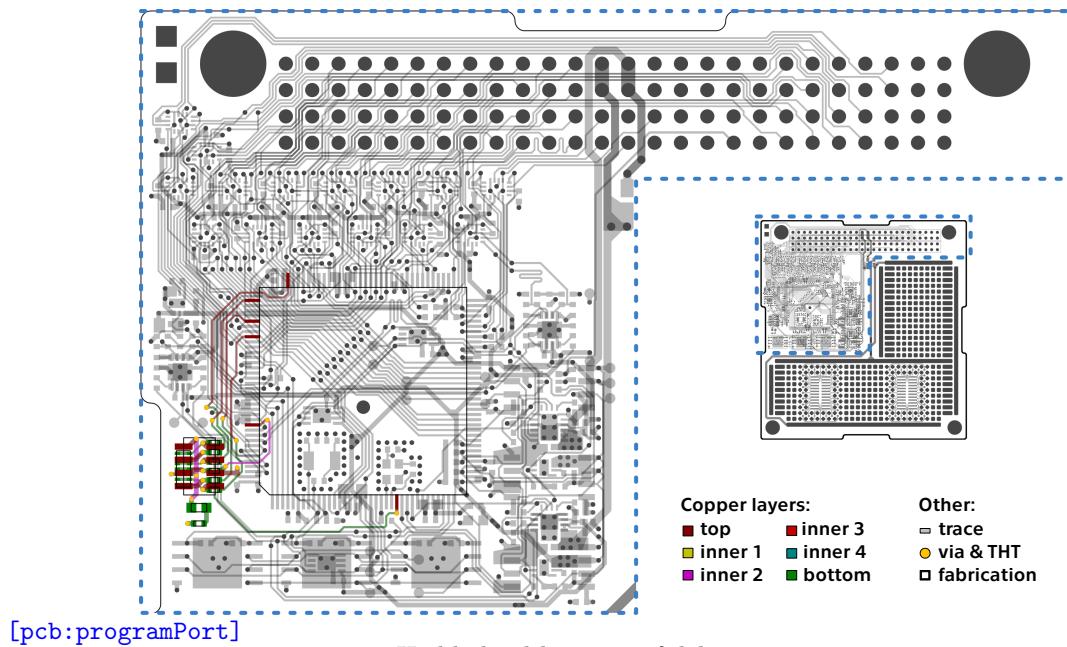


Figure 4.19. Highlighted location of debug connector circuitry.

two universal SO-24 footprints are available on each PCB side for rapid prototyping. Every pad of these footprints is routed to a small circular pad for easier soldering.

[chap:boardDelta]

Chapter 5

Board Delta

5.1 Circuit modification

5.2 PCB modification

Chapter 6

Element Foxtrot

- 6.1 PCB specifications**
- 6.2 Power input handling**
 - 6.2.1 Ordinary power source**
 - 6.2.2 USB-C power source**
- 6.3 Voltage conversion**
- 6.4 PC104 modules slots**

Chapter 7

Board Sierra - testing

- 7.1 Testing software**
- 7.2 Radiation testing**
- 7.3 Environmental testing**

Chapter 8

Conclusion

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Appendix A

Thesis Assignment



BACHELOR'S THESIS ASSIGNMENT

I. Personal and study details

Student's name: **Geib Filip** Personal ID number: **483567**
Faculty / Institute: **Faculty of Electrical Engineering**
Department / Institute: **Department of Measurement**
Study program: **Cybernetics and Robotics**

II. Bachelor's thesis details

Bachelor's thesis title in English:

On-board computer for PC104 format CubeSats

Bachelor's thesis title in Czech:

Palubní počítač pro CubeSaty formátu PC104

Guidelines:

- Design a concept of an STM32 based on-board computer for PC104 frame based CubeSats.
- Implement redundancy for the critical components to improve reliability of the design.
- Construct the device and conduct testing of the whole system, e.g. using a flatsat platform.
- Concentrate on providing detailed and accurate documentation of the system.

Bibliography / sources:

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Name and workplace of bachelor's thesis supervisor:

Ing. Vojtěch Petrucha, Ph.D., 13138

Name and workplace of second bachelor's thesis supervisor or consultant:

Date of bachelor's thesis assignment: **13.01.2021** Deadline for bachelor thesis submission: _____

Assignment valid until:
by the end of summer semester 2021/2022

Ing. Vojtěch Petrucha, Ph.D.
Supervisor's signature

Head of department's signature

prof. Mgr. Petr Páta, Ph.D.
Dean's signature

III. Assignment receipt

The student acknowledges that the bachelor's thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the bachelor's thesis, the author must state the names of consultants and include a list of references.

Date of assignment receipt

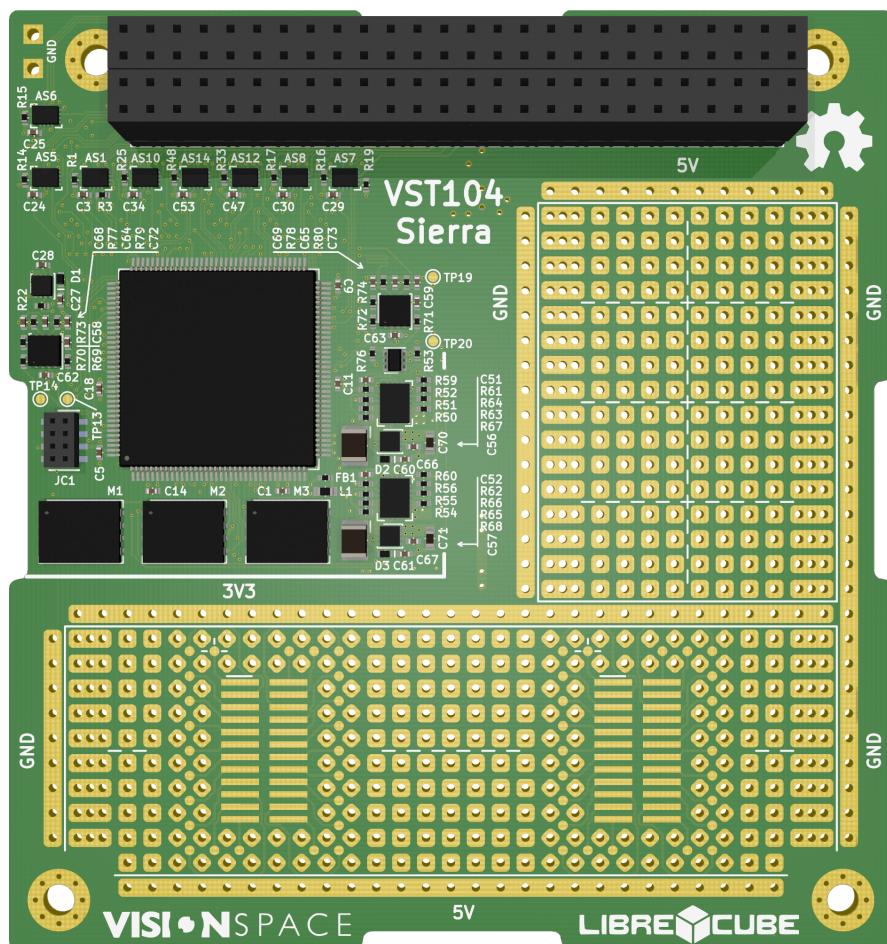
Student's signature

[app:thesisAssignment]

Figure 8.1. Assignment of this bachelor's thesis.

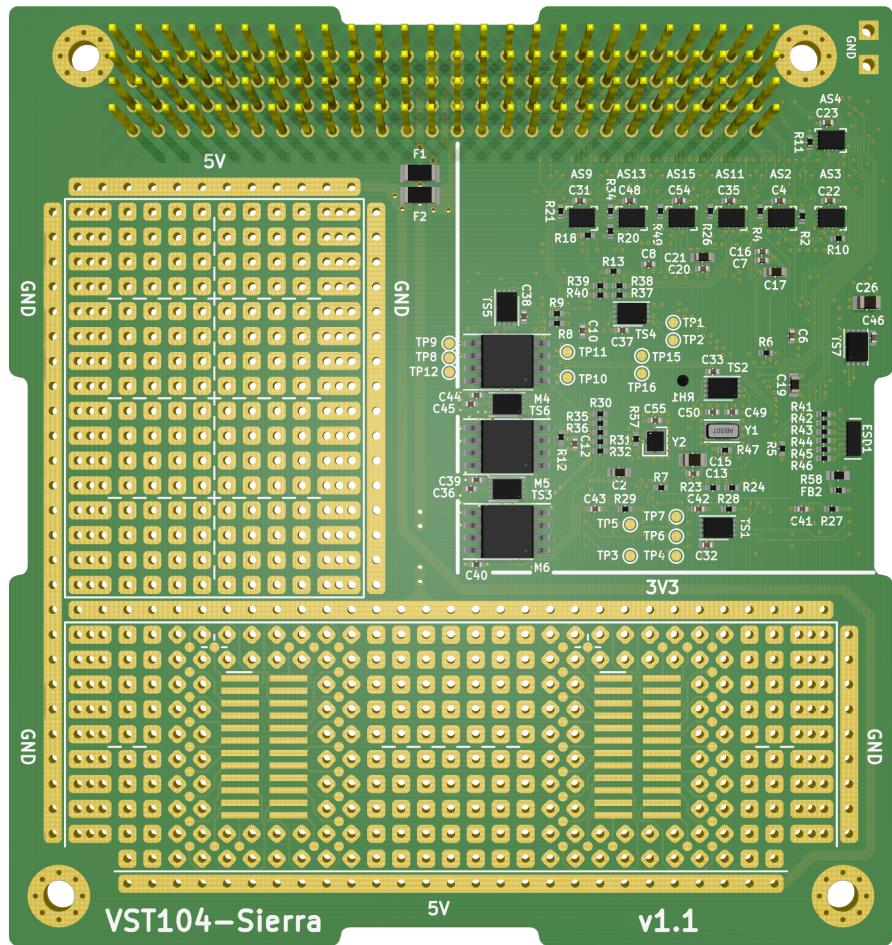
Appendix B

Board Sierra



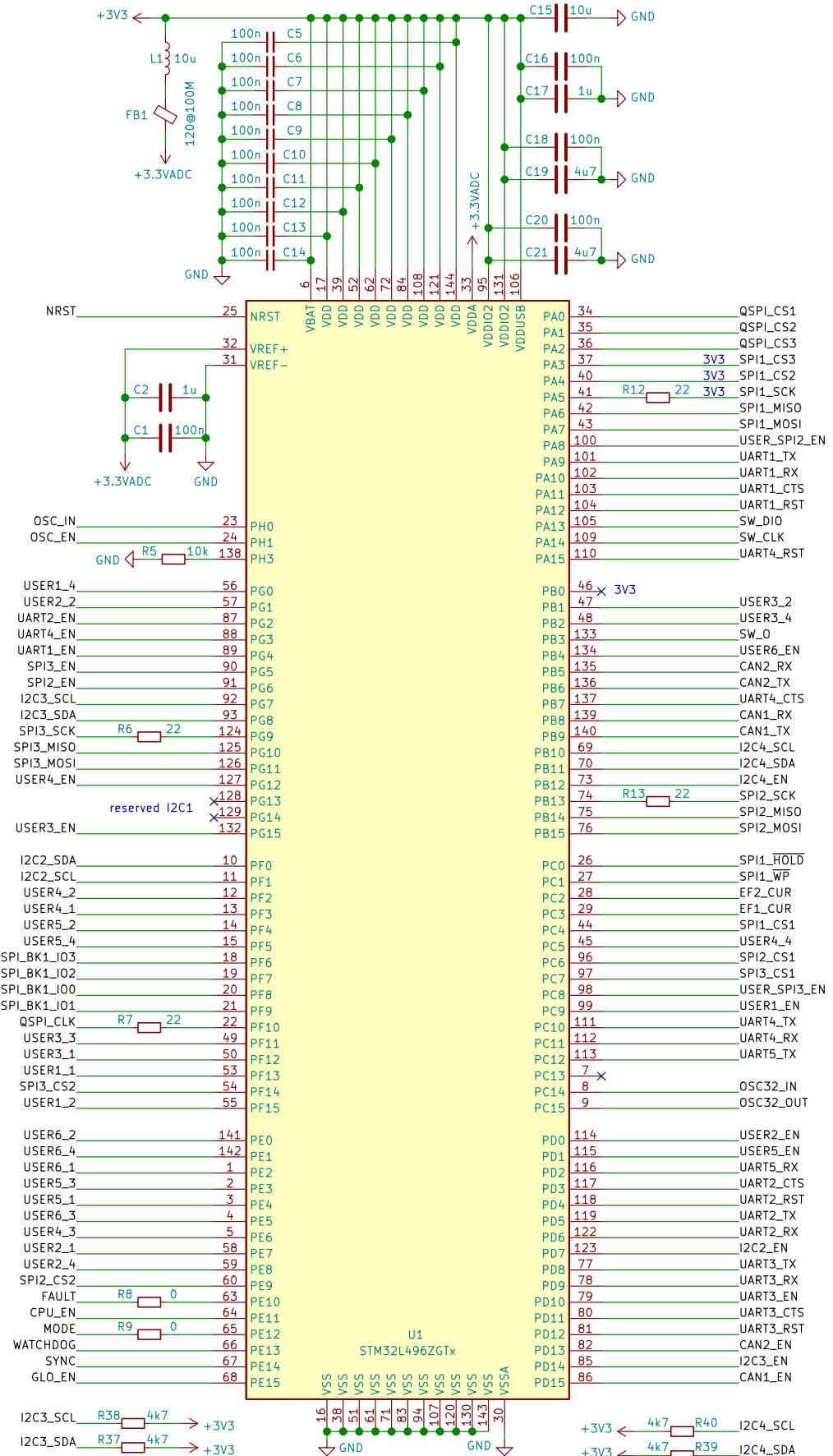
[app_vis:sierraTop]

Figure 8.2. Visualization of the Board Sierra captured from its top side.



[app_vis:sierraBottom]

Figure 8.3. Visualization of the Board Sierra captured from its bottom side.



[app_sch:microcontroller]

Figure 8.4. Schematic diagram of microcontroller and its auxiliaries.

Appendix C

Additional materials

Designator	3.3[V] current [mA]			5[V] current [mA]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
AS[1-15]	-	0.024	0.060			
EF[1,2]	0.140	0.210	0.300			
LG1	-	0.100	4			
M[1-3]	10	-	40			
M[4-6]	-	-	5			
TS[1-7]	-	0.200	0.400			
U1	-	-	-			
U[2,3]	-	40	70			
Y1	-	-	-			
Y2	-	4.0	4.8			

[tab:componentsConsumption]

Table 8.1. List of components power consumption.

Designator	Certified part no.	Uncertified part no.	Difference
LG1	74LVC1G11GW-Q100	74LVC1G11GW	auto.
M[1-3]	S25FL256LAGNFI	S25FL256LAGNFI S25FL256LDPNFI	temp. temp., speed
TS[1-7]	MCP9804x-E/MC	MCP9808x-E/MC	accuracy
Q[1-3]	TPS22965W-Q1	TPS22965-Q1 TPS22975	temp. temp., auto.

[tab:uncertifiedParts]

Table 8.2. List of available uncertified variants to some of the OBCs electronics components. Legend: auto. - missing AEC certification, temp. - shrink operational temperature range, speed - decreased frequency, accuracy - decreased accuracy of measurements.

Requests for correction