CZECH TECHNICAL
UNIVERSITY
IN PRAGUE

F3

Faculty of Electrical Engineering
Department of Measurement

Bachelor's Thesis

On-board computer for PC104 format CubeSats

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Cybernetics and Robotics

February 2021
https://github.com/visionspacetec/VST104
Supervisor: Ing. Vojtěch Petrucha, Ph.D.

Draft: 22. 2. 2021

Acknowledgement / Declaration

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In Prague on February 25, 1999

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Abstrakt / Abstract

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Kľúčové slová: CubeSat; PC104; OBC; hardvér; PCB dizajn; schémy.

Preklad titulu: Palubný počítač pre CubeSaty formátu PC104

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Keywords: CubeSat; PC104; OBC; hardware; PCB design; schematics.

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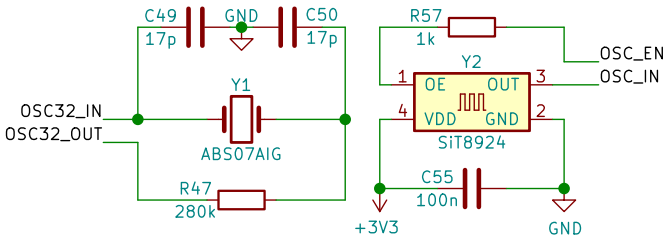
4.1.1 Microcontroller

4.1.2 External clock sources

The MCU has two internal RC oscillators that can be used to drive the system and auxiliary clocks [1]. These internal oscillators have a lower frequency stability and a higher temperature dependency than the external ones [2]. To ensure clock reliability in the harsh space environment, we had to implement external clock sources.

A $4 - 48$[MHz] HSE oscillator can drive the system clock. Supported types are crystal, ceramic resonator, or silicone oscillator [1]. The last option seems to be the best as it is insensitive to EMI and vibration. The only downside is its slightly lower temperature rejection [3]. We chose the SiT8924B, a 26[MHz] silicon MEMS oscillator [4]. Accordingly to the clock configuration tool of the stm32cube software, we can reach various system clock frequencies up to 78[MHz] (the max. is 80[MHz] [1]). The circuitry follows the HSE datasheet [4] and is shown on the right side of figure 4.1. The HSE output OSE_IN can be enabled or disabled by the binary OSC_EN signal.



[fig:clockSource]

Figure 4.1. Schematic diagram of external clock sources.

A 32.768[kHz] LSE oscillator can drive the RTC, hardware auto calibration, or other timing functions. Table 7 in [5] recommends individual crystal resonators for this specific purpose with STM32 MCUs. After a consideration of these options, we decided to use the ABS07AIG ceramic base crystal [6]. The LSE oscillator circuitry is based on the reference design in figure 5 in [5]. To achieve a stable frequency of this so-called Pierce oscillator, it is required to determine the values of two load capacitors C_{L1}, C_{L2} and an external resistor R_{Ext}. This can be obtained using the equations

$$C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + C_S \quad \wedge \quad C_{L1} = C_{L2}, \tag{1}$$

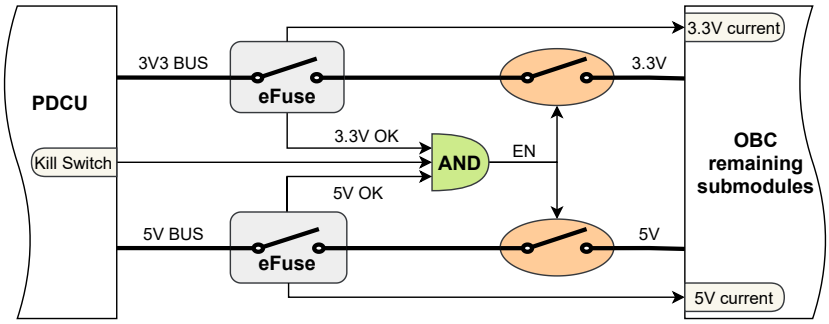
$$R_{Ext} = \frac{1}{2\pi f C_{L2}}, \tag{2}$$

where C_L is the crystal load capacitance, f is the crystal oscillation frequency and C_S is the stray capacitance [5]. Values of C_L and f are listed in the crystal datasheet [6]. We can assume as a rule of thumb, that $C_S = 4$[pF]. The final LSE circuitry with computed values of the components is shown on the left side of figure 4.1.

4.1.3 Power management

The electrical power and distribution subsystem is known to be the most vital subsystem of a spacecraft. Its reliability and error handling should be ensured by the PDCU. However, it is a good engineering practice by professional OBCs manufacturers to include an additional power control circuitry to their designs [7–14]. Our OBC requires 3.3[V] and [5V] power inputs from the main power buses. In the case of their malfunction, it is our responsibility to sense it and power down the OBC.

A functional diagram of the implemented power management is shown in figure 4.2. The OBC is connected to each power bus through an electronic fuse. This device continuously monitors the bus for events of under-voltage, over-voltage, and over-current[1]. As a response to such an event, the eFuse will switch into high impedance and pull down specific input of an AND logic gate. This gate simultaneously controls two load switches, one for each power line. This approach ensures that a fault on one power bus will result in a high impedance of both OBC power inputs. It also eliminates the risk of a death loop, a state where a reset of eFuses is not possible as they are switching each other off. Added benefits of this design are simple current measurements (using the eFuse analog output) and a kill switch integration into the AND logic gate.



[fig:powerManagement]

Figure 4.2. Functional diagram of power management circuitry.

The final schematic diagram of power management circuitry is shown in figure 7.2. The most important part of this design is the eFuse, as it covers all of the power control features. We decided to use the TPS25940-Q1 device [15]. Custom monitoring thresholds values can be set following the typical application schematic in figure $10-1$ in [15]. This was achieved by connecting specific resistors to the device, with values calculated using the TPS2594x design calculation tool [16]. As the logic AND gate, we chose the 74LVC1G11-Q100 [17]. This device is designed to operate in a mixed 3.3V and 5V environment, what corresponds with our application. The last important component is the load switch. In our case, the TPS22965W-Q1 with an inbuilt output discharge function [18]. For a correct operation of the switch, the VBIAS pin should stay saturated for a while after disconnecting the VIN voltage. We achieved this behavior by charging a capacitor connected to the VBIAS from the VIN through a Schottky diode. Four reservoir capacitors are placed on both sides of the load switches, following

[1] This is a crucial feature in handling and resolving a latch-up event.

the suggestions in [15, 18]. Nominal logic values of all switching signals are set by pull-up or pull-down resistors. The summary of the final power management ratings is listed in table 4.3. These values were chosen considering the power requirements of the remaining OBC components and are a subject of change by a potential user.

Power input	Parameter	Min	Typ	Max	Unit
3V3 BUS	voltage	2.9	3.3	3.5	V
	current	0.0	-	1.2	A
5V BUS	voltage	4.6	5.0	5.4	V
	current	0.0	-	1.2	A

[tab:powerManagement]

Figure 4.3. OBC power rating. Value out of range will cause a protective shutdown.

4.1.4 Peripheral isolators

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4.1.6 CAN bus drivers

4.1.7 Temperature sensing

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5.1.2 USB-C power source

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Chapter 6
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6.1 Testing software

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Chapter 7
Conclusion

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Appendix A
Thesis Assignment

CTU CZECH TECHNICAL UNIVERSITY IN PRAGUE

BACHELOR'S THESIS ASSIGNMENT

I. Personal and study details

Student's name: **Geib Filip** Personal ID number: **483567**

Faculty / Institute: **Faculty of Electrical Engineering**

Department / Institute: **Department of Measurement**

Study program: **Cybernetics and Robotics**

II. Bachelor's thesis details

Bachelor's thesis title in English:

On-board computer for PC104 format CubeSats

Bachelor's thesis title in Czech:

Palubní počítač pro CubeSaty formátu PC104

Guidelines:

- Design a concept of an STM32 based on-board computer for PC104 frame based CubeSats.
- Implement redundancy for the critical components to improve reliability of the design.
- Construct the device and conduct testing of the whole system, e.g. using a flatsat platform.
- Concentrate on providing detailed and accurate documentation of the system.

Bibliography / sources:

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[4] Dogan Ibrahim: "ARM-Based Microcontroller Projects Using Mbed", Elsevier Science & Technology, 2019

Name and workplace of bachelor's thesis supervisor:

Ing. Vojtěch Petrucha, Ph.D., 13138

Name and workplace of second bachelor's thesis supervisor or consultant:

Date of bachelor's thesis assignment: **13.01.2021** Deadline for bachelor thesis submission: _____

Assignment valid until:
by the end of summer semester 2021/2022

Ing. Vojtěch Petrucha, Ph.D.	Head of department's signature	prof. Mgr. Petr Páta, Ph.D.
Supervisor's signature		Dean's signature

III. Assignment receipt

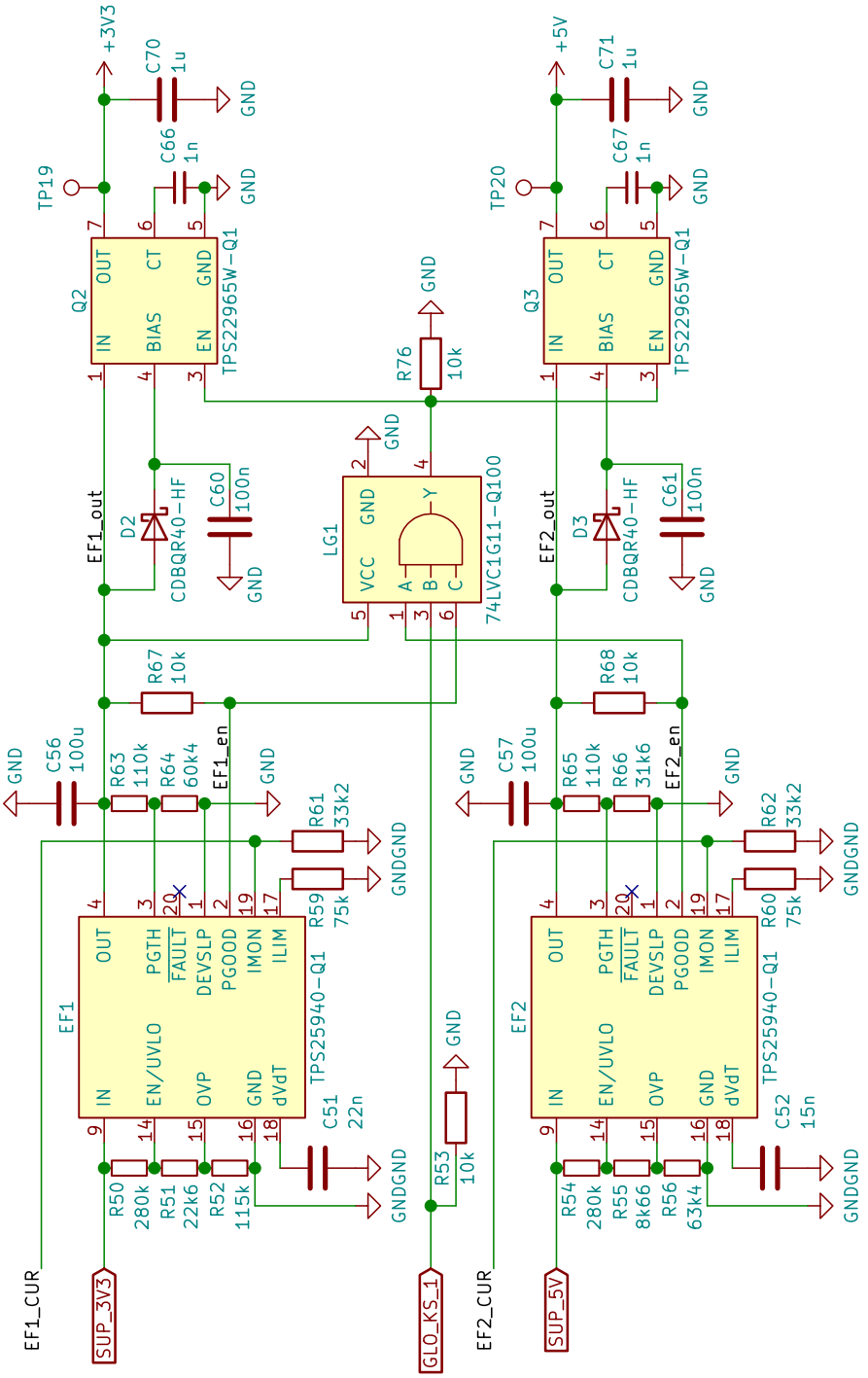
The student acknowledges that the bachelor's thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the bachelor's thesis, the author must state the names of consultants and include a list of references.

Date of assignment receipt	Student's signature

[app:thesisAssignment]

Figure 7.1. Assignment of this bachelor's thesis.

Appendix B
Schematic diagrams



[app:powerManagement]

Figure 7.2. Schematic diagram of power management circuitry.

Requests for correction