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UNIVERSITY
IN PRAGUE

F3

**Faculty of Electrical Engineering
Department of Measurement**

Bachelor's Thesis

On-board computer for PC104 format CubeSats

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Cybernetics and Robotics

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<https://github.com/visionspacetec/VST104>
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Draft: 31. 3. 2021

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Abstrakt / Abstract

Klúčové slová: CubeSat; PC104; OBC; hardvér; PCB dizajn; schémy.

Preklad titulu: Palubný počítač pre CubeSaty formátu PC104

Keywords: CubeSat; PC104; OBC; hardware; PCB design; schematics.

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[chap:intro]

Chapter 1

Introduction

Chapter 2

Board Sierra - description

2.1 CubeSat concept

2.2 OBC requirements

2.2.1 Radiation and redundancy

Occasionally traveling through weaker parts of the Earth's magnetic field and not shielded by the Earth's atmosphere, the CubeSats have to operate in an environment full of radiation. A direct hit of a high-energy particle might have serious consequences for OBC functionality. These include transistor gate ruptures, memory bit flips, software upsets, or latch-ups. A proper strategy must be taken to increase the OBC durability and ability to handle such an error, resulting in maximizing a possible mission life.

One approach is to use special radiation-hardened components. This strategy is typical for professional and more expensive satellites than the CubeSats. These components are usually bigger, more costly, and have less functionality than ordinary COTS.

Considering the size and budget requirements of our OBC, we chose to implement another option. Instead of the previously mentioned physical hardening technique, a logical one was realized. The OBC hosts many schematic design-related features ensuring the proper handling of any radiation-related event. These include: i) over-current sensing power management, ii) separate peripheral isolators, iii) full high-impedance mode requested by the higher logic, iv) triple-redundant memories, v) multiple temperature sensors. A fully double-redundant OBC is presented in chapter ??.

2.2.2 Capabilities and features

[1–9]

Having in mind the expectations of the VST supervisors, features common for OBCs by different professional manufacturers, and design requirements implied by the radiation, we created and implemented the following list of desired OBC's features:

- **Microcontroller:**
- **External clock sources:**
- **Robust power management:**
- **Isolation of the peripherals:**
- **Redundant external memory:**
- **CAN bus peripherals:**
- **Temperature monitoring:**
- **Maximal payload sector:**

2.2.3 Components certification

[chap:componentsSelection]

2.2.4 Components selection

After listing all of the technical requirements for a specific electronic part, we had to chose a particular component. As there are usually multiple similar components from various manufacturers, we had to use additional criteriums for the selection process.

As this OBC module is not primarily designed for an actual space flight (explained in chapter ??), an individual component's price is not negligible. With a lower overall cost of the OBC, a broader project expansion in the LibreCube community can be achieved. Thus components with sufficient attributes but lower price were favored.

Another criterium in the component selection was the available PCB surface. As a result of maximizing the payload sector of the PC104 module, the actual OBC subsystem area was significantly decreased. Therefore the components of smaller dimensions available in fine-pitch packages (e.g. SSOP or QFN) were preferred. After researching the technical capabilities and related costs of PCB manufacturers, we decided not to use the BGA package components. Their significantly small footprints would require more precise fanout, resulting in increased manufacturing difficulty and price.

Different components are available from various distributors, which can prolong the assembling process. We chose to use Mouser Electronics for purchasing the components. Therefore the availability of a specific component in this store was also a selection factor. This decision was influenced by the VST supervisors and previous experiences.

2.3 PCI104 standard

2.3.1 Mechanical specification

2.3.2 Main header pinout

2.4 PCB design and assembly

2.4.1 PCB specifications

2.4.2 Routing and fanout

Chapter 3

Board Sierra - submodules

3.1 Microcontroller

The processing unit is the most important part of the OBC. Professional designs use a wide variety of different instruction set architectures [1, 3, 5–6, 9]. However, the ARM architecture seems to be more popular [2, 7–8, 4]. This architecture is known for its good multiprocessing support, low power consumption, affordable pricing, and broad spectrum of existing applications. Considering these benefits and influenced by the LibreCube and TUDSaT, our VST supervisors decided to pick an STM32 MCU.

Our task was to choose a particular model of this 32-bit, Arm and Cortex-M based MCU. Aiming rather for a low-power than high-performance characteristics, we decided to select an L series. Particularly the L4 series as it combines the largest flash memory size with the highest number of general-purpose input/output pins (GPIOs) [10]. Although, only one device from the L4 series is equipped with two CAN bus channels. As the presence of a second bus is crucial for our double-redundant approach, the STM32L496xx option was selected. This family comes in six different packages. Avoiding all of the BGA-like ones (as described in chapter 2.2.4) narrows the selection to Zx, Vx, and Rx variants. The Zx is the most capable one in terms of flash size and GPIO count. Therefore the STM32L496ZG (where G stands for extended operating temperature range) was our final choice [11]. From now on, we will refer to this particular device as the MCU. Some of its key characteristics are listed in table 3.1.

Max. frequency	80 [MHz]	SPI	3
Flash memory	1 [MB]	I2C	4
Static RAM	320 [kB]	UART	5
Comparators	2	CAN	2
Op. amplifiers	2	GPIO	115
Temperature	–40 to 125 [°C]	DAC	2

[tab:microcontroller]

Table 3.1. Highlighted characteristics of the STM32L496ZG microcontroller [11].

3.1.1 Schematic design

The MCU pin assignment was continuously changing during the entire process of OBC schematic and PCB design. Its final state is presented in figure 7.2. We attempted to maximize the number of user-free GPIOs with added functionalities such as ADC or PWM while keeping the fanout manageable. A significant help during this process was the CubeMX tool of the STM32CubeIDE, visualizing all of the pinout combinations with a specific functionality. Each of the 3.3[V] tolerant pins was used only for the internal circuitry, resulting in a fully 5[V] tolerant main PC104 header connection.

A significant number of filtering and reservoir capacitors is needed to ensure the proper MCU functionality. The assignment of correct capacitors to required MCU pins

was pretty straightforward, following the device datasheet [11] and STM32L4 hardware development application note [12]. Furthermore, a $10[\mu\text{H}]$ choke and $120[\Omega]$ at $100[\text{MHz}]$ ferrite bead were placed in series with the analog power input. This LC filter supported by the bead should effectively eliminate both low and high-frequency interference.

The clock and data lines of both I²C busses are equipped with standard $4.7[\text{k}\Omega]$ resistors. Multiple $22[\Omega]$ resistors were placed in series with high-speed clock signals of the SPI interface. Two $0[\Omega]$ resistors are present on *FAULT* and *MODE* lines to facilitate an optional hardware isolation. A $10[\text{k}\Omega]$ resistor at *PH3* is suggested by [12].

3.1.2 PCB design

Location and fanout of the MCU are shown in figure 3.1. The MCU is placed on the PCB top side, covering most of the non-payload area. This big footprint of a LQFP144 package (approximately $2 \times 2[\text{cm}]$) is a consequence of avoiding the BGA packages while still trying to keep the pin count high. All of the capacitors were placed as close to their assigned pins as possible. In some cases, it was necessary to use the bottom side of the PCB. The same approach was applied to all of the resistors.

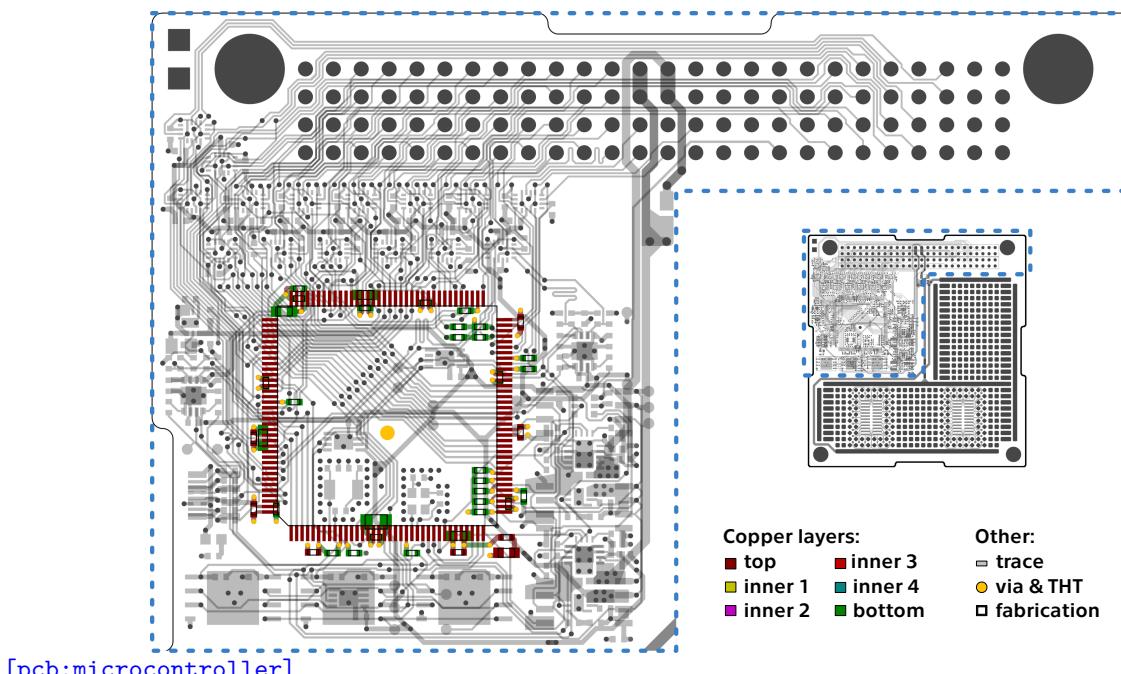


Figure 3.1. Highlighted location of microcontroller circuitry.

3.2 External clock sources

Proper timing and synchronization are the key features while dealing with high-speed data busses, ADCs, or other precise applications. The MCU is equipped with two internal RC oscillators that can be used to drive a master system clock and other auxiliary clocks [11]. These internal oscillators generally have a significantly lower frequency stability, a higher temperature dependency, and smaller overall accuracy than their external equivalents [13]. Therefore, to increase the clock precision and reliability in the harsh space environment, we had to implement external clock sources.

A $4 - 48[\text{MHz}]$ high speed external oscillator (HSE) can drive the system clock. Supported types are crystal, ceramic resonator, or silicone oscillator [11]. The last option seems to be the best as it is insensitive to electromagnetic interference (EMI) and

vibration. The only downside is its slightly lower temperature rejection [14]. We chose the SiT8924B, a 26[MHz] silicon microelectromechanical system (MEMS) oscillator [15]. Accordingly to the clock configuration tool of the stm32cube software, we can reach various system clock and auxiliary clocks frequencies up to 78[MHz] (maximum is 80[MHz] [11]). This is done using the phase-locked loop (PLL) clock generation.

A 32.768[kHz] low speed external oscillator (LSE) can drive the real time clock (RTC), hardware auto calibration, or other timing functions [11]. Table 7 in [16] recommends individual crystal resonators for combination with STM32 MCUs. After a consideration of these options, we decided to pick the ABS07AIG ceramic base crystal [17].

3.2.1 Schematic design

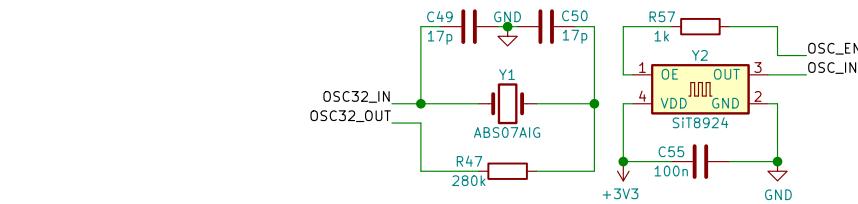
The HSE circuitry follows the oscillator datasheet [15] and is shown on the right side of figure 3.2. Only a decoupling capacitor and a terminator resistor are required. The clock output *OSE_IN* can be enabled or disabled by the binary *OSC_EN* signal.

The LSE circuitry is based on a reference design in the oscillator design guide [16]. To achieve a stable frequency of this Pierce oscillator, it is required to find the values of load capacitors C_{L1} , C_{L2} and external resistor R_E . This can be done using equations

$$C_L = \frac{C_{L1}C_{L2}}{C_{L1} + C_{L2}} + C_S \quad \wedge \quad C_{L1} = C_{L2}, \quad (1)$$

$$R_E = \frac{1}{2\pi f C_{L2}}, \quad (2)$$

where C_L is the crystal load capacitance, f is the crystal oscillation frequency and C_S is the stray capacitance [16]. Values of C_L and f are listed in the crystal datasheet [17]. We can assume as a rule of thumb, that $C_S = 4[\mu F]$. The final LSE circuitry with computed values of the components is shown on the left side of figure 3.2.

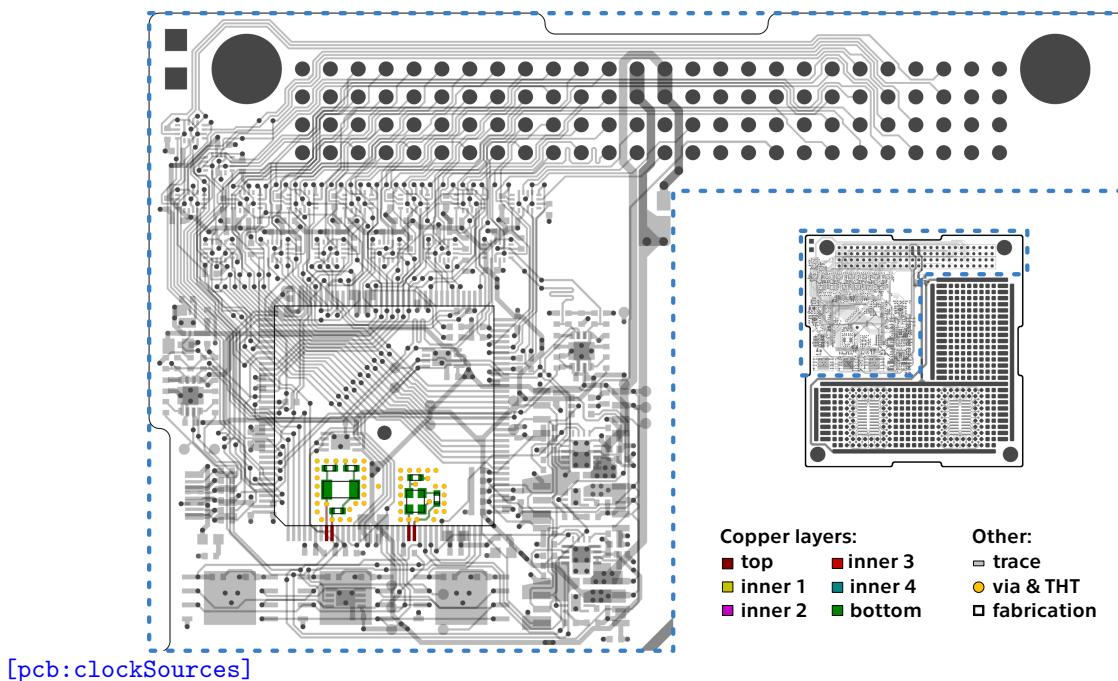


[sch:clockSources]

Figure 3.2. Schematic diagram of external clock sources.

3.2.2 PCB design

Location and fanout of the external clock circuitry are shown in figure 3.3. All of the components are placed on the bottom side of the PCB. The circuitry layout follows multiple tips presented in the oscillator design guide [16]. Separate GND planes are assigned to both the HSE and LSE circuitry. These planes are bounded by guard rings, formed by series of vias. Each of the planes is connected to a common GND only at one point. This approach provides proper EMI shielding while reducing a ground loop effect. We also minimized the distance between the MCU pins and both oscillators. All these measures combined should improve the clock generation stability and robustness.

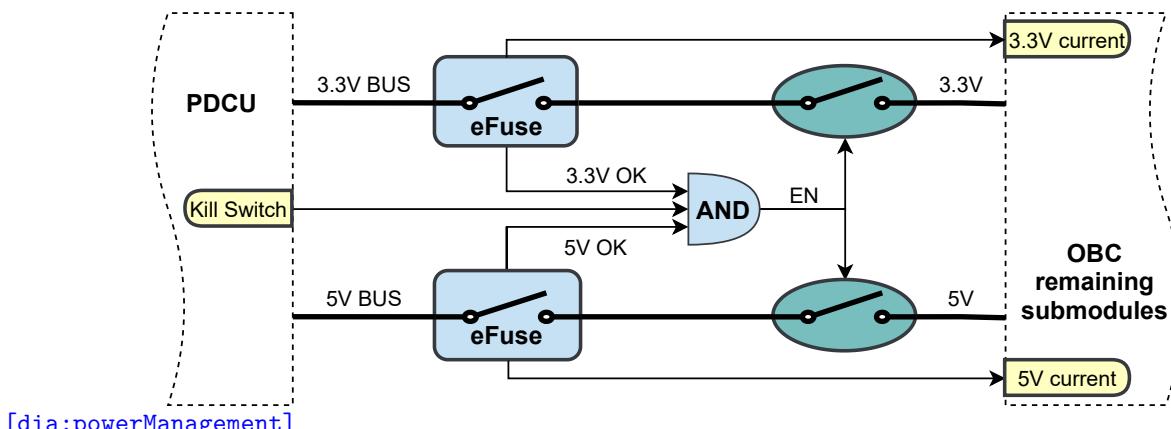


[pcb:clockSources]

Figure 3.3. Highlighted location of external clock sources circuitry.

3.3 Power management

The electric power subsystem (EPS) is known to be the most vital subsystem of a spacecraft. Its reliability and error handling should be ensured by the power control and distribution unit (PDCU). However, it is a good practice by professional manufacturers to include an additional power monitoring and control to their OBC module designs [1–9]. We have to implement circuitry that can sense a power bus malfunction and, as a response, power down the OBC. This feature is also important for some of the OBC on-earth user cases. During a hardware development or a system presentation, the user might misconnect the power line or use an unsupported power source by a mistake.

**Figure 3.4.** Functional diagram of power management circuitry.

A functional diagram of the implemented power management is shown in figure 3.4. To increase the overall efficiency and decrease complexity, we decided to avoid any voltage conversion independent from the PDCU. Therefore, our OBC requires two separate inputs from the main power buss (3.3[V] and 5[V]). The OBC is connected to each of these inputs through an electronic fuse (eFuse). This device continuously

monitors the bus for events of under-voltage, over-voltage, and over-current¹. As a response to such an event, the eFuse will switch into high impedance and pull down specific input of an AND logic gate. This gate simultaneously controls two load switches, one for each power line. This approach ensures that a fault on one power bus will result in a high impedance of both OBC power inputs. It also eliminates the risk of a death loop, in which a reset of eFuses is not possible as they are switching each other off. Added benefits of this design are an inbuild current measurement and a Kill Switch integration into the logic gate. A summary of the final power management rating is listed in table 3.2. These values were chosen considering the power requirements of the remaining OBC components and are a subject of change by a future user.

Power input	Parameter	Min	Typ	Max	Unit
3V3 BUS	voltage	2.9	3.3	3.5	V
	current	0.0	-	1.2	A
5V BUS	voltage	4.6	5.0	5.4	V
	current	0.0	-	1.2	A

[tab:powerManagement]

Table 3.2. OBC power rating. Value out of range will cause a protective shutdown.

3.3.1 Schematic design

An actual schematic diagram of power management circuitry is shown in figure 3.5. The most important part of this design is the eFuse, as it covers all of the power control features. We decided to use the TPS25940-Q1 device [18]. Custom threshold values can be set following the typical application schematic in the datasheet [18]. This is done by connecting specific resistors, with values calculated using the TPS2594x design calculation tool [19]. As the logic AND gate, we chose the 74LVC1G11-Q100 [20]. This device is designed to operate in a mixed logic level environment, what corresponds with our application. The last important component is the load switch. In our case, the TPS22965W-Q1 with an inbuilt output discharge function [21]. For a correct operation of the switch, the *VBIAS* pin should stay saturated for a while after disconnecting the *VIN* voltage. We achieved this behavior by charging a capacitor connected to the *VBIAS* from the *VIN* through a Schottky diode. Four reservoir capacitors are placed on both sides of the load switches, following the suggestions in both datasheets [18, 21]. Nominal logic values of all switching signals are set by pull-up or pull-down resistors.

3.3.2 PCB design

Location and fanout of the power management circuitry are shown in figure 3.6. All of the power management components are placed on the top side of the PCB. Similarly, all of the power tracks are on the top copper layer. Only a few signal traces are running within the second or the bottom layer. Both the 3.3[V] and 5[V] control circuitry share the same layout and tracing regarding recommendations presented in the eFuse and load switch datasheets [18, 21]. The 3.3[V] part is situated closer to the main PC104 header, while the 5[V] part is right below it. Both eFuses are connected to the main PC104 header power pins through strengthened 0.77[mm] traces in the third copper layer. Considering a standard copper thickness of 35[μm], each of the input traces is rated to deliver up to 2[A] of current. The logic gate with associated pull-down resistors is located above all of the remaining circuitry, closest to the main PC104 header.

¹ This is a crucial feature in handling and resolving a latch-up event.

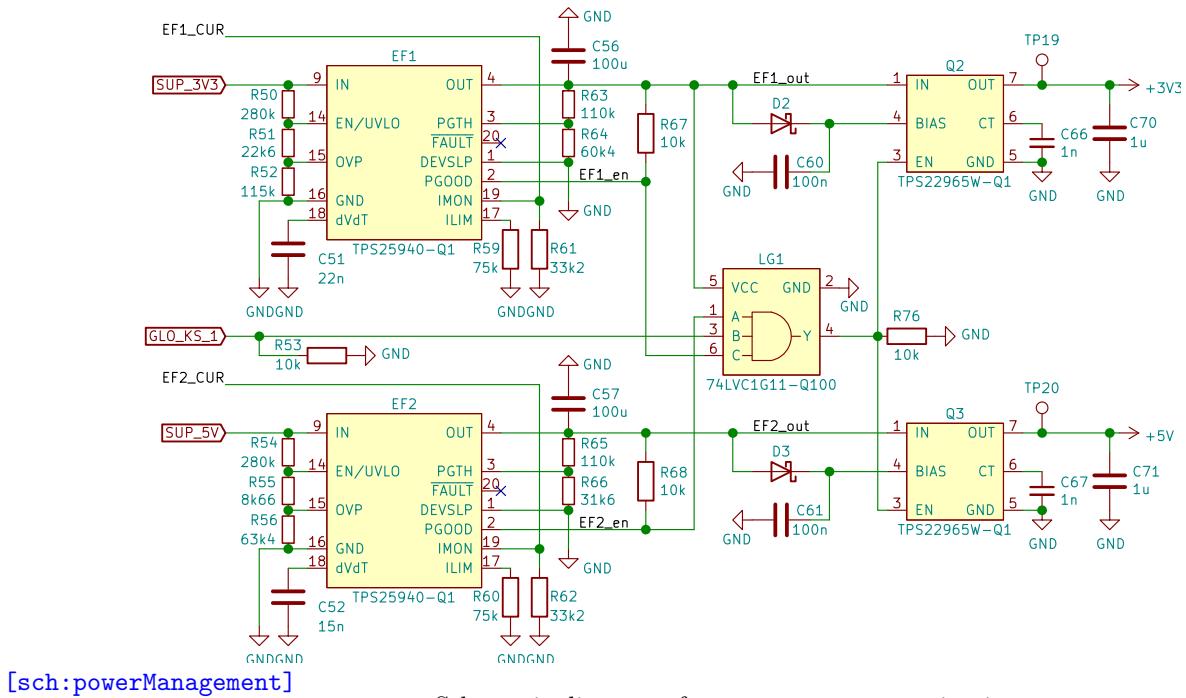


Figure 3.5. Schematic diagram of power management circuitry.

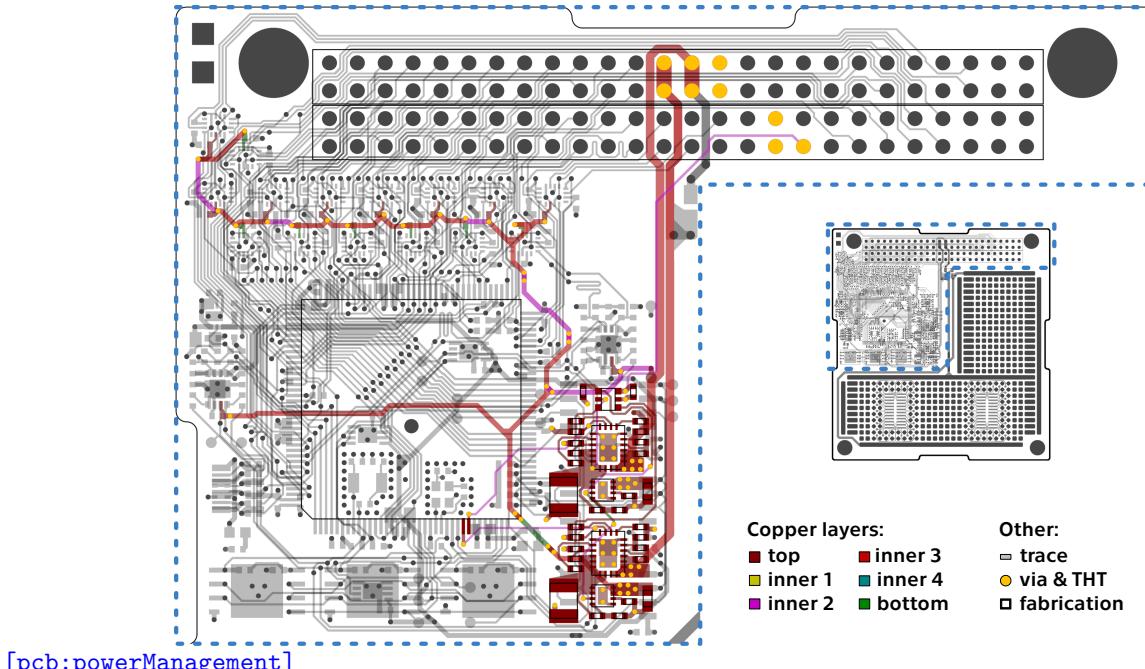


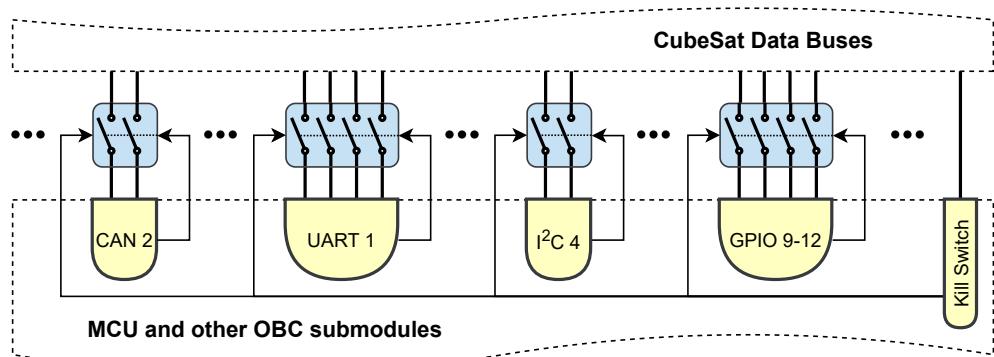
Figure 3.6. Highlighted location of power management circuitry.

3.4 Peripheral isolators

The spacecraft OBC is connected to many data buses shared among all other subsystems. In some scenarios, the OBC must be able to isolate itself from a specific or multiple data buses. For example, to switch between OBCs in a redundant configuration, handle the failure on a data bus, or prevent unintentional interferences. Standard approaches to addressing this isolation feature are analog switches [22], optocouplers

[23], or FPGAs [1]. These isolators should also guarantee that all data lines are high impedance when the OBC is powered off.

We chose to implement the design using robust analog switches as isolators of data lines. This approach is more straightforward, less expensive, and requires a smaller PCB area than an optocoupler-based or an FPGA-based ones (referred in chapter ??). A functional diagram of the implementation is shown in figure 3.7. OBC data lines are connected to the rest of the spacecraft through a series of analog switches. These lines are grouped by particular data buses and are assigned to a separate switch. The OBC can enable or disable a specific switch and therefore isolate a particular data bus from the remaining spacecraft subsystems. Pulling low the Kill Switch will result in high impedance of all switches and completely isolating the OBC data lines.



[fig:peripheralIsolatorsDiag]

Figure 3.7. Functional diagram of peripheral isolators circuitry.

3.4.1 Schematic design

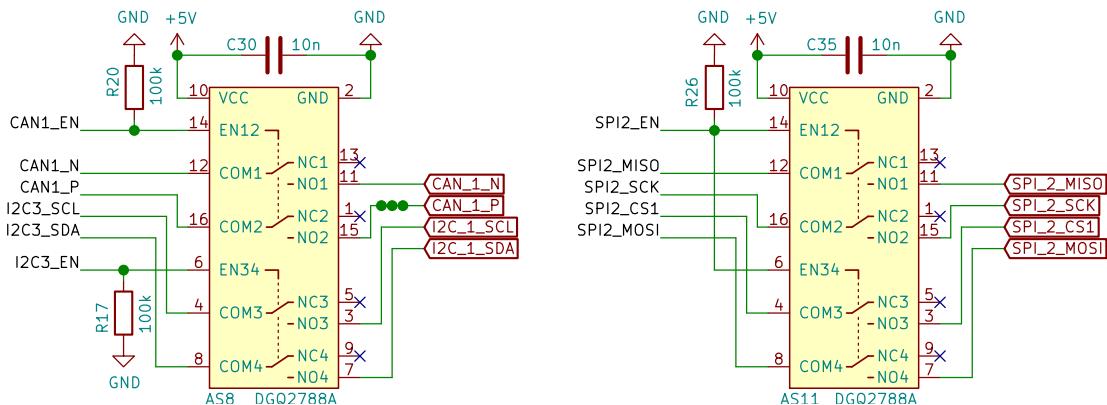
Schematic diagrams of two isolators are shown in figure 3.8. We decided to use the DGQ2788A device [24]. To cover all of the data buses, the OBC hosts fifteen of these analog switches in a dual double pole double throw (DPDT) configuration. The OBC data lines are connected to common (COM) terminals. Normally closed (NC) terminals are left floating, whereas normally open (NO) terminals are connected to the spacecraft data lines. The important Kill Switch functionality is implemented using the device's power down protection. If the switch loses power, it will enter the normal state. This approach simplifies the circuitry a lot as it substitutes an otherwise necessary system of multiple logic gates. The other beneficial features of this analog switch are inbuild signal clamping diodes and a high latch-up current of 300[mA]. The presence of pull-down resistors and decoupling capacitors in the schematic follows the device datasheet.

3.4.2 PCB design

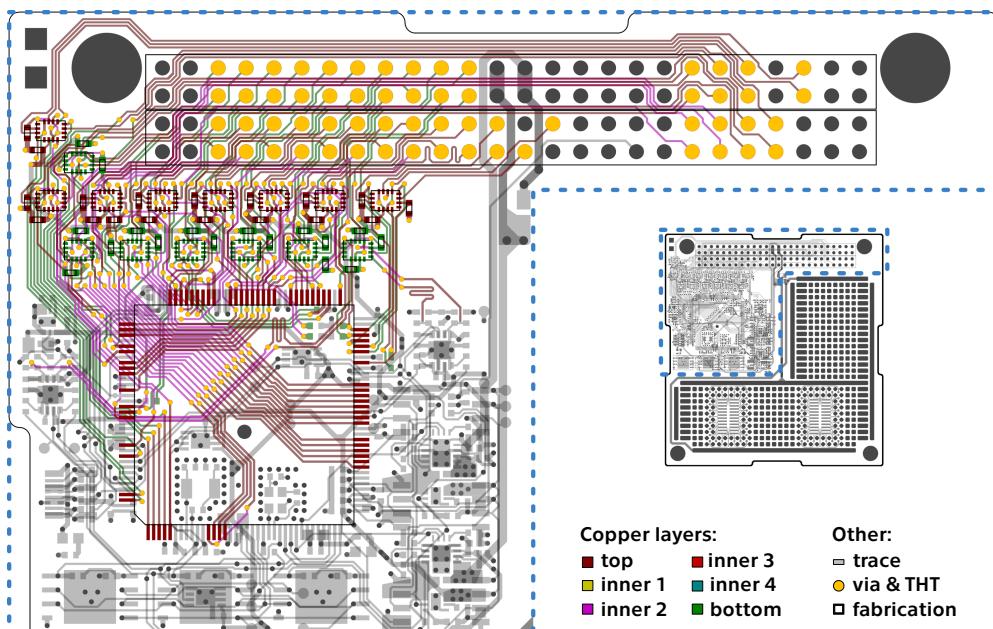
3.5 External memory

3.5.1 Schematic design

3.5.2 PCB design



[fig:peripheralIsolatorsSchem]

Figure 3.8. Schematic diagram of two peripheral isolators.

[pcb:peripheralIsolators]

Figure 3.9. Highlighted location of peripheral isolators circuitry.

3.6 CAN bus drivers

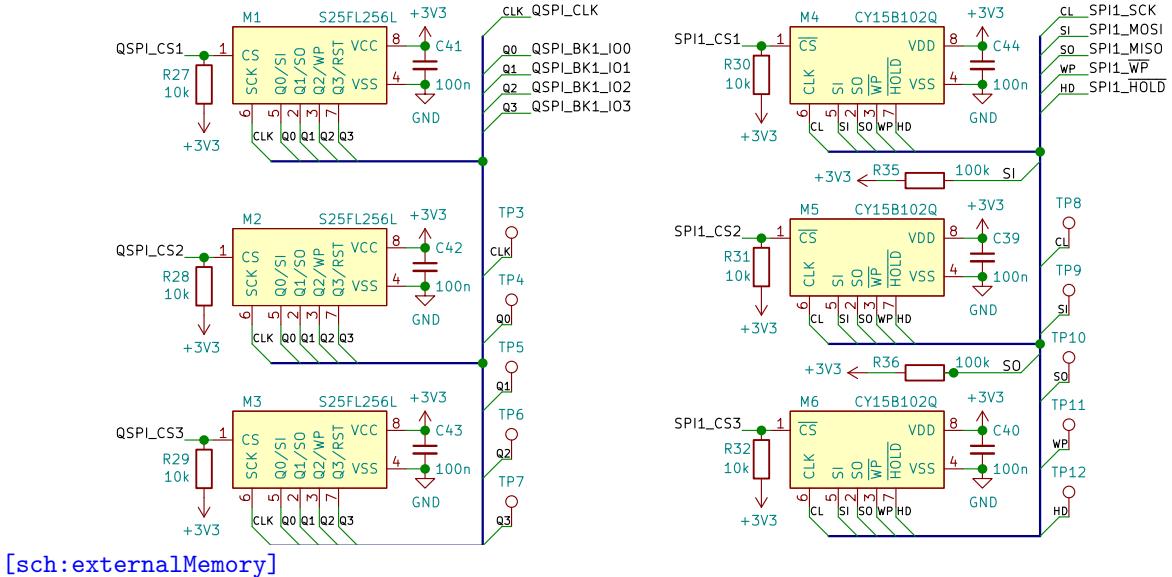
3.6.1 Schematic design

3.6.2 PCB design

3.7 Temperature monitoring

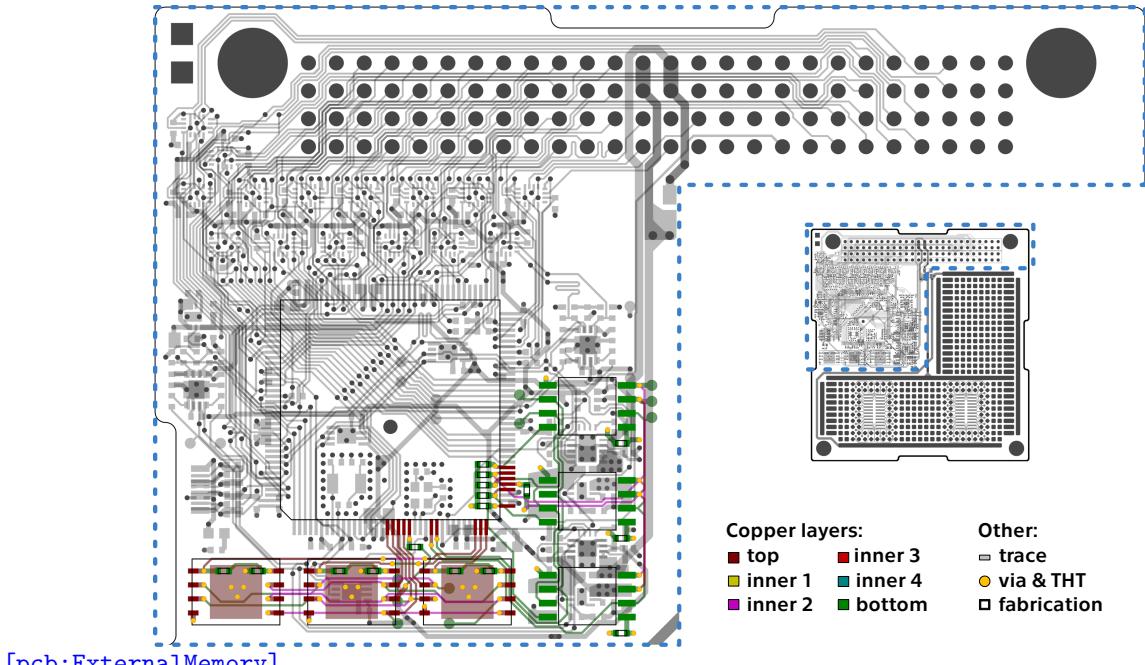
3.7.1 Schematic design

3.7.2 PCB design



[sch:externalMemory]

Figure 3.10. Schematic diagram of external memory circuitry.



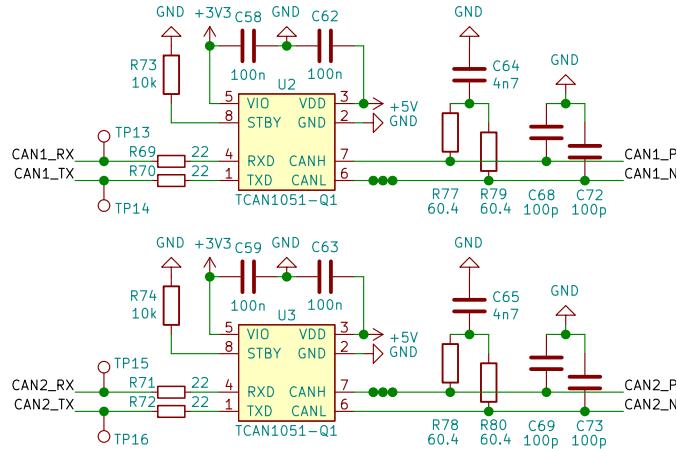
[pcb:ExternalMemory]

Figure 3.11. Highlighted location of external memory circuitry.

3.8 Programming port

3.8.1 Schematic design

3.8.2 PCB design



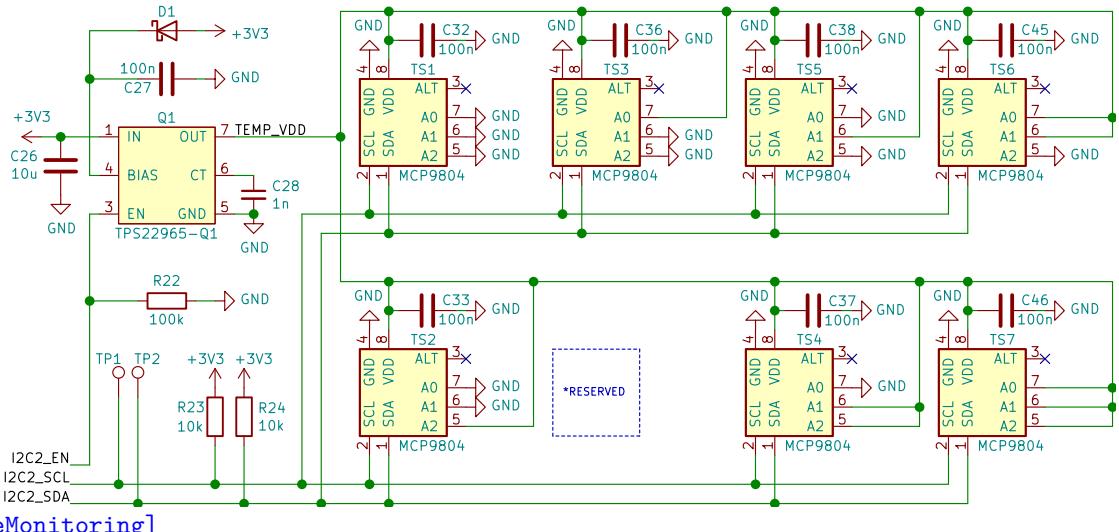


Figure 3.14. Schematic diagram of temperature monitoring circuitry.

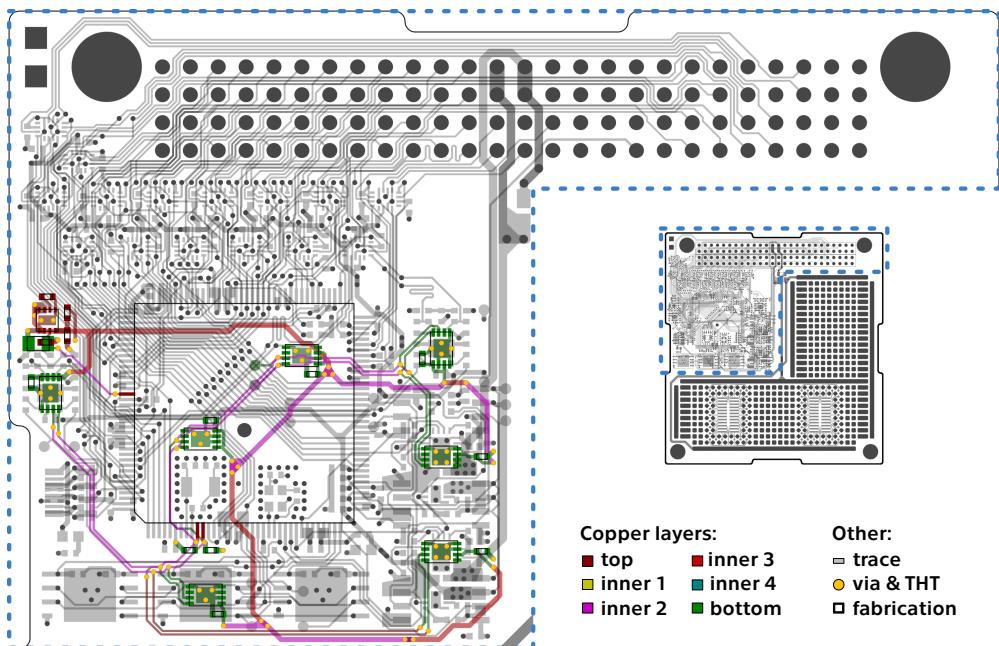


Figure 3.15. Highlighted location of temperature monitoring circuitry.

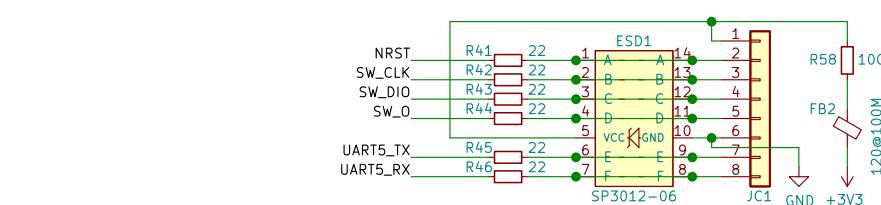
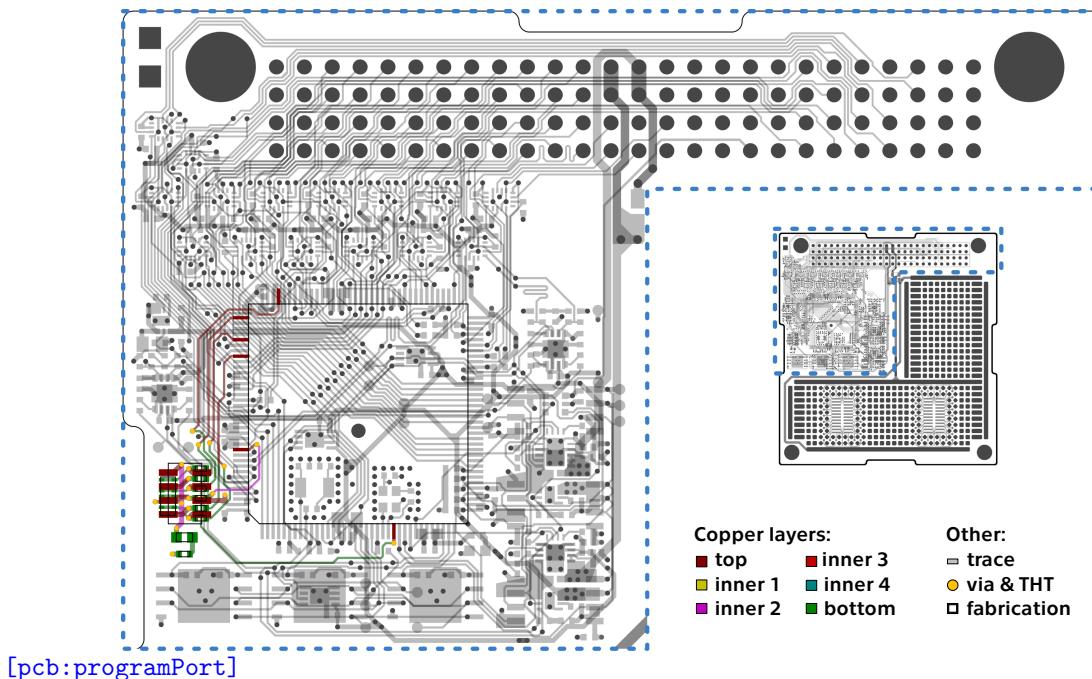
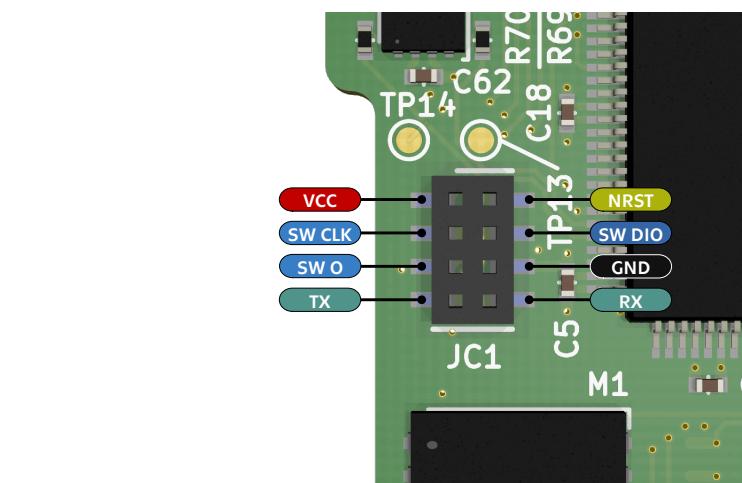


Figure 3.16. Schematic diagram of programming port circuitry.

**Figure 3.17.** Highlighted location of programming port circuitry.**Figure 3.18.** Programming port pinout.

Chapter 4

Board Delta

4.1 Circuit modification

4.2 PCB modification

Chapter 5

Element Foxtrot

- 5.1 PCB specifications**
- 5.2 Power input handling**
 - 5.2.1 Ordinary power source**
 - 5.2.2 USB-C power source**
- 5.3 Voltage conversion**
- 5.4 PC104 modules slots**

Chapter 6

Board Sierra - testing

- 6.1 Testing software**
- 6.2 Radiation testing**
- 6.3 Environmental testing**

Chapter 7

Conclusion

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Appendix A

Thesis Assignment



BACHELOR'S THESIS ASSIGNMENT

I. Personal and study details

Student's name: **Geib Filip** Personal ID number: **483567**
Faculty / Institute: **Faculty of Electrical Engineering**
Department / Institute: **Department of Measurement**
Study program: **Cybernetics and Robotics**

II. Bachelor's thesis details

Bachelor's thesis title in English:

On-board computer for PC104 format CubeSats

Bachelor's thesis title in Czech:

Palubní počítač pro CubeSaty formátu PC104

Guidelines:

- Design a concept of an STM32 based on-board computer for PC104 frame based CubeSats.
- Implement redundancy for the critical components to improve reliability of the design.
- Construct the device and conduct testing of the whole system, e.g. using a flatsat platform.
- Concentrate on providing detailed and accurate documentation of the system.

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Name and workplace of bachelor's thesis supervisor:

Ing. Vojtěch Petrucha, Ph.D., 13138

Name and workplace of second bachelor's thesis supervisor or consultant:

Date of bachelor's thesis assignment: **13.01.2021** Deadline for bachelor thesis submission: _____

Assignment valid until:
by the end of summer semester 2021/2022

Ing. Vojtěch Petrucha, Ph.D.
Supervisor's signature

Head of department's signature

prof. Mgr. Petr Páta, Ph.D.
Dean's signature

III. Assignment receipt

The student acknowledges that the bachelor's thesis is an individual work. The student must produce his thesis without the assistance of others, with the exception of provided consultations. Within the bachelor's thesis, the author must state the names of consultants and include a list of references.

Date of assignment receipt

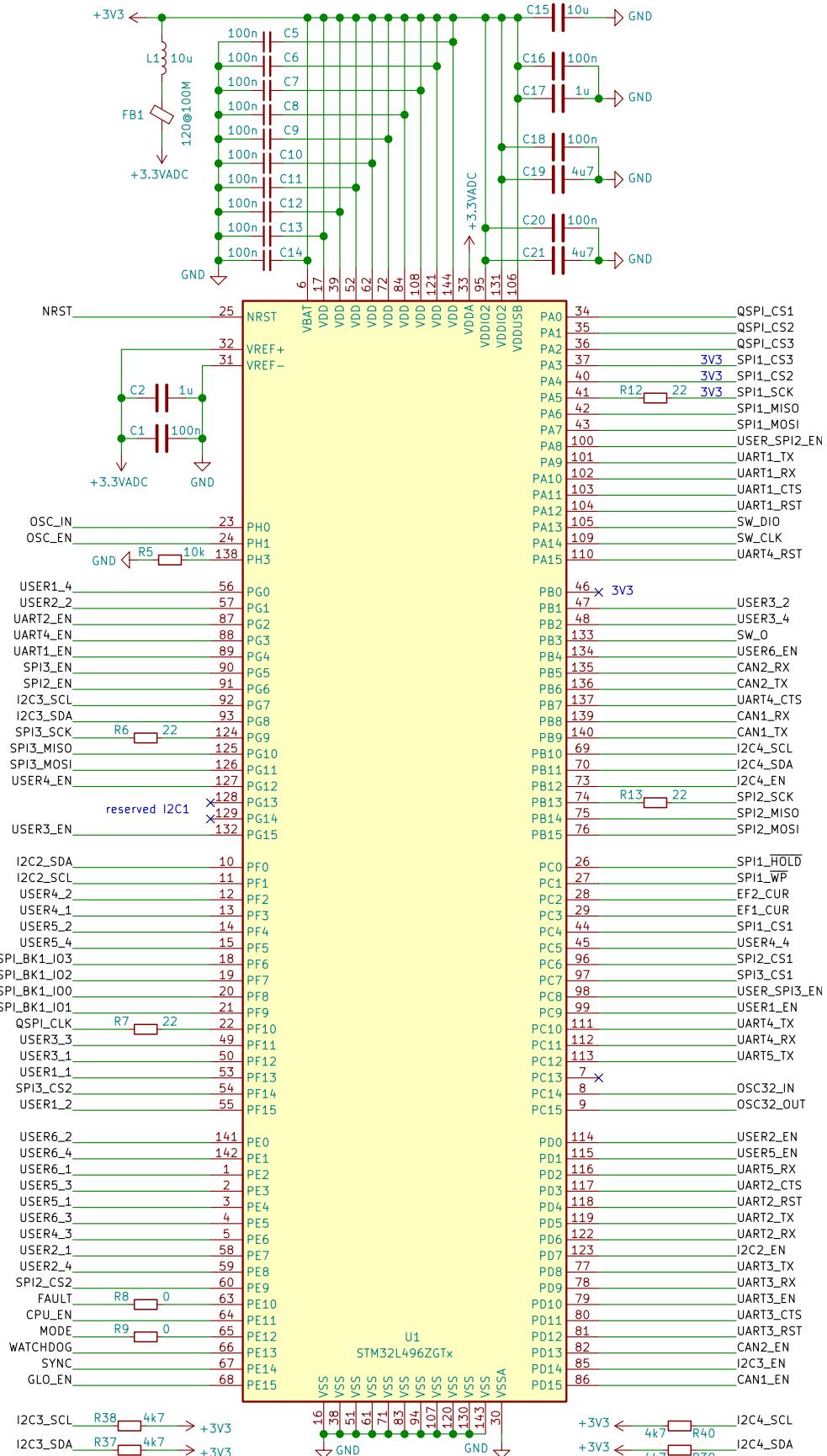
Student's signature

[app:thesisAssignment]

Figure 7.1. Assignment of this bachelor's thesis.

Appendix B

Schematic diagrams



[app_sch:microcontroller]

Figure 7.2. Schematic diagram of microcontroller and its auxiliaries.

Appendix C

Additional materials

Designator	Qualified part no.	Unqualified part no.	Difference
M1 - M3	S25FL256LAGNFI	S25FL256LAGNFI	temp.
	S25FL256LDPNFI	S25FL256LDPNFI	temp., speed
Q1 - Q3	TPS22965W-Q1	TPS22965-Q1	temp.
	TPS22975	TPS22975	temp., auto.
TS1 - TS7	MCP9804x-E/MC	MCP9808x-E/MC	accuracy
LG1	74LVC1G11GW-Q100	74LVC1G11GW	auto.

[tab:unqualifiedParts]

Table 7.1. List of available unqualified variants to some of the qualified parts.

Requests for correction