Rockchip RK2108 Datasheet

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Revision 1.3
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Revision History

Date	Revision	Description
2020-9-25	1.3	Update the package quantity information
2020-9-10	1.2	Update IO name and description
2019-12-20	1.1	Update the order QTY, marking information and add the thermal information
2019-6-26	1.0	Initial released

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Chapter 1 Introduction

1.1 Overview

RK2108 is an ultra low power consumption application processor with integrated ARM Cortex-M4F and HiFi3 DSP, and designed for smart home and IoT applications.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- ARM Cortex-M4F processor
- Integrated 16KB instruction cache, 16KB data cache
- Nested Vectored Interrupt Controller closely integrated with processor core to achieve low latency interrupt processing, support 64 external interrupts
- Include Floating Point Unit (FPU)

1.2.2 DSP

- HiFi3 with 4 24-bit MAC or dual 32-bit MAC architecture
- 3 VLIW slots, 2-Way SIMD Vector FPU
- Voice noise reduction optimization
- Integrated 64KB/512KB I/D TCM
- Integrated 16KB/16KB I/D Cache

1.2.3 Memory Organization

- Internal on-chip memory
  - BootRom
  - Share Memory
- External off-chip memory
  - FSPI NorFlash
  - FSPI pSRAM

1.2.4 System SRAM

- Internal BootRom
  - Support system boot from the following device:
    - FSPI NorFlash interface
  - Support system code download by the following interface:
    - USB2 interface (Device mode)
- Share Memory
  - Size: 1MB

1.2.5 External Storage device

- FSPI Serial flash interface
  - Support transfer data from/to serial flash device
  - Support x1,x2,x4 data bits mode
  - Support 1 chip select

1.2.6 System Component

- CRU (clock & reset unit)
  - Support 2 PLLs to generate all clocks
  - Support clock gating control for individual components

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- One oscillator with 24MHz clock input
- Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - Support 4 separate power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Support DSP auto power down mode

- Timer
  - Support 6 64-bit timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - Support 4 on-chip PWMs(PWM0~PWM3) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - One Watchdog for CM4, the other for DSP

- Interrupt Controller
  - Support 2 interrupt controllers for DSP and AP
  - Support 50 SPI interrupt sources input from different components inside RK2108
  - Input interrupt level is fixed, only high-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - DMAC features:
    - Support 8 channels
    - 17 hardware request from peripherals
    - 2 interrupt output

1.2.7 Video input interface

- VIP
  - Support BT601 YCbCr 422 8-bit input

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- Support BT656 YCbCr 422 8-bit input
- Support UYVY/VYUY/YUYV/YVYU configurable
- Support RAW 8/10/12-bit input
- Support window cropping
- Support virtual stride when write to internal memory
- Support different stored address for Y and UV

1.2.8 Display interface

- Display interface
  - Support RGB Parallel Display interface

- RGB Parallel Display interface
  - Up to serial 8-bit

1.2.9 Video Output Processor

- Display interface
  - Parallel RGB LCD interface
  - Max input/output resolution
    - Max input size: 512KB
    - Max output: 800x480
- Display process
  - Background layer
    - programmable 24-bit color
  - Win0 layer and Win1 layer
    - Format :
      1BPP/2BPP/4BPP/8BPP
      RGB888, ARGB888, RGB565, RGB444
      YUV422, YUV420, YUV444 4-bit/8-bit
      YUYV422 4-bit/8-bit
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
  - Win2 layer
    - Format :
      RGB888, ARGB888, RGB565, RGB444
      YUV422, YUV420, YUV444 4-bit/8-bit
      YUYV422 4-bit/8-bit
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
- Overlay
  - RGB/YUV overlay
  - Layer1/2/3 exchange
- POST process
  - BCSH
  - Y-gamma
  - Post scale up: 2/3/4
  - Color matrix

1.2.10 Audio Interface

- I2S0
  - Up to 2 channels TX and 4 channels RX path
  - Audio resolution from 16bits to 32bits

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- Sample rate up to 192KHz
- Provide master and slave work mode, software configurable
- Support 3 I2S formats (normal, left-justified, right-justified)

- I2S1
  - Up to 2 channels for TX and 6 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provide master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time

- PDM
  - Up to 6 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode

- Codec ADC
  - Up to 2 channels
  - Support I2S 2 channels or PDM 2 channels
  - Sample rate up to 192KHz
  - Provide master and slave work mode, software configurable

- Audio Bypass
  - Support I2SIN interface bypass to AP by I2SOUT interface
  - Support PDMIN interface bypass to AP by PDMOUT interface
  - Support I2S from Codec ADC bypass to AP by I2SOUT interface
  - Support PDM from Codec ADC bypass to AP by PDMOUT interface

- VAD(Voice Activity Detection)
  - Support read voice data from I2S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

- Audio PWM
  - Support 2 channels audio PWM
  - Audio data width from 16bits to 32bits
  - Support up to 16 oversampling
  - Support audio resolution 8/9/10/11bits
  - Support linear interpolation by 2/4/6/8 oversampling

1.2.11 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4bits data bus widths

- USB 2.0 for Device
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- SPI interface
  - Support 2 SPI Controllers, both support one chip-select output
  - Support serial-master and serial-slave mode, software-configurable

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- SPI2APB interface
  - Support slave mode SPI protocol
  - Support serial-slave mode only
  - Embedded a APB master interface

- I2C Master controller
  - Support 3 I2C Master(I2C0-I2C2)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode

- I2C Slave controller
  - One on-chip I2C slave controller
  - Software programmable clock frequency and transfer rate 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at 100Kbit/s in the standard mode

- UART interface
  - Support 3 UART interfaces(UART0-UART2)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART0/UART2

1.2.12 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- LDO
  - Support input 1.8V power supply
  - Output 3 power supply: digital 0.9V, analog 0.9V, codec 1.6V

- Package Type
  - QFN68L (body: 7mm x 7mm; ball size: 0.15mm; ball pitch: 0.35mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

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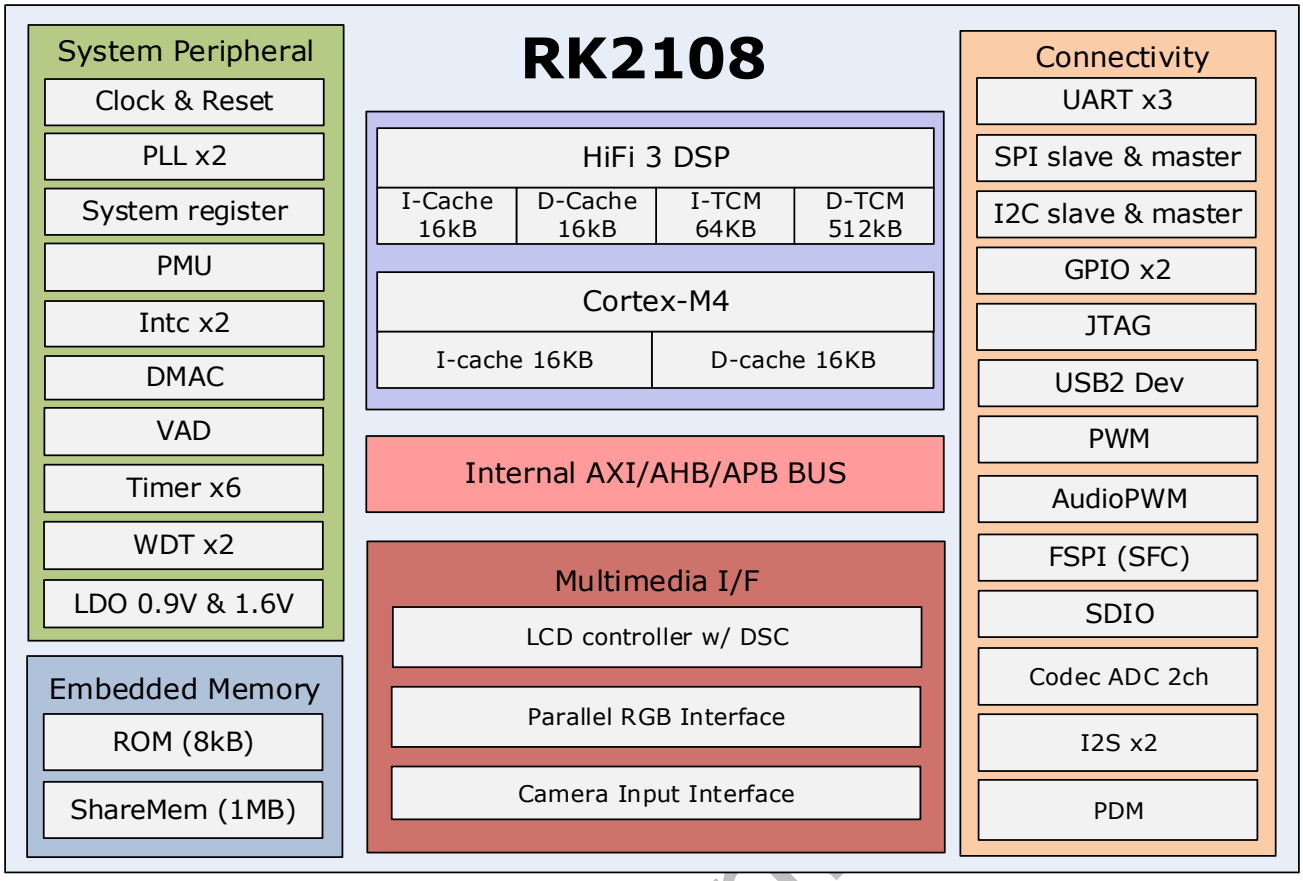

Fig.1-1 Block Diagram

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Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK2108	RoHS	QFN68L	2000 by reel	Audio application processor includes Cortex-M4F and HiFi3 DSP

2.2 Top Marking

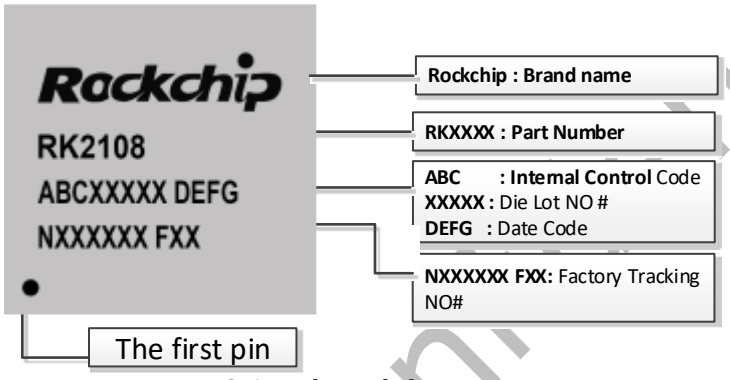
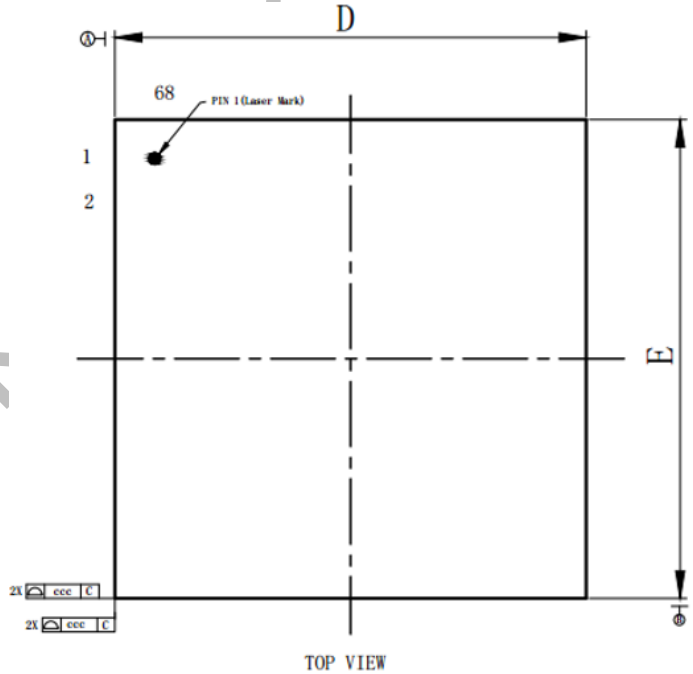


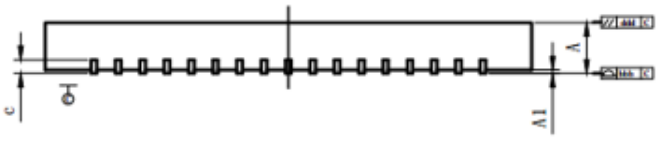
Fig.2-1 Package definition

2.3 QFN68L Dimension



TOP VIEW

Fig.2-2 Package Top View



SIDE VIEW

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Fig.2-3 Package Side View

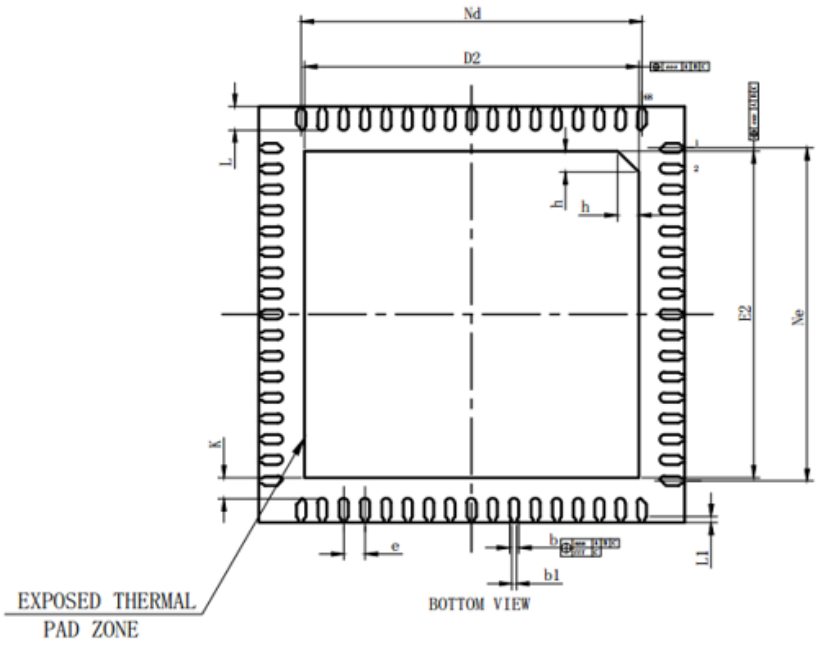

Fig.2-4 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.39	5.49	5.59
e	0.35BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.39	5.49	5.59
Ne	5.60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	--	--
h	0.30	0.35	0.40
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		
fff	0.05		
L/F載体尺寸 (mil)	232*232		

Fig.2-5 Package Dimension

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2.4 Ball Map

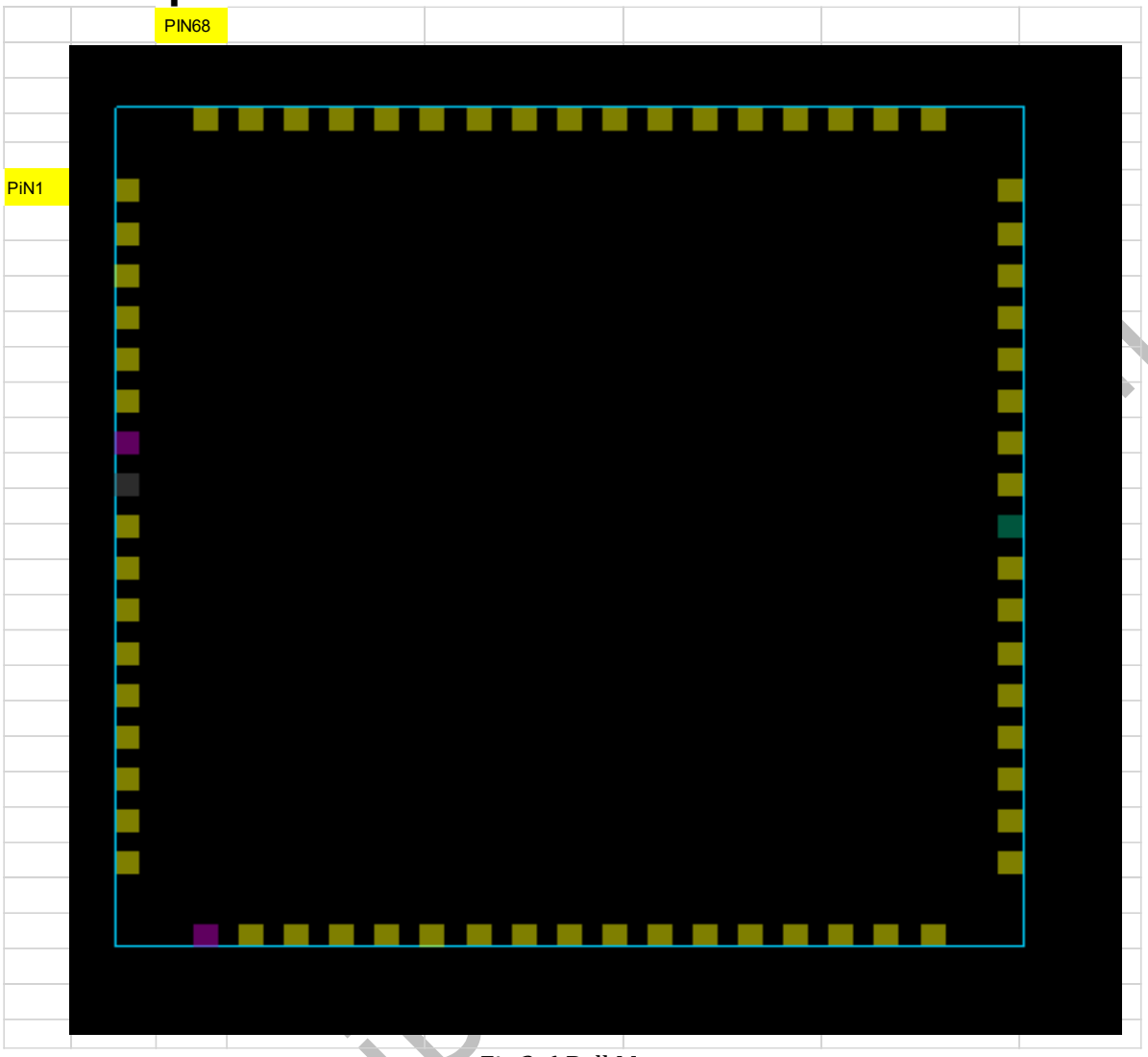

Fig.2-6 Ball Map

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2.5 Pin Number List

Table 2-1 Pin Number Order Information

Pin#	Pin Name	Pin#	Pin Name
1	SDIO_D2/SPI_MST1_MISO_M0/I2C_MST2_SDA_M0/DSP_JTAG0_TDO/GPIO0_C4_D	36	I2C_MST0_SDA_M1/CIF_D11/I2S1_SDI0_M1/PCM_SYNC_M0/GPIO0_D4_U
2	SDIO_CLK/I2C_MST0_SCL_M0/DSP_JTAG0_TCK/TEST_CLK_OUT0/GPIO0_C0_U	37	LCDC_RS/CIF_MCLK/PWM3/AUDIO_LOUT_M1/GPIO1_A4_D
3	CORE_VDD	38	I2C_MST0_SCL_M1/CIF_D10/I2S1_SDO0_M1/PCM_CLK_M0/GPIO0_D3_U
4	DVDD_1V8	39	CIF_VSYNC/I2S1_SCLK_TX_RX_M1/PCM_OUT_M0/KEY_IN_M2/GPIO0_D6_D
5	CORE_VDD_OUT	40	CIF_PCLK/I2S1_MCLK_M1/KEY_OUT_M2/GPIO0_D7_D
6	AVDD_0V9_OUT	41	CIF_HREF/I2S1_LRCK_TX_RX_M1/PCM_IN_M0/GPIO0_D5_D
7	AVSS	42	32K_CLK_OUT/PCM_CLK_M1/GPIO1_A7_D
8	AVDD_1V8	43	VCCIO_1V8
9	CODEC_1V6	44	VCC_IO
10	VREF	45	UART0_RTSN/UART1_TX_M0/PWM2/AUDIO_ROUT_M0/KEY_OUT_M1/GPIO0_D2_U
11	MIC_IN1_P	46	UART0_TX/M4_JTAG1_TMS/GPIO0_D0_U
12	MIC_IN1_N	47	UART0_CTSN/UART1_RX_M0/PWM1/AUDIO_LOUT_M0/KEY_IN_M1/GPIO0_D1_U
13	MIC_IN2_P	48	UART0_RX/M4_JTAG1_TCK/GPIO0_C7_U
14	MIC_IN2_N	49	UART2_RX/SPI_MST2_CS0_M0/PMU_DEBUG0/GPIO1_A0_U
15	AVDD_0V9	50	UART2_TX/SPI_MST2_CLK_M0/PMU_DEBUG1/GPIO1_A1_D
16	XIN24M	51	UART2_CTS/SPI_MST2_MISO_M0/I2C_MST0_SCL_M2/PMU_DEBUG2/GPIO1_A2_D
17	XOUT24M	52	UART2_RTS/SPI_MST2_M0SI_M0/I2C_MST0_SDA_M2/PMU_DEBUG3/GPIO1_A3_D
18	AVSS	53	GPIO1_D0_D
19	USB_AVDD_3V3	54	TEST_D
20	USB_AVDD_1V8	55	M4_DSP_JTAG_SEL/GPIO1_A6_D
21	USB_DM	56	NPOR_U
22	USB_DP	57	KEY_OUT_M0/GPIO1_B7_D
23	CORE_VDD	58	KEY_IN_M0/GPIO1_B6_D
24	IO_VTG_SEL_D	59	SFC_CS/I2C_MST2_SCL_M1/SPI_SLV0_MOSI/GPIO0_B4_U
25	PDM_IN_CLK0/I2S1_SCLK_RX_M0/CIF_D0/LCDC_D0/GPIO0_A0_D	60	SFC_D2/I2C_MST1_SDA_M1/SPI_SLV0_CLK/GPIO0_B3_U
26	PDM_IN_CLK1/I2S1_LRCK_RX_M0/CIF_D1/LCDC_D1/GPIO0_A1_D	61	SFC_D3/I2C_MST1_SCL_M1/SPI_SLV0_CS/GPIO0_B2_U
27	PDM_IN_DAT0/I2S1_SDI0_M0/CIF_D2/LCDC_D2/GPIO0_A2_D	62	SFC_D0/I2C_SLV0_SCL/GPIO0_B6_U
28	PDM_IN_DAT1/I2S1_SDI1/CIF_D3/LCDC_D3/GPIO0_A3_D	63	SFC_D1/I2C_SLV0_SDA/GPIO0_B7_U
29	I2S1_MCLK_M0/UART1_TX_M1/TEST_CLK_OUT1/CIF_D4/LCDC_D4/GPIO0_A4_D	64	SFC_CLK/I2C_MST2_SDA_M1/SPI_SLV0_MISO/GPIO0_B5_D
30	I2S1_SDI2/UART1_RX_M1/UART1_RX_M3/TEST_CLK_OUT2/CIF_D5/LCDC_D5/GPIO0_A5_D	65	SDIO_D3/SPI_MST1_MOSI_M0/I2C_MST2_SCL_M0/GPIO0_C5_D
31	PDM_OUT_CLK0/I2S1_SCLK_TX_M0/CIF_D6/LCDC_D6/GPIO0_A6_D	66	SDIO_D1/SPI_MST1_CLK_M0/I2C_MST1_SCL_M0/DSP_JTAG0_TDI/GPIO0_C3_D
32	PDM_OUT_DAT0/I2S1_SDO0_M0/CIF_D8/LCDC_WR/GPIO0_B0_d	67	SDIO_CMD/I2C_MST0_SDA_M0/DSP_JTAG0_TMS/TES_CLK_OUT3/GPIO0_C1_U
33	PDM_OUT_CLK1/I2S1_LRCK_TX_M0/CIF_D7/LCDC_D7/GPIO0_A7_D	68	SDIO_D0/SPI_MST1_CSN_M0/I2C_MST1_SDA_M0/DSP_JTAG0_TRSTN/GPIO0_C2_U
34	PDM_OUT_DAT1/CIF_D9/LCDC_RD/UART1_TX_M3/GPIO0_B1_d	EPAD	VSS
35	LCDC_CS/SPI_MST2_CS1/PWM0/AUDIO_ROUT_M1/GPIO1_A5_D		

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2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	EPAD	Internal Core Ground Digital IO Ground
AVSS	7 18	Analog Ground
CORE_VDD	3 23	Digital Logic Power
CORE_VDD_OUT	5	CORE LDO output power
DVDD_1V8	4	CORE LDO input power
AVDD_1V8	8	MIPI LDO input power AUDIO LDO input power OSC IO Analog Power FRAC PLL Analog Power
AVDD_0V9	15	FRAC PLL Analog Power INT PLL Analog Power
AVDD_0V9_OUT	6	MIPI LDO output power
CODEC_1V6	9	Codec ADC Analog Power
VCCIO_1V8	43	1.8V IO Power
VCC_IO	44	1.8V/3.3V IO Power
USB_AVDD_1V8	20	USB2 1.8V Analog Power
USB_AVDD_3V3	19	USB2 3.3V Analog Power
VREF	10	Codec ADC VREF

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2.7 Function IO Description

Table 2-3 Function IO description

Pin #	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type①	Def②	Driver Strength	Pull up /Pull down	IO Domain
25	PDM_IN_CLK0/I2S1_SCLK_RX_M0/CIF_D0/LCDC_D0/GPIO0_A0_d	GPIO0_A0_d	PDM_IN_CLK0		LCDC_D0	I2S1_SCLK_RX_M0	CIF_D0		I/O	O	4	down	
26	PDM_IN_CLK1/I2S1_LRCK_RX_M0/CIF_D1/LCDC_D1/GPIO0_A1_d	GPIO0_A1_d	PDM_IN_CLK1		LCDC_D1	I2S1_LRCK_RX_M0	CIF_D1		I/O	O	4	down	
27	PDM_IN_DAT0/I2S1_SDI0_M0/CIF_D2/LCDC_D2/GPIO0_A2_d	GPIO0_A2_d	PDM_IN_DAT0		LCDC_D2	I2S1_SDI0_M0	CIF_D2		I/O	I	4	down	
28	PDM_IN_DAT1/I2S1_SDI1/CIF_D3/LCDC_D3/GPIO0_A3_d	GPIO0_A3_d	PDM_IN_DAT1		LCDC_D3	I2S1_SDI1	CIF_D3		I/O	I	4	down	
29	I2S1_MCLK_M0/UART1_TX_M1/TEST_CLK_OUT1/CIF_D4/LCDC_D4/GPIO0_A4_d	GPIO0_A4_d	I2S_IN_MCLK	UART1_TX_M1	TEST_CLKOUT1	I2S1_MCLK_M0	CIF_D4	LCDC_D4	I/O	I	4	down	
30	I2S1_SDI2/UART1_RX_M1/UART1_RX_M3/TEST_CLK_OUT2/CIF_D5/LCDC_D5/GPIO0_A5_d	GPIO0_A5_d	I2S_OUT_MCLK	UART1_RX_M1_M3	TEST_CLKOUT2	I2S1_SDI2	CIF_D5	LCDC_D5	I/O	I	4	down	
31	PDM_OUT_CLK0/I2S1_SCLK_TX_M0/CIF_D6/LCDC_D6/GPIO0_A6_d	GPIO0_A6_d	PDM_OUT_CLK0		LCDC_D6	I2S1_SCLK_TX_M0	CIF_D6		I/O	I	4	down	
33	PDM_OUT_CLK1/I2S1_LRCK_TX_M0/CIF_D7/LCDC_D7/GPIO0_A7_d	GPIO0_A7_d	PDM_OUT_CLK1		LCDC_D7	I2S1_LRCK_TX_M0	CIF_D7		I/O	I	4	down	
32	PDM_OUT_DAT0/I2S1_SDO0_M0/CIF_D8/LCDC_WR/GPIO0_B0_d	GPIO0_B0_d	PDM_OUT_DAT0		LCDC_WR	I2S1_SDO0_M0	CIF_D8		I/O	O	4	down	
34	PDM_OUT_DAT1/CIF_D9/LCDC_RD/UART1_TX_M3/GPIO0_B1_d	GPIO0_B1_d	PDM_OUT_DAT1		LCDC_RD	UART1_TX_M3	CIF_D9		I/O	O	4	down	
61	SFC_D3/I2C_MST1_SCL_M1/SPI_SLV0_CS/GPIO0_B2_u	GPIO0_B2_u	SPI_SLV0_CS	I2C_MST1_SCL_M1	SFC_D3				I/O	I	4	up	VCC_IO
60	SFC_D2/I2C_MST1_SDA_M1/SPI_SLV0_CLK/GPIO0_B3_u	GPIO0_B3_u	SPI_SLV0_CLK	I2C_MST1_SDA_M1	SFC_D2				I/O	I	4	up	
59	SFC_CS/I2C_MST2_SCL_M1/SPI_SLV0_MOSI/GPIO0_B4_u	GPIO0_B4_u	SPI_SLV0_MOSI	I2C_MST2_SCL_M1	SFC_CS				I/O	I	4	up	
64	SFC_CLK/I2C_MST2_SDA_M1/SPI_SLV0_MISO/GPIO0_B5_d	GPIO0_B5_d	SPI_SLV0_MISO	I2C_MST2_SDA_M1	SFC_CLK				I/O	I	4	down	
62	SFC_D0/I2C_SLV0_SCL/GPIO0_B6_u	GPIO0_B6_u	I2C_SLV0_SCL	SFC_D0					I/O	I	4	up	
63	SFC_D1/I2C_SLV0_SDA/GPIO0_B7_u	GPIO0_B7_u	I2C_SLV0_SDA	SFC_D1					I/O	I	4	up	
2	SDIO_CLK/I2C_MST0_SCL_M0/DSP_JTAG0_TCK/TEST_CLK_OUT0/GPIO0_C0_u	GPIO0_C0_u	I2C_MST0_SCL_M0	TEST_CLK_OUT0	DSP_JTAG0_TCK	SDIO_CLK			I/O	I	4	up	
67	SDIO_CMD/I2C_MST0_SDA_M0/DSP_JTAG0_TMS/TES_CLK_OUT3/GPIO0_C1_u	GPIO0_C1_u	I2C_MST0_SDA_M0	TEST_CLK_OUT3	DSP_JTAG0_TMS	SDIO_CMD			I/O	I	4	up	
68	SDIO_D0/SPI_MST1_CSN_M0/I2C_MST1_SDA_M0/DSP_JTAG0_TRSTN/GPIO0_C2_u	GPIO0_C2_u	SPI_MST1_CSN_M0	I2C_MST1_SDA_M0	DSP_JTAG0_TRSTN	SDIO_D0			I/O	O	4	up	
66	SDIO_D1/SPI_MST1_CLK_M0/I2C_MST1_SCL_M0/DSP_JTAG0_TDI/GPIO0_C3_d	GPIO0_C3_d	SPI_MST1_CLK_M0	I2C_MST1_SCL_M0	DSP_JTAG0_TDI	SDIO_D1			I/O	O	4	down	
1	SDIO_D2/SPI_MST1_MISO_M0/I2C_MST2_SDA_M0/DSP_JTAG0_TDO/GPIO0_C4_d	GPIO0_C4_d	SPI_MST1_MISO_M0	I2C_MST2_SDA_M0	DSP_JTAG0_TDO	SDIO_D2			I/O	I	4	down	

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Pin #	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up /Pull down	IO Domain
65	SDIO_D3/SPI_MST1_MOSI_M0/I2C_MST2_SCL_M0/GPIO0_C5_d	GPIO0_C5_d	SPI_MST1_MOSI_M0	I2C_MST2_SCL_M0	SDIO_D3				I/O	I	4	down	
48	UART0_RX/M4_JTAG1_TCK/GPIO0_C7_u	GPIO0_C7_u	UART0_RX	M4_JTAG1_TCK					I/O	I	4	up	
46	UART0_TX/M4_JTAG1_TMS/GPIO0_D0_u	GPIO0_D0_u	UART0_TX	M4_JTAG1_TMS					I/O	O	4	up	
47	UART0_CTSN/UART1_RX_M0/PWM1/AUDIO_LOUT_M0/KEY_IN_M1/GPIO0_D1_u	GPIO0_D1_u	UART0_CTSN	UART1_RX_M0	AUDIO_LOUT_M0	PWM1	KEY_IN_M1		I/O	I	4	up	
45	UART0_RTSN/UART1_TX_M0//PWM2/AUDIO_ROUT_M0/KEY_OUT_M1/GPIO0_D2_u	GPIO0_D2_u	UART0_RTSN	UART1_TX_M0	AUDIO_ROUT_M0	PWM2	KEY_OUT_M1		I/O	O	4	up	
38	I2C_MST0_SCL_M1/CIF_D10/I2S1_SDO0_M1/PCM_CLK_M0/GPIO0_D3_u	GPIO0_D3_u		I2C_MST0_SCL_M1	I2S1_SDO0_M1	PCM_CLK_M0	CIF_D10		I/O	O	4	up	
36	I2C_MST0_SDA_M1/CIF_D11/I2S1_SDI0_M1/PCM_SYNC_M0/GPIO0_D4_u	GPIO0_D4_u		I2C_MST0_SDA_M1	I2S1_SDI0_M1	PCM_SYNC_M0	CIF_D11		I/O	I	4	up	
41	CIF_HREF/I2S1_LRCK_TX_RX_M1/PCM_IN_M0/GPIO0_D5_d	GPIO0_D5_d		CIF_HREF	I2S1_LRCK_TX_RX_M1	PCM_IN_M0			I/O	I	4	down	
39	CIF_VSYNC/I2S1_SCLK_TX_RX_M1/PCM_OUT_M0/KEY_IN_M2/GPIO0_D6_d	GPIO0_D6_d		CIF_VSYNC	I2S1_SCLK_TX_RX_M1	PCM_OUT_M0	KEY_IN_M2		I/O	I	4	down	
40	CIF_PCLK/I2S1_MCLK_M1/KEY_OUT_M2/GPIO0_D7_d	GPIO0_D7_d		CIF_PCLK	I2S1_MCLK_M1	KEY_OUT_M2			I/O	O	4	down	
49	UART2_RX/SPI_MST2_CS0_M0/PMU_DEBUG0/GPIO1_A0_u	GPIO1_A0_u		PMU_DEBUG0	SPI_MST2_CS0_M0	UART2_RX			I/O	I	4	up	
50	UART2_TX/SPI_MST2_CLK_M0/PMU_DEBUG1/GPIO1_A1_d	GPIO1_A1_d		PMU_DEBUG1	SPI_MST2_CLK_M0	UART2_TX			I/O	I	4	down	
51	UART2_CTS/SPI_MST2_MISO_M0/I2C_MST0_SCL_M2/PMU_DEBUG2/GPIO1_A2_d	GPIO1_A2_d		PMU_DEBUG2	SPI_MST2_MISO_M0	UART2_CTS	I2C_MST0_SCL_M2		I/O	O	4	down	
52	UART2_RTS/SPI_MST2_M0SI_M0/I2C_MST0_SDA_M2/PMU_DEBUG3/GPIO1_A3_d	GPIO1_A3_d		PMU_DEBUG3	SPI_MST2_MOSI_M0	UART2_RTS	I2C_MST0_SDA_M2		I/O	O	4	down	
37	LCDC_RS/CIF_MCLK/PWM3/AUDIO_LOUT_M1/GPIO1_A4_d	GPIO1_A4_d		LCDC_RS	CIF_MCLK	PWM3	AUDIO_LOUT_M1		I/O	O	4	down	
35	LCDC_CS/SPI_MST2_CS1/PWM0/AUDIO_ROUT_M1/GPIO1_A5_d	GPIO1_A5_d		LCDC_CS	SPI_MST2_CS1	PWM0	AUDIO_ROUT_M1		I/O	I	4	down	
55	M4_DSP_JTAG_SEL/GPIO1_A6_d	GPIO1_A6_d	M4_DSP_JTAG_SEL						I/O	I	4	down	
42	32K_CLK_OUT/PCM_CLK_M1/GPIO1_A7_d	GPIO1_A7_d		32K_CLK_OUT	PCM_CLK_M1				I/O	O	4	down	
58	KEY_IN_M0/GPIO1_B6_d	GPIO1_B6_d	KEY_IN_M0						I/O	I	4	down	
57	KEY_OUT_M0/GPIO1_B7_d	GPIO1_B7_d	KEY_OUT_M0						I/O	O	4	down	
53	GPIO1_D0_d	GPIO1_D0_d							I/O	I	4	down	
56	NPOR_u	NPOR_u							I/O	I	4	up	
54	TEST_d	TEST_d							I/O	I	4	down	
24	IO_VTG_SEL_d	IO_VTG_SEL_d							I/O	I	4	down	VCCIO_1V8
16	XIN24M	XIN24M							I/O	I		NA	OSC
17	XOUT24M	XOUT24M							I/O	O		NA	

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Pin #	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type①	Def②	Driver Strength	Pull up /Pull down	IO Domain
14	MIC_IN2_N	MIC_IN2_N							A			NA	MIC
13	MIC_IN2_P	MIC_IN2_P							A			NA	
12	MIC_IN1_N	MIC_IN1_N							A			NA	
11	MIC_IN1_P	MIC_IN1_P							A			NA	
21	USB_DM	USB_DM							A			NA	USB
22	USB_DP	USB_DP							A			NA	

Notes:

①:Type: I = input, O = output, I/O = input/output (bidirectional), A = Analog

②:Output Drive Unit is mA, only Digital IO has driver strength value;

③:Def: I = input without any pull resistor, O = output without any pull resistor;

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2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR_u	I	Chip hardware reset
	TEST_d	I	Test mode enable
	IO_VTG_SEL_d	I	Control to select 3.3V or 1.8V for IO

Interface	Pin Name	Direction	Description
M4 SWJ-DP	M4_JTAG1_TCK	I	M4 JTAG interface clock input/SWD interface clock input
	M4_JTAG1_TMS	I/O	M4 JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
DSP JTAG	DSP_JTAG0_TCK	I	DSP JTAG interface clock input
	DSP_JTAG0_TMS	I	DSP JTAG interface tms input
	DSP_JTAG0_TRSTN	I	DSP JTAG interface reset input
	DSP_JTAG0_TDI	I	DSP JTAG interface data in
	DSP_JTAG0_TDO	O	DSP JTAG interface data out

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLK	O	SDIO card clock
	SDIO_CMD	I/O	SDIO card command output and response input
	SDIO_D*i* (*i*=0~3)	I/O	SDIO card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	SFC_CLK	I/O	SFC serial clock
	SFC_CS	I/O	SFC chip select signal, low active
	SFC_Di*(i=0~3)*	O	SFC serial data output

Interface	Pin Name	Direction	Description
LCDC	LCDC_RS	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_CS	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LDCC_WR	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	LCDC_RD	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_D*i* (*i*=0~7)	O	LCDC data output

Interface	Pin Name	Direction	Description
I2S1	I2S1_MCLK	I/O	I2S1 clock from or to external device
	I2S1_SCLK_RX	I/O	I2S1 receiving serial clock
	I2S1_LRCK_RX	I/O	I2S1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

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Interface	Pin Name	Direction	Description
	I2S1_SDI*i* (*i*=0~2)	I	I2S1 receiving serial data
	I2S1_SCLK_TX	I/O	I2S1 transmitting serial clock
	I2S1_LRCK_TX	I/O	I2S1 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_SDO0	O	I2S1 transmitting serial data

Interface	Pin Name	Direction	Description
PDM	PDM_IN_CLK*i* (*i*=0~1)	O	PDMIN serial output clock
	PDM_IN_DAT*i* (*i*=0~1)	I	PDMIN serial input data
	PDM_OUT_CLK*i* (*i*=0~1)	I/O	PDMOUT serial input or output clock
	PDM_OUT_DAT*i* (*i*=0~1)	O	PDMOUT serial output data

Interface	Pin Name	Direction	Description
SPI	SPI_MST*i*_CLK(*i*=0,1,2)	I/O	SPI serial clock
	SPI_MST*i*_CS(*i*=0,1,2)	I/O	SPI chip select signal, low active
	SPI_MST*i*_MOSI(*i*=0,1,2)	I/O	SPI serial data output in master mode, and input in slave mode
	SPI_MST*i*_MISO(*i*=0,1,2)	I/O	SPI serial data input in master mode, and output in slave mode

Interface	Pin Name	Direction	Description
SPI2APB	SPI_SLV0_CLK	I	SPI2APB serial clock
	SPI_SLV0_CS	I	SPI2APB chip select signal, low active
	SPI_SLV0_MOSI	I	SPI2APB serial data input
	SPI_SLV0_MISO	O	SPI2APB serial data output

Interface	Pin Name	Direction	Description
I2C2APB	I2C_SLV_SCL	I/O	I2C2APB clock
	I2C_SLV_SDA	I/O	I2C2APB data

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input or output
	PWM1	I/O	Pulse Width Modulation input or output
	PWM2	I/O	Pulse Width Modulation input or output
	PWM3	I/O	Pulse Width Modulation input or output, used for IR application recommended

Interface	Pin Name	Direction	Description
AUDIO PWM	AUDIO_LOUT	O	AUDIO PWM left channel output data
	AUDIO_ROUT	O	AUDIO PWM right channel output data

Interface	Pin Name	Direction	Description
KEY	KEY_IN	I	KEY input clock
	KEY_OUT	O	KEY output clock

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Interface	Pin Name	Direction	Description
I2C	I2C_MST*i*_SDA (*i*=0,1,2)	I/O	I2C data
	I2C_MST*i*_SCL (*i*=0,1,2)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX (*i*=0,1,2)	I	UART serial data input
	UART*i*_TX (*i*=0,1,2)	O	UART serial data output
	UART*i*_CTS (*i*=0,2)	I	UART clear to send modem status input
	UART*i*_RTS (*i*=0,2)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
USB2	USB_DP	I/O	USB 2.0 Data signal DP
	USB_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
VIP (Camera IF)	CIF_D*i*(*i*=0~11)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_PCLK	I	Camera interface input pixel clock
	CIF_HREF	I	Camera interface horizontial sync signal

Interface	Pin Name	Direction	Description
Codec ADC	MIC_IN1_P	I	Codec channel1 positive differential data
	MIC_IN1_N	I	Codec channel1 negative differential data
	MIC_IN2_P	I	Codec channel2 positive differential data
	MIC_IN2_N	I	Codec channel2 negative differential data

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Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Digital logic supply voltage	CORE_VDD	-0.3	1.26	V
Analog 0.9V supply voltage	AVDD_0V9	-0.3	1.26	V
1.8V supply voltage	DVDD_1V8 AVDD_1V8 VCCIO_1V8 USB_AVDD_1V8	-0.3	2.16	V
3.3V supply voltage	VCC_IO USB_AVDD_3V3	-0.3	3.96	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
CORE LDO power	DVDD_1V8	1.74	1.80	1.86	V
MIPI LOO and AUDIO LDO power	AVDD_1V8	1.74	1.80	1.86	V
Digital Logic power	CORE_VDD	0.81	0.90	0.99	V
Analog 0.9V power	AVDD_0V9	0.81	0.90	0.99	V
Digital GPIO Power (1.8V)	VCCIO_1V8	1.62	1.80	1.98	V
Digital GPIO Power (3.3V/1.8V)	VCC_IO	2.97 1.62	3.30 1.80	3.63 1.98	V
USB 2.0 Analog Power (1.8V)	USB_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 Analog Power (3.3V)	USB_AVDD_3V3	3.0	3.30	3.60	V
OSC input clock frequency		NA	24	NA	MHz
Ambient Operating Temperature	T_A	TBD	25	85	℃

Notes:① *Symbol name is same as the pin name in the io descriptions*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	NA	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	NA	V
	Pullup Resistor	Rpu	20	40	100	KΩ
	Pulldown Resistor	Rpd	20	40	100	KΩ
Digital GPIO @1.8V	Input Low Voltage	Vil	NA	NA	0.3*VCC	V
	Input High Voltage	Vih	0.7*VCC	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	0.75*VCC	NA	NA	V
	Pull-up Resistor	Rpu	10	22	55	KΩ
	Pull-down Resistor	Rpd	10	22	55	KΩ

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Parameters		Symbol	Min	Typ	Max	Unit
USB2	Input Low Voltage	Vil	NA	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.2	V
	Output High Voltage	Voh	VCC-0.2	NA	NA	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Iin	Vin = 3.3V or 0V	NA	1.0	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	1.0	10	uA
	High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	NA	uA
			Vin = 3.3V, pull down enabled	NA	NA	NA	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	NA	uA
			Vin = 0V, pull up enabled	NA	NA	NA	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	1.0	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	1.0	10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	NA	uA
			Vin = 1.8V, pull down enabled	NA	NA	NA	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	NA	uA
			Vin = 0V, pull up enabled	NA	NA	NA	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
INT PLL(GPLL)	Reference frequency Range	Fref		5	NA	800	MHz
	VCO Frequency Range	Fvco		625	NA	2500	MHz
	PFD Frequency Range	Fpfd		5	NA	Fvco/16	MHz
	Output Frequency Range	Fout		12	NA	2500	MHz
	Lock time	Tlt	Input clock cycle is REFDIV/Fref. Example: Fref=25MHz REFDIV=1, Lock time is 40us	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
FRAC PLL(GPLL)	Reference frequency Range (Int)	Fref		1	NA	1200	MHz
	Reference frequency Range (Frac)	Fref		10	NA	1200	MHz
	VCO Frequency Range	Fvco		800	NA	3200	MHz
	PFD Frequency Range (Int)	Fpfd		1	NA	Fvco/16	MHz
	PFD Frequency Range (Frac)	Fpfd		10	NA	Fvco/16	MHz
	Output Frequency Range	Fout		16	NA	3200	MHz

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Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Lock time	Tlt	Input clock cycle is REFDIV/Fref. Example: Fref=25MHz REFDIV=1, Lock time is 10us	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-7 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Data signaling common mode voltage range	Vhscm		-50	NA	500	mV
Squelch detection threshold	Vhssq	Squelch detected	NA	NA	100	mV
		No squelch detected	200	NA	NA	
Disconnect detection threshold	Vhsdsc		525	NA	625	mV
High-speed idle level output voltage	Vhsoi		-10	NA	10	mV
High-speed low level output voltage	Vhsol		-10	NA	10	mV
High-speed high level output voltage	Vhsoh		360	400	440	mV
Chirp-J output voltage(Differential)	Vchirpj		700	NA	1100	mV
Chirp-K output voltage(Differential)	Vchirpk		-900	NA	-500	mV
Slew rate of rising edge	Thsrlew		NA	NA	1600	V/usec
Slew rate of falling edge	Thsflew		NA	NA	1600	V/usec
Differential cable impedance	Zo		76.5	90	103.5	Ω
Common mode cable impedance	Zcm		21	30	39	Ω
Cable skew	Tskew		NA	NA	100	ps
Unmated contact capacitance	Cuc		NA	NA	2	ps
High input level	Vih		2.0	NA	NA	V
Low input level	Vil		NA	NA	0.8	V
High output level	Voh		VCC-0.2	NA	NA	V
Low output level	Vol		NA	NA	0.2	V

3.7 Electrical Characteristics for Codec ADC

Table 3-8 Electrical Characteristics for Codec ADC

Parameters	Symbol	Test condition	Min	Type	Max	Units
ADC Performance (16K Sample)						
Resolution				24		Bit
Full Scale Input Range		0dB Gain in PGA stage		0.82		Vrms
Dynamic Range		A-Weight filter open, No boost in PGA stage, -60dBFs input, 20-20K Bandwidth		85		dB
THD+N		A-Weight filter open, No boost in PGA stage, -3dBFs input, 20-20K Bandwidth		-70		dB
ADC Digital Filter Pass Band			20		7.2K	Hz
ADC Digital Filter Pass Band Ripple				0.1		dB
Crosstalk		One channel drive 100mVrms signal		85		dB
Noise Floor		PGA 21db		-103		dB
ADC Performance (48K Sample)						
Resolution				24		bit
Full Scale Input Range		0dB Gain in PGA stage		0.82		Vrms
Dynamic Range		A-Weight filter open, No boost in PGA stage, -60dBFs input, 20-20K Bandwidth		83		dB
THD+N		A-Weight filter open, No boost in PGA stage, -3dBFs input, 20-20K Bandwidth		-70		dB

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Parameters	Symbol	Test condition	Min	Type	Max	Units
ADC Digital Filter Pass Band			20		20K	Hz
ADC Digital Filter Pass Band Ripple				0.1		dB
Crosstalk		One channel drive 100mVrms signal		85		dB
Noise Floor		PGA 21db		-99		dB

3.8 Electrical Characteristics for LDO

Table 3-9 Electrical Characteristics for LDO

Parameters	Symbol	Test condition	Min	Typ	Max	Units
LDO Input Voltage			1.74	1.8	1.86	V
AUDIO LDO						
V_{OUT} Output Voltage Adjustable Range (step=50mV)			1.5	NA	1.65	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT1		NA	1.6	NA	V
Power Supply Reject Ratio	PSRR		NA	70	NA	dB
Dropout voltage @ 20mA	V_{DROP}		NA	100	NA	mV
Operating Quiescent Current, No load	I_Q		NA	20	NA	uA
Rated output current	I_{MAX}		NA	10	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		20	30	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
V_{OUT} Discharge Switch ON Resistance	R_{DIS}		NA	400	NA	Ω
CORE LDO						
V_{OUT} Output Voltage Adjustable range (step=50mV)			0.75	NA	1.05	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT2		0.877	0.9	0.923	V
V_{OUT} Load Regulation, I_{OUT} = 1mA to 200mA			NA	0.01	NA	%/mA
Power Supply Reject Ratio	PSRR		NA	50@1k	NA	dB
Dropout voltage @ 200mA	V_{DROP}		NA	500	NA	mV
Operating Quiescent Current, No load	I_Q		NA	40	NA	uA
Rated output current	I_{MAX}		NA	200	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		250	300	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
MIPI LDO						
V_{OUT} Output Voltage Adjustable range (step=50mV)			0.75	NA	1.05	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT3		0.877	0.9	0.923	V
V_{OUT} Load Regulation, I_{OUT} = 1mA to 100mA			NA	0.01	NA	%/mA
Power Supply Reject Ratio	PSRR		NA	50@1k	NA	dB
Dropout voltage @ 100mA	V_{DROP}		NA	500	NA	mV
Operating Quiescent Current, No load,	I_{Q1}		NA	40	NA	uA
Rated output current	I_{MAX}		NA	100	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		150	200	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
V_{OUT} Discharge Switch ON Resistance	R_{DIS}		NA	400	NA	Ω

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Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	29	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	6.6	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	8.69	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 4 layers, 102mmx114mm, 1.6mm thickness, Ambient temperature is 25℃.

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