MedRadio Receiver Design

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***Abstract*—In this paper, we present the design of a high gain, low power, and low noise front-end Medical Device Radiocommunications Service (MedRadio) receiver for wireless medical technology applications. We employ a low-IF architecture operating at 400 MHz using 0.18 um CMOS technology from the IBM7RF library. Cumulatively, we present individual designs for a low noise amplifier (LNA), a mixer, and a voltage controlled oscillator (VCO) that have been tuned to minimize power while matching to one another's design constraints. The receiver achieves 36 dB gain with a 3.65 dB noise figure and 1.8 mW of power consumption.**

I. Introduction

The accelerating growth of both aging populations and the number of technologically savvy, health minded citizens around the world comes with them the requirements to provide advanced new medical solutions to meet growing demand. Some of the ways these solutions have presented themselves over the last five to six years were in the form of new designs involving both integrated circuit and medical technology devices. The devices could be implantable (e.g. cochlear implants, pacemakers) or body worn (health monitoring devices, e.g. accelerometer).

To implement these technologies requires reliable wireless links that need to transmit over several feet. To meet that end, the FCC announced in 2009 the establishment of a dedicated amount of spectrum to wireless medical device technology, entitled MedRadio [1]. Selected for a frequency band that would not cause interference with other devices in a patient's daily life, MedRadio occupies the spectrum from 401 to 406 MHz and is subdivided into the following sub-bands [1, 2]:

- Two "wing" bands between 401-402 MHz and 405-406 MHz. Wing bands can be used for either body-worn devices or fully implantable ones.
- One "core" band between 402-405 MHz. The core band can be used *only* for fully implanted devices.

Additionally, the devices need to consume relatively low power while possessing the smallest possible physical footprint [3]. Reducing the power requires either reducing the supply voltage (typical applications hover around 1V to 1.8V) [3] or reducing the current required to drive the circuitry. Reducing the dimensions of the device necessitates smaller process technologies (typically 0.18 micron or lower) with minimizing circuit components as well as employing tight packaging skills when creating layouts for the circuit. The wireless nature requires that the range of the device be, nominally, greater than 2 meters [3]. This requires that the device sensitivity be quite low (around -80 dBm and lower) while having good matching to reduce reflective losses in receiving and transmitting.

Designing circuits to meet the constraints can be quite challenging for a designer. Reducing power consumption is the most important factor, but that typically comes at a cost to other values that necessitate the proper operation of the circuit such as a high gain, minimum noise figure, and maximum sensitivity. Moving forward, we present our implementation of a MedRadio receiver that seeks to meet all of the design constraints and more.

II. Receiver Architecture

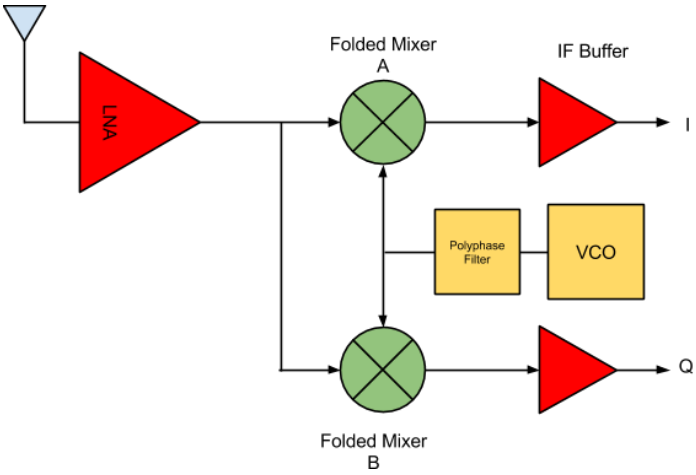

Fig. 1: Block diagram of our low-IF receiver architecture. Folder mixers A and B are meant to implement quadrature downconversion. Due to time constraints, only the LNA, mixer A, and the VCO were fully implemented and integrated.

We considered several different architectures so as to make an informed decision as to what would be the best choice for the receiver. Our final choice was the low-IF architecture, but we will include what demotivated us towards selecting the other available ones. Primarily, we referred to Razavi [4] when studying each architecture choice.

A. Receiver Tradeoffs

1) Direct Conversion: We have a channel bandwidth of 300 kHz in the 402-405 MHz core band and 100 kHz in the 401-402 MHz, 405-406 MHz sidebands. This channel bandwidth being downconverted directly would expose it to damaging flicker noise since CMOS technology is the primary circuit component in the LNA, filter, et cetera. Additionally, there are DC offset and local oscillator leakage problems that will contribute further to signal degradations.

2) Super Regenerative: Super regenerative receiver architectures have very good gains for the frequency range MedRadio operates at but requires a low number of interferers from neighboring bands and channels. The positive feedback architecture can serve to amplify noise to an unstable degree. As such, it suffers from poor selectivity, sensitivity (can be from 5-20 dB lower than heterodyne architectures), data rates, and has limited demodulation capability.

3) Dual-IF: Dual down conversion allows for both good channel selection and image rejection. However, multiple mixers increase the complexity of the circuit layout and requires additional band select, image reject, and channel selection components along the chain. This makes it difficult to manage reasonable linearity with good noise, power dissipation, and gain. So this wont work for our application either. Also, we want to avoid as many mixing spurs as possible and multiple image problems.

4) Zero-Second IF: This fixes the secondary image problem from Dual-IF but doesnt fix the other issues. Additionally, it operates in the baseband – where the flicker noise is the highest! This is unfeasible for us.

B. Target Architecture: Low-IF

Low-IF is an optimal choice for this type of application. The spectrum can be downconverted to a point where the Q factor is much lower and circuits can be designed using lower, optimal values. Downconverting the signal to a low frequency that isn't inside of the baseband (as in zero-IF) can help to avoid degradation from flicker noise of the MOSFETs. Additionally, there is better frequency isolation in this architecture because the IF frequency can be selected such that the difference between the local oscillator (LO) frequency and the RF frequency is quite small.

The downsides to this selection is that there are tradeoffs betwen image rejection and channel selection. High-IF implementations causes substantial image rejection since the image would be far outside of the bandwidth of the image-reject filter. However, this allows for close-by interferers to be allowed in with the spectrum of interest. Similarly, low-IF implementations cause substantial channel rejection by narrowly selecting the spectrum but allowing in images that are nearby to be downconverted to the same point. This issue, however, can be fixed by implementing quadrature downconversion after the mixer.

III. Circuit Design

A. Low Noise Amplifier

Low noise amplifiers(LNA) are typically one of the starting blocks in the front end receiver chain. LNAs need to exhibit low noise, high gain, and low power dissipation. The linearity doesn't need to be so good, but it can't be so bad as to limit the overall linearity of the chain. The noise figure needs to be low because the noise figure of the system can be approximately equal to the noise figure of the first block, assuming there is no other block in the system that isn't so large that it won't be scaled by the gain of the prior blocks.

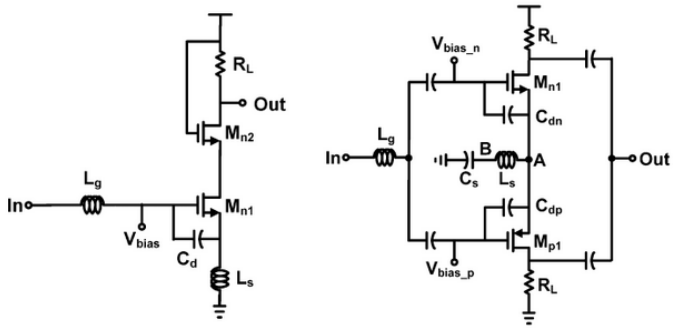

Fig. 2: Cascode (left) and Current Reuse (right) structure, both figures borrowed from Cha et. al [5].

1) Design Procedure: As shown in Figure 2, there are two structures that are popularly used when designing LNAs: cascode [4] and current reuse [5].

It isn't clear exactly which structure would be better: cascode or current-reuse. As such, what follows is our analysis of current reuse to figure out if there are any problems with it.

With the current reuse structure, the active components are heavily restrained so as to limit the power consumption [5]. As such, the passive networks depicted in Fig. 2 perform much of the gain [5]. The power consumption is minimized by using this kind of structure since we need a small operating current to activate the MOSFETs and we will achieve gain from the other components. Additionally, the two transistors in the current reuse structure can be biased into subthreshold region to minimize the power consumption. The g_m parameter of this component is the g_m of NMOS plus the g_m of the PMOS. In this way, the effective transconductance is larger than it would be otherwise. The gain of the current reuse LNA is:

$$A_v = \frac{g_{mtot}}{2R_s\omega_0 C_{gs}} Z_{load} \tag{1}$$

The C_{gs} given in (1) is the total C_{gs} of the stacked transistor pair. The input matching should be matched to 50 Ω. From the gates of the transistors, the input impedance would be given by:

$$Z_{in}(j\omega) = \frac{g_m L_s}{C_{gs}} + j[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}] \tag{2}$$

The real part in (2) should be matched to 50 Ω, and imaginary part should be matched to 0 Ω. Input matching is a simple problem. Output matching, however, is much more difficulty. Examining the output impedance:

$$Z_{out}(j\omega) = r_0 + j\omega \frac{(r_0 g_{mtot} L_s + L_s - \omega^2 L_s L_g C_{gs})}{1 - (L_s + L_g)C_{gs}\omega^2} \tag{3}$$

The imaginary part has the same two poles, but also the pole which is considered to be the center frequency. At the

center frequency, the imaginary part diverges to infinity – this makes it difficult to do the output matching. Because of this reason, we switched back to the cascode structure is used.

In the cascode structure, the common source amplifier is the main amplifier. By applying the common gate, we can get good reverse isolation since there is no connecting path for current to flow between the ports when the gate is an AC ground [4]. Fortunately, the input impedance of this structure is the same as the current reuse one (2). Thus, the input matching can be easily achieved. The output impedance of the cascode structure is given by:

$$Z_{out}(j\omega) = \frac{SLR_L}{j\omega L + R_L - \omega^2 LCR_L} \tag{4}$$

At the center frequency, the output impedance can be made equal to the load resistance of the next stage. Next, we consider the gain parameters of this structure. The gain is given by:

$$A_v = \frac{R_L}{2\omega_0 L_s} \tag{5}$$

The load resistor and center frequency are fixed parameters. To get a high gain with this LNA, the only free parameter that can be adjusted is the source degenerated inductor. However, this inductor is selected in such a way as to perform input matching. This is where the iterative design process begins to take off and now all the components can be carefully selected to get good results.

B. Mixer

A mixer takes two signals and produces an output that contains both the sum and the difference of the frequencies of the original signals. Mixers can be subclassed into active mixers and passive mixers. For our purposes, we need the mixer stage to exhibit some gain to meet design criteria so passive mixers were never considered.

Internally, active mixers split down into single balanced and double balanced mixers. Double-balanced mixers can provide better input linearity, relatively low noise, and completely isolate the LO to RF ports resulting in very little feedthrough when compared to single balanced mixers. The cons are that the circuit requires large off-chip baluns/transformers to split the signal outputs if the other components do not do it already.

1) Design Procedure: The typical mixer implementation is a standard Gilbert cell [6], which is a stock double-balanced mixer. The Gilbert cell original design doesn't have low noise, consumes relatively high power (for MedRadio), and needs to operate from a much larger supply voltage (must be capable of activating all transistors across ground). We employed the modified Gilbert cell from Krcmar et. al [7]. It is pictured in Fig. 3.

The advantages of this circuit is that the biasing of the switching pairs and the transconductors are now totally separated, allowing it to operate at a lower supply voltage without weakening circuit operationc̃itekrcmar1. The transconductors have control over the gain portion of the circuit and need to have careful current control through them, hence a current sink

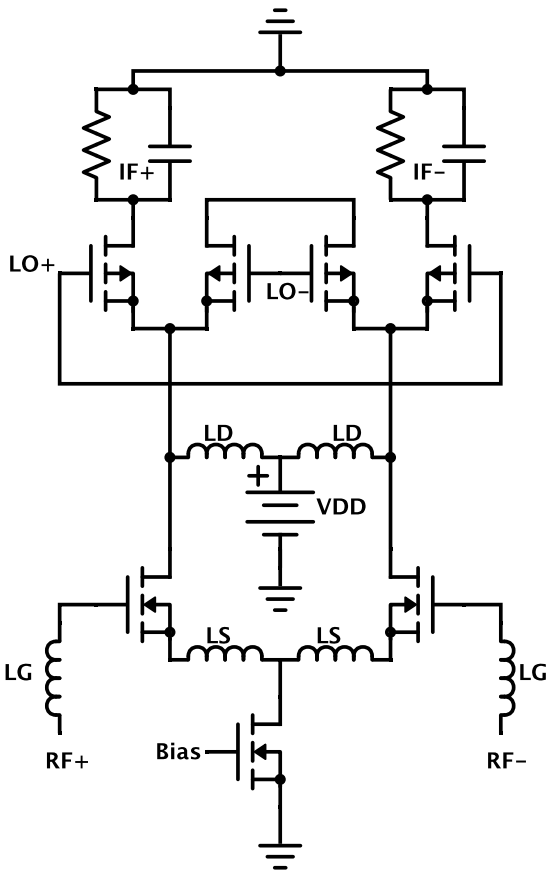

Fig. 3: Circuit schematic of the modified Gilbert cell [7] used in our mixer. The top row of PMOS transistors are the switching pairs. The middle row of NMOS transistors are the transconductors with current being driven by the current sink at the bottom.

is connected to the source of the MOSFETs. For the switching pairs, the PMOS are biased to be barely on; mostly off. The VCO signal will come into the switching pairs and quickly switch it into saturation and then back out again. It is to our disadvantage if the switching pairs enter the triode region since that will reduce the linearity and cause the gain to compress faster [4].

The source and gate inductors connected to the transconductors are selected for input matching and to resonate the circuit. The drain inductor is sized to resonate with the VCO's parasitic source capacitance [7]. Accordingly, the input impedance is given by:

$$Z_{in}(j\omega) = \frac{g_m}{C_{gs}} L_{source} + j(\omega[L_{source} + L_{gate}] - \frac{1}{\omega C_{gs}}) \tag{6}$$

The resonance frequency is given by:

$$\omega = \frac{1}{\sqrt{C_{gs}(L_{source} + L_{gate})}} \tag{7}$$

The source inductor is selected to match to an input resistance:

$$L_{source} = \frac{R_{input}}{\frac{g_m}{C_{gs}}} \tag{8}$$

While the gate inductor is selected to achieve resonance at the input frequency to the transconductors:

$$L_{gate} = \frac{1 - \omega^2 L_{source} C_{gs}}{\omega^2 C_{gs}} \tag{9}$$

With these equations, the values of the gate and drain inductors can be properly chosen. The conversion gain of the double balanced mixer is given typically by [4]:

$$C.G. = \frac{2}{\pi} g_m Z_{out} \tag{10}$$

Because of the input matching the transconductance term is modified and the final equation becomes:

$$C.G. = \frac{1}{\pi} \frac{g_m Z_{out}}{\sqrt{(1 - \omega^2 L_{source} C_{gs})^2 + (\omega L_{source} g_m)^2}} \tag{11}$$

As a starting point, we made an assumption for the value of C_{gs} using estimates culled from the IBM7RF [8] library for the NMOS transistors and also assumed the output impedance was a single load resistor matched to 50 Ω. Using that, we were able to make substitutions into the C.G. equation and solved for the desired value of the transconductance. After that, the input inductors were sized using the previous equations and assuming a center frequency of 403.5 MHz. Our initial design estimate assumed the current to start at 1 mA and we were able to get the sizing ratio using the below:

$$\frac{W}{L} = \frac{g_m^2}{2 K_n I} \tag{12}$$

Finally, the drain inductor values were obtained assuming simple resonance:

$$L_{drain} = \frac{1}{\sqrt{\omega_{VCO}^2 C_{gs}}} \tag{13}$$

At this point, the circuit was fully sized and allowed us to begin iterating the design to achieve the desired results. The parameters that affected our results the most are as follows:

- Width. This affected virtually every figure of merit (noise, gain, linearity), so it had to be tuned with great care. Accordingly, we wanted to keep the width below the millimeter scale at all costs.
- Switching DC bias and VCO swing. The DC bias of the LO PFETs was selected at a point where the VCO would have to swing as little as possible to switch the transistor from off to saturation (in order to reduce VCO power consumption). This primarily affected the gain and linearity of the circuit.
- Transistor fingers. The more fingers available lowered the parasitics of the transconductor stages. Increasing the fingers led to improved noise figure and linearity.
- Input impedance. The value of the input impedance had a large effect on our noise figure; we opted to increase the value we input matched to in order to reduce our overall noise.
- Output impedance. We needed to increase the gain without increasing the current. The only way to do that was to increase the size of the load resistor.
- Inductor values. The inductor values needed to be swept to compensate for tradeoffs between linearity and gain. The source inductor was kept relatively constant but the gate and drain inductors were tweaked often in an effort to improve the linearity of the mixer.

These are a small subset of the variables used when iterating over the design. Results are discussed later on.

C. Voltage Controlled Oscillator

As shown in Figure 4, the proposed single-ended VCO uses a pair of complementary PN-MOSFETs so that the DC current can be reused and a low power VCO can be realized, following the logic given by Jang et. al [9]. The LC tank determines the oscillation frequency:

$$\omega_0 = \frac{1}{\sqrt{L_2 C_V}} \tag{14}$$

Note that, C_V includes the varactors as well as the parasitic gate-source and drain-source capacitors of the PN-MOSFETs. The varactors are used to tune the VCO oscillation frequency and the transistors are configured to provide a negative resistance to compensate for the tank loss.

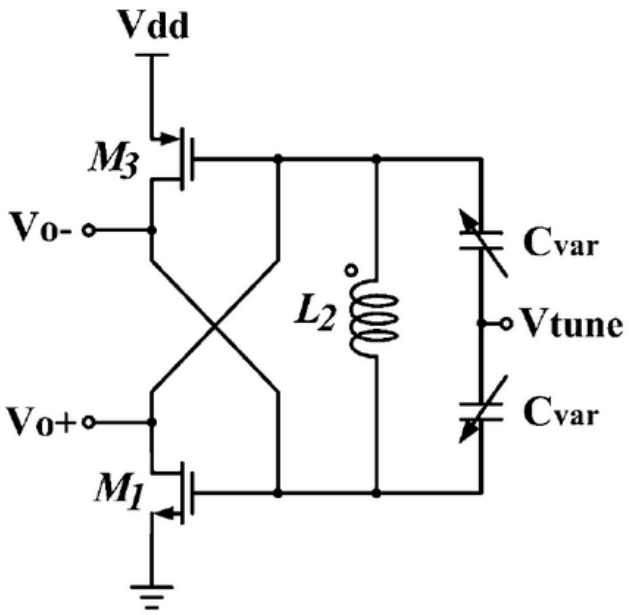

Fig. 4: Schematic of the VCO, borrowed from Jang [9].

The NMOS has the dimension of $\frac{W}{L} = \frac{30}{0.18}$ and the PMOS has the dimension of $\frac{W}{L} = \frac{200}{0.18}$, both in micro. The values for inductor and varactors are optimized to center the oscillation frequency at 400 MHz.

IV. Results

A. Low Noise Amplifier

Fig. 5 shows the S11 parameters of the LNA, which indicates the input matching quality. The minimum input matching is -21 dB. Fig. 6, the S22, output matching is presented. The minimum matching point is -33 dB. Also, the gain (S21 parameters) can be seen from Fig. 7. This LNA provides a relative high gain, 17.5 dB. To show the linearity property of the LNA, the 1 dB compression point plot is presented in Fig. 8. From the figure, the 1 dB compression point is -16.46 dBm. Also, the IIP3 is preformed in cadence simulation, which is shown in Fig. 9. The IIP3 point is -7.77 dBm. Noise Figure and minimum Noise Figure of the LNA is presented In Fig. 10 and Fig. 11 respectively. The Noise Figure is 3.4 dB and the minimum Noise Figure is 1.2 dB. To match the design requirement, the DC power consumption of the LNA is 0.57 mW. Final LNA results can be found in TABLE I.

S11	-21 dB
S21	17.50 dB
S22	-33 dB
NF	3.40 dB
NF_{min}	1.2 dB
IIP3	-7.77 dBm
1 dB Compression	-16.46 dBm
Power Consumption	0.57 mW

TABLE I: Final results from LNA simulations

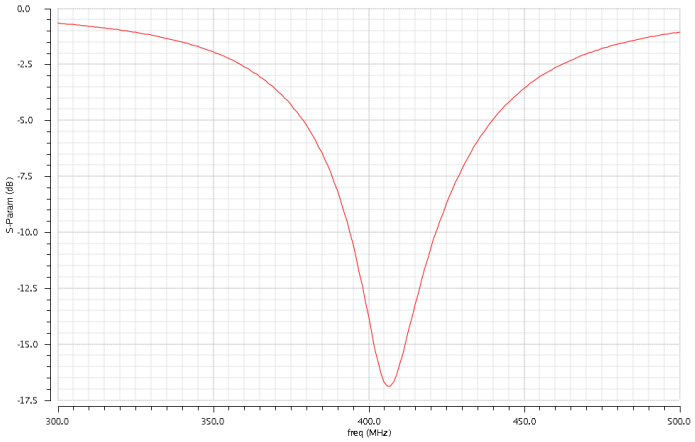

Fig. 5: Graph of LNA S11 input matching

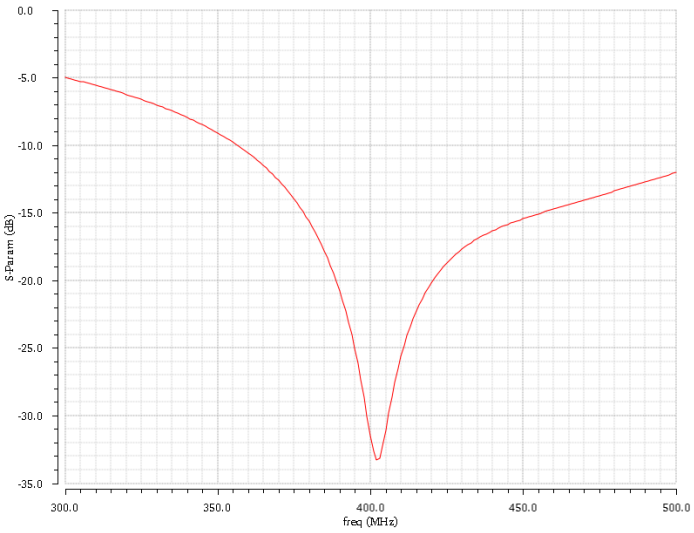

Fig. 6: Graph of LNA S22 output matching

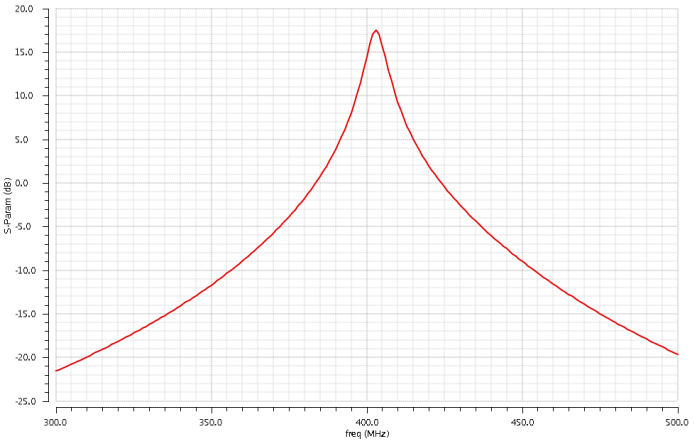

Fig. 7: Graph of LNA S21 gain

B. Mixer

Although the assignment only asked to see conversion gain with respect to frequency as shown in Fig. 12 we also simulated for conversion gain with respect to input power as shown in Fig. 13. These graphs show that the mixer is able to maintain good gain across the frequencies of interest as well as consistent gain across sensitivities as low as -100 dBm. Fig. 14 and Fig. 15 show the VCO feedthrough to the input and output ports. As can be seen in the graphs, the setup of the mixer causes these figures to be very low. The noise of the mixer was found to be 4.40 dB as shown in Figure 16. Lastly, the linearity of the mixer can be found in Fig. 17. The linearity is quite lower than expected however this was a trade-off to achieve a high gain and low noise. Final mixer results can be found in TABLE II.

Conversion Gain	10.50 dB
LO-IF Feedthrough	-75.06 dB
LO-RF Feedthrough	-103.40 dB
NF	4.40 dB
IIP3	-13.26 dBm
Power	0.8 mW

TABLE II: Final results from Mixer simulations

C. Voltage Controlled Oscillator

Fig. 18 shows the simulated output transients of the proposed VCO; the VCO provides two differential outputs with

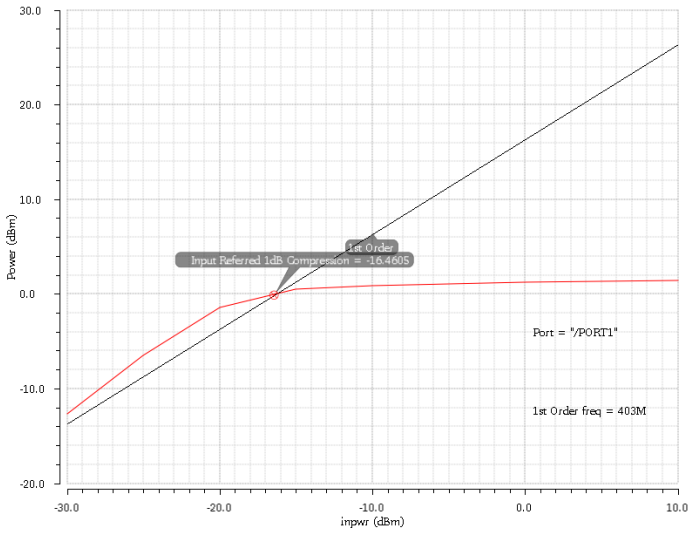

Fig. 8: LNA 1 dB compression point

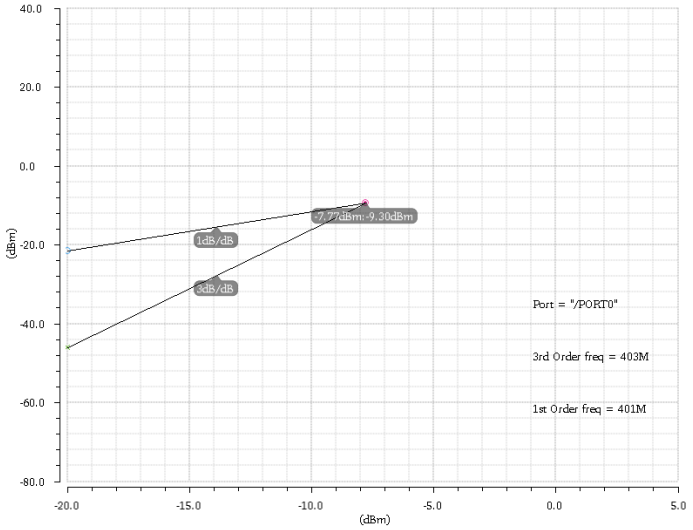

Fig. 9: LNA Linearity

the same peak-peak value of 305 mV. The oscillation frequency can also be calculated from the period of sinusoidal waveform, which is 400 MHz. The phase noise is shown in Fig. 19 and it is -119 $\frac{dBc}{Hz}$ at 1 MHz offset from the center frequency of 400 MHz. Fig. 20 plots the simulated tuning curve by varying the controllable voltage. As the tuning voltage sweeps from -0.5 V to 1 V, the oscillation frequency changes from 393 MHz to 400 MHz, indicating a tunable range of 6 MHz. The VCOs power consumption, which is a critical consideration in MedRadio application, is 0.2 mW. A table of results can be found in TABLE III.

Tuning Range	6 MHz
Phase Noise	-119 $\frac{dBc}{Hz}$
Power	0.2 mW

TABLE III: Final results from VCO simulations

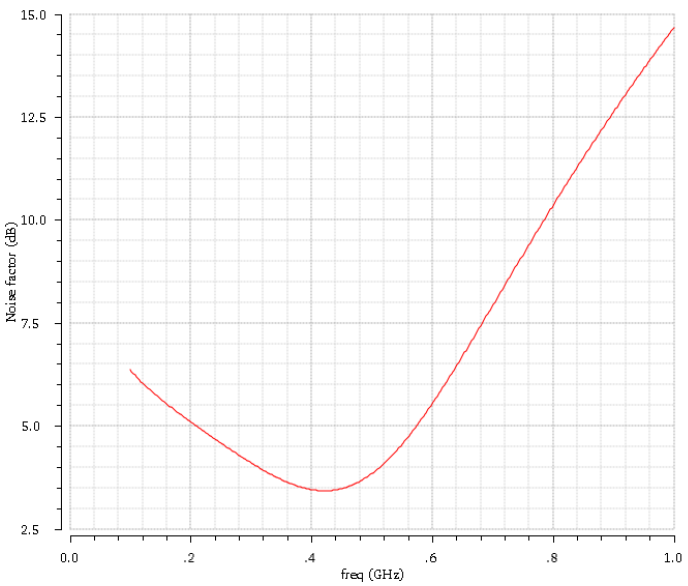

Fig. 10: Graph of LNA noise figure

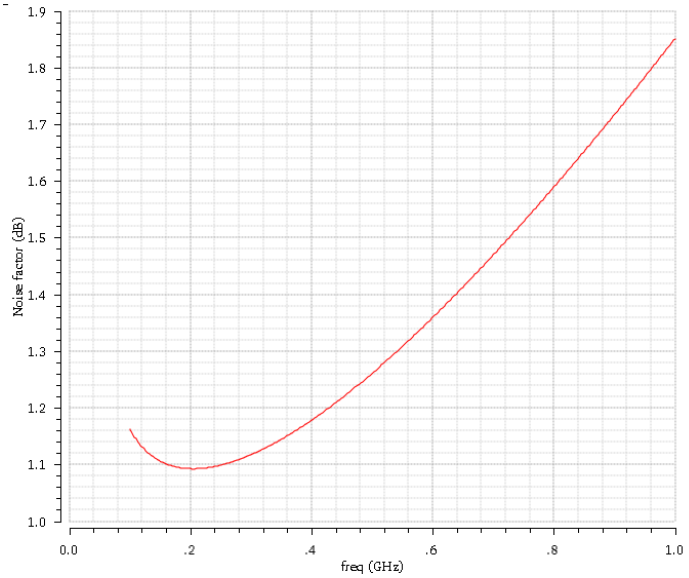

Fig. 11: Graph of LNA minimum noise figure

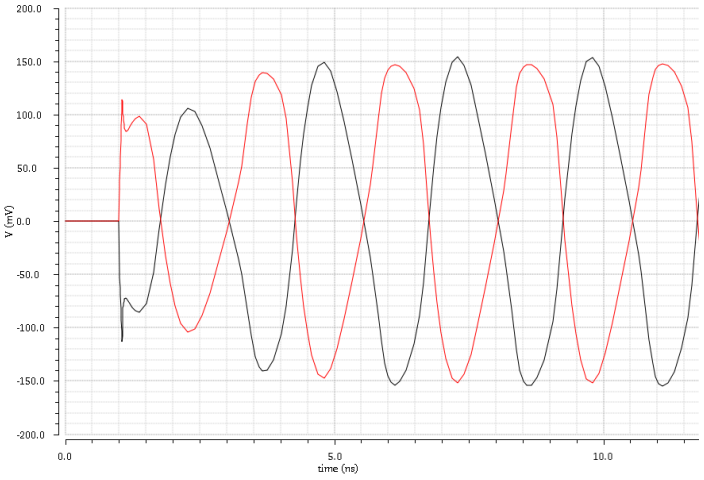

Fig. 18: Graph of VCO transient response

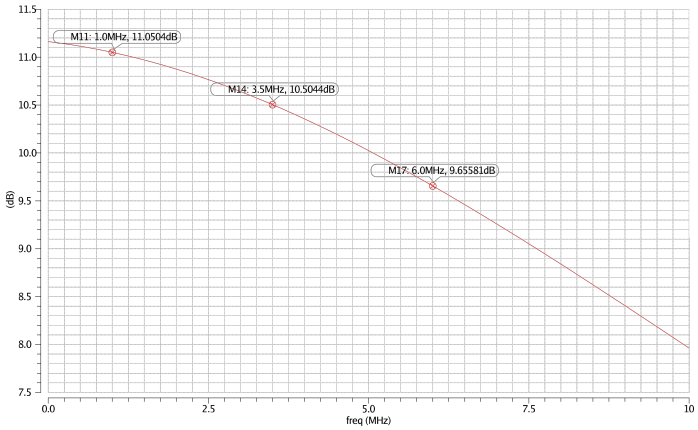

Fig. 12: Mixer conversion gain with respect to frequency

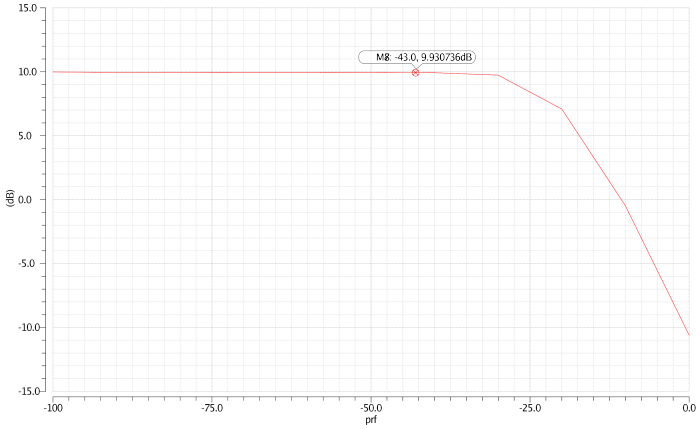

Fig. 13: Mixer conversion gain with respect to input power

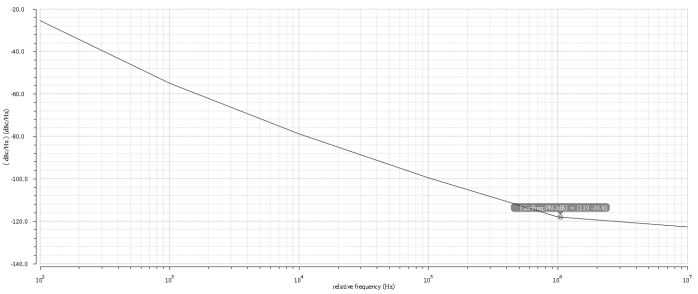

Fig. 19: Graph of VCO phase noise

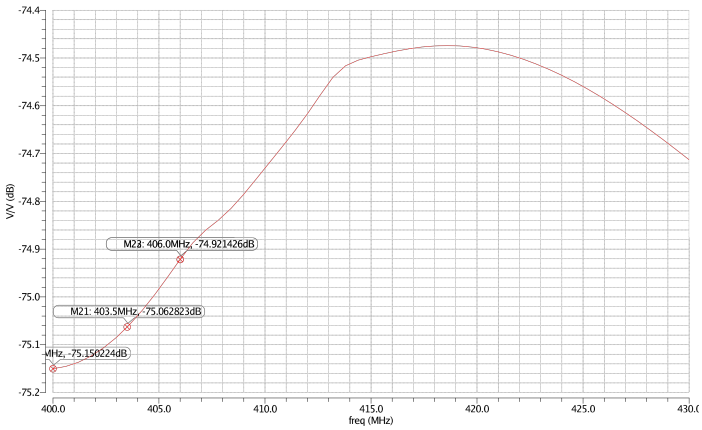

Fig. 14: Mixer oscillator to IF output feedthrough

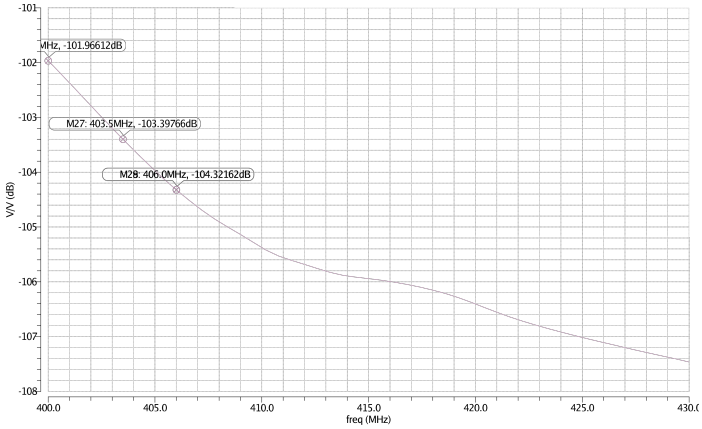

Fig. 15: Mixer oscillator to RF input feedthrough

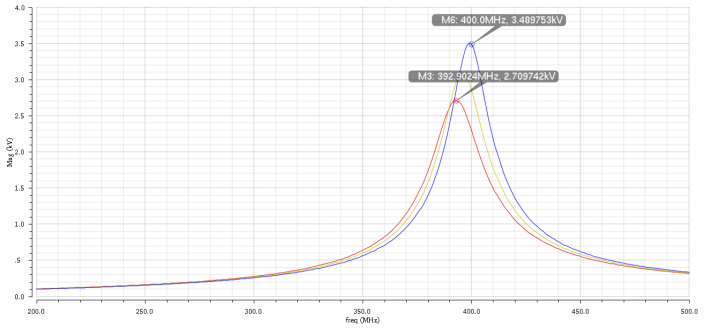

Fig. 20: Graph of VCO tuning curve

V. System Integration

Since it was known ahead of time that the receiver was to be fully integrated together, a lot of effort was put towards perfecting input and output matching to guarantee maximum power transfer across components. The LNA input, VCO output, and Mixer output are all matched to 50 Ω. The LNA output and Mixer signal input are matched to 500 Ω, we found this to help improve the gain of the Mixer. Since all of the components were matched properly, full system integration was as simple as placing the components together (Fig. 21).

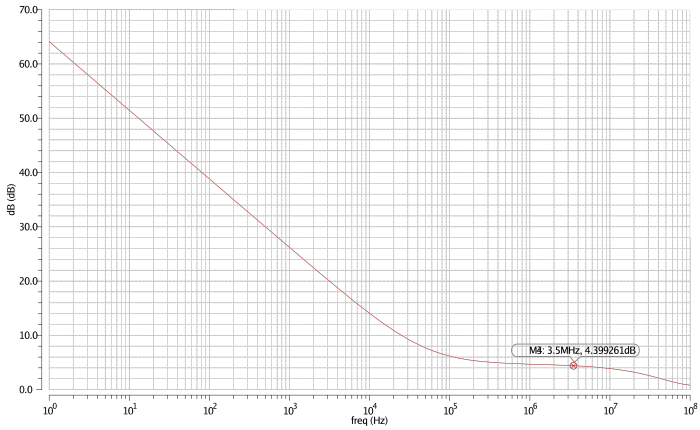

Fig. 16: Graph of Mixer Noise Figure

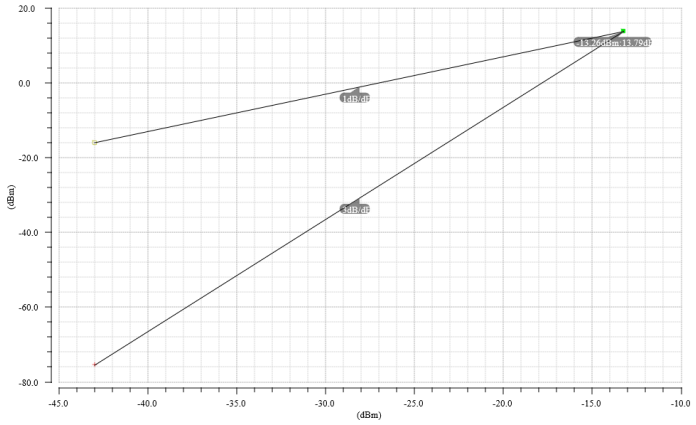

Fig. 17: Graph of Mixer linearity

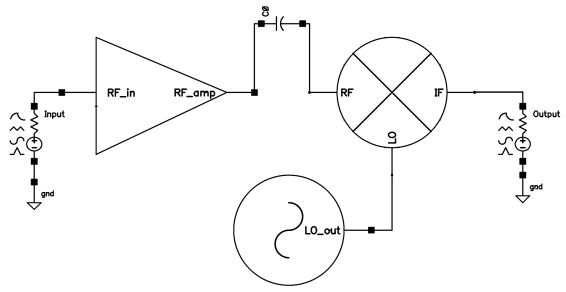

Fig. 21: Full system circuit integration, with LNA, Mixer, and VCO. Coupling capacitor removes DC offset from LNA.

In order to test the system, a transient analysis was preformed with an initial input signal of 1 mV at 403.5 MHz. Fig. 22 shows a clean output response from the system that swings from 55 mV to -70 mV at 3.5 MHz. This leads to an overall swing of 62.5 mV, therefore the conversion gain of the entire system is $20log(\frac{62.5mV}{1mV})$ or **35.92 dB**.

In order to measure the Noise Figure, the VCO was removed and an ideal source was used instead. Although the

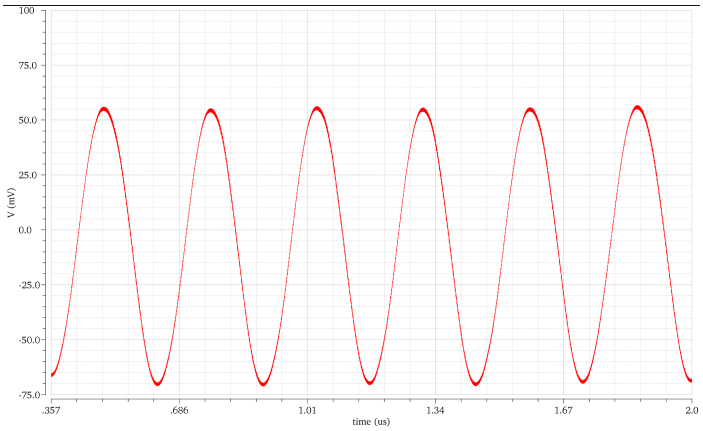

Fig. 22: Transient response of receiver after 357ns startup time.

oscillator in theory would contribute slightly to the noise, it was determined that due to its low LO-IF feed-through that the oscillator has a negligible effect to the total noise. Fig. 23 shows the total noise of the system, at the corner frequency of the output, it was determined that the total noise was **3.65 dB**.

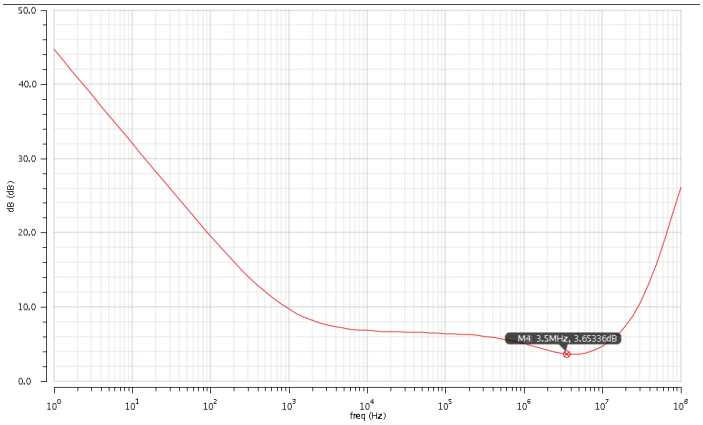

Fig. 23: Full system noise due to LNA and Mixer.

The overall linearity of the system is about **-31 dBm** however a graph is not shown due to technical issues with the Cadence software. Overall the full system results can be found in TABLE IV.

Conversion Gain	35.92 dB
Noise Figure	3.65 dB
IIP3	-31 dBm
Power	1.8 mW

TABLE IV: Final results from system integration.

VI. Conclusions

To summarize: we implemented a front end receiver using 0.18 μm CMOS technology. The LNA has a cascode topology with current reuse and the mixer was a modification of a Gilbert cell with separate PMOS switching pairs and NMOS transconductors.

Future work on this receiver would have to be to improve the linearity and lower the power consumption. The linearity of the system is limited by the linearity of the mixer, which operated at a less-than-expected -12 dBm. According to Razavi [4], the gain of the LNA reduces the linearity of the mixer. This in turn reduces the linearity of the overall system, since the linearity of the chain can be approximated to be equal to the linearity of the last block in the receiver chain divided by the gain of the preceding blocks. Since the LNA gain was high and the mixer linearity was already low, it resulted in sub-par total linearity for the total system.

Improvements to the LNA would most likely include a change to the current-reuse topology, it is believed that this would lead to a better linearity and lower power consumption, however within the time constraints of the project, the implemented cascode works well for our purposes.

To improve the linearity of the mixer requires extremely precise and careful iteration over the device parameters. The switching pairs DC bias and oscillator swing voltage need to be tuned more carefully to increase the linearity without sacrificing too much of the total gain. Additionally, high side injection could be used with the VCO instead of low-side injection. This would mean the oscillator is switching even faster, keeping the switches in triode for a shorter transition period and thus improving the linearity. A different way would be to tweak the inductor values without sacrificing too much gain. A third way would be to both increase the supply voltage and reduce the current so as to keep power consumption minimal.

A current reuse VCO structure is proposed to provide the LO frequency of 400 MHz while only 0.2 mW power is consumed and achieving a tunable frequency range of 6 MHz. To further improve the VCO performance, two single-ended half-circuit oscillators can be combined into one differential circuit. Theoretically, this structure will offer a larger tunable frequency range while consuming nearly the same power.

Overall, the entire receiver achieves a gain of 36 dB which is much greater than the project requirements of 25 dB. The Noise Figure is almost five times less than the specifications of 15 dB at 3.65 dB. The only problem with our design is the low linearity which did not meet the final specification of -25 dBm where instead this receiver is -31 dBm. However, the total power consumption is 1.8 mW which is fairly small, it is also possible to improve this by implementing some of the changes proposed here. The final results are neatly summarized in TABLE V.

Value	Assigned	Proposed	Actual
Gain	>25 dB	>28.7 dB	36 dB
Noise Figure	<15 dB	<5.5 dB	3.65 dB
IIP3	>-25 dBm	-25 dBm	-31 dBm

TABLE V: Summary of total results. Assigned are the values given in the assignment, proposed are the target ones we set to achieve, and actual are the final results we got.

REFERENCES

[1] FCC. (2008) Medical device radiocommunications service (medradio). [Online]. Available: http://www.fcc.gov/encyclopedia/medical-device-radiocommunications-service-medradio

[2] H.-K. Cha, M. Raja, X. Yuan, and M. Je, "A cmos medradio receiver rf front-end with complementary current-reuse lna for biomedical applications," in *Solid State Circuits Conference (A-SSCC), 2010 IEEE Asian*, Nov 2010, pp. 1–4.

[3] P. Bradley, "Wireless medical implant technology: Recent advances and future developments," in *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, Sept 2011, pp. 37–41.

[4] B. Razavi, *RF Microelectronics*. Reading, MA: Prentice Hall, 2011.

[5] H.-K. Cha, M. Raja, X. Yuan, and M. Je, "A cmos medradio receiver rf front-end with a complementary current-reuse lna," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 59, no. 7, pp. 1846–1854, July 2011.

[6] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *Solid-State Circuits, IEEE Journal of*, vol. 3, no. 4, pp. 365–373, Dec 1968.

[7] M. Krcmar, V. Subramanian, M. Deen, and G. Boeck, "High gain low noise folded cmos mixer," in *Wireless Technology, 2008. EuWiT 2008. European Conference on*, Oct 2008, pp. 13–16.

[8] IBM, "Foundry technologies: 180-nm cmos, rf cmos and sige bicmos," IBM, NY, Tech. Rep. G224-7148-02, Aug. 2012.

[9] S.-L. Jang, C.-C. Liu, C.-Y. Wu, and M.-H. Juang, "A 5.6 ghz low power balanced vco in 0.18 μ m cmos," *Microwave and Wireless Components Letters, IEEE*, vol. 19, no. 4, pp. 233–2 35, April 2009.