

MedRadio Receiver Design

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Abstract—In this paper, we present the design of a high gain, low power, and low noise front-end Medical Device Radiocommunications Service (MedRadio) receiver for wireless medical technology applications. We employ a low-IF architecture operating at 400MHz using 0.18 μm CMOS technology from the IBM7RF library. Cumulatively, we present individual designs for a low noise amplifier (LNA), a mixer, and a voltage controlled oscillator (VCO) that have been tuned to minimize power while matching to one another's design constraints. The receiver achieves 36dB gain with a 3.65dB noise figure and 1.8mW of power consumption.

I. INTRODUCTION

include description of the targeted application, introduction of the problem with relevant literature review [1], [2].

The accelerating growth of both aging populations and the number of technologically savvy, health minded citizens around the world comes with them the requirements to provide advanced new medical solutions to meet growing demand. Some of the ways these solutions have presented themselves over the last five to six years were in the form of new designs involving both integrated circuit and medical technology devices. The devices could be implantable (e.g. cochlear implants, pacemakers) or body worn (health monitoring devices, e.g. accelerometer).

To implement these technologies requires reliable wireless links that need to transmit over several feet. To meet that end, the FCC announced in 2009 the establishment of a dedicated amount of spectrum to wireless medical device technology, entitled MedRadio. Selected for a frequency band that would not cause interference with other devices in a patient's daily life, MedRadio occupies the spectrum from 401 to 406 MHz and is subdivided into the following sub-bands:

- Two “wing” bands between 401-402 MHz and 405-406 MHz. Wing bands can be used for either body-worn devices or fully implantable ones.
- One “core” band between 402-405 MHz. The core band can be used *only* for fully implanted devices.

Additionally, the devices need to consume relatively low power while possessing the smallest possible physical footprint. Reducing the power requires either reducing the supply voltage (typical applications hover around 1V to 1.8V) or reducing the current required to drive the circuitry. Reducing the dimensions of the device necessitates smaller process technologies (typically 0.18 micron or lower) with minimizing circuit components as well as employing tight packaging skills when creating layouts for the circuit. The wireless nature requires that the range of the device be, nominally, greater than 2 meters. This requires that the device sensitivity be quite low

(around -80dBm and lower) while having good matching to reduce reflective losses in receiving and transmitting.

Designing circuits to meet the constraints can be quite challenging for a designer. Reducing power consumption is the most important factor, but that typically comes at a cost to other values that necessitate the proper operation of the circuit such as a high gain, minimum noise figure, and maximum sensitivity. Moving forward, we present our implementation of a MedRadio receiver that seeks to meet all of the design constraints and more.

II. RECEIVER ARCHITECTURE

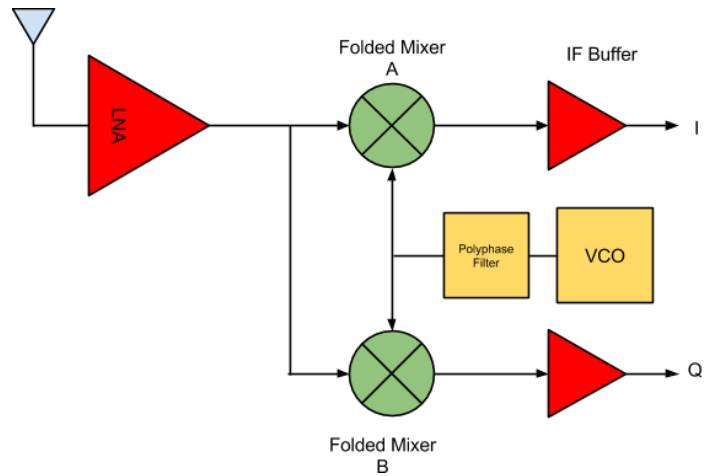


Fig. 1: Block diagram of our low-IF receiver architecture. Folder mixers A and B are meant to implement quadrature downconversion. Due to time constraints, only the LNA, mixer A, and the VCO were fully implemented and integrated.

We considered several different architectures so as to make an informed decision as to what would be the best choice for the receiver. Our final choice was the low-IF architecture, but we will include what demotivated us towards selecting the other available ones.

A. Receiver Tradeoffs

1) *Direct Conversion*: We have a channel bandwidth of 300 kHz in the 402-405 MHz core band and 100 kHz in the 401-402 MHz, 405-406 MHz sidebands. This channel bandwidth being downconverted directly would expose it to damaging flicker noise since CMOS technology is the primary circuit component in the LNA, filter, et cetera. Additionally, there are DC offset and local oscillator leakage problems that will contribute further to signal degradations.

2) *Super Regenerative*: Super regenerative receiver architectures have very good gains for the frequency range MedRadio operates at but requires a low number of interferers from neighboring bands and channels. The positive feedback architecture can serve to amplify noise to an unstable degree. As such, it suffers from poor selectivity, sensitivity (can be from 5-20 dB lower than heterodyne architectures), data rates, and has limited demodulation capability.

3) *Dual-IF*: Dual down conversion allows for both good channel selection and image rejection. However, multiple mixers increase the complexity of the circuit layout and requires additional band select, image reject, and channel selection components along the chain. This makes it difficult to manage reasonable linearity with good noise, power dissipation, and gain. So this won't work for our application either. Also, we want to avoid as many mixing spurs as possible and multiple image problems.

4) *Zero-Second IF*: This fixes the secondary image problem from Dual-IF but doesn't fix the other issues. Additionally, it operates in the baseband – where the flicker noise is the highest! This is unfeasible for us.

B. Target Architecture: Low-IF

Low-IF is an optimal choice for this type of application. The spectrum can be downconverted to a point where the Q factor is much lower and circuits can be designed using lower, optimal values. Downconverting the signal to a low frequency that isn't inside of the baseband (as in zero-IF) can help to avoid degradation from flicker noise of the MOSFETs. Additionally, there is better frequency isolation in this architecture because the IF frequency can be selected such that the difference between the local oscillator (LO) frequency and the RF frequency is quite small.

The downsides to this selection is that there are tradeoffs between image rejection and channel selection. High-IF implementations causes substantial image rejection since the image would be far outside of the bandwidth of the image-reject filter. However, this allows for close-by interferers to be allowed in with the spectrum of interest. Similarly, low-IF implementations cause substantial channel rejection by narrowly selecting the spectrum but allowing in images that are nearby to be downconverted to the same point. This issue, however, can be fixed by implementing quadrature downconversion after the mixer.

III. CIRCUIT DESIGN

include three sub-sections: one for LNA, one for Mixer and one for VCO. For each subsection discuss the design procedure (describe the circuit architecture, provide justification, and describe your approach for determining the size of transistors and the values of passive elements), include transistor-level schematic, simulation results, and a table summarizing the performance metrics of the circuit.

A. Low Noise Amplifier

As shown in Figure 1, there are two structures are popular used in the design of LNA, cascade structure and current-reuse structure.

As the current reuse structure, the two common source amplifiers use the same drain to source current. The power consumption is minimized by using this kind of structure. Also, the gm parameter of this component is the g_m of nFET plus the gm of pFET. In this way, the gain of this structure has been increased. The gain of the current reuse LNA is:

$$\frac{g_{mtot}}{2R_s\omega_0C_{gs}}Z_{load} \quad (1)$$

Here the C_{gs} in 1 is the total C_{gs} of nFET and pFET. Also, the two transistors in the current reuse structure can be biased into subthreshold region to minimize the power consumption. The input matching should be matched to 50 Ω . From the gates of the transistors, input impedance is:

$$\frac{g_m L_s}{C_{gs}} + j[\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}] \quad (2)$$

The real part in 2 should be matched to 50 Ω , and imaginary part should be matched to 0 Ω . The input can be easily matched. The output, however, is difficult to be matched. The output impedance of this structure is:

$$r_0 + j\frac{\omega(r_0 g_{mtot} L_s + L_s - \omega^2 L_s L_g C_{gs})}{1 - (L_s + L_g)C_{gs}\omega^2} \quad (3)$$

The imaginary part has the two same poles, also the pole is considered to be the central frequency. At the central frequency, the imaginary part goes to infinite, which makes it difficult to do the output matching. Because of this reason, cascade structure is used.

In cascade structure, the common source amplifier is the main amplifier. By applying the common gate, a good reverse isolation property is obtained. Fortunately, the input impedance of this structure is the same as the current reuse one (2). Thus, the input matching can be easily achieved. The output impedance of the cascade structure is (ignore channel length modulation):

$$\frac{SLR_L}{SL + R_L - \omega^2 LCR_L} \quad (4)$$

At the central frequency, the output impedance equals to the load resistance. For matching the output, the load resistance is similar to the input impedance of next stage of the system, which is 500 Ω . To analysis the gain parameters, the equation of cascade structure gain is derived:

$$\frac{R_L}{2\omega_0 L_s} \quad (5)$$

The load resistor and central frequency is fixed. To get a high gain LNA, the only free parameter can be adjusted is the source degenerated inductor. But, this inductor can affect the input matching. Therefore, the value of all of the components should be carefully selected. Cadence simulator is used to do the simulation of the proposed LNA.

assuming a center frequency of 403.5 MHz. Our initial design estimate assumed the current to start at 1mA and we were able to get the sizing ratio using the below:

$$\frac{W}{L} = \frac{g_m^2}{2K_n I} \quad (12)$$

Finally, the drain inductor values were obtained assuming simple resonance:

$$L_{drain} = \frac{1}{\sqrt{\omega_{VCO}^2 C_{gs}}} \quad (13)$$

At this point, the circuit was fully sized and allowed us to begin iterating the design to achieve the desired results. The parameters that affected our results the most are as follows:

- Width. This affected virtually every figure of merit (noise, gain, linearity), so it had to be tuned with great care. Accordingly, we wanted to keep the width below the millimeter scale at all costs.
- Switching DC bias and VCO swing. The DC bias of the was selected at a point where the VCO would have to swing as little as possible to switch the transistor from off to saturation (in order to reduce VCO power consumption). This primarily affected the gain and linearity of the circuit.
- Transistor fingers. The more fingers available lowered the parasitics of the transconductor stages. Increasing the fingers led to improved noise figure and linearities.
- Input impedance. The value of the input impedance had a large effect on our noise figure; we opted to increase the value we input matched to in order to reduce our overall noise.
- Output impedance. We needed to increase the gain without increasing the current. The only way to do that was to increase the size of the load resistor.
- Inductor values. The inductor values needed to be swept to compensate for tradeoffs between linearity and gain. The source inductor was kept relatively constant but the gate and drain inductors were tweaked often in an effort to improve the linearity of the mixer.

These are a small subset of the variables used when

C. Voltage Controlled Oscillator

As shown in Figure /refvco, the proposed single-ended VCO uses a pair of complementary np-MOSFETs so that the dc current can be reused and a low power VCO can be realized [1]. The LC tank will determine the oscillation frequency by:

Note that, C_v includes varactors, gate-source and drain-source capacitors of np-MOSFETs. The varactors are used to tune the VCO oscillation frequency. And on the other hand, the transistors are configured to provide a negative resistance to compensate the tank loss.

FIGURE HERE

The nMOS has the dimension of $L/W = 0.18/30$ and the pMOS has the dimension of $L/W = 0.18/200$, both in μm . The values for inductor and varactors are optimized to center the oscillation frequency at 400 MHz. Note that, for better estimation of the VCO performance, all the capacitors, inductors and resistors are used as non-ideal components in the Cadence simulation.

IV. RESULTS

A. Low Noise Amplifier

Fig. 3 shows the S11 parameters of the LNA, which indicates the input matching quality. The minimum input matching is -21 dB. Fig. 4, the S22, output matching is presented. The minimum matching point is -22 dB. Also, the gain (S21 parameters) can be seen from Fig. 5. This LNA provides a relative high gain, 17.5 dB. To show the linearity property of the LNA, the 1 dB compression point plot is presented in Fig. 7. From the figure, the 1 dB compression point is ?? . Also, the IP3 is done by cadence simulation, which is shown in Fig. 6. The IP3 point is. What is more, noise figure should be presented to analysis the LNA. In Fig. 8 and Fig. 9, we display the noise figure and minimum noise figure of the proposed LNA. The noise figure is 3.4 dB and the minimum noise figure is 1.2 dB. To match the design requirement, the DC power consumption of the LNA is 0.57 mW.

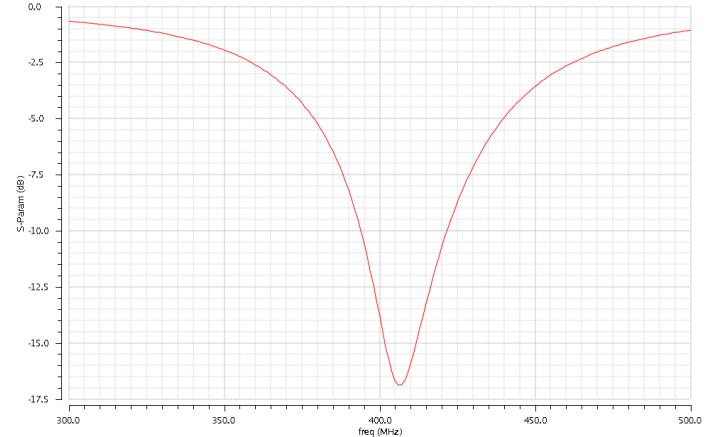


Fig. 3: Graph of LNA S11 input matching

B. Mixer

Although the assignment only asked to see conversion gain with respect to frequency as shown in Fig. 10 we also simulated for conversion gain with respect to input power as shown in Fig. 11. These graphs show that the mixer is able to maintain good gain across the frequencies of interest as well as consistent gain across sensitivities as low as -100 dBm. Fig. 12 and Fig. 13 show the VCO feedthrough to the input and output ports. As can be seen in the graphs, the setup of the mixer causes this these figures to be very low. The noise of the mixer was found to be 4.40 dB as shown in Fig. 14. Lastly, the linearity of the mixer can be found in Fig. 15. The linearity is quite lower than expected however this was a trade-off to achieve a high gain and low noise. Final mixer results can be found in TABLE I.

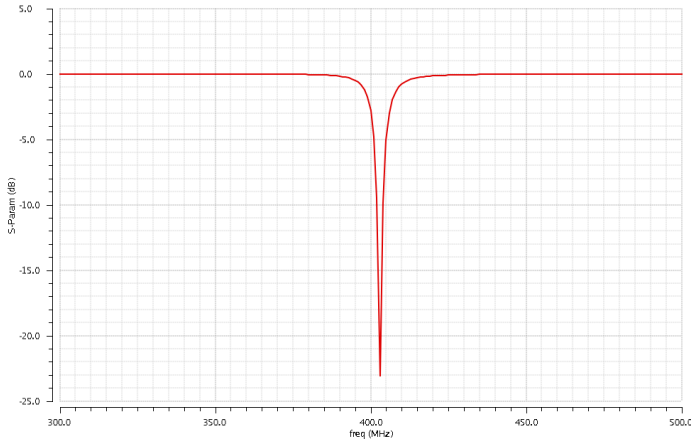


Fig. 4: Graph of LNA S22 output matching

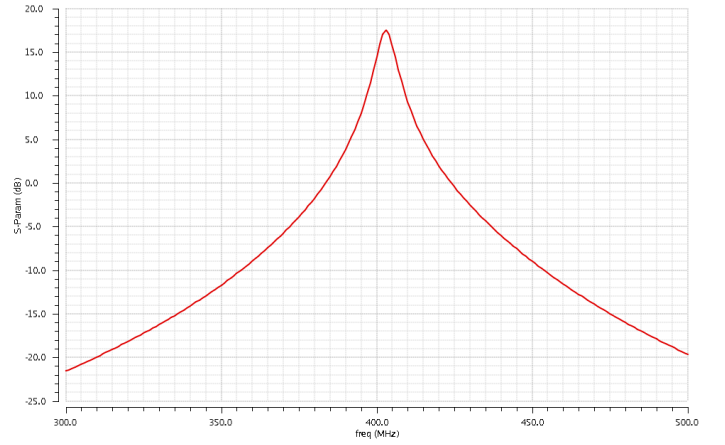


Fig. 6: LNA 1 dB compression point

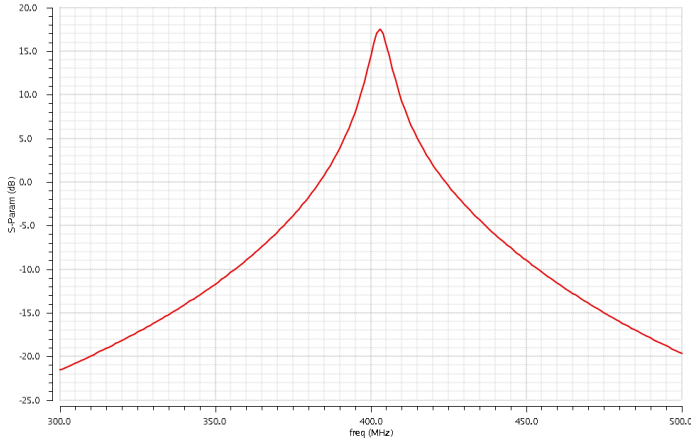


Fig. 5: Graph of LNA S21 gain

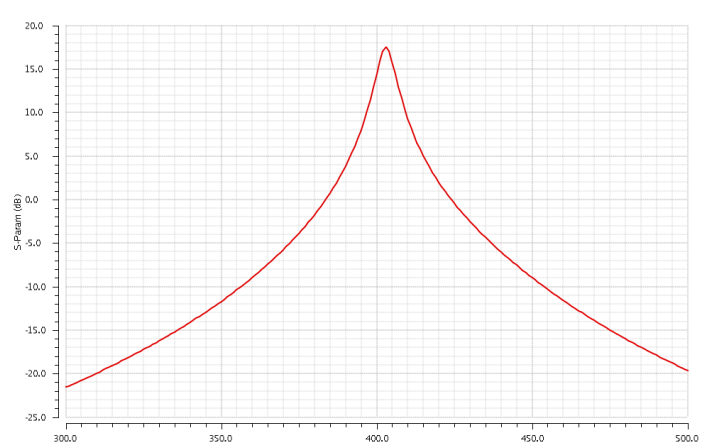


Fig. 7: LNA Linearity

C. Voltage Controlled Oscillator

Fig. 16 shows the simulated output transients of the proposed VCO; the VCO provides two differential outputs with the same peak-peak value of 305 mV. The oscillation frequency can also be calculated from the period of sinusoidal waveform, which is 400 MHz. The phase noise is shown in Fig. 17 and it is $-119 \frac{dBc}{Hz}$ at 1MHz offset from the center frequency of 400 MHz. Fig. 18 plots the simulated tuning curve by varying the controllable voltage. As the tuning voltage sweeps from -0.5 V to 1 V, the oscillation frequency changes from 393 MHz to 400 MHz, indicating a tunable range of 6 MHz. The VCOs power consumption, which is a critical consideration in MedRadio application, is 0.2 mW. A table of results can be found in TABLE II.

V. SYSTEM INTEGRATION

Since it was known ahead of time that the receiver was to be fully integrated together, a lot of effort was put towards perfecting input and output matching to guarantee maximum power transfer across components. The LNA input, VCO output, and Mixer output are all matched to 50 ohms. The LNA output and Mixer signal input are matched to 500 ohms, we found this to help improve the gain of the Mixer. Since all of

the components were matched properly, full system integration was as simple as placing the components together (Fig. 19).

In order to test the system, a transient analysis was performed. An initial input signal of 1mV at 403.5MHz was used to test the system. Fig. 20 shows a clean output response from the system that swings from 55mV to -70mV at 3.5MHz. This leads to an overall swing of 62.5mV, therefore the conversion gain of the entire system is $20\log(\frac{62.5mV}{1mV})$ or **35.92 dB**.

In order to measure the noise figure, the oscillator was removed and an ideal source was used instead. Although the oscillator in theory would contribute slightly to the noise, it was determined that due to its low LO-IF feed-through that the oscillator has a negligible effect to the total noise. Fig. 21 shows the total noise of the system, at the corner frequency of the output, it was determined that the total noise was **3.65 dB**.

The overall linearity of the system is about **-31 dBm** however a graph is not shown due to technical issues with the Cadence software. Overall the full system results can be found in TABLE III.

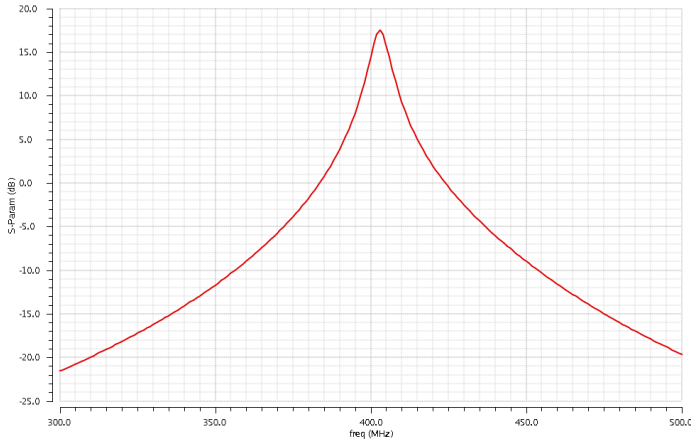


Fig. 8: Graph of LNA noise figure

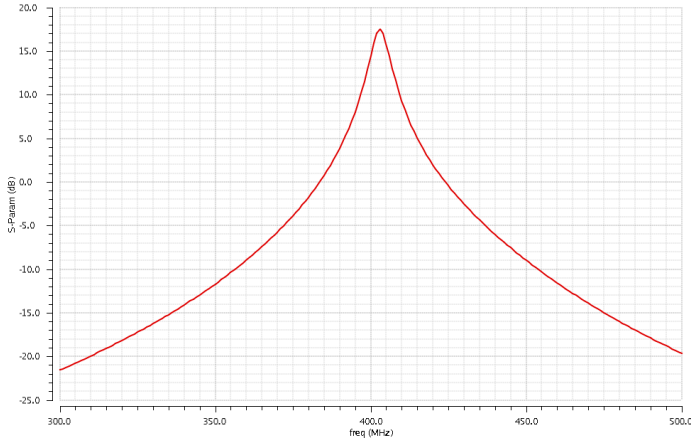


Fig. 9: Graph of LNA minimum noise figure

VI. CONCLUSIONS

summarize the report and suggest future work to further improve the performance of your receiver

A current reuse VCO structure is proposed to provide the LO frequency of 400 MHz. Only 0.2 mW power is consumed. A tunable frequency range of 6 MHz is achieved.

To further improve the VCO performance, two single-ended half-circuit oscillators can be combined into one differential circuit. Theoretically, this structure will offer larger tunable frequency range while consume nearly the same power.

REFERENCES

- [1] H.-K. Cha, M. Raja, X. Yuan, and M. Je, "A cmos medradio receiver rf front-end with complementary current-reuse lna for biomedical applications," in *Solid State Circuits Conference (A-SSCC), 2010 IEEE Asian*, Nov 2010, pp. 1–4.
- [2] —, "A 1-v 1.2-mw cmos medradio receiver for biomedical applications," in *Microw. Opt. Technol. Lett.*, Sept 2012, p. 54: 28212825.

Conversion gain	10.50 dB
LO-IF feedthrough	-75.06 dB
LO-RF feedthrough	-103.40 dB
Noise Figure	4.40 dB
IIP3	-13.26 dBm
Power	0.8 mW

TABLE I: Final results from Mixer simulations

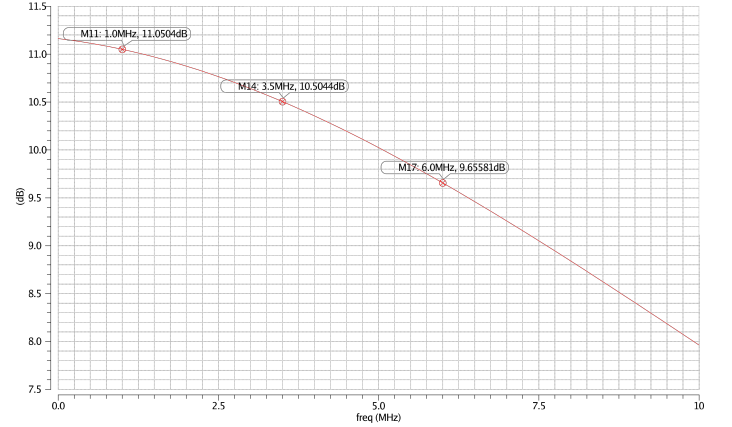


Fig. 10: Mixer conversion gain with respect to frequency

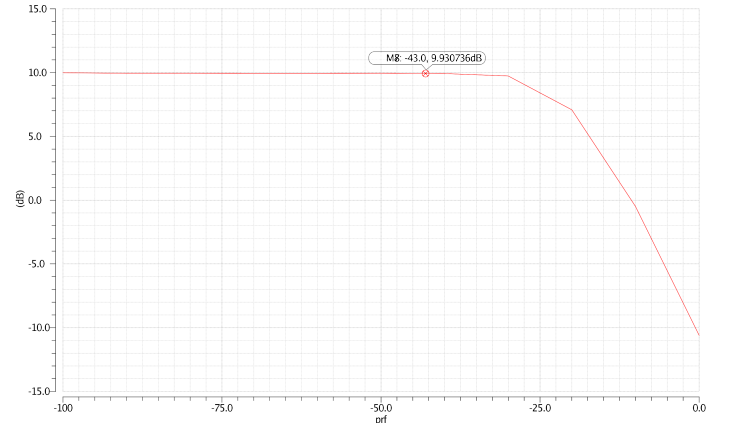


Fig. 11: Mixer conversion gain with respect to input power

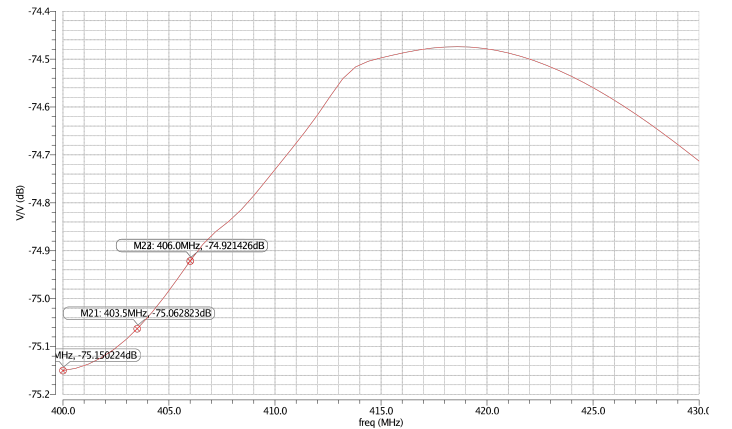


Fig. 12: Mixer oscillator to IF output feedthrough

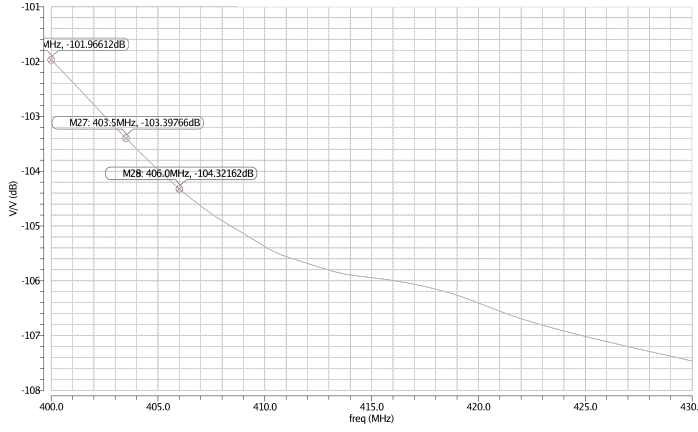


Fig. 13: Mixer oscillator to RF input feedthrough

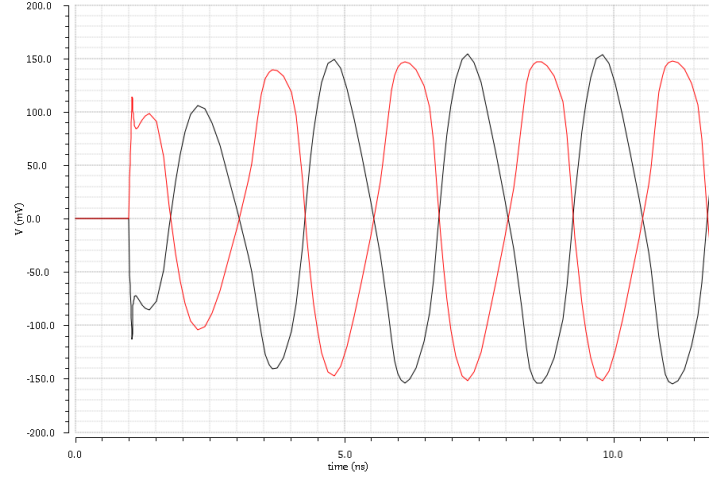


Fig. 16: Graph of VCO transient response

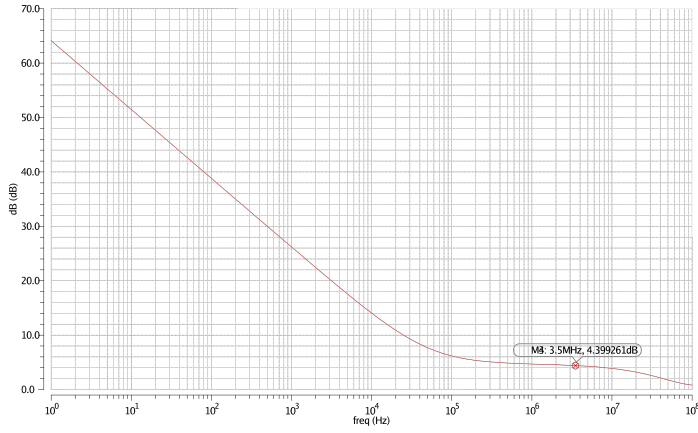


Fig. 14: Graph of Mixer Noise Figure

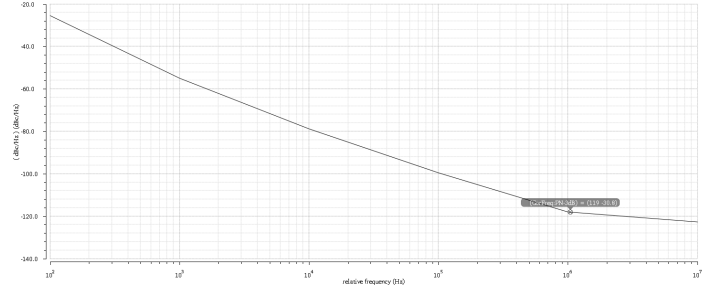


Fig. 17: Graph of VCO phase noise

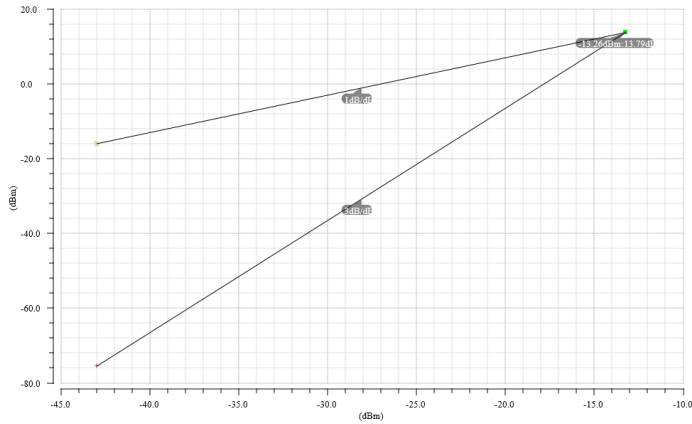


Fig. 15: Graph of Mixer linearity

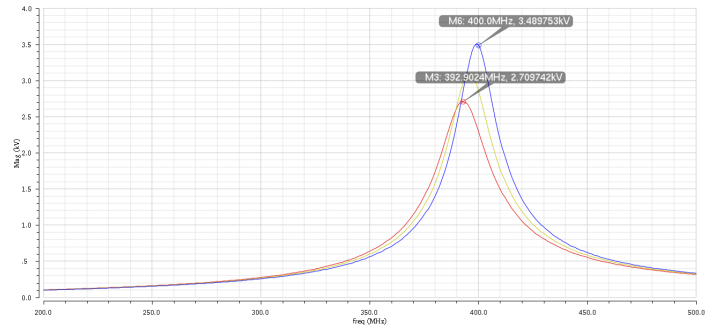


Fig. 18: Graph of VCO tuning curve

Tuning Range	6 MHz
hline Phase noise	-119 $\frac{dBc}{Hz}$
Power	0.2 mW

TABLE II: Final results from VCO simulations

Conversion Gain	35.92 dB
Noise Figure	3.65 dB
IIP3	-31 dBm
Total Power	1.8mW

TABLE III: Final results from system integration

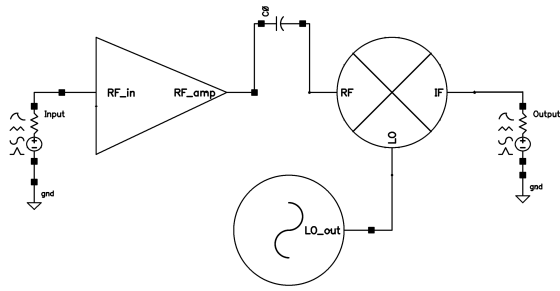


Fig. 19: Full system circuit integration, comprised of a Low Noise Amplifier, Mixer, and Voltage Controlled Oscillator. Coupling capacitors are used to remove the DC offset from the LNA.

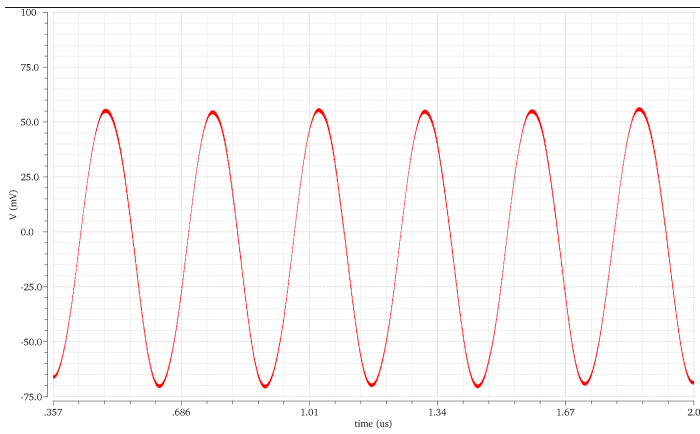


Fig. 20: Transient response of receiver after 357ns startup time

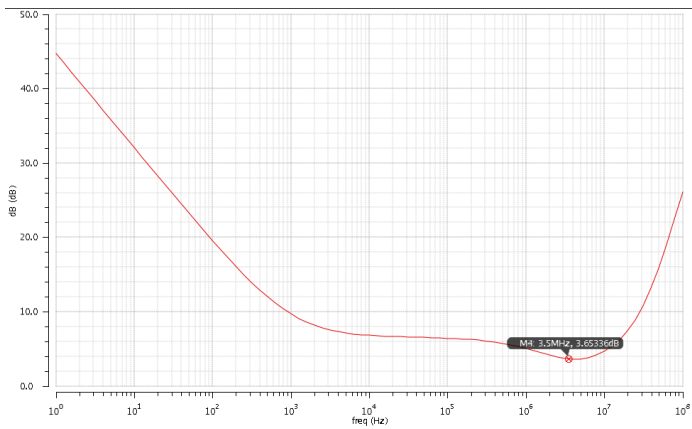


Fig. 21: Full system noise due to LNA and Mixer