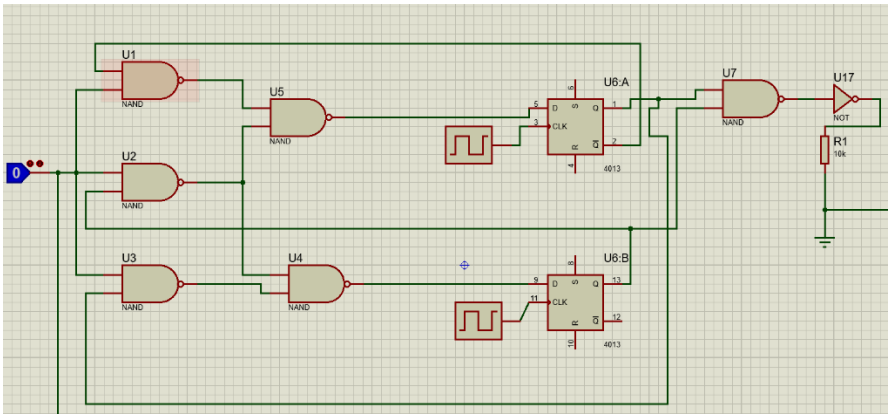
Digital Circuits Laboratory report	**Year 2020** **Number of the exercise: 4**
1. Name and surname (author of realized circuit/this report): Nykonchuk Illia, 245693 CAD[1]	**Title of the exercise: Analysis of synchronous circuit**
2. Name and surname (author of the second circuit/report): CAD[1]	
Laboratory group number[2]: Z00-38e Breadboard number:	Week day[3]: Thursday Realization date: 03.11.20 Hours of the lab: 17:05-18:45

Analysis of the circuit

The following circuit is the example of synchronous circuit in which the changes in the state are synchronized by a clock signal. It is performed by using D flip-flops – it provides a solution since it “allows” the pulse to enter to the next elements only when it was clocked.

Converted circuit using only NAND gates and 1 NOT gate



Excitation tables of flip-flops

D1:

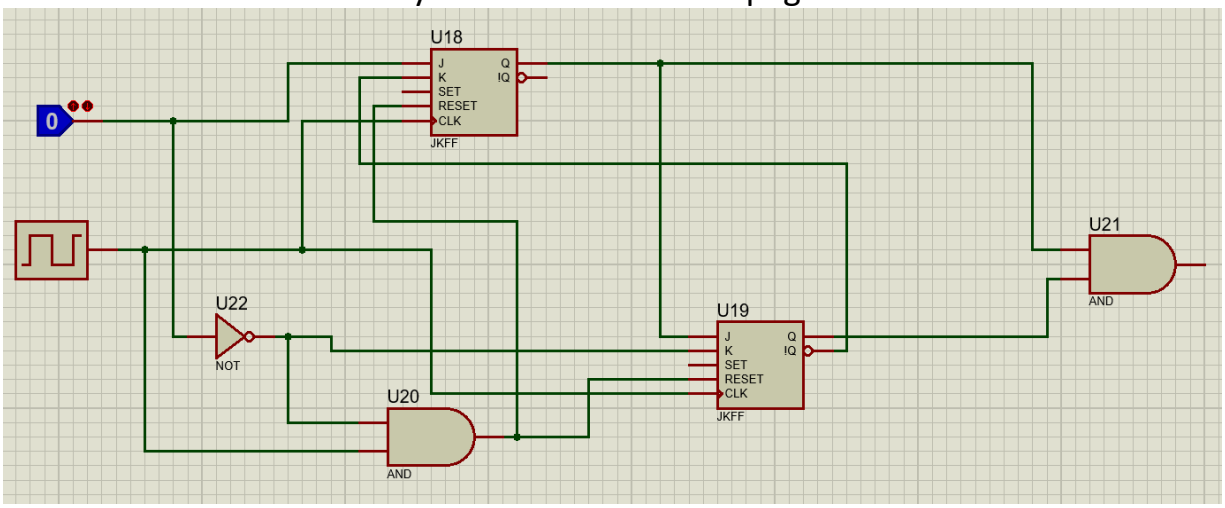
Y1	Y1*	X	Y2
0	0	0	0
0	1	1	x
1	0	x	x
1	1	1	1

D2:

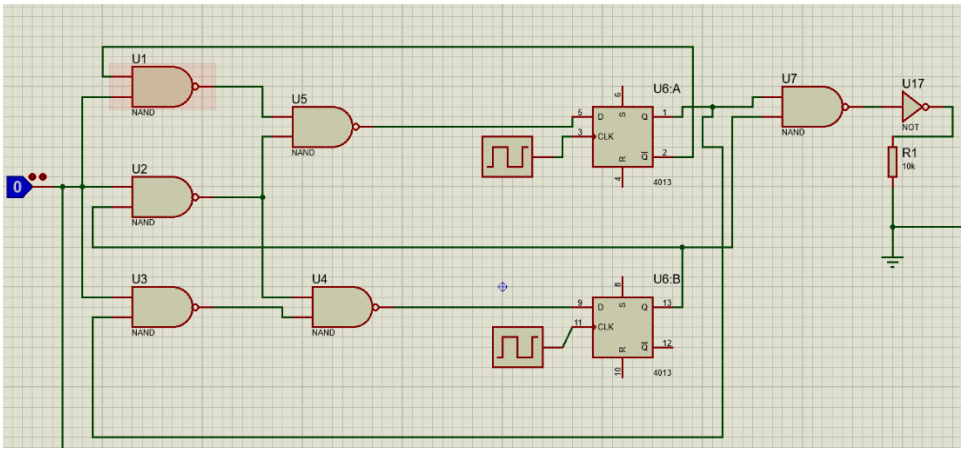
Y2	Y2*	X	Y1
0	0	x	x
0	1	1	1
1	0	0	x
1	1	1	x

Where Y – initial value. last columns mean which value we should have to get instead of of Y

Circuit with JK flip-flops with 1xNOT and 2xAND gates that behaves exactly as the circuit on the page 1



a) Default circuit



b) Table of transitions-outputs

y_1y_2 \ X	0	1	Z
00	00	10	0
01	00	11	1
10	00	01	0
11	00	11	1

c)

Results of experiment

time	t_1	t_2	t_3	t_4	t_5	t_6
X	1	1	1	1	0	0
y_1y_2	00	01	10	11	10	00
Z	0	0	0	1	0	0

d) Schematic of realized circuit