1. Using geometric means of normalized execution times
    A. We can easily predict the execution time
    B. We cannot predict the execution time (CORRECT)
    C. Depending on the workload, sometimes we can predict the execution time and sometimes not
    D. No correct answer

2. How can we calculate the physical memory address when using memory segmentation?
    A. We need to concatenate the offset from virtual address and physical segment address taken from the segment table
    B. We need to add the offset from virtual and physical segment address taken from the segment table (CORRECT)
    C. It is a virtual address
    D. No correct answer
3. When external memory occurs?
    A. When we use memory segmentation
    B. When we use memory paging (CORRECT)
    C. No correct answer
    D. When we use memory segmentation or memory paging
4. When we use procedure calls we need to save addresses, how we can do it?
    A. We have two basic conventions: *caller saving*, that means that the called procedure must save unrestrained and *callee saving* when the calling procedure must save the register that it wants preserved for access after the call
    B. We have two basic conventions: *callee saving*, that means that the called procedure must save unrestrained and *caller saving* when the calling procedure must save the register that it wants preserved for access after the call (CORRECT)
    C. We can use global variables
    D. No correct answer
5. What it means that the cache is one-way set associative?
    A. It means that each block has only one place it can appear in the cache (CORRECT)
    B. It means that the block can be placed in a restricted set of places in the cache
    C. It means that block can be placed anywhere in the cache
    D. No correct answer
6. A (2,3)-predictor uses:
    A. 2-bit global history to choose from among 8 predictors for each branch address
    B. 3-bit global history to choose among 4 predictors for each branch address
    C. 2-bit global history to choose among 4 predictors for each branch address (CORRECT)
    D. No correct answer
7. Hardware-based speculation combines the following key ideas:
    A. Dynamic branch prediction, dynamic scheduling and speculation dependences are solved (CORRECT)
    B. Static branch predictions, dynamic scheduling and speculation dependences are solved
    C. Static branch predictions and register renaming
    D. No correct answer
8. What it means that the cache is fully associative?
    A. It means that each block has only one place it can appear in the cache
    B. It means that block can be placed in a restricted set of places in the cache
    C. It means that block can be placed anywhere in the cache (CORRECT)
    D. No correct answer
9. In the delayed branch, the sequential successor
    A. Is executed whether or not the branch is taken (CORRECT)
    B. Is executed only when the branch is taken
    C. Is executed only when the branch is not taken
    D. No correct answer

10. Comparing variable and fixed encoding we can conclude that
    A. For variable encoding the program is longer
    B. For fixed encoding the program is longer (CORRECT)
    C. The length of the program is the same
    D. No correct answer
11. What is the difference between write back and write through cache startegies?
    A. In write through the information is written only to the block in the cache, when in the write back the information is written to both the block in the cache and the main memory
    B. There are no any differences
    C. In write back the information is written only to the block in the main memory, when in the write through the information is written to both the block in the cache and the main memory
    D. No correct answer (CORRECT)
12. How to calculate the physical memory address when using memory paging?
    A. We need to concatenate the offset from virtual address and physical page address taken from the page table (CORRECT)
    B. We need to add the offset from the virtual address and physical page address taken from the page table
    C. It is a virtual address
    D. No correct answer
13. Are segments can be divided on pages, when using virtual memory?
    A. It is not used the memory organization
    B. Yes, it depends on the operating system (CORRECT)
    C. No correct answer
    D. Yes, it is a virtual addressing mode
14. When internal memory fragmentation occurs?
    A. When we use memory segmentation
    B. When we use memory paging (CORRECT)
    C. No correct answer
    D. When we use memory segmentation or memory paging
15. What UMA abbreviation means?
    A. This means that the memory access time depends on the cell address (its location)
    B. It is the computer main memory
    C. This abbreviation is not used
    D. This means that the memory access time does not depend on the cell address (its location) (CORRECT)
16. The meaning of the instruction slt reg1, reg2, reg3 is as follows:
    A. If (reg2 > reg3) reg1 = 1; else reg1 = 0;
    B. If (reg2 != reg3) reg1 = 1; else reg1 = 0;
    C. If (reg2 < reg3) reg1 = 1; else reg1 = 0; (CORRECT)
    D. No correct answer
17. What it means that access to the memory is aligned?
    A. The access is aligned if the size of the word is 4 bytes
    B. No correct answer (CORRECT)
    C. The access is aligned if the address A of an object of size s bytes satisfy the following condition $A \ mod \ s \neq 0$.
    D. The access is aligned if we have different word formats
18. When we use the reservation station and Tomasulo's scheme, instruction execution is divided onto:
    A. Five steps like using standard pipeline
    B. Three steps: Issue, Execute, Write Result (CORRECT)
    C. Four steps: Fetch, Decode, Execute, Write Result
    D. No correct answer

19. When using hardware based speculation we need to add additional step during instruction execution called commit. There are the following types of commits:
    A. We have only one type of commit
    B. Normal and incorrect branch prediction commits
    C. Normal commit, store instruction commit and incorrect branch prediction commit (CORRECT)
    D. Normal and store commits
20. How we define the average memory access time?
    A. Average memory access time = Hit time + miss rate * miss penalty, where the hit time is the time to hit the cache (CORRECT)
    B. Average memory access time = Hit time * miss rate * miss penalty, where the hit time is the time to hit the cache
    C. There is no such metric
    D. No correct answer
21. The following code is equivalent to:

```
beq $s4, $s5, Lab1
add $s3, $s4, $s5
j Lab2
Lab1: sub $s3, $s4, $s5
Lab2: …
```

    A. If (i != j) h = i + j; else h = i - j; (CORRECT)
    B. If (i == j) h = i + j; else h = i - j;
    C. If (i < j) h = i + j; else h = i - j;
    D. No correct answer
22. What does it mean that network has blocking property?
    A. It means that if one processor is accessing some memory block, other processor can not access the same memory block
    B. It means that two different processors cannot access the same memory location at the same time
    C. It means that when one processor is accessing some memory block other processor can not access different memory block (CORRECT)
    D. No correct answer
23. What is branch target buffer?
    A. Branch target buffer stores branch predictions – branch taken or branch not taken
    B. Branch target buffer stores the predicted addresses for the next instruction after a branch, when branch is predicted as taken (CORRECT)
    C. Branch target buffer stores the global history of branch predictions
    D. No correct answer
24. What does NUMA abbreviation mean
    A. This means that the memory access time depends on the cell address (its location) (CORRECT)
    B. It is the computer main memory
    C. This abbreviation is not used
    D. This means that the memory access time does not depend on the cell address (its location)

What is the disadvantage of Princeton (von Neumann) architecture?

- as instructions and data are in the same memory, it can lead to creating of "bad code" which will be executed (correct)

Which one from below architectures will fastest execute one specific task?

- FPGA (correct)

To which class according to Flynn's taxonomy we can match GPU?

- SIMD - single instruction multiple data (correct)

Which one of below computer architecture classification doesn't exist?

- Stanford's taxonomy (correct)

In one line in MIPS assembler u can:

- declare variable, then type comment (correct)

What is branch delay slot in MIPS

- executing of the next operation after jump in purpose to minimally disturb pipelining process

What is NOT defined by ISA?

- avilable processors models

What is "endiannes"

- byte order in word (correct)

Which approach is supported my RISC architecture?

- load and store (arithmetic operations with use of registers) (correct)

How can we describe SISD class in Flynn's taxonomy?

- no parallelism, systems executes one instruction.... (correct)

What distinguish GPR?

- they are small and there is small amount of them (correct)

RISC architecture in comparison to CISC architecture:

- is more often used in mobile devices (correct)

Which one of below architectures has common memory for data and instructions:

- Princeton (von Neumann) architecture (correct)

1. What is the disadvantage of Princeton (von Neumann) architecture?

- as instructions and data are in the same memory, it can lead to creating of "bad code" which will be executed

2. How many general-purpose registers are in MIPS?

- 32

3. Which one from below architectures will fastest execute one specific task?

- FPGA

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6. In one line in MIPS assembler u can:

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- executing of the next operation after jump in purpose to minimally disturb pipelining process

8. What is NOT defined by ISA?

- avilable processors models

9. Is this MIPS instruction correct: lw $t0, 4($t1) ?

- yes

10. What are general-purpose registers?

- closest to processor place when data can be stored

11. What is "endiannes"

- byte order in word

12. Which approach is supported my RISC architecture?

- load and store (arithmetic operations with use of registers)

13. MIPS assembler allows:

- loading words from memory into registers

14. How can we describe SISD class in Flynn's taxonomy?

- no parallelism, systems executes one instruction....

15. What is the role of $ra register in MIPS?

- stores information about return adress after executing jal instruction

16. What distinguish GPR?

- they are small and there is small amount of them

17. RISC architecture in comparison to CISC architecture:

- is more often used in mobile devices

18. Which one of below architectures has common memory for data and instructions:

- Princeton (von Neumann) architecture

19. Instruction in MIPS architecture:

- always is 32-bit long

20. What value will be stored in $0 register after MIPS instruction: add $0, $1, $2

- zero

21. What is the word length in MIPS?

- 32 bits

22. I- type instructions in MIPS:

- are working on values (immediate)

23. What is at the top of memory hierarchy?

- processor registers

24. What is a branch delay slot size in MIPS?

- one instruction
- two instructions

25. Which family of instructions DO NOT exist in MIPS:

- S-type

1. What is the disadvantage of Princeton (von Neumann) architecture?
- as instructions and data are in the same memory, it can lead to creating of
 "bad code" which will be executed (correct)
- it is not possible to implement, just a concept
- memory for data and instructions is separate
- does not contain ALU

2. How many general-purpose registers are in MIPS?
- 32 (correct)
- 64

3. Which one from below architectures will fastest execute one specific task?
- FPGA (correct)
- CPU in CISC architecture
- ASIC (correct ? )
- CPU in RISC architecture

4. To which class according to Flynn's taxonomy we can match GPU?
- MISD - multiple instructions single data
- MIMD - multiple instructions multiple data
- SIMD - single instruction multiple data (correct)
- SISD - single instruction single data

5. Which one of below computer architecture classification doesn't exist?
- Stanford's taxonomy (correct)
- Handler's classification
- Flynn's taxonomy
- Feng's classification

6. In one line in MIPS assembler u can:
- give machine code straight away (sequence of 0's and 1's)
- first type comment, then instruction
- declare variable, then type comment (correct)
- type more than one instruction

7. What is branch delay slot in MIPS
- jump to address contained in $ra to exit from function properly,
 to place where function was called
- executing of the next operation after jump in purpose to minimally disturb pipelining process (correct)
- delay size which is the result of  executed instruction type
- its necessary to calculate branch size in case of program branching

8. What is NOT defined by ISA?
- instruction set
- available registers set
- memory organization
- avilable processors models (correct)

9. Is this MIPS instruction correct: lw $t0, 4($t1) ?
- no, because 4 should be divided without rest by 8
- no, because lw instruction doesn't exist
- no, because lw instruction needs on more argument
- yes (correct)

10. What are general-purpose registers?
- closest to processor place when data can be stored (correct)
- register of operations available in specified architecture

- register of available general-purpose entires and exits
- list of available RAM  sources

11. What is "endiannes"
- byte order in word (correct)

12. Which approach is supported my RISC architecture?
- load and verity (verification of every instruction loaded from memory)
- memory privileged (priviledge for read and save operation)
- memory only (arithmetic operation only in memory)
- load and store (arithmetic operations with use of registers) (correct)

13. MIPS assembler allows:
- loading words from memory into registers (correct)
- using more than one immediate value in addi instruction
- change of order of source and destiny registers in instructions
- loading multiple words into GPR registers

14. How can we describe SISD class in Flynn's taxonomy?
- no parallelism, systems executes one instruction.... (correct)

15. What is the role of $ra register in MIPS?
- stores information about return adress after executing jal instruction (correct)

16. What distinguish GPR?
- u cant get to them from assembly language lvl
- are in diffrent places in computer system
- they are small and there is small amount of them (correct)
- because of their size they are vey slow

17. RISC architecture in comparison to CISC architecture:
- is less safe and therefore ISA was created
- has more comlpex instructions of varying lenghts
- is more often used in mobile devices (correct)
- is old architecture, which is not used atm.

18. Which one of below architectures has common memory for data and instructions:
- Princeton (von Neumann) architecture (correct)

19. Instruction in MIPS architecture:
- can have varying length
- always has it's equivalent with same name in CISC architecture
- always is 32-bit long (correct)
- is secured from unauthorized GU execution

20. What value will be stored in $0 register after MIPS instruction: add $0, $1, $2
- zero (correct)
- we don't know because we dont know values in $1 and $2
- instruction is wrong, it should have 4 arguments
- value in $0 wont change, value in $2 will change and it will be sum of $0 and $1

21. What is the word length in MIPS?
- 32 bits (correct)
- 16 bits
- 64 bits
- 8 bits

22. I- type instructions in MIPS:
- are working on values (immediate) (correct)

23. What is at the top of memory hierarchy?
- processor registers (correct)
- processor cache
- RAM
- backup tape

24. What is a branch delay slot size in MIPS?
- one instruction
- two instructions
- 3 or more instructions
- there is no brach delay slot in MIPS

25. Which family of instructions DO NOT exist in MIPS:
- J-type
- R-type
- S-type (correct)
- I-type