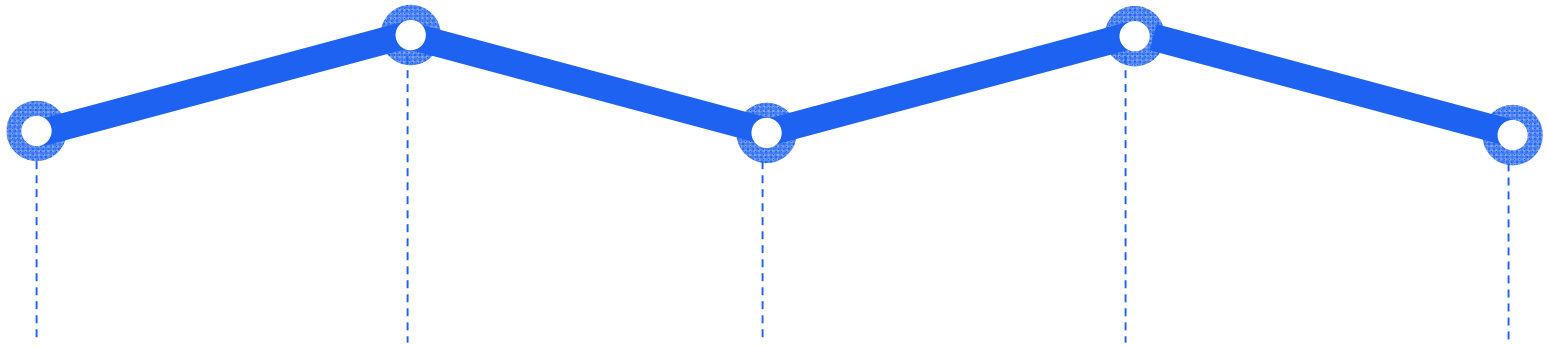
임베디드 시스템

5주차 실험

<2조>
정진호 201524578
박대언 201345814
이상훈 201524525

목차

CONTENTS



01 Clock 개념

02 Clock Tree

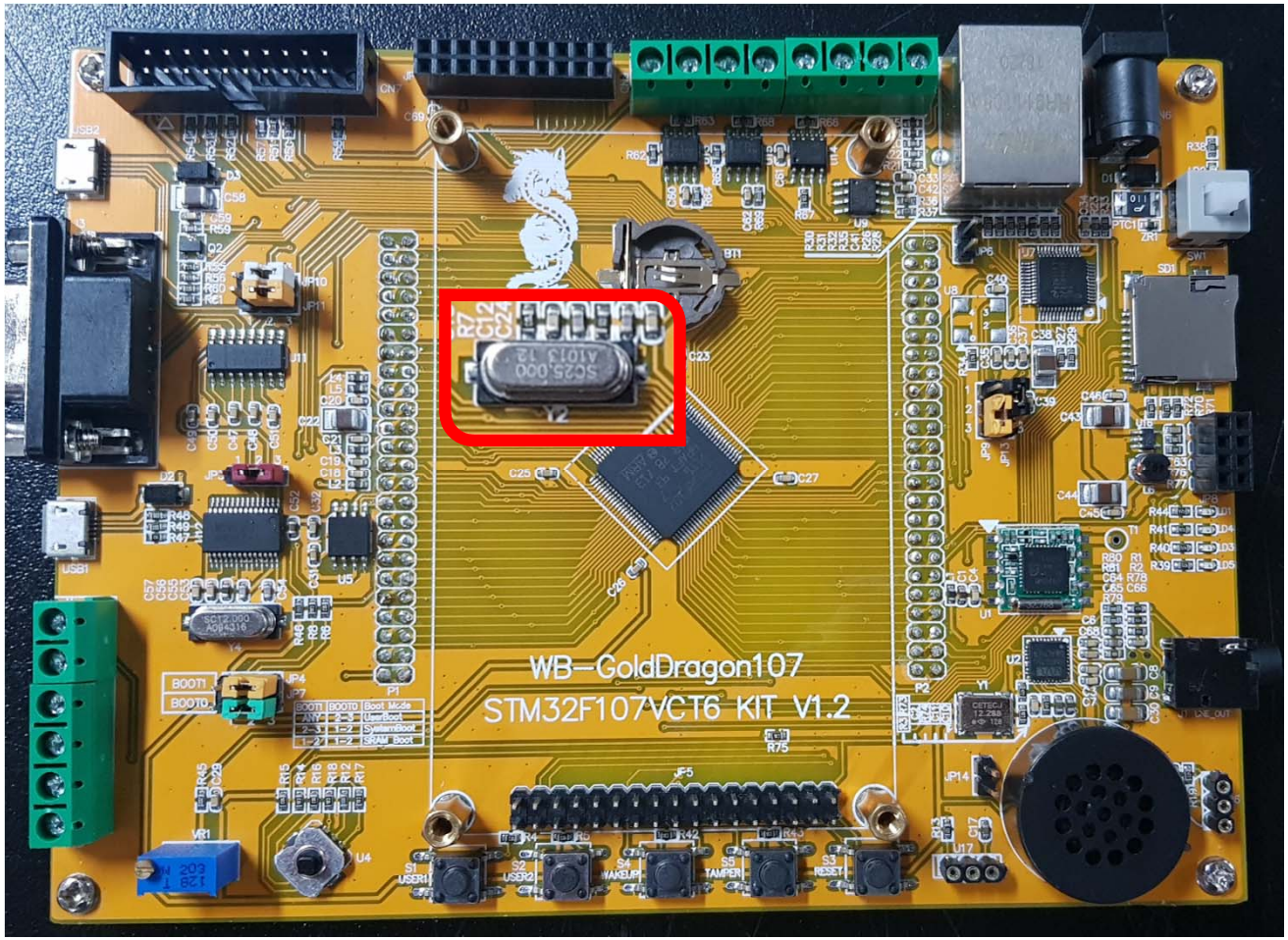
03 Clock Setting

04 오실로스코프

05 예비 실험

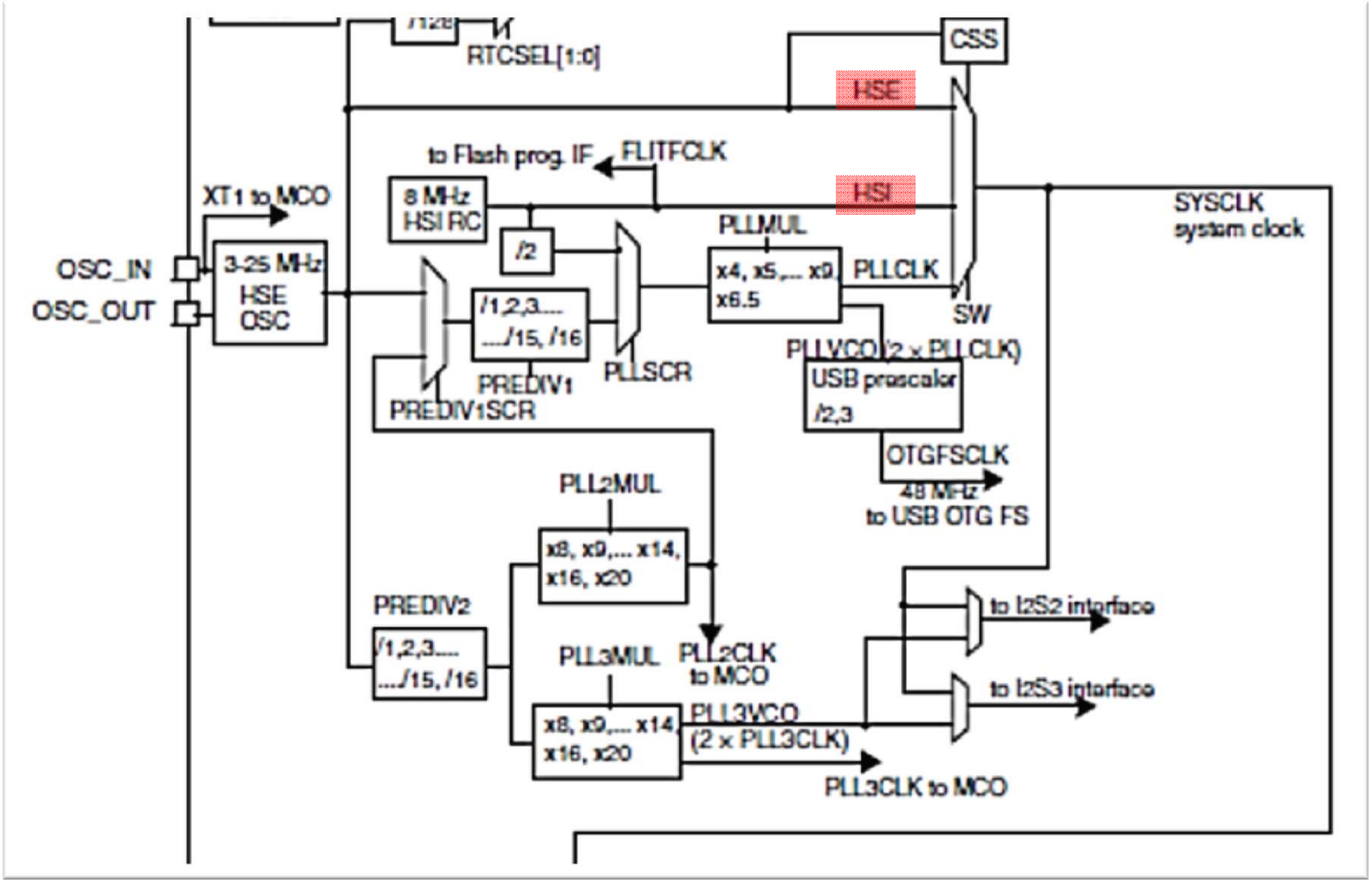
01 Clock

HSI Clock(High Speed Internal)
HSE Clock(High Speed External)



02 Clock Tree

HSI(High Speed Internal) : 내부에 존재하는 8MHz 클럭
HSE(High Speed External) : 외부에 존재하는 3-25MHz 클럭



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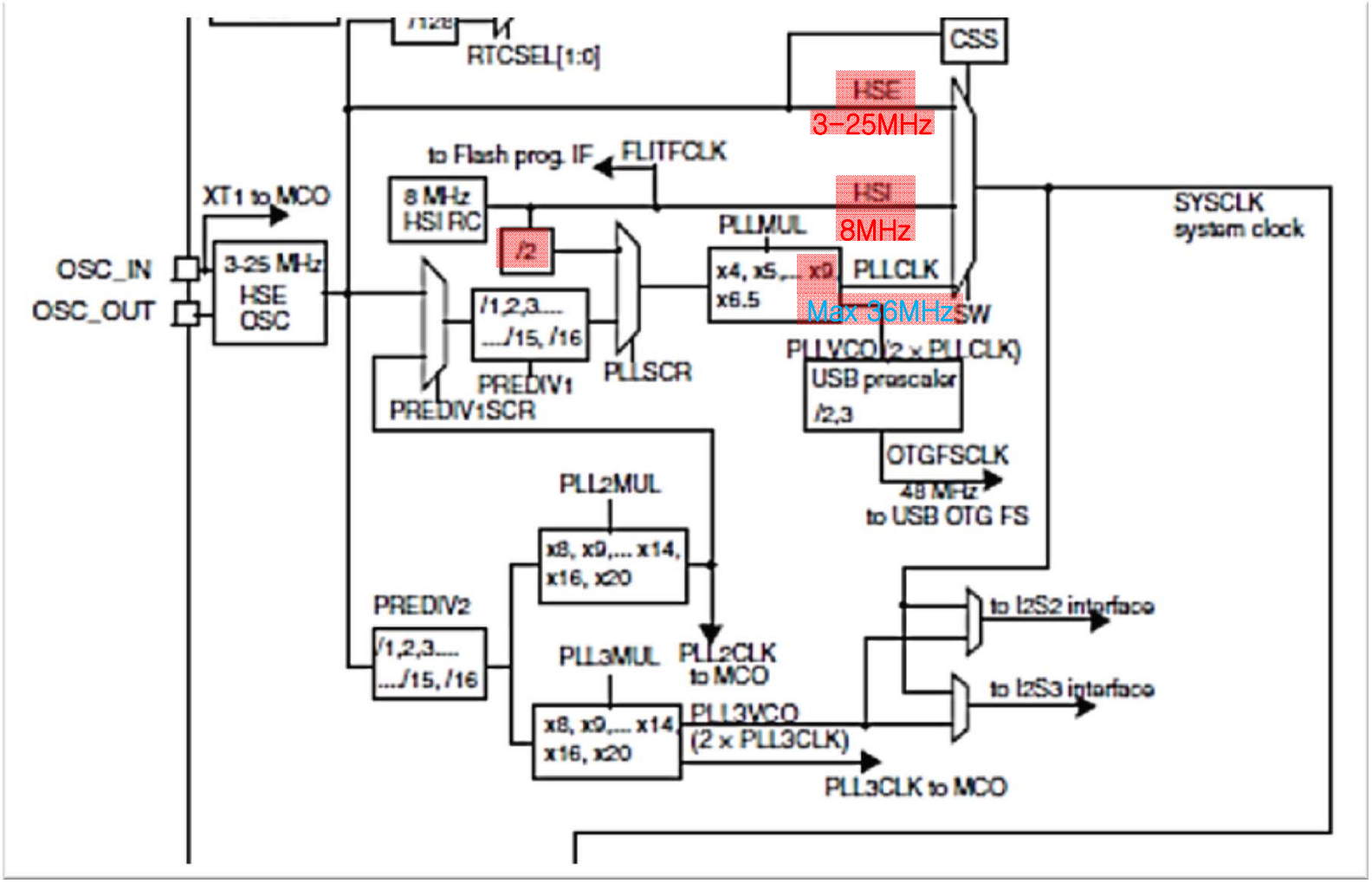
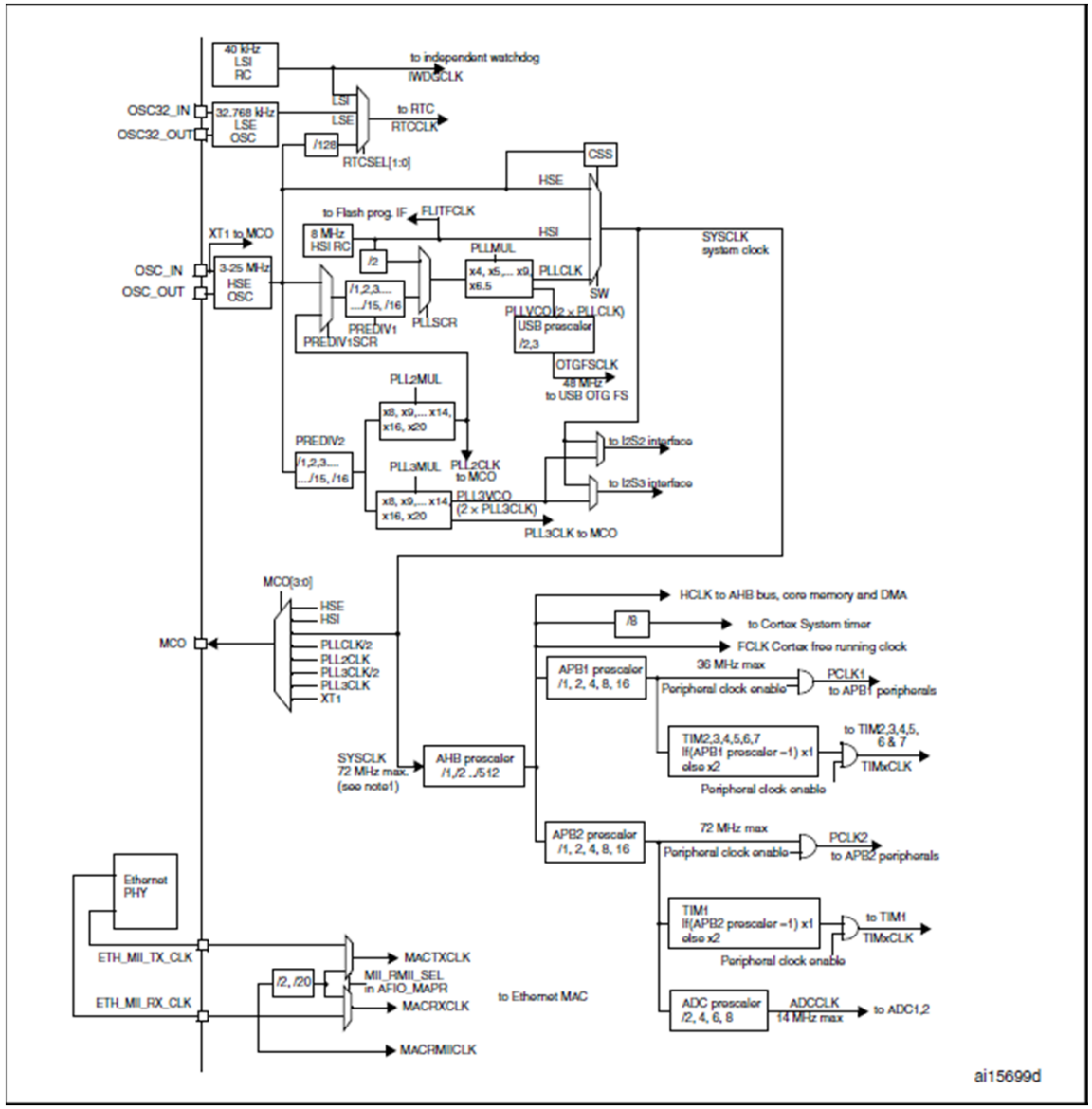


02 Clock Tree



Reference Manual 126p

1. FCLK

CPU에 사용

2. HCLK, PCLK

APB Bus에 사용되고 고속 · 저속 입출력 장치에 인가

3. PLL

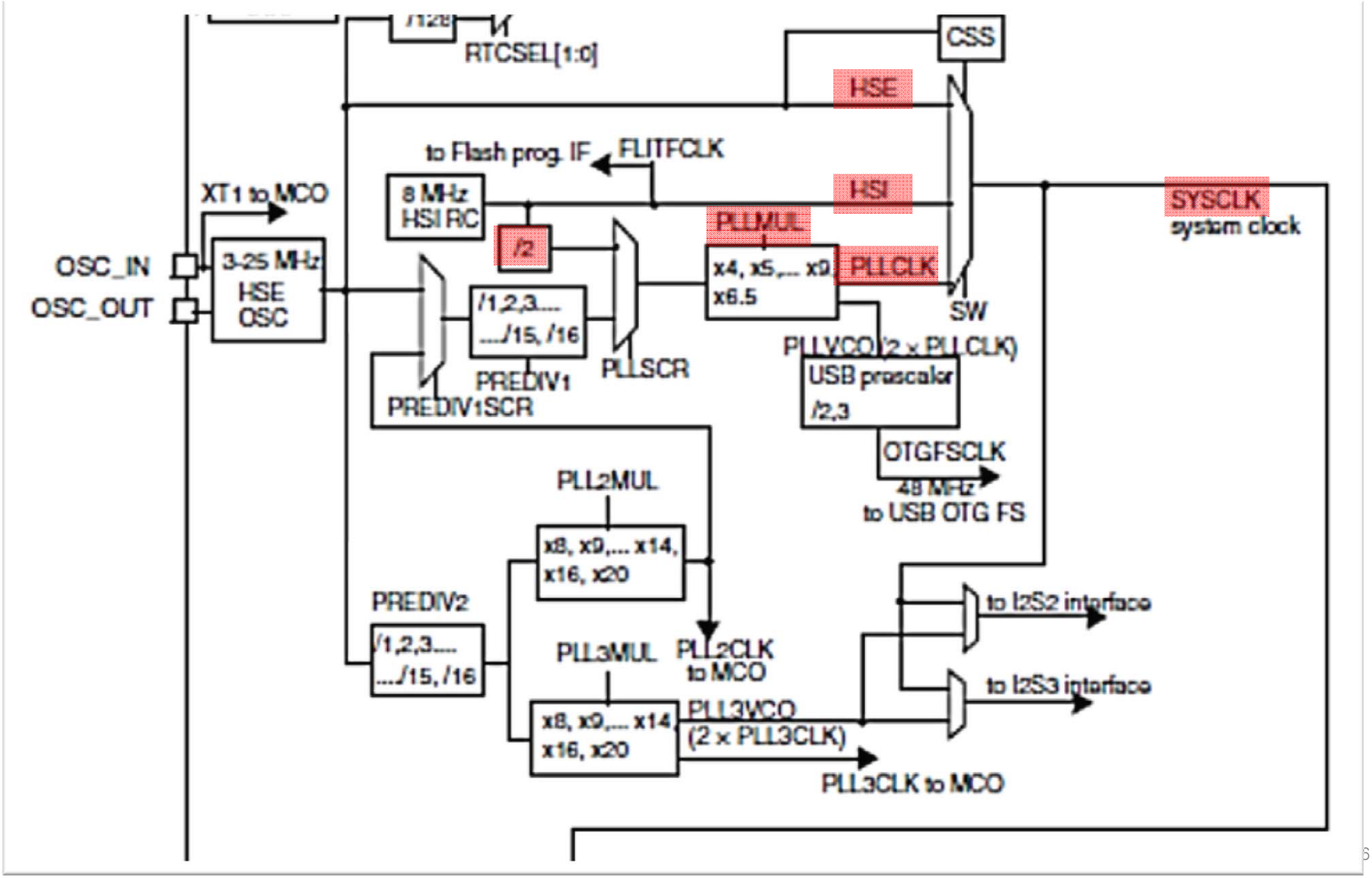
Phase Lock Loop clock
안정화 및 조작

4. SYSCLOCK

5. MCO

Microcontroller Clock Output

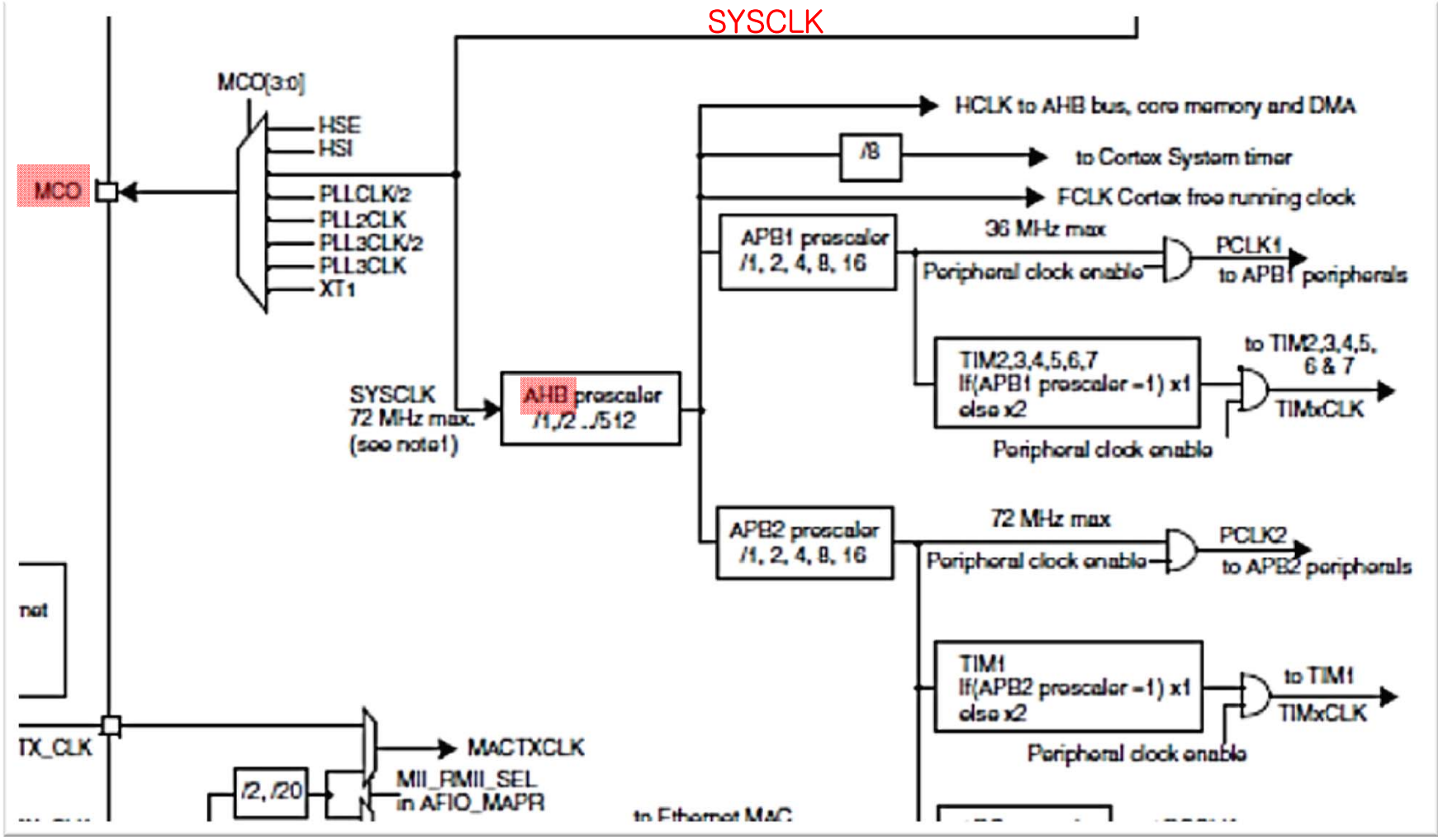
02 Clock Tree



02 Clock Tree

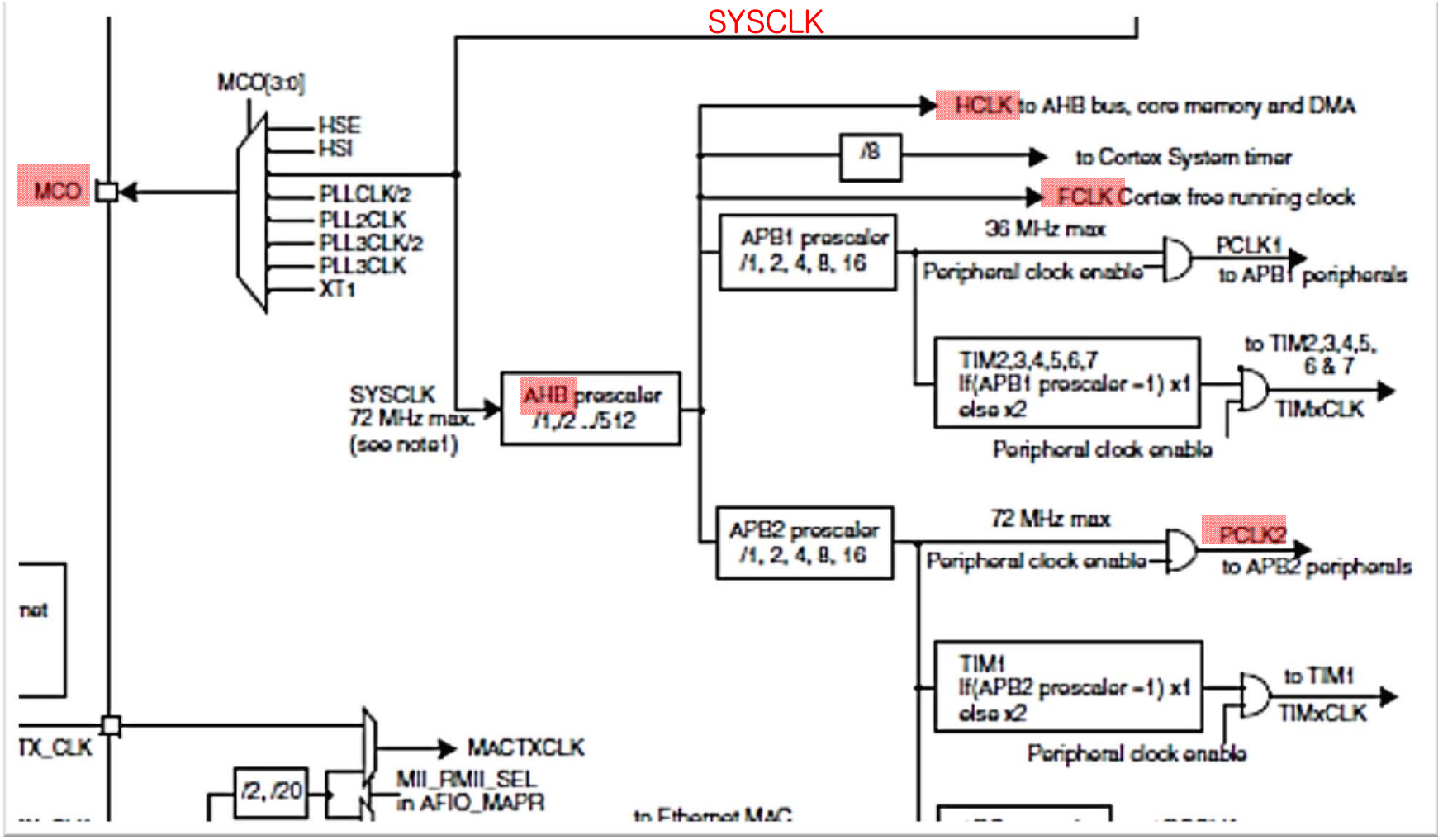
MCO(Microcontroller Clock Output) : 내부의 클럭을 외부로 출력

★ GPIO 최대 속도(50MHz)를 넘으면 안 됨.

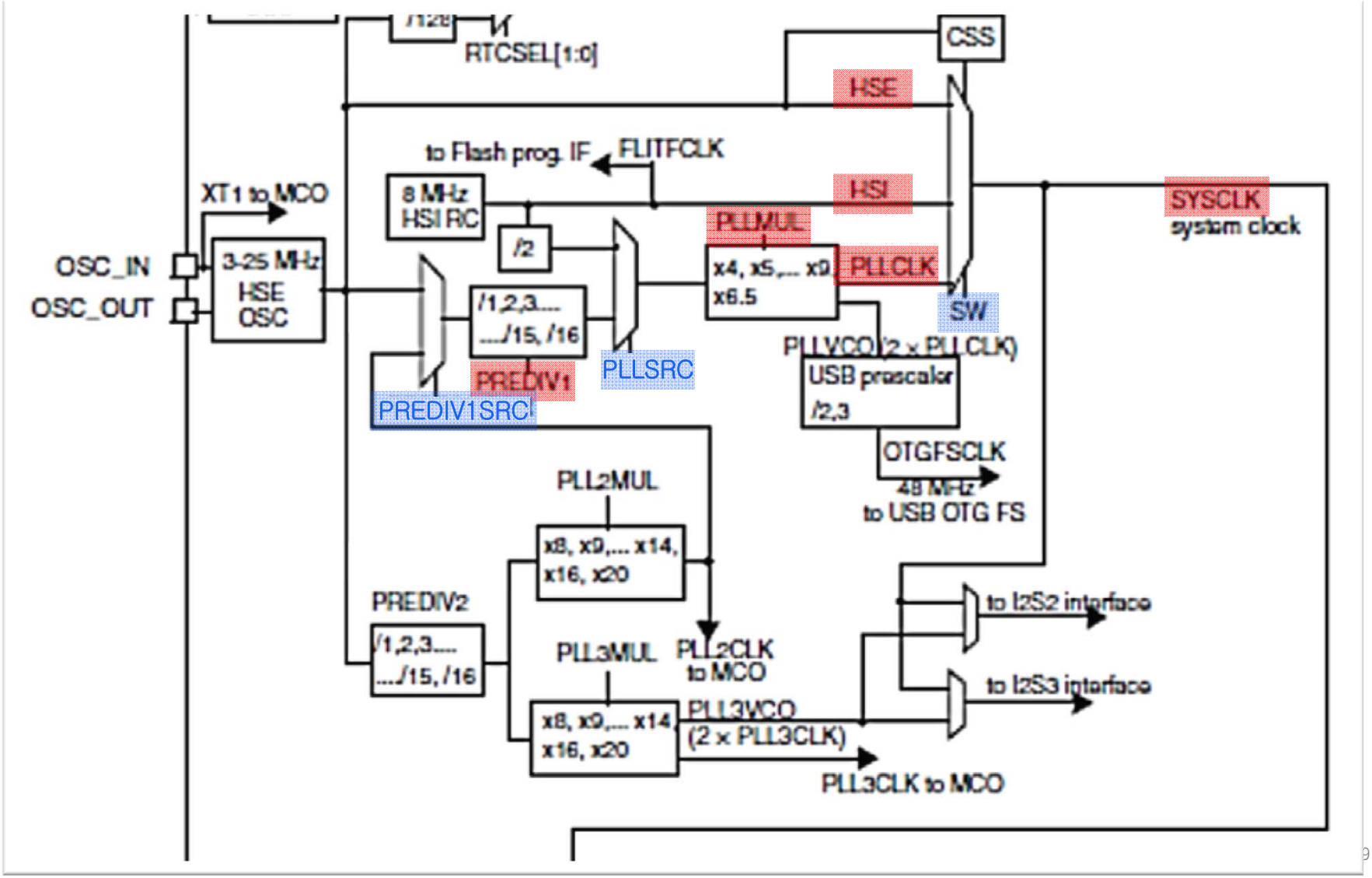


02 Clock Tree

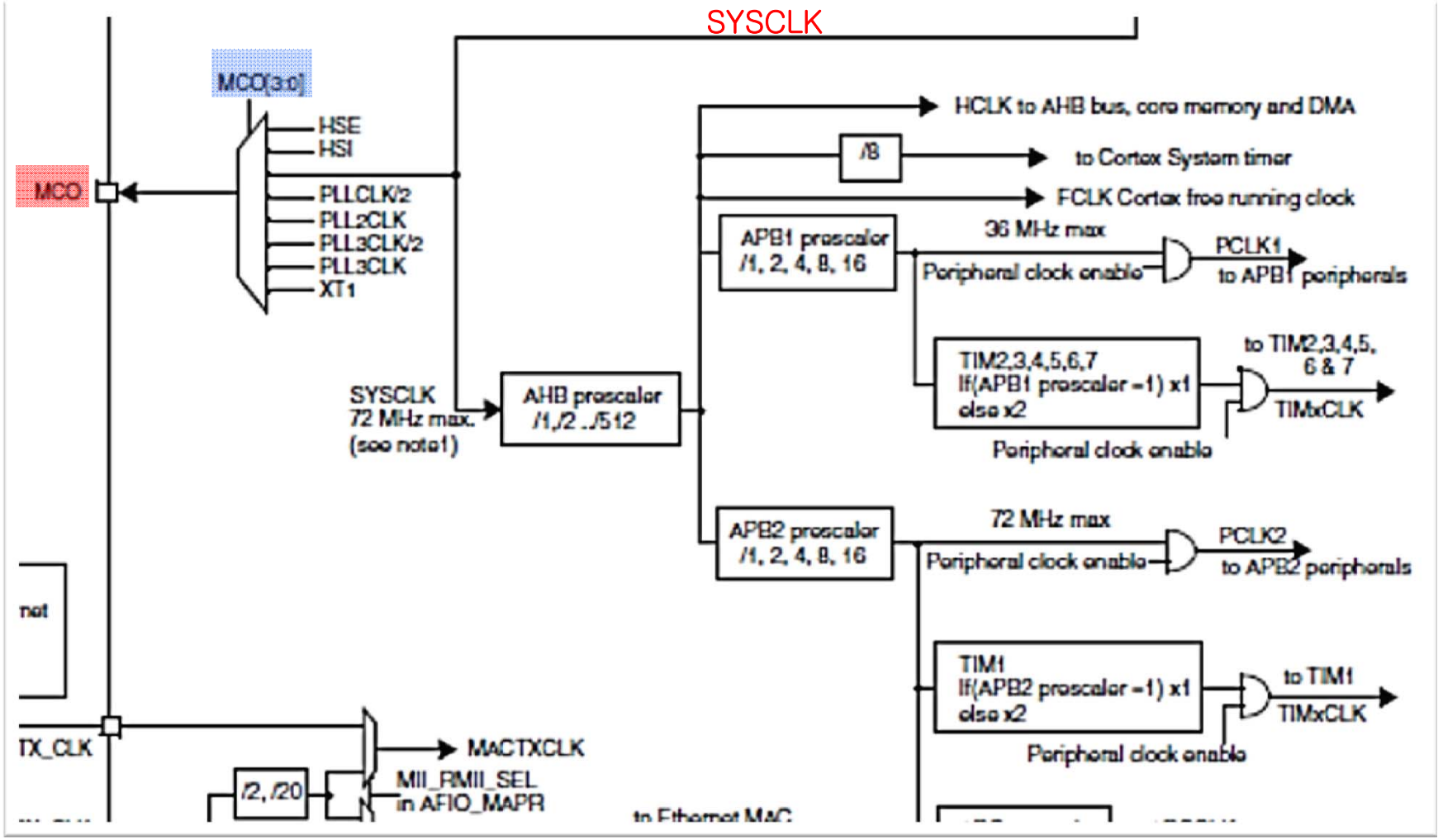
FCLK : CPU에 사용되는 클럭
HCLK, PCLK : APB Bus에 사용되고, 고속 ·저속 입출력 장치에 인가



03 Clock Setting



03 Clock Setting



03 Clock Setting

8.3.2 Clock configuration register (RCC_CFGR)

Address offset: 0x04

Reset value: 0x0000 0000

Access: 0 ≤ wait state ≤ 2, word, half-word and byte access

1 or 2 wait states inserted only if the access occurs during a clock source switch.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved				MCO[3:0]				Res.	OTGFS PRE	PLLMUL[3:0]				PLL XTPRE	PLL SRC
				rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC PRE[1:0]		PPRE2[2:0]			PPRE1[2:0]			HPRE[3:0]				SWS[1:0]		SW[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	r	rw	rw

8.3.12 Clock configuration register2 (RCC_CFGR2)

Address offset: 0x2C

Reset value: 0x0000 0000

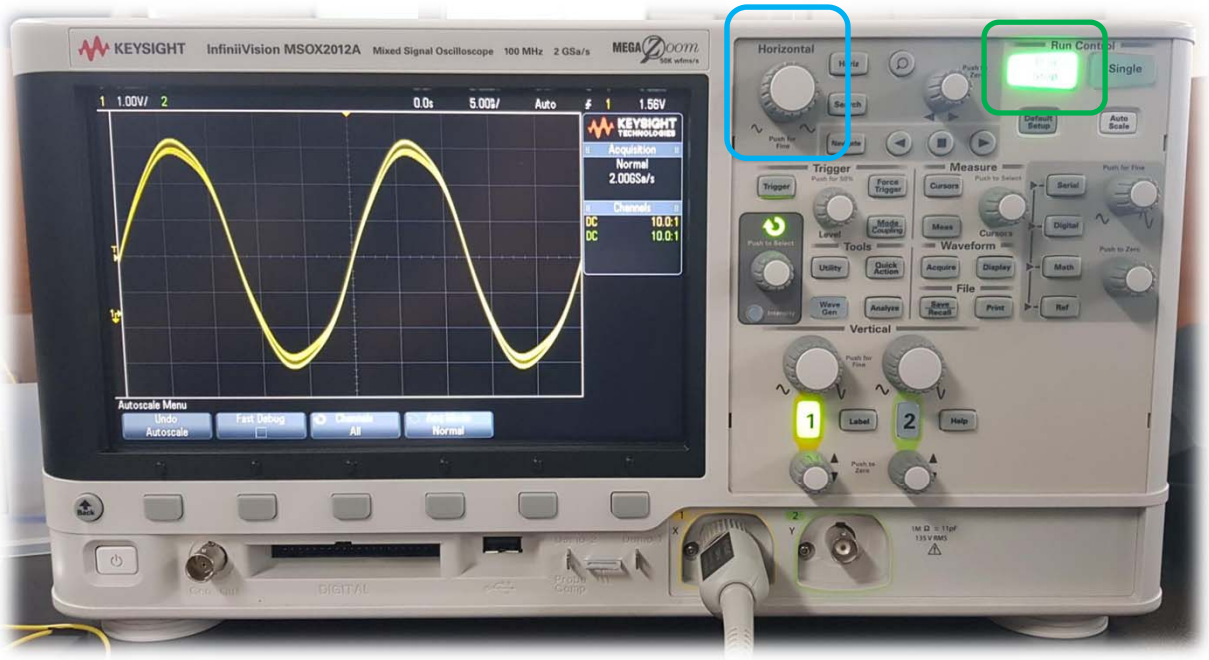
Access: no wait state, word, half-word and byte access

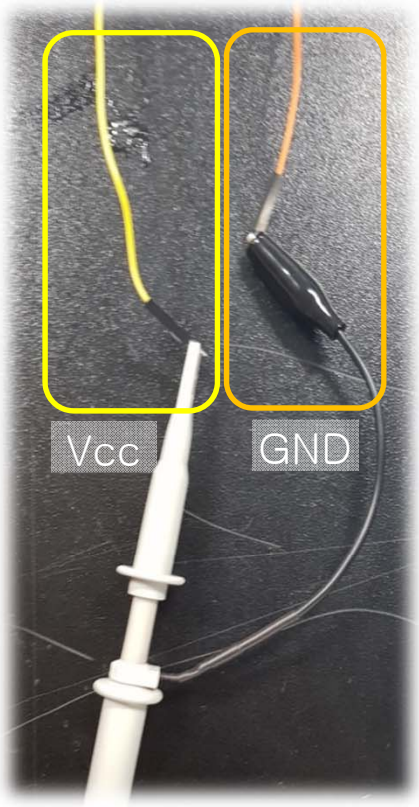
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													I2S3SRC	I2S2SRC	PREDIV1SRC
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL3MUL[3:0]				PLL2MUL[3:0]				PREDIV2[3:0]				PREDIV1[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

04 오실로스코프

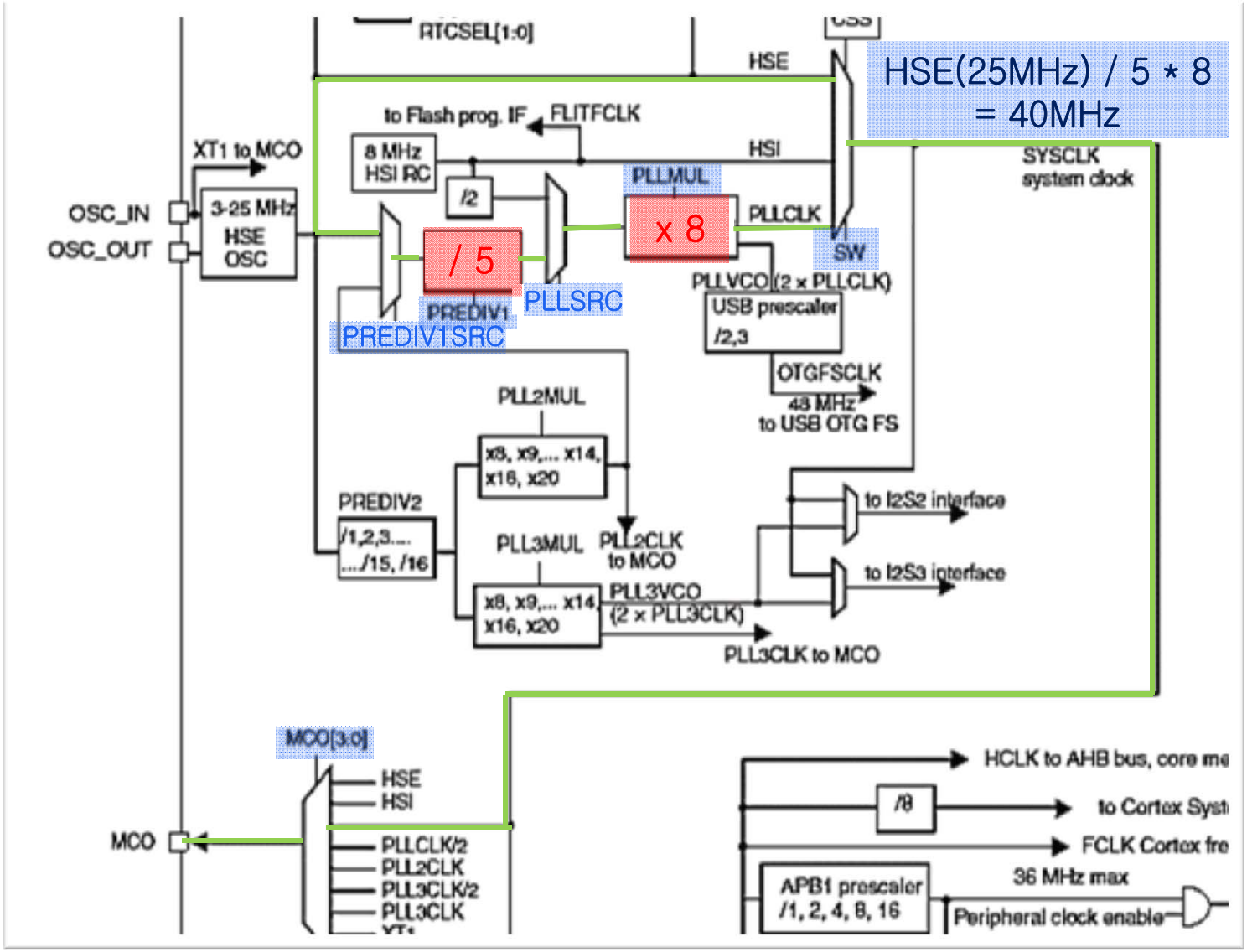
전압이 들어오는 단자와 Ground 단자로 구성
Horizontal 다이얼로 x축 조절 가능





05 예비 실험

SYSCLOCK을 40MHz로 설정하고, MCO를 통해 오실로스코프로 40MHz 클럭 확인



05 예비 실험

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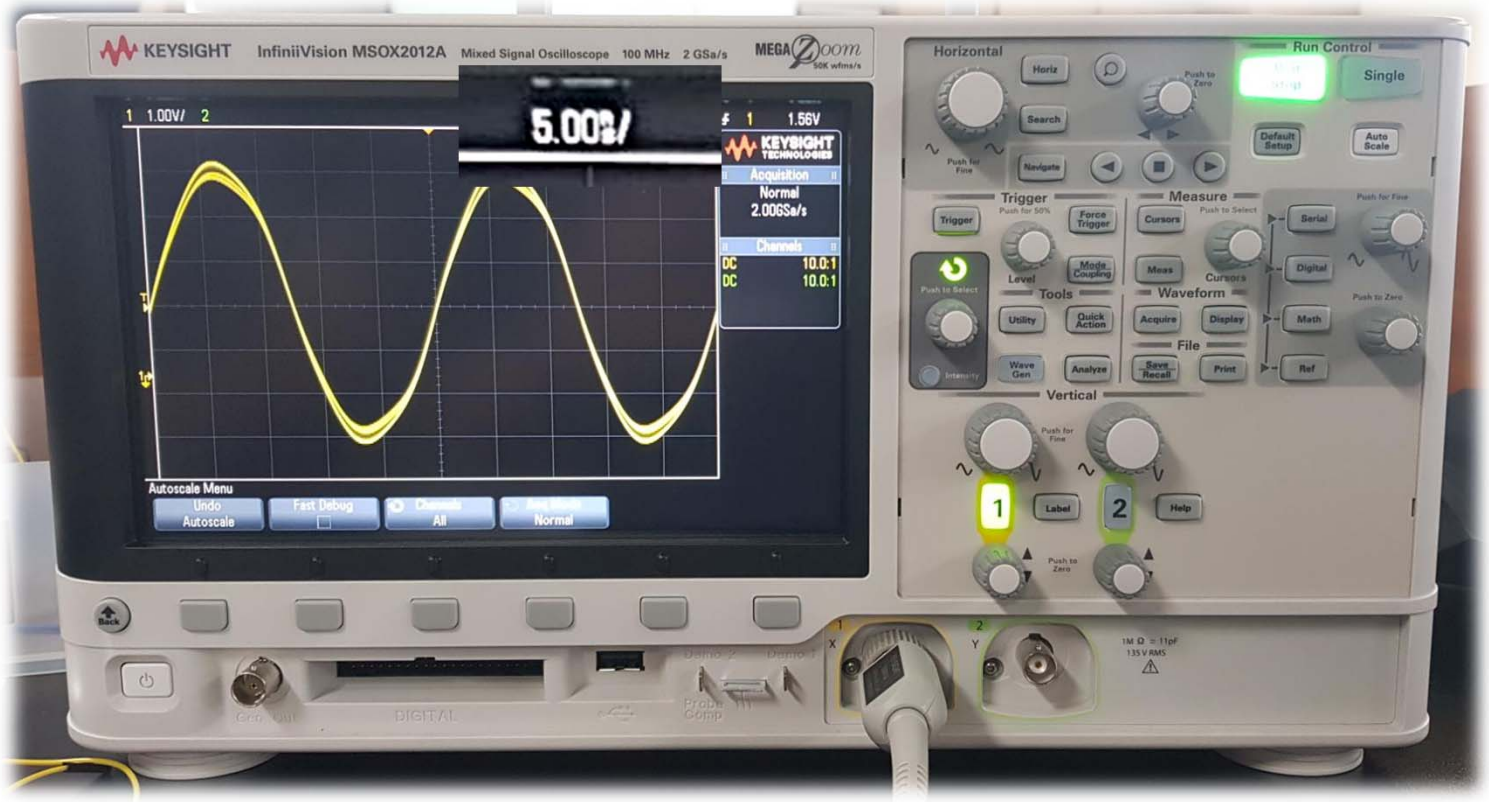

$$T = 5ns * 5 = 25ns$$

$$f = \frac{1}{25ns} = 40\text{MHz}$$

감사합니다.