FFT Processor IP Cores synthesis on the base of configurable pipeline architecture

Anatoly Melnyk, Bohdan Dunets

Abstract - **The INTRON FFT Processor IP Cores Generator, based on newest INTRON IP Core Generator creation methodology, which allows generating optimized FFT IP Cores on base of scalable source IP modules is presented.**

Keywords – **FFT, FPGA, IP Core, IP Cores Generator, VHDL.**

I. INTRODUCTION

Fast Fourier Transform (FFT) Processors are widely used for digital signal and image processing. Last forty seven years, after FFT algorithm by Cooley-Turkey invention, large number of FFT processors were designed. Distinct place among them have pipeline FFT processors, which have efficient using of the hardware recourses, low latency time and make possible real-time data processing. Such features are important for signal and image processing procedures. But, pipeline FFT processors in comparison with iterative ones had important disadvantages, which restricted their usage: they have been designed for selected FFT size only. The number of processor elements (PE) of this processor is equal FFT algorithm stages number $m=\log_2 N$. On this reason, for multifunction FFT processor building the programmable pipeline structure have been designed with PE number $m=\log_2 N_{max}$, where N_{max} – maximum FTT transform size. Low point FFT in this programmable pipeline processor was calculated by bypassing unused PE. Such approach increases control unit complexity and is not gate count effective, because for less than N_{max} transform some number of PE ($\log_2 N_{max}$-$\log_2 N$) stands idle. As result, most of known FFT processors have iterative structure. Situation cardinally has changed during last years. Up-to-date multiple times programmable FPGA and hardware description languages (VHLD, Verilog) allow creating flexible IP Cores. Designers of complex electronic FPGA face a large and growing dilemma, – they must build products with more functionality and greater performance with no increase in time or engineering staff. Such problem can be solved by IP Cores Generators usage. IP Cores Generators allow automatically generate selected IP Core by users-defined parameters.

Anatoly Melnyk, Bohdan Dunets – INTRON, Ltd, Lviv, UKRAINE,
E-mail: intron@mail.lviv.ua

II. FFT ALGORITHM

Discrete Fourier Transform (DFT) is the most universal among all Fast Orthogonal Transforms. Its direct and inverse form are described by the following equations:

$$X(k)=\sum_{n=0}^{N-1} x(n)\, W_N^{kn},\quad W_N^r=exp(-j2\pi r/N)$$

$$x(n)=\frac{1}{N}\sum_{k=0}^{N-1} X(k)\, W_N^{-kn},\quad n,k=0,1,2,...,N-1,$$

where $X(k)$ and $x(n)$ in common case are complex sequences, N is the transform size. Direct DFT calculation requires perform N^2 multiplications and $N(N-1)$ additions of the complex numbers. FFT requires perform only N/2*logN base operations. On Fig.1 FFT algorithm graph is shown for N=16, and on Fig.2 the performed operations symbols are described. Here last two versions describe the FFT algorithm base operations with decimation in time and in frequency.

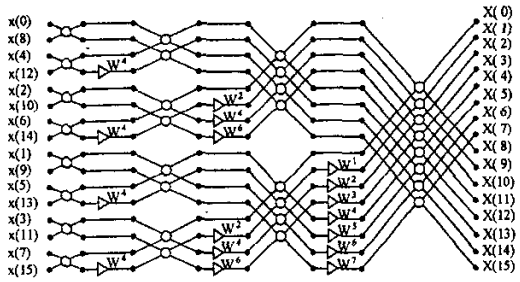

Fig.1 Direct FFT algorithm graph for N=16.

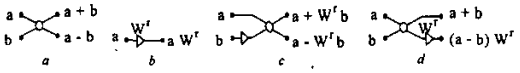

Fig.2. FFT algorithm base operations.

III. Configurable Parametrizable FFT Processor Architecture

The FFT Processor computes the N-point complex direct or inverse FFT.

The input (output) data is a vector of N complex values represented as 2's complement numbers – real and imaginary components of a data sample. The input data stream is represented in natural order, output in binary-inverse order. The control interface of the FFT Processor consists of system clock *clk*, the high active asynchronous reset input *reset*, the high active input and output data acknowledge signals *i_ack* and *o_ack*. The data interface consists of the data input bus *re_in* (real), *im_in*(imaginary) and the data output bus *re_out* (real), *im_out*(imaginary).

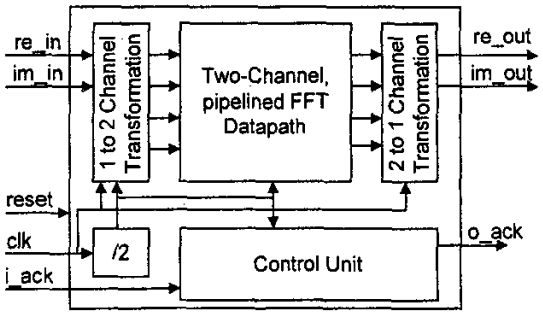

Fig.3. FFT Processor Structure.

INTRON FFT Processor features: no external memory required; fixed-point arithmetic; simple interface and timing; no dead clock cycles; fully pipelined structure, fully synchronous; registered Inputs and Outputs; natural order input, binary-inverse output.

IV. FFT Processor IP Cores Generator

The INTRON FFT Processor IP Cores Generator is intended for generation fully optimized FFT Processor architecture and test-bench with test patterns. The INTRON FFT Processor IP Cores Generator is based on newest INTRON IP Core Generator methodology, which allows generating optimized IP Cores on base of scalable source IP modules.

The Generator generates target VHDL description of FFT Processor on base of scalable FFT Processor Architecture template. The FFT Processor Architecture template is presented as scalable parametrizable VHDL description of pipelined FFT architecture. This model is presented as VHDL code with included Lisp-code. The Generator reads such Lisp directives and generates target VHDL model. True configuration makes possible the effectively using of the resources of available hardware. It's achieved by precision optimization of all parts of FFT Processor by Generator. The FFT IP Cores Generator generate test bench with test patterns.

TABLE 1. FFT Processor IP Cores Generator Parameters

Parameter	Description
FFT Size	Number of points, must be power of 2.
FFT External Wordwidth	Wordwidth of each input real and imaginary part of complex data
FFT Internal Wordwidth	Wordwidth of sine and cosine coefficients, wordwidth of internal data.
Transform Type	Direct or Inverse.
Test Patterns	Test patterns number, skip test bench if 0.

INTRON FFT Processor IP Cores Generator features: any radix-2 length direct or inverse FFT; fixed complex I/O with any width; internal data and coefficient word width – any width; full test bench supplied.

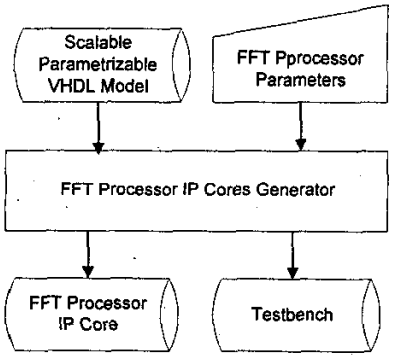

Fig.4. IP Core Generator Structure.

Using proposed FFT Processor IP Cores Generator was generated and implemented on Altera FPGA several kind of FFT Processor. Implementation result is summarized on Tab.2.

Table 2. Sample realization on ALTERA APEX20KE FPGA

Parameters	Characteristics
16-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth	Utilization - 6432 LE. Fmax - 72,4 MHz. Performance - 2,31 Gbit/s. Transform Time* - 220 ns. Pipeline Delay -855ns.
64-point FFT, 24-bit ext. datawidth, 32-bit internal datawidth	Utilization - 35117 LE. Fmax - 39,04 MHz. Performance - 1,87 Gbit/s. Transform Time - 1,639 us. Pipeline Delay - 4,559 us.
1024-point FFT, 16-bit ext. datawidth, 20-bit internal datawidth	Utilization - 35982 LE, 69504 ESB. Fmax - 65 MHz. Performance - 2,08 Gbit/s. Transform Time - 15,749 us. Pipeline Delay - 33,128 us.
8192-point FFT, 4-bit ext. datawidth, 8-bit internal datawidth	Utilization - 20383 LE, 181888 ESB. Fmax - 100,1 MHz. Performance - 800 Mbit/s. Transform Time - 81,912 us. Pipeline Delay - 165,263 us.

* Where Transform Time = N / Fmax

REFERENCES

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V. CONCLUSION

Proposed INTRON FFT Processor IP Cores Generator allows to automatically generating high-speed pipelined direct or inverse FFT Processor IP Cores by users-defined parameters.