

Chapter 4

Chapter 4. Modules and Ports

4.5 Exercises

1. What are the basic components of a module? Which components are mandatory?

My answer:

1) Module Name, Port List, Port Declarations, Parameters, Declarations of wires, regs and other variables, Data flow statements, Instantiation of lower level modules, always and initial blocks, Tasks and functions, endmodule statement.

2) module, module name, and endmodule.

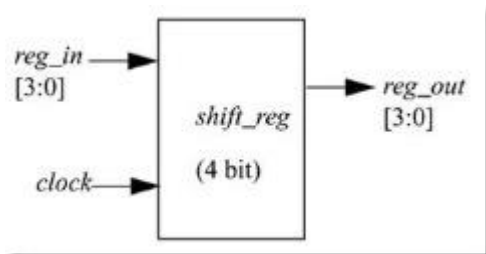
2. Does a module that does not interact with its environment have any I/O ports? Does it have a port list in the module definition?

My answer:

1) have

2) no

3. A 4-bit parallel shift register has I/O pins as shown in the figure bellow. Write the module definition for this module `shift_reg`. Include the list of ports and port declarations. You do not need to show the internals.



My answer:

```
module shift_reg(reg_out,reg_in,clock);
```

```
output reg [3:0]reg_out;
```

```
input [3:0]reg_in;  
input clock;  
endmodule
```

4. Declare a top-level module stimulus. Define REG_IN(4-bit)and CLK(1-bit)as reg register variables and REG_OUT(4-bit)as wire. Instantiate the module shift_reg and call it sr1. Connect the ports by ordered list.

My answer:

```
module stimulus;  
reg [3:0]REG_IN;  
reg CLK;  
wire [3:0]REG_OUT;  
shift_reg sr1(REG_OUT,REG_IN,CLK);  
endmodule
```

5. Connect the ports in Step 4 by name.

My answer:

```
shift_reg(.reg_out(REG_OUT),.reg_in(REG_IN),.clock(CLK));
```

6. Write the hierarchical names for variables REG_IN,CLK,REG_OUT;

My answer:

```
stimulus.REG_IN, stimulus.CLK, stimulus.REG_OUT
```

7. Write the hierarchical name for the instance sr1. Write the hierarchical names for its ports clock and reg_in.

My answer:

```
stimulus.sr1,
```

stimulus.sr1.clock

stimulus.sr1.reg_in