ASSIGNMENT WEEK 5

DATAFLOW MODEL, TESTBENCH AND CODE COVERAGE REPORT

Problem 1. Verilog tutorial: Create code coverage report in ModelSim.

Instructions: Link

Screenshot your report.

Problem 2. Make the requirements for each circuit below.

Requirement 1. Write design code: Use dataflow model.

Requirement 2. Write testbench code: Use *$monitor / $dislay* syntax.

Requirement 3. Create code coverage report.

Requirement 4. Screenshot your code, code coverage report,

waveform and transcript.

[1]. Full Adder n – bit.

[2]. Carry Look Ahead Adder n – bit.

[3]. Majority n – bit.

[4]. Gray Counter n – bit.

[5]. Full Adder n – bit.

[6]. Design a 4 – bit comparator: Using 2 – bit comparator. (Lecture 3).