FINAL PROJECT

Each group chooses one of the following topics

1. Implement CNN on FPGA.

- Description:

- Research simple Neural network in image processing, recognize handwritten digits by using Verilog language and upload design to FPGA kit.

- Documents:

- Roman A. Solovyev, Alexandr A. Kalinin, Alexander G. Kustov, Dmitry V. Telpukhov, and Vladimir S. Ruhlov, “FPGA Implementation of Convolutional Neural Networks with Fixed-Point Calculations”

- Link paper: https://ieeexplore.ieee.org/document/8656778

- Source code: https://github.com/ZFTurbo/Verilog-Generator-of-Neural-Net-Digit-Detector-for-FPGA.

2. Implement RTL for I2C protocol

- Description:

- I2C protocol was invented by Philips semiconductors in the 1980s, to provide easy onboard communications between a CPU and various peripheral chips. I²C stands for Inter-Integrated Circuit. It is used for attaching lower-speed peripheral ICs to microcontrollers in short-distance communication. Low-speed peripherals include external EEPROMs, digital sensors, I2C LCD, and temperature sensors.

- Documents:

- I2C Bus Specification, Philips Semiconductor, version 2.1, January 2000
  Link: https://vdocument.in/bus-i2c-philips.html?page=1

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- Bollam Eswari, N.Ponmagal, K.Preethi, S.G.Sreejeesh, "Implementation of I2C Master Bus Controller on FPGA"
  Link paper: https://ieeexplore.ieee.org/document/6577141
- Source code: https://github.com/trondd/oc-i2c

3. Design FFT/IFFT 128 points IP core

- Description:
- FFT is an algorithm for the effective Discrete Fourier Transform calculation.
- Documents:
- Pipelined FFT/IFFT 128 points (Fast Fourier Transform) IP Core User Manual
  Link: FFT/IFFT 128 points
- Source code: https://github.com/freecores/pipelined_fft_128

4. Design a RISC Stored – Program Machine.

- Description:
- Follow the steps in Section 7.3 Design and Synthesis of a RISC Stored Program Machine – Chapter 7. Design and Synthesis of Datapath Controller – Advanced Digital Design with Verilog HDL.
- Documents: Michael D. Ciletti, Advanced Digital Design with the Verilog HDL book.