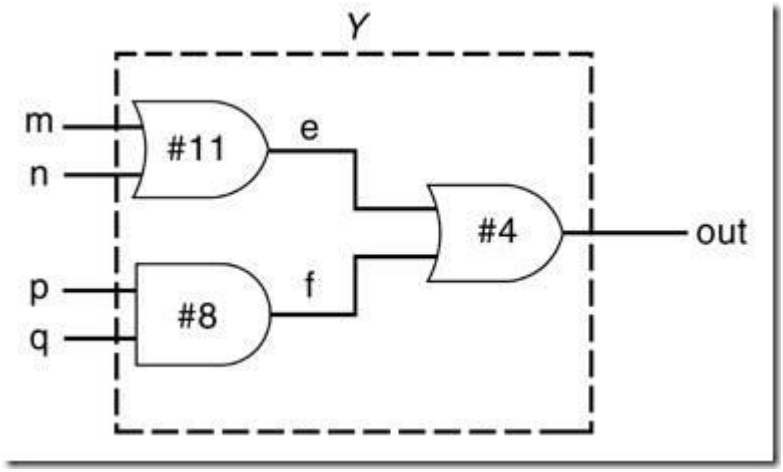
Chapter 10

Chapter 10. Timing and Delays

10.6 Exercises

1. What type of delay model is used in the following circuit? Write the Verilog description for the module Y.



My answer:

Distributed Delay.

```
1   //ex10-1
2   module Y(out,m,n,p,q);
3   output out;
4   input m,n,p,q;
5
6   wire e,f;
7
8   or #11 (e,m,n);
9   and #8 (f,p,q);
10  or #4 (out,e,f);
11
12  endmodule
```

```
1   //stimulus
2   module test;
3
4   reg m,n,p,q;
5   wire out;
6
7   Y y1(out,m,n,p,q);
8
9   initial
10  begin
11    $monitor($time, "out= %b, m= %b, n= %b, p= %b,
12              q= %b",out,m,n,p,q);
13    m=1; n=0; p=1; q=0;
14    #30 m=0; n=0; p=1; q=0;
15    #30 m=0; n=0; p=1; q=1;
16    #30 m=0; n=0; p=0; q=0;
17
18    #50 $finish;
19  end
20
21  endmodule
```

```
  0out= x, m= 1, n= 0, p= 1,
                                q= 0
 15out= 1, m= 1, n= 0, p= 1,
                                q= 0
 30out= 1, m= 0, n= 0, p= 1,
                                q= 0
 45out= 0, m= 0, n= 0, p= 1,
                                q= 0
 60out= 0, m= 0, n= 0, p= 1,
                                q= 1
 72out= 1, m= 0, n= 0, p= 1,
                                q= 1
 90out= 1, m= 0, n= 0, p= 0,
                                q= 0
102out= 0, m= 0, n= 0, p= 0,
                                q= 0
```

2. Use the largest delay in the module to convert the circuit to a lumped delay model. Using a lumped delay model, write the Verilog description for the module Y.

My answer:

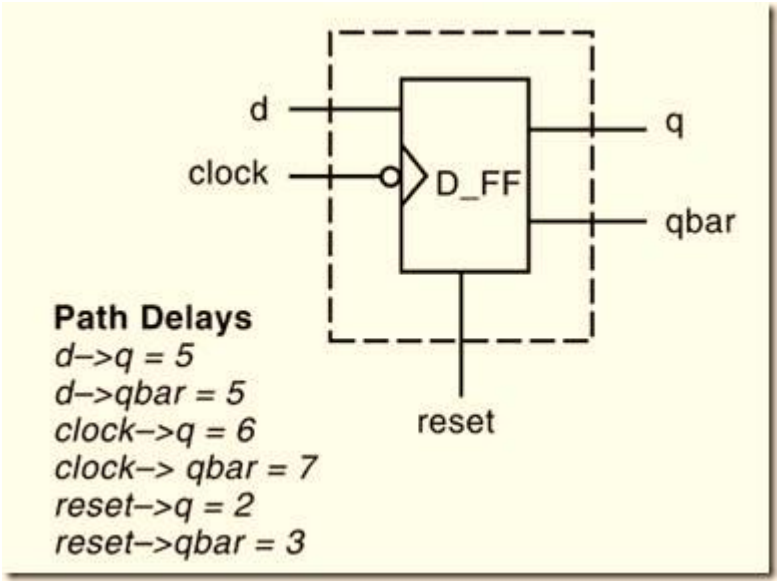
```
1   //ex10-2 lumped delay
2   module Y(out,m,n,p,q);
3   output out;
4   input m,n,p,q;
5
6   wire e,f;
7
8   or (e,m,n);
9   and (f,p,q);
10  or #15 (out,e,f);
11
12  endmodule
```

3. Compute the delays along each path from input to output for the circuit in Exercise 1. Write the Verilog description, using the path delay model. Use specify blocks.

My answer:

```
1   //ex10-3 path delay model
2
3   module Y(out,m,n,p,q);
4   output out;
5   input m,n,p,q;
6
7   wire e,f;
8
9   specify
10    (m=>out)=15;
11    (n=>out)=15;
12    (p=>out)=12;
13    (q=>out)=12;
14  endspecify
15
16  or (e,m,n);
17  and (f,p,q);
18  or (out,e,f);
19
20  endmodule
```

4. Consider the negative edge-triggered with the asynchronous reset D-flipflop shown in the figure below. Write the Verilog description for the module D_FF. Show only the I/O ports and path delay specification. Describe path delays, using parallel connection.



My answer:

```
1   //ex10-4 dff
2   module dff(q,qbar,d,clock,reset);
3   output reg q,qbar;
4   input d,clock,reset;
5
6   specify
7     (d=>q)=5;
8     (d=>qbar)=5;
9     (clock=>q)=6;
10    (clock=>qbar)=7;
11    (reset=>q)=2;
12    (reset=>qbar)=3;
13  endspecify
14
15  always @(negedge clock or posedge reset)
16  begin
17    if(reset)
18      begin
19      q=0;
20      qbar=1;
21      end
22    else
23      begin
24      q=d;
25      qbar=~d;
26      end
27  end
28
29  endmodule
```

```
1   //stimulus
2   module test;
3   reg d,clock,reset;
4   wire q,qbar;
5
6   dff d1(q,qbar,d,clock,reset);
7
8   initial
9   begin
10    clock=1'b0;
11    forever #10 clock=~clock;
12  end
13
14  initial
15  begin
16    d=1'b1;
17    forever #20 d=~d;
18  end
19
20  initial
21  begin
22    reset=1'b1;
23    #34 reset=1'b0;
24    #120 reset=1'b1;
25  end
26
27  endmodule
```

5. Modify the D-flipflop in Exercise 4 if all path dealys are 5 units. Describe the path delays, using full connections to q and qbar.

My answer:

```
6   specify
7     (d,clock,reset *> q,qbar)=5;
8   endspecify
```

6. Assume that a six-delay specification is to be specified for all path delays. All path delays are equal. In the specify block, define parameters t_01=4,t_10=5,t_0z=7,t_z1=2,t_1z=3,t_z0=8. Use the D-flipflop in Exercise 4 and write the six-delay specification for all paths, using full connections.

My answer:

```
6   specify
7     specparam t_01=4,t_10=5,t_0z=7,t_z1=2,t_1z=3,t_z0=8;
8     (d,clock,reset *> q,qbar)=(t_01,t_10,t_0z,t_z1,t_1z,t_z0);
9   endspecify
```

7. In Exercise 4,modify the delay specification for the D-flipflop if the delays are dependent on the value of d as follws:

clock -> q = 5 for d = 1'b0, clock -> q= 6 otherwise

clock -> qbar = 4 for d = 1'b0, clock ->qbar = 7 otherwise

All other delays are 5 units.

My answer:

```
6   specify
7     if(~d) (clock=>q)=5;
8     if(d) (clock=>q)=6;
9     if(~d) (clock=>qbar)=4;
10    if(d) (clock=>qbar)=7;
11    (d,reset *> q,qbar)=5;
12  endspecify
```

8. For the D-flipflop in Exercise 7, add timing checks for the D_flipflop in the specify block as follows:

The minimum setup time for d with respect to clock is 8.

The minimum hold time for d with respect to clock is 4.

The reset signal is active high. The minimum width of a reset pulse is 42.

My answer:

```
6   specify
7     $setup(d,clock,8);
8     $hold(clock,d,4);
9     $width(posedge reset,42);
```