## Chapter 7: (Part 1)

## **Chapter 7. Behavioural Modelling**

#### 7.11 Exercises

1. Declare a register called oscillate. Initialize it to 0 and make it toggle every 30 time units. Do not use always statement (Hint: Use the forever loop).

My answer:

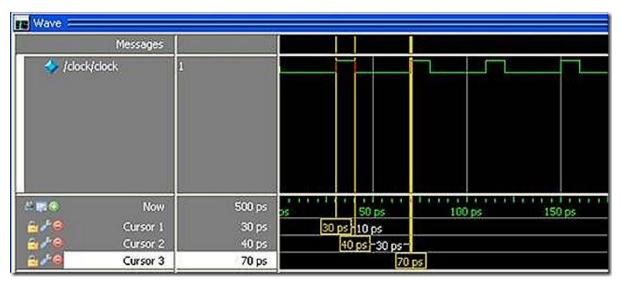
```
1 //ex7 1 forever loop
2 //module test;
3 reg oscillate;
5 initial
6 begin
7
    oscillate=1'b0;
    forever #30 oscillate=~oscillate;
9 end
10
11 /*initial
12
    $monitor($time, " oscillate= %b",oscillate);
13
14 initial
15
    #500 $finish;
16
17 endmodule*/
```

```
0 oscillate= 0
30 oscillate= 1
60 oscillate= 0
90 oscillate= 1
120 oscillate= 0
150 oscillate= 1
180 oscillate= 0
210 oscillate= 1
240 oscillate= 0
270 oscillate= 1
300 oscillate= 0
```

2. Design a clock with time period = 40 and a duty cycle of 25% by using the always and initial statements. The value of clock at time = 0 should be initialized to 0.

My answer:

```
1 //ex7 2 clock
2 module clock;
3 reg clock;
5 initial
6
    clock=1'b0;
7
 8 always
9 begin
    #30 clock=~clock;
10
    #10 clock=~clock;
11
12 end
13
14 initial
    $monitor($time, " clock= %b", clock);
15
16
17 endmodule
```



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3. Given below is an initial block with blocking procedural assignments. At what simulation time is each statement executed? What are the intermediate and final values of a, b, c, d?

```
initial
begin
    a = 1'b0;
    b = #10 1'b1;
    c = #5 1'b0;
    d = #20 {a, b, c};
end
```

My answer:

```
0 a= 0, b= x, c= x, d= xxx

10 a= 0, b= 1, c= x, d= xxx

15 a= 0, b= 1, c= 0, d= xxx

35 a= 0, b= 1, c= 0, d= 010
```

4. Repeat exercise 3 if nonblocking procedural assignments were used.

My answer:

```
0 a= 0, b= x, c= x, d= xxx
5 a= 0, b= x, c= 0, d= xxx
10 a= 0, b= 1, c= 0, d= xxx
```

5. What is the order of execution of statements in the following Verilog code? Is there any ambiguity in the order of execution? What are the final values of a,b,c,d?

My answer:

# 6. What is the final value of d in the following example? (Hint: See intraassignment delays.)

### My answer: