

Chapter 2

Chapter 2. Hierarchical Modelling Concepts

2.8 Exercises

1. An interconnect switch (IS) contains the following components, a shared memory (MEM), a system controller (SC) and a data crossbar (Xbar).

a) Define the modules MEM, SC, and Xbar, using the module/endmodule keywords. You do not need to define the internals. Assume that the modules have no terminal lists.

b) Define the module IS, using the module/endmodule keywords. Instantiate the modules MEM, SC, Xbar and call the instance mem1, sc1, and xbar1, respectively. You do not need to define the internals. Assume that the module IS has no terminals.

c) Define a stimulus block (Top), using the module/endmodule keywords. Instantiate the design block IS and call the instance is1. This is the final step in building the simulation environment.

My answer:

a)

```
1 module MEM;
2 endmodule
3
4 module SC;
5 endmodule
6
7 module Xbar;
8 endmodule
```

b)

```
10 module IS;
11
12 MEM mem1;
13 SC sc1;
14 Xbar xbar1;
15
16 endmodule
```

c)

```
18 module Top;  
19  
20 IS is1;  
21  
22 endmodule
```

2. A 4-bit ripple carry adder (Ripple_Add) contains four 1-bit full adders (FA).

a) Define the module FA. Do not define the internals or the terminal list.

b) Define the module Ripple_Add. Do not define the internals or the terminal list. Instantiate four full adders of the type FA in the module Ripple_Add and call them fa0, fa1, fa2, fa3.

My answer:

a)

```
24 module FA;  
25  
26 endmodule;
```

b)

```
28 module Ripple_Add;  
29  
30 FA fa0;  
31 FA fa1;  
32 FA fa2;  
33 FA fa3;  
34  
35 endmodule
```