Chapter 3

Chapter 3. Basic Concepts

3.5 Exercises

1. Practice writing the following numbers:

a) Decimal number 123 as a sized 8-bit number in binary. Use _ for readability.

b) A 16-bit hexadecimal unknown number with all x's.

c) A 4-bit negative 2 in decimal. Write the 2's complement form for this number.

d) An unsized hex number 1234.

My answer:

a) 123 = 8'b0111_1011

b) 16'hx

c) -4'd2=4'b1110

d) 32'h1234

2. Are the following legal strings? If not, write the correct strings.

a) "This is a string displaying the % sign"

b) "out=in1+in2"

c) "Please ring a bell \007"

d) "This is a backslash \ character\n"

My answer:

a) "This is a string displaying the %% sign"

b) right

c) right

d) "This is a backslash \\ character"

3. Are these legal identifiers ?

a) system1

b) 1reg

c) $latch

d) exec$

My answer:

a) right

4. Declare the following variables in Verilog:

a) An 8-bit vector net called a_in.

b) A 32-bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32-bit decimal number equal to 3.

c) An integer called cout.

d) A time variable called snap_shot.

e) An array called delays. Array contains 20 elements of the type integer.

f) A memory MEM containing 256 words of 64 bits each.

g) A parameter cache_size equal to 512.

My answer:

a) wire [7:0] a_in;

b) reg [31:0] address=32'd3;

c) integer cout;

d) time snap_shot;

e) integer delays [0:19];

f) reg [63:0] MEM [0:255];

g) parameter cache_size=512;

5. What would be the output/effect of the following statements ?

a) latch = 4'd12;

$display("The current value of latch = %b\n", latch);

b) in_reg=3'd2;

$monitor($time, " In register value = %b\n", in_reg[2:0]);

c) `define MEM_SIZE 1024

$display(" The maximum memory size is %h", `MEM_SIZE);

My answer:

a) The current value of latch =4'b1100

b) 0 In register value = 3'b010

c) The maximum memory size is 'h400