ASSIGNMENT WEEK 14

1. **FSM, ASM.**

a. Draw state diagram and ASM for code in page 124 (FPGA PROTOTYPING BY VERILOG EXAMPLES book).

Write testbench for that design (screenshot your waveform)

b. Draw state diagram and ASM for number detection circuit (the number is 0100)

Write RTL and testbench code.

2. **Blocking and non – blocking statement**

Draw timing diagram for *signal1* and *signal2*

```
module block();
reg signal1;
initial begin
signal1 = 0;
#10 signal1 = 1'b1;
#30 signal1 = 1'b0;
#40 signal1 = 1'b1;
.........................
```

```
module non_block();
reg signal2;
initial begin
signal2 <= 0;
#10 signal2 <= 1'b1;
#30 signal2 <= 1'b0;
#40 signal2 <= 1'b1;
.........................
```

3. **Draw the circuit after synthesizing the following code**

```
reg a, b, result, c1, c2;
if (c1)
    result = a & b;
else if (c2)
    result = a ^ b;
else
    result = a | b;
```

```
reg a, b, result, c1;
if (c1)
    result = a & b;
else
    result = a | b;
```

```
always @ (a, b, c, sel)
  begin
    case (sel)
      2'b00  :  out = a;
      2'b01  :  out = b;
      2'b10  :  out = c;
      default:  out = 0;
    endcase
  end
```