ASSIGNMENT WEEK 6

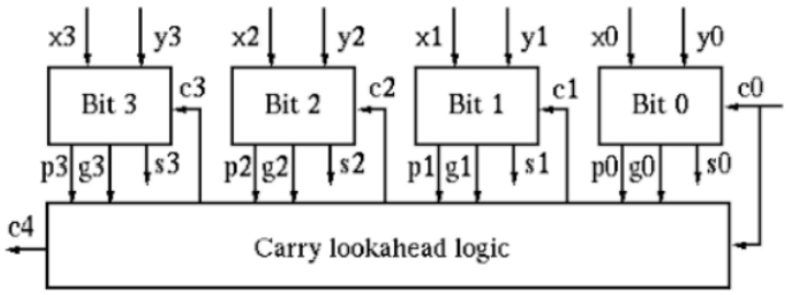
Problem 1. Use data flow model, screenshot desgin code, testbench code, waveform, code coverage report.

1. Design circuits two numbers 4 – bit

- Input: [3:0]A, B.
- Output :

- A_lt_B = 1 if A < B.
- A_eq_B = 1 if A = B.
- A_gt_B = 1 if A > B.

2. Design and compare 4 – bit Full Adder with Carry Look Ahead Adder 4 – bit about: Structure, delay, speed.



Problem 2. Answer the following questions:

1. Describe the statement assign (continuous assignment).
2. Define, give examples of expressions, operands, operator in DataFlow Modeling.
3. List the types of operators used in DataFlow Modeling (arithmetic, logical, relational, equality, bitwise, reduction, shift, concatenation, and conditional), give examples.

   Instruction: 6.1 Continuous Assignments,6.3 Expressions , Operators, and Operands, 6.4 Operator Types–Chapter 6. Dataflow Modeling–Verilog HDL Samir

Problem 3. Read and follow the steps in Chapter 8. Automated Simulation in ModelSim Turtorial.