ASSIGNMENT WEEK 4:
STRUCTURAL MODEL AND TESTBENCH BASICS

Problem 1. 16 – bit Carry Look Ahead Adder

Write code Verilog: Design code and testbench code.

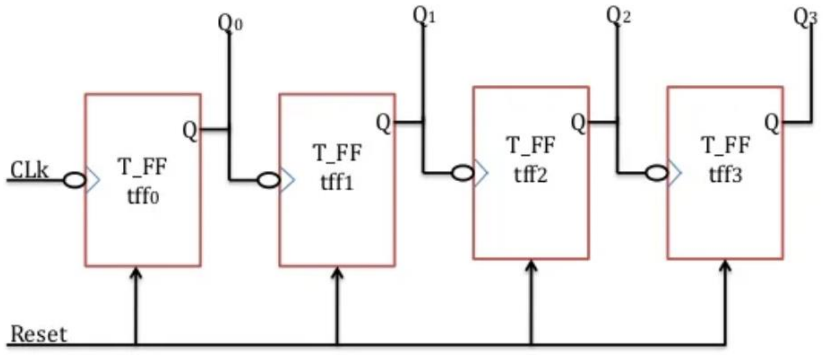
Note: A 16 – bit Carry Look Ahead Adder can be formed by cascading four 4 – bit Carry Look Ahead Adder.

Problem 2. Ripple Carry Counter

Write code Verilog: Design code and testbench code for Ripple Carry Counter

Simulate and explain your design.

Note: Using T - flipflop (structural model) you designed in week 3.



Problem 3. Design 4 – bit Gray Counter.

Write code Verilog: Design code and simulation by testbench.

Note: Using $display syntax and screenshot waveform.

Problem 4. Design BCD to 7 Segment Display Decoder.

Write code Verilog: Design code and simulation by testbench.