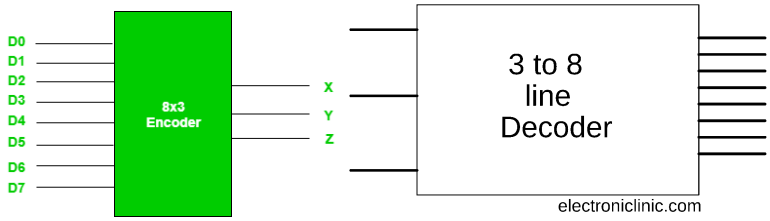
WEEK 3. STRUCTURAL MODEL

1. **Learn the basics of *initial* and *always* block.**
2. **Write testbench file for all problems in W2.pdf file.**

   (Problem 1, Majority, Mux 2x1, Adder circuit)
3. **Encoder (8x3) and Decoder (3x8)**
   a. Construct truth table.
   b. Determine output function.
   c. Write code Verilog for that circuit: design code and simulation by testbench.



4. **Flip flops (FFs): T-FF, D-FF, JK-FF, SR-FF.**
   a. Draw the logic circuit of flip flops
   b. Construct truth table.
   c. Write code Verilog for those circuits: design code and simulation by testbench.

   Note:

   - *Using structural model.*
   - *Flip flops include reset signal.*