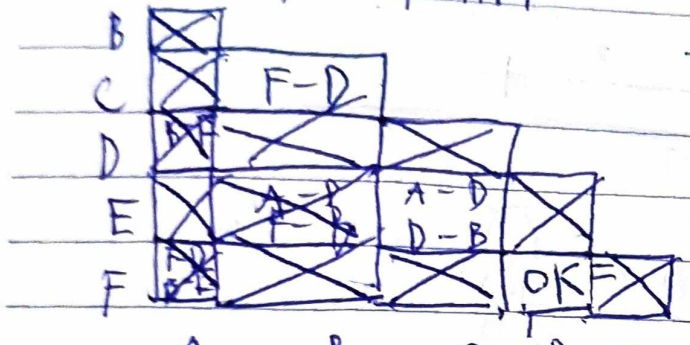
## Sequential Circuit

Prob 5 1, FSM, JKFF




⇒ $u_0 = \{A\}$

$u_1 = \{B, C\}$

$u_2 = \{D, F\}$

$u_3 = \{E\}$

Moore machine

using straight forward encoding ⇒

$u_0 = 00$ A

$u_1 = 01$ (B, C)

$u_2 = 10$ (D, F)

$u_3 = 11$ (E)

Next state table

| Current State | Next State $x=0$ | Next State $x=1$ | Output z |
|---|---|---|---|
| 00 | 10 | 01 | 0 |
| 01 | 00 | 10 | 1 |
| 10 | 10 | 11 | 0 |
| 11 | 10 | 01 | 1 |

KLONG

Date . . No.

| Current state $(Q_1 Q_0)$ | Next state $(Q_1' Q_0')$ $x=0$ | $J_1 K_1$ | $J_0 K_0$ | $x=1$ | $J_1 K_1$ | $J_0 K_0$ | Output z |
|---|---|---|---|---|---|---|---|
| 00 | 10 | 1d | 0d | 01 | 0d | 1d | 0 |
| 01 | 00 | 0d | d1 | 10 | 1d | d1 | 1 |
| 10 | 10 | d0 | 0d | 11 | d0 | d1 | 0 |
| 11 | 10 | d0 | d1 | 01 | d1 | d0 | 1 |

| JK | | J | K |
|---|---|---|---|
| A | B | | |
| 0 | 0 | 0 | d |
| 0 | 1 | 1 | d |
| 1 | 0 | d | 1 |
| 1 | 1 | d | 0 |

$J_1$

| $Q_1Q_0$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 0 | 1 |
| 11 | d | d |
| 10 | d | d |

$\Rightarrow J_1 = Q_0 x + Q_0' x'$

$= Q_0 \oplus x$

$K_1$

| $Q_1Q_0$ \ x | 0 | 1 |
|---|---|---|
| 00 | d | d |
| 01 | d | d |
| 11 | 0 | 1 |
| 10 | 0 | 0 |

$\Rightarrow K_1 = Q_0 x$

$J_0$

| $Q_1Q_0$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | d | d |
| 11 | d | d |
| 10 | 0 | d |

$\Rightarrow J_0 = x$

$K_0$

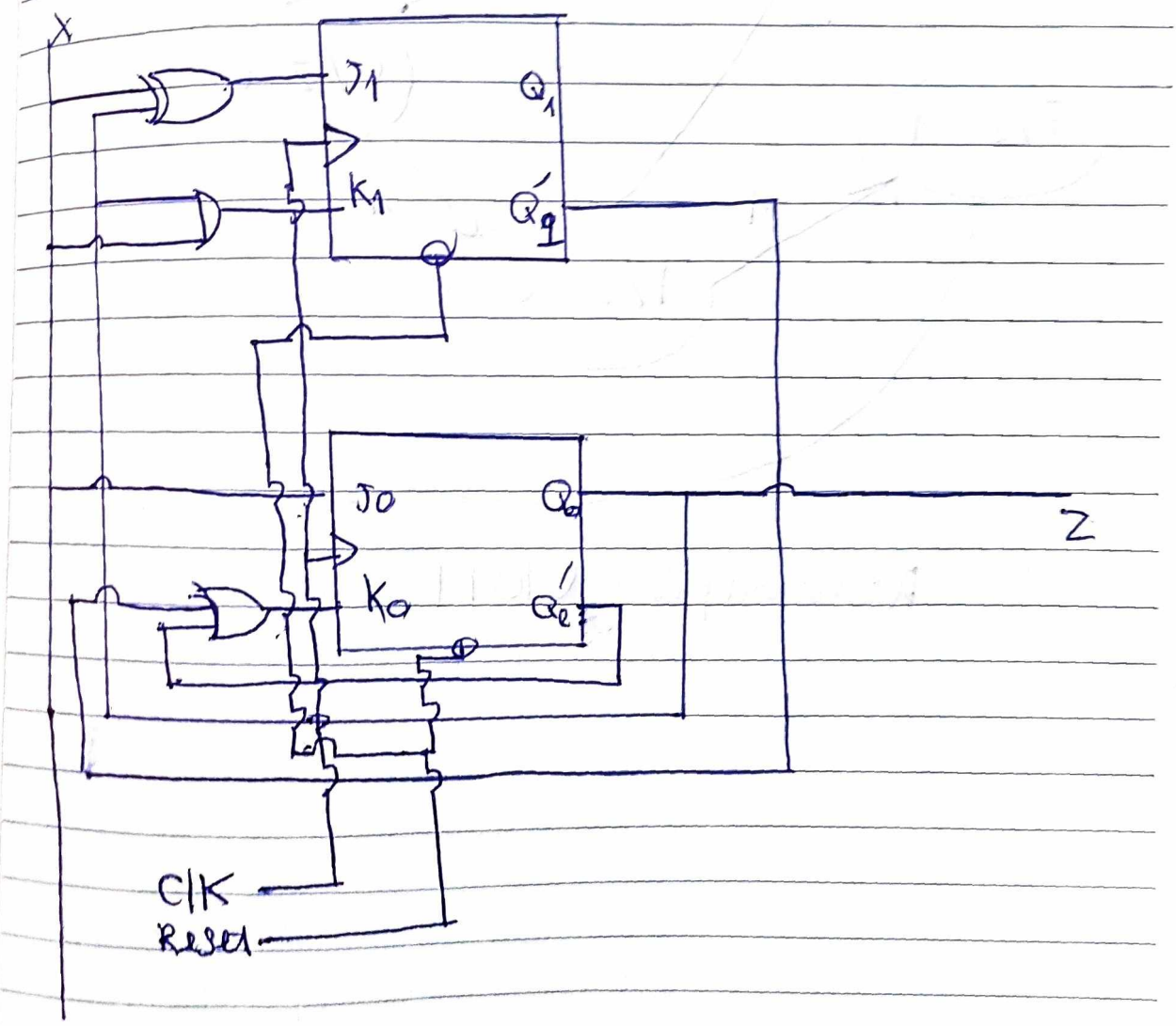
| $Q_1Q_0$ \ x | 0 | 1 |
|---|---|---|
| 00 | d | d |
| 01 | 1 | 1 |
| 11 | 1 | 0 |
| 10 | d | 1 |

$\Rightarrow K_0 = Q_1' + Q_0'$

Date

$\Rightarrow z = Q_0$

| $Q_1 Q_0$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | 1 | 1 |
| 11 | 1 | 1 |
| 10 | 0 | 0 |




2) output 01011

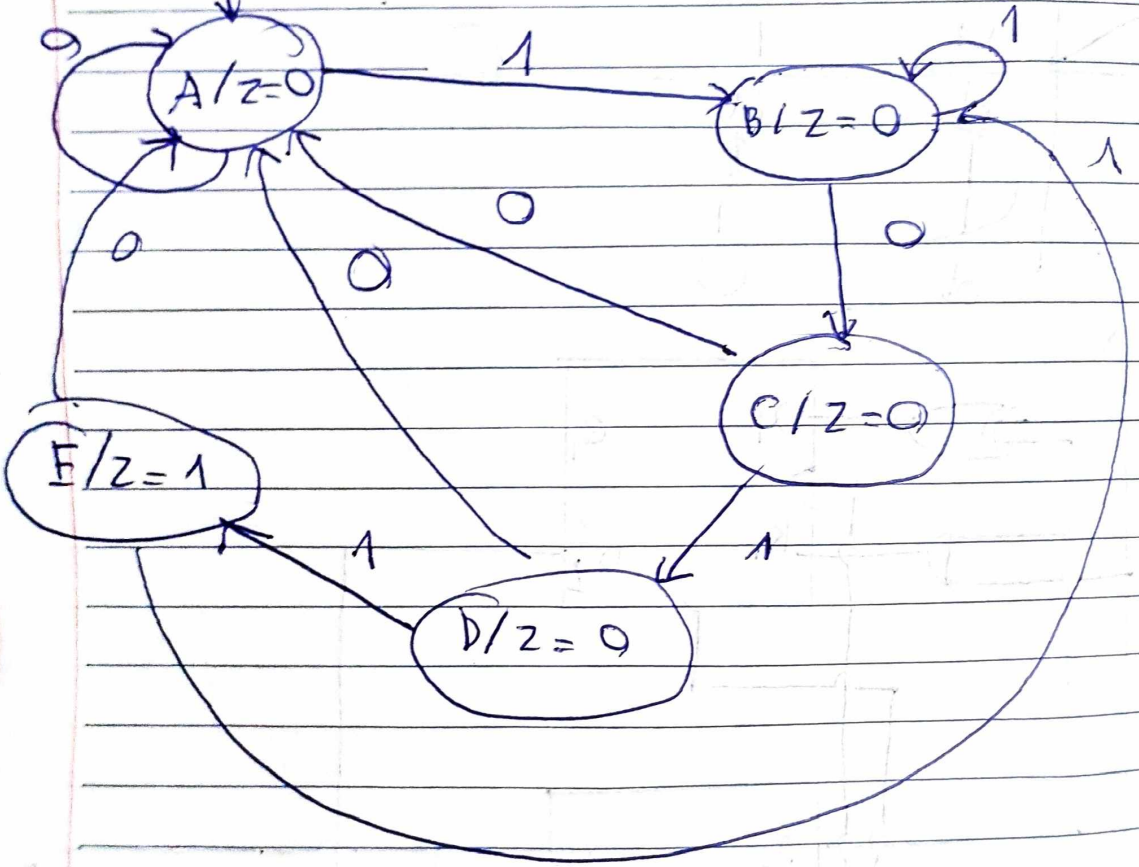
KLONG

Where A : 00
B : 01
C : 010
D : 0101
E : 01011

Moore machine

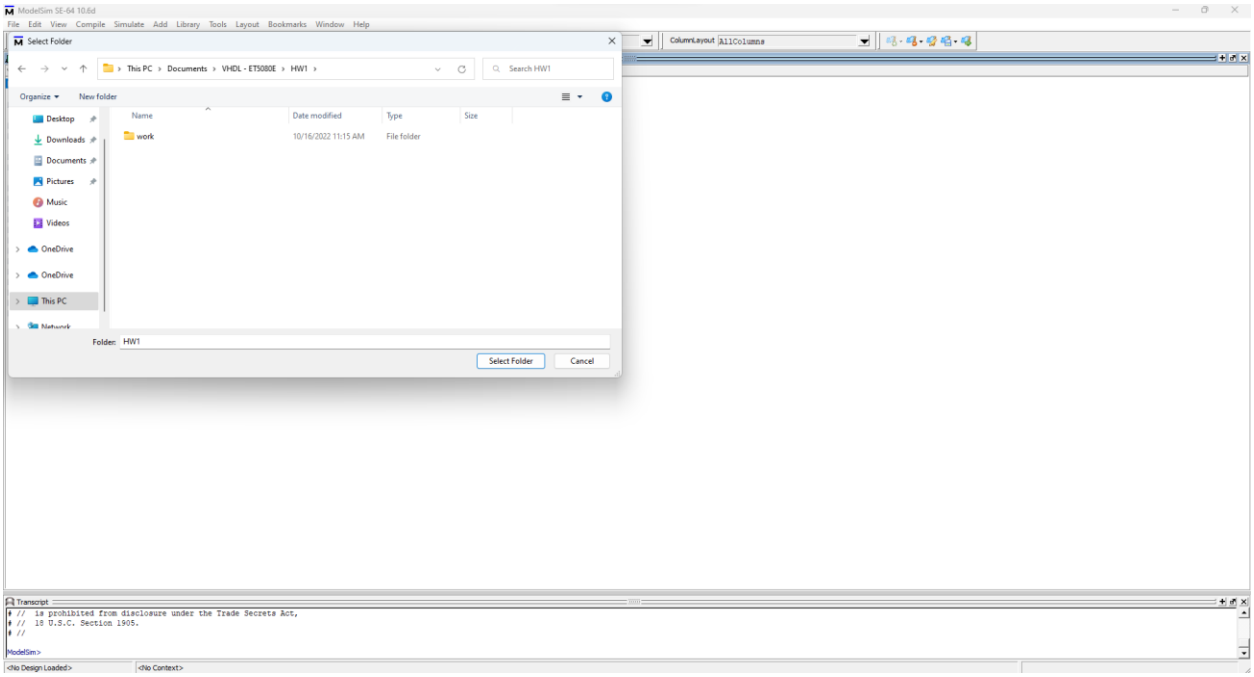
Reset

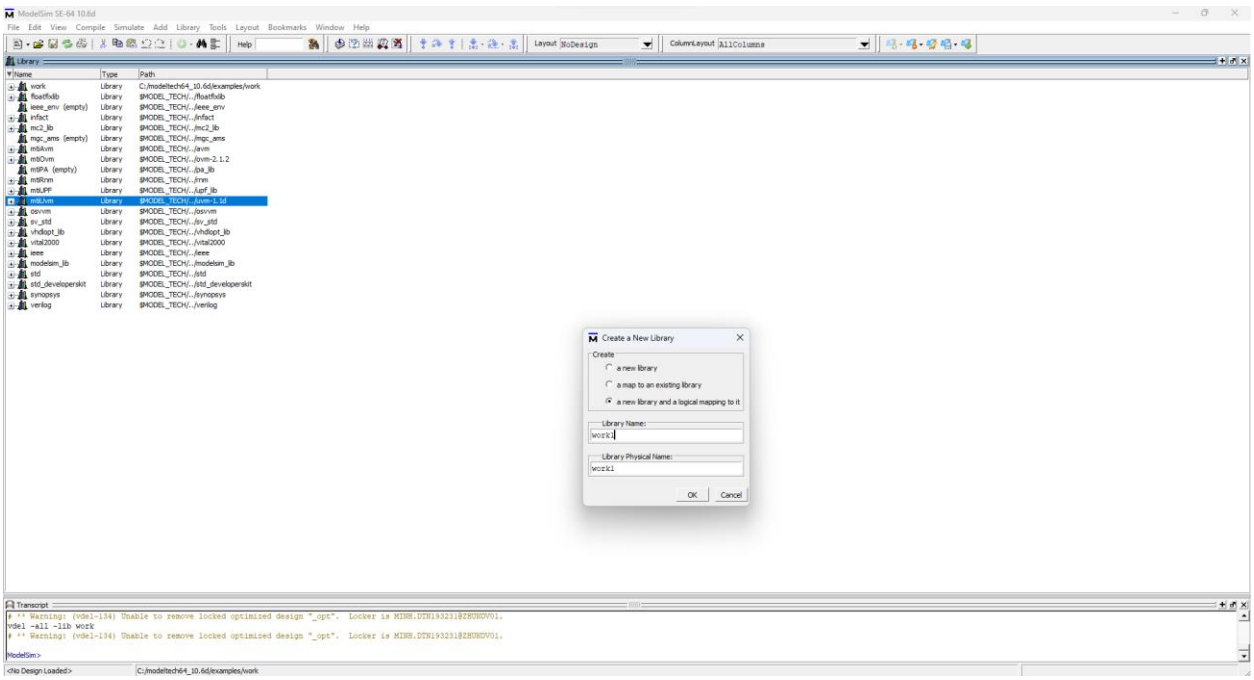
Num Enter (0/1)

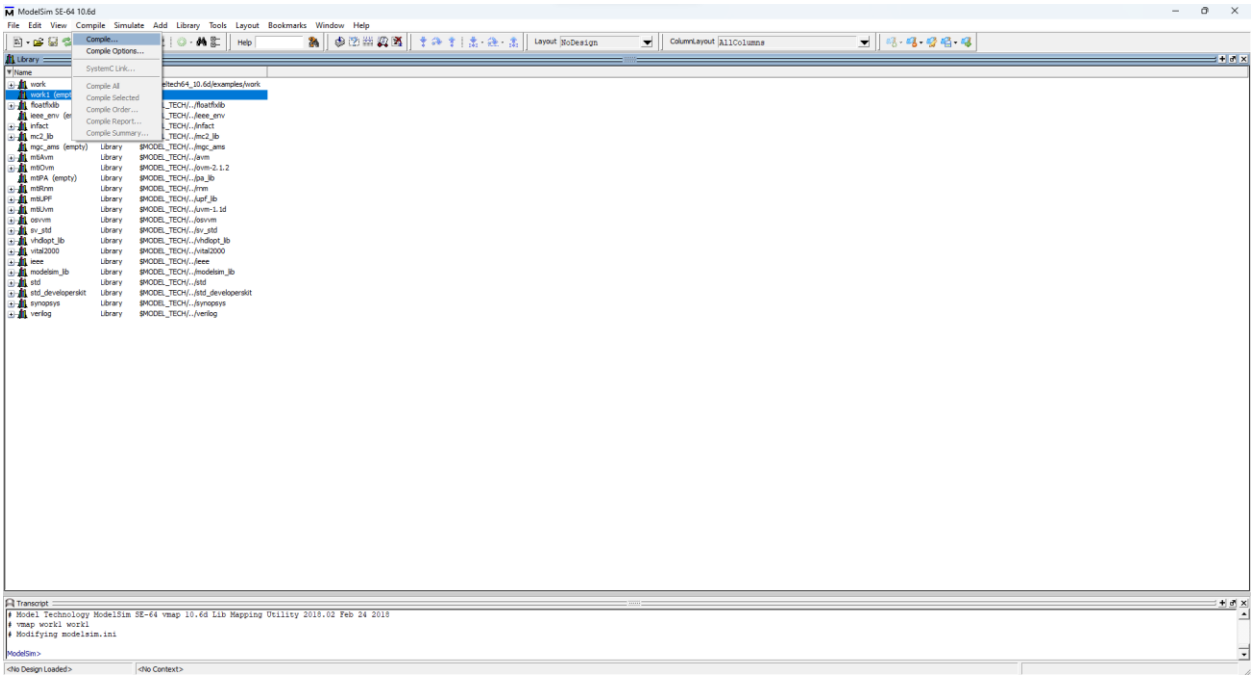


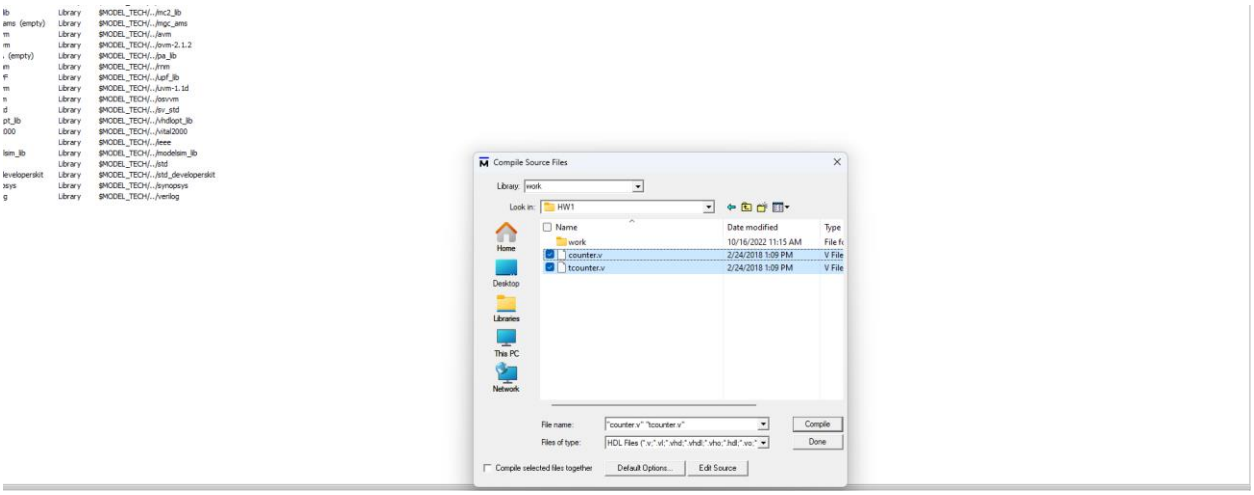

Desired output : 01011

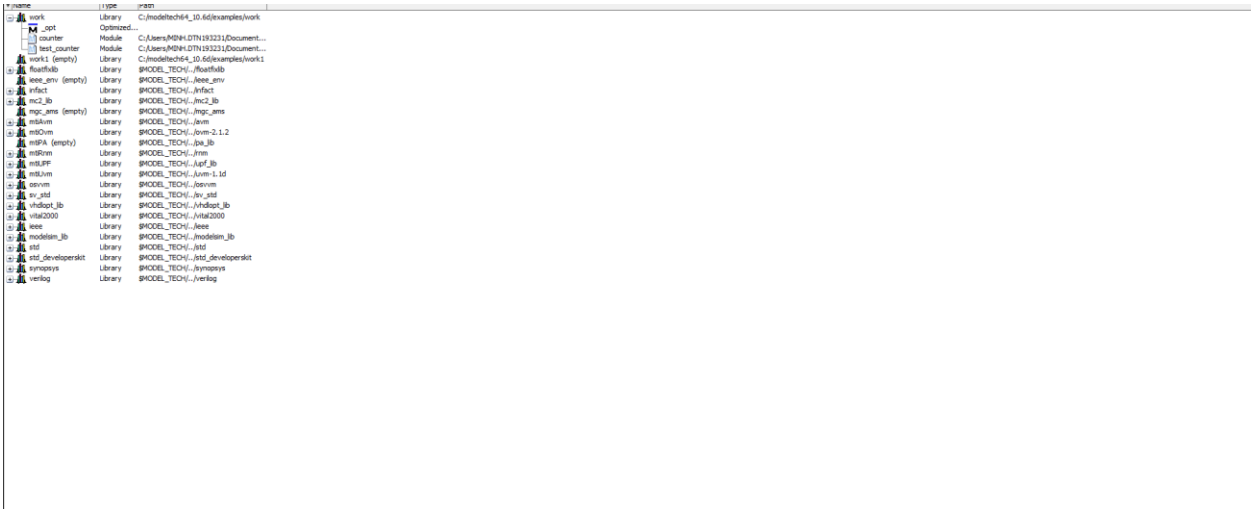
## Chapter 3 Simulation

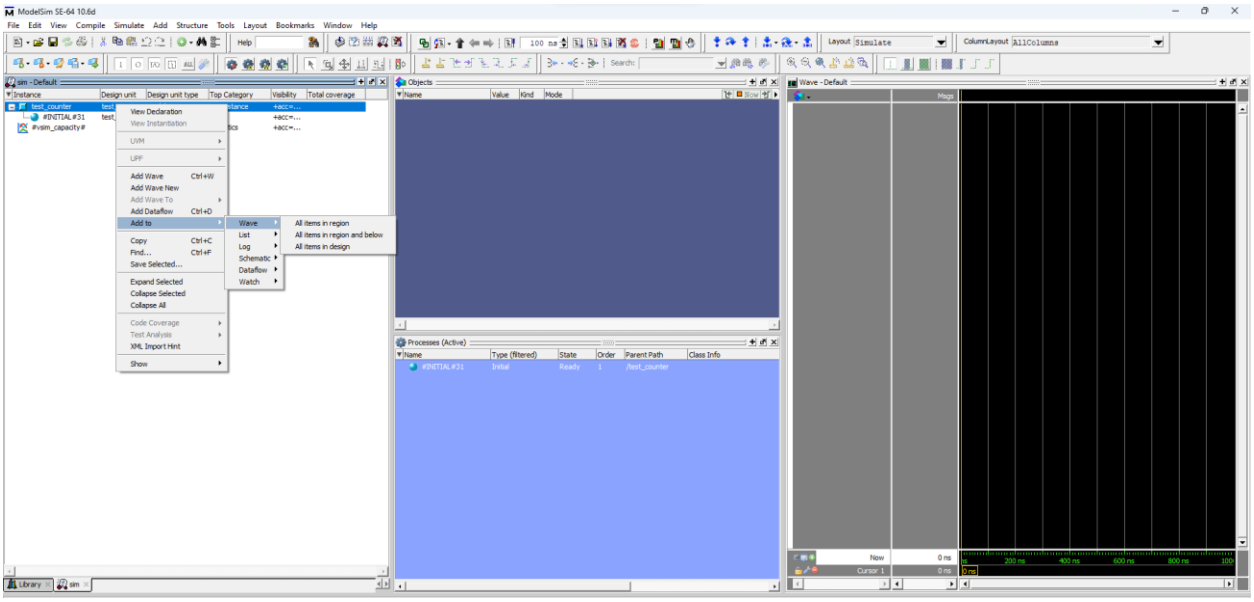


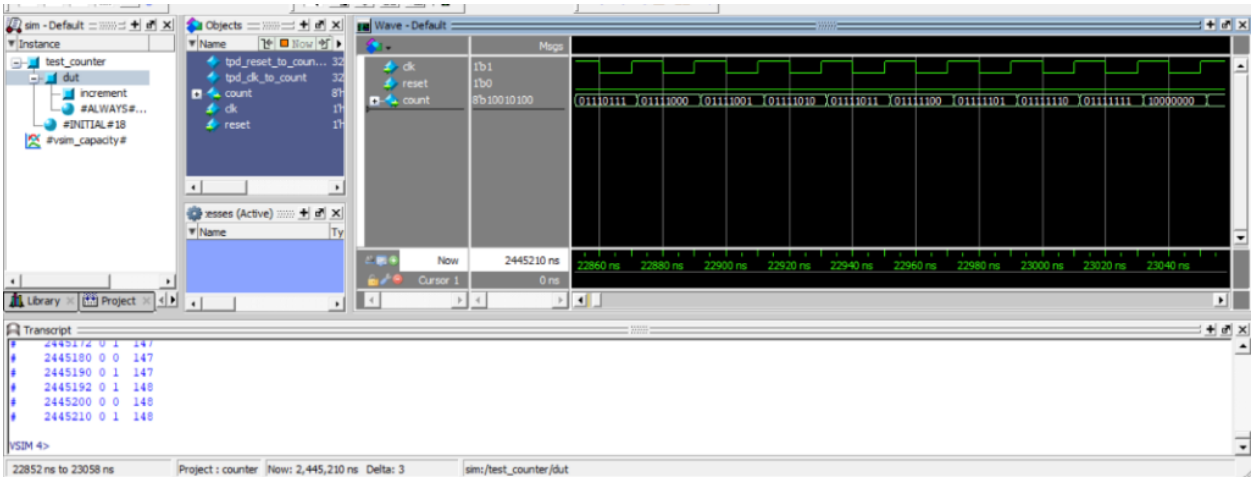




ModelSim SE-64 10.6d
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
Compile...
Compile Options...
SystemC Link...
Compile All
Compile Selected
Compile Order...
Compile Report...
Compile Summary...
Transcript
# Model Technology ModelSim SE-64 vmap 10.6d Lib Mapping Utility 2018.02 Feb 24 2018
# vmap work1 work1
# Modifying modelsim.ini
ModelSim>
<No Design Loaded>
<No Context>

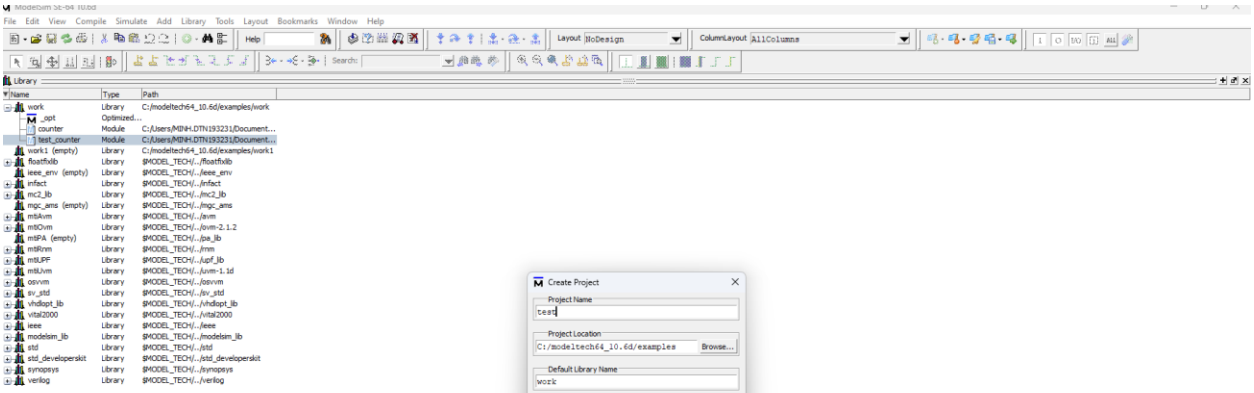

Compile Source Files
Library: work
Look in: HW1
Name
Date modified
Type
work
10/16/2022 11:15 AM
counter.v
2/24/2018 1:09 PM
tcounter.v
2/24/2018 1:09 PM
Home
Desktop
Libraries
This PC
Network
File name: "counter.v" "tcounter.v"
Files of type: HDL Files (*.v;*.vl;*.vhd;*.vhdl;*.vho;*.hdl;*.vo;*...
Compile
Done
Compile selected files together
Default Options...
Edit Source


work
Library
C:/modeltech64_10.6d/examples/work
_opt
Optimized...
counter
Module
test_counter
Module
work1 (empty)
Library
C:/modeltech64_10.6d/examples/work1


ModelSim SE-64 10.6d
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
sim - Default
Instance
Design unit
Design unit type
Top Category
Visibility
Total coverage
test_counter
#INITIAL#31
#vsim_capacity#
View Declaration
View Instantiation
UVM
UPF
Add Wave Ctrl+W
Add Wave New
Add Wave To
Add Dataflow Ctrl+D
Add to
Copy Ctrl+C
Find... Ctrl+F
Save Selected...
Expand Selected
Collapse Selected
Collapse All
Code Coverage
Test Analysis
XML Import Hint
Show
Wave
List
Log
Schematic
Dataflow
Watch
All items in region
All items in region and below
All items in design
Objects
Name
Value
Kind
Mode
Processes (Active)
Type (filtered)
State
Order
Parent Path
Class Info
Wave - Default
Msgs
Now
Cursor 1
Library
sim

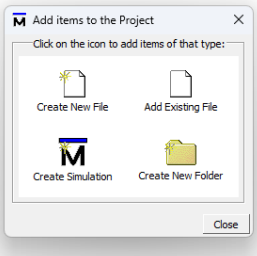

sim - Default
Instance
test_counter
dut
increment
#ALWAYS#...
#INITIAL#18
#vsim_capacity#
Objects
Name
tpd_reset_to_coun... 32
tpd_clk_to_count 32
count 8'h
clk 1'h
reset 1'h
Wave - Default
Msgs
clk 1'b1
reset 1'b0
count 8'b10010100
(01110111) (01111000) (01111001) (01111010) (01111011) (01111100) (01111101) (01111110) (01111111) (10000000)
Now 2445210 ns
Cursor 1 0 ns
22860 ns 22880 ns 22900 ns 22920 ns 22940 ns 22960 ns 22980 ns 23000 ns 23020 ns 23040 ns
Library
Project
Transcript
# 2445180 0 0 147
# 2445190 0 1 147
# 2445192 0 1 148
# 2445200 0 0 148
# 2445210 0 1 148
VSIM 4>
22852 ns to 23058 ns
Project : counter
Now: 2,445,210 ns Delta: 3
sim:/test_counter/dut

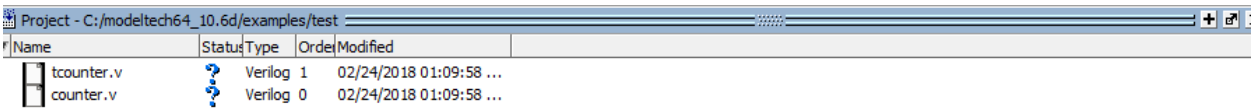
# Chapter 4 Simulation

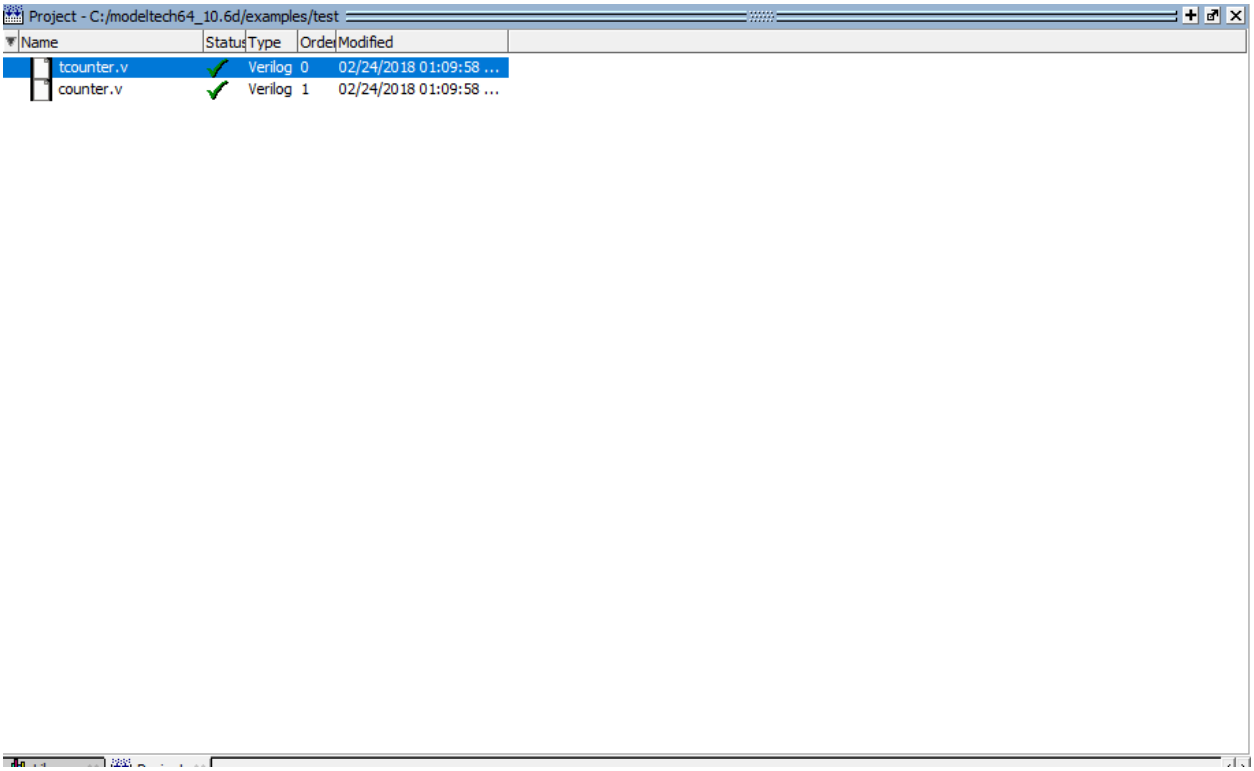


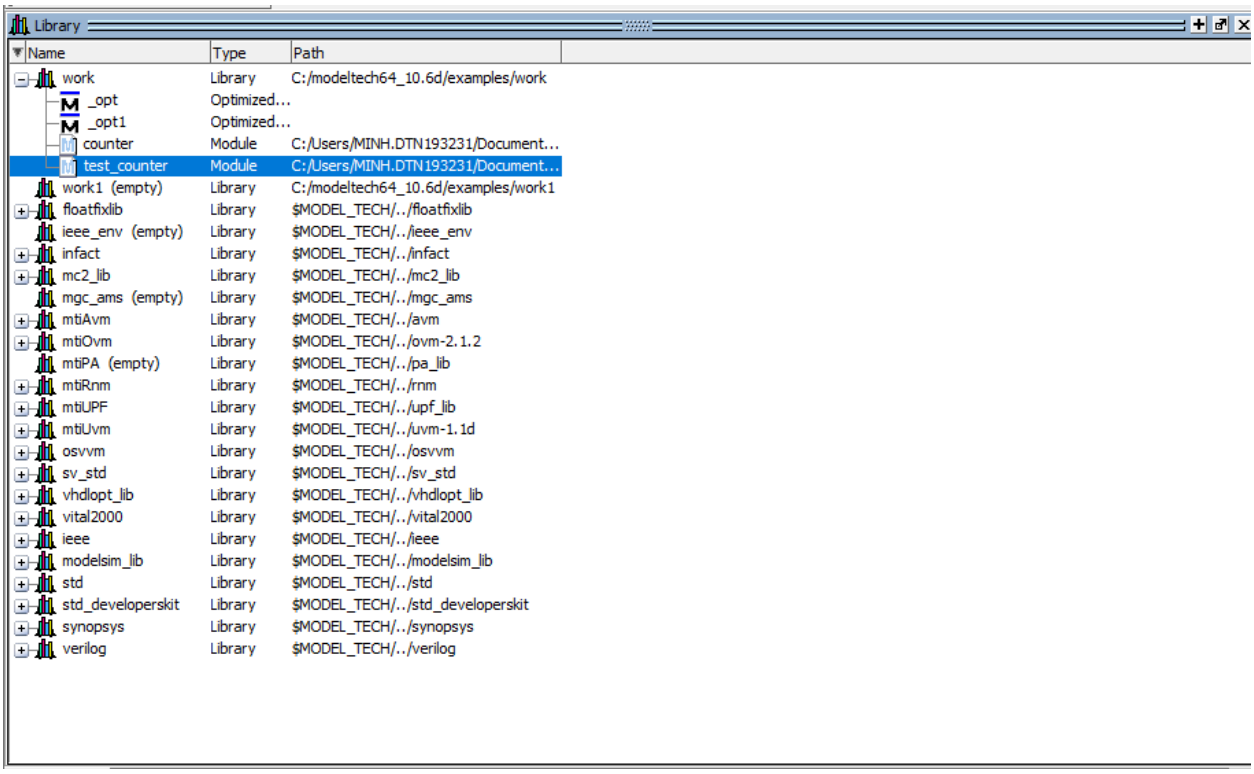


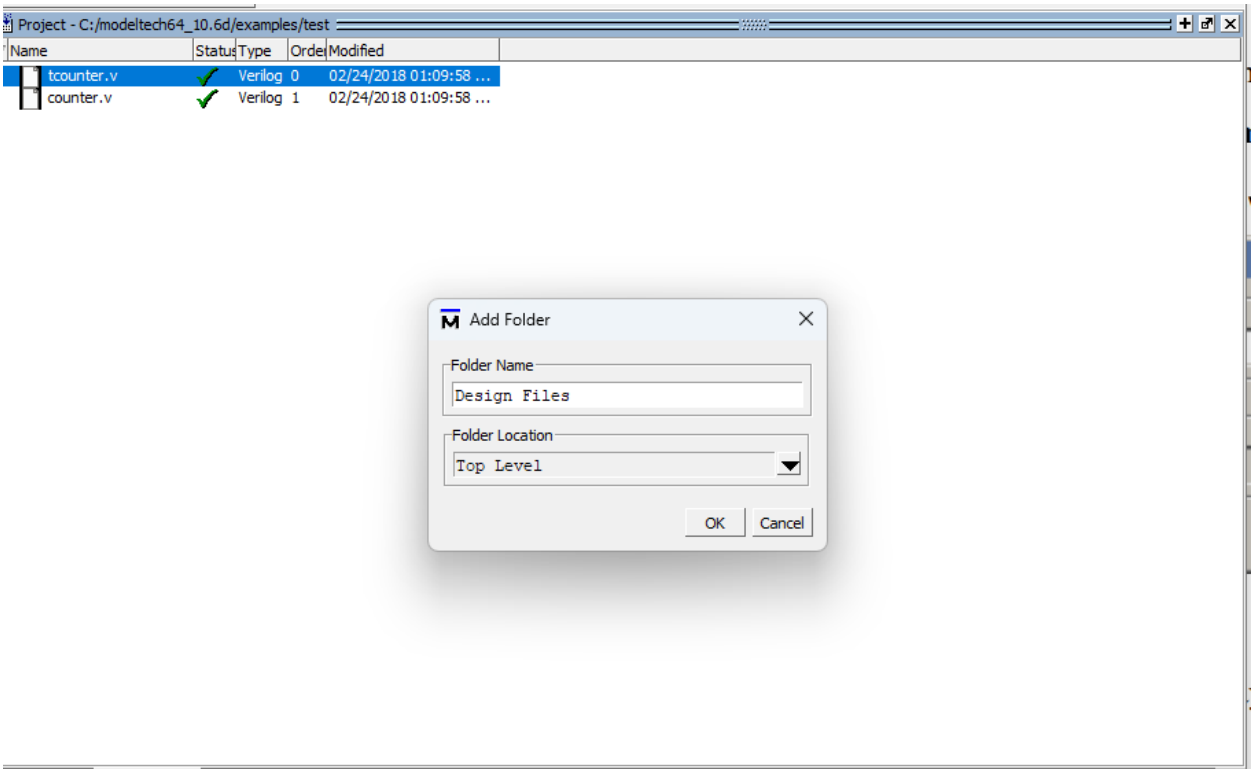




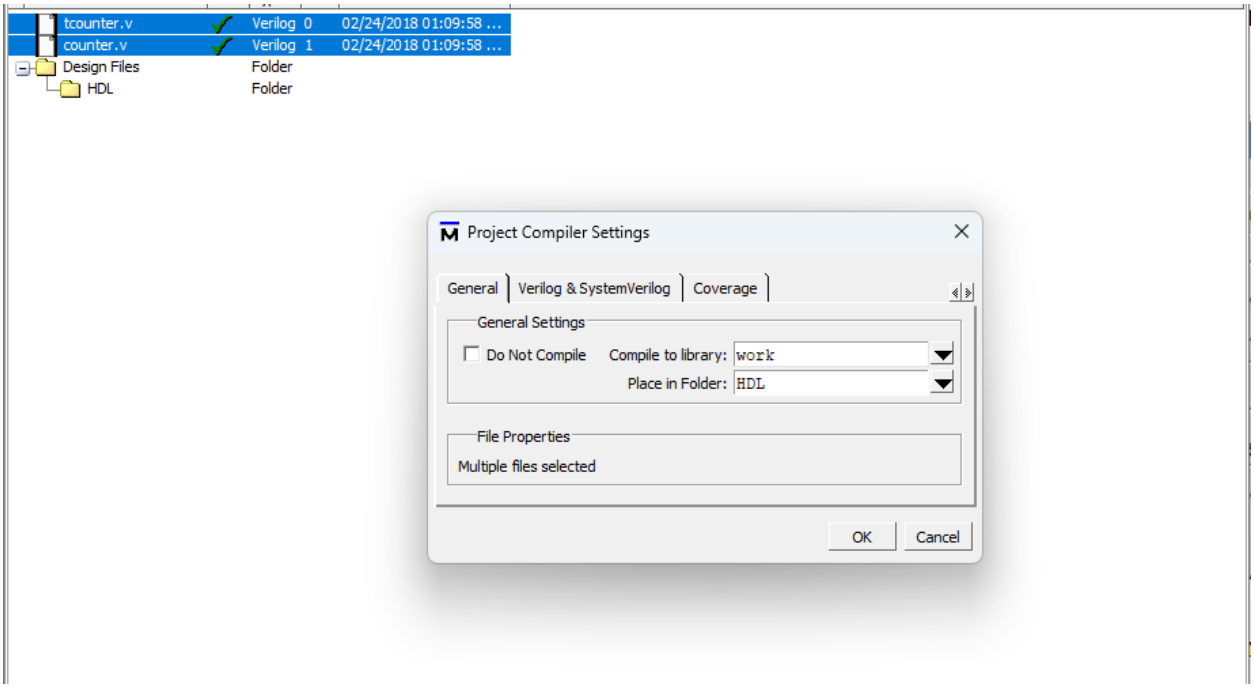

Project - C:/modeltech64_10.6d/examples/test
Name
Status
Type
Order
Modified
tcounter.v
Verilog
1
02/24/2018 01:09:58 ...
counter.v
Verilog
0
02/24/2018 01:09:58 ...


Project - C:/modeltech64_10.6d/examples/test
Name
Status
Type
Order
Modified
tcounter.v
Verilog
0
02/24/2018 01:09:58 ...
counter.v
Verilog
1
02/24/2018 01:09:58 ...

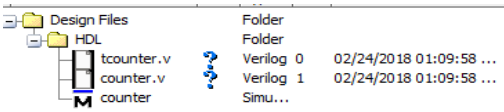

Library
Name
Type
Path
work
Library
C:/modeltech64_10.6d/examples/work
_opt
Optimized...
_opt1
Optimized...
counter
Module
C:/Users/MINH.DTN193231/Document...
test_counter
Module
C:/Users/MINH.DTN193231/Document...
work1 (empty)
Library
C:/modeltech64_10.6d/examples/work1
floatfixlib
Library
$MODEL_TECH/../floatfixlib
ieee_env (empty)
Library
$MODEL_TECH/../ieee_env
infact
Library
$MODEL_TECH/../infact
mc2_lib
Library
$MODEL_TECH/../mc2_lib
mgc_ams (empty)
Library
$MODEL_TECH/../mgc_ams
mtiAvm
Library
$MODEL_TECH/../avm
mtiOvm
Library
$MODEL_TECH/../ovm-2.1.2
mtiPA (empty)
Library
$MODEL_TECH/../pa_lib
mtiRnm
Library
$MODEL_TECH/../rnm
mtiUPF
Library
$MODEL_TECH/../upf_lib
mtiUvm
Library
$MODEL_TECH/../uvm-1.1d
osvvm
Library
$MODEL_TECH/../osvvm
sv_std
Library
$MODEL_TECH/../sv_std
vhdlopt_lib
Library
$MODEL_TECH/../vhdlopt_lib
vital2000
Library
$MODEL_TECH/../vital2000
ieee
Library
$MODEL_TECH/../ieee
modelsim_lib
Library
$MODEL_TECH/../modelsim_lib
std
Library
$MODEL_TECH/../std
std_developerskit
Library
$MODEL_TECH/../std_developerskit
synopsys
Library
$MODEL_TECH/../synopsys
verilog
Library
$MODEL_TECH/../verilog

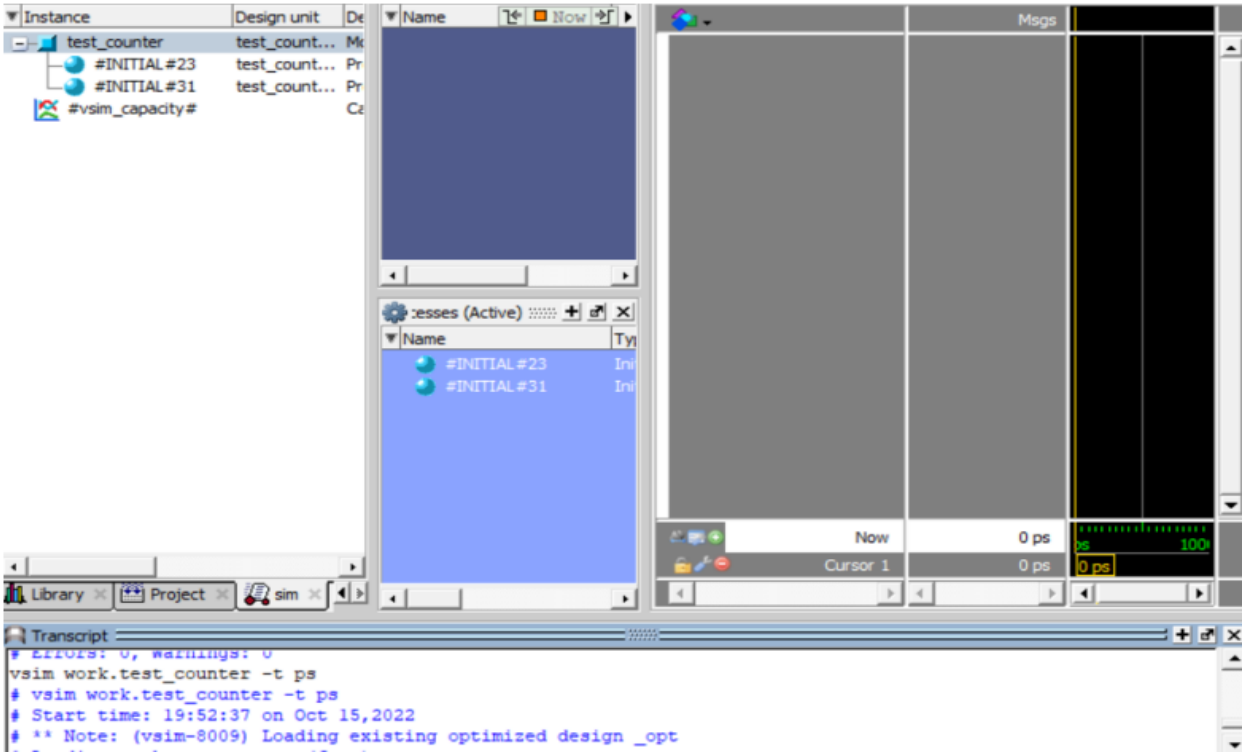

Project - C:/modeltech64_10.6d/examples/test
Name
Status
Type
Orde
Modified
tcounter.v
Verilog
0
02/24/2018 01:09:58 ...
counter.v
Verilog
1
02/24/2018 01:09:58 ...
Add Folder
Folder Name
Design Files
Folder Location
Top Level
OK
Cancel


tcounter.v Verilog 0 02/24/2018 01:09:58 ...
counter.v Verilog 1 02/24/2018 01:09:58 ...
Design Files Folder
HDL Folder


tcounter.v Verilog 0 02/24/2018 01:09:58 ...
counter.v Verilog 1 02/24/2018 01:09:58 ...
Design Files Folder
HDL Folder
Project Compiler Settings
General
Verilog & SystemVerilog
Coverage
General Settings
Do Not Compile
Compile to library: work
Place in Folder: HDL
File Properties
Multiple files selected
OK
Cancel


Design Files
Folder
HDL
Folder
tcounter.v
Verilog 0
02/24/2018 01:09:58 ...
counter.v
Verilog 1
02/24/2018 01:09:58 ...


Design Files
Folder
HDL
Folder
tcounter.v
Verilog 0
02/24/2018 01:09:58 ...
counter.v
Verilog 1
02/24/2018 01:09:58 ...
counter
Simu...


Instance
Design unit
test_counter
test_count...
#INITIAL#23
test_count...
#INITIAL#31
test_count...
#vsim_capacity#
Name
Now
Msgs
Name
#INITIAL#23
#INITIAL#31
Now
0 ps
Cursor 1
0 ps
Library
Project
sim
Transcript
vsim work.test_counter -t ps
# vsim work.test_counter -t ps
# Start time: 19:52:37 on Oct 15,2022
# ** Note: (vsim-8009) Loading existing optimized design _opt