ASSIGNMENT WEEK 8

Problem 1. For each student

1. Compare **blocking** and **nonblocking assignments.**
2. How to use **case, casex, casez** in Behavioral model.
3. Describe sequential circuit with mixed blocking and nonblocking assignments

(Section 7.1.4 in FPGA PROTOTYPING BY VERILOG EXAMPLES book)

Problem 2. For each group: Simulate your designs on ModelSim. Create code coverage report, and waveform. Implement the content in section 3.9 Design Examples, Chapter 3 RT-Level Combination Circuit, FPGA Prototyping by Verilog.

1. Example 3.9.1 Hexadecimal digit to seven-segment LED decoder **(Group 1, 2)**
2. Example 3.9.2 Sign - magnitude adder **(Group 3, 5)**
3. Example 3.9.3 Barrel shifter **(Group 8, 9)**
4. Example 3.9.4 Simplified floating - point adder **(Group 10, 11, 12)**

The group leaders need to upload the report to Teams folder, the next lesson will be presented. In addition to delving into your topic, the team members also need to understand the others.