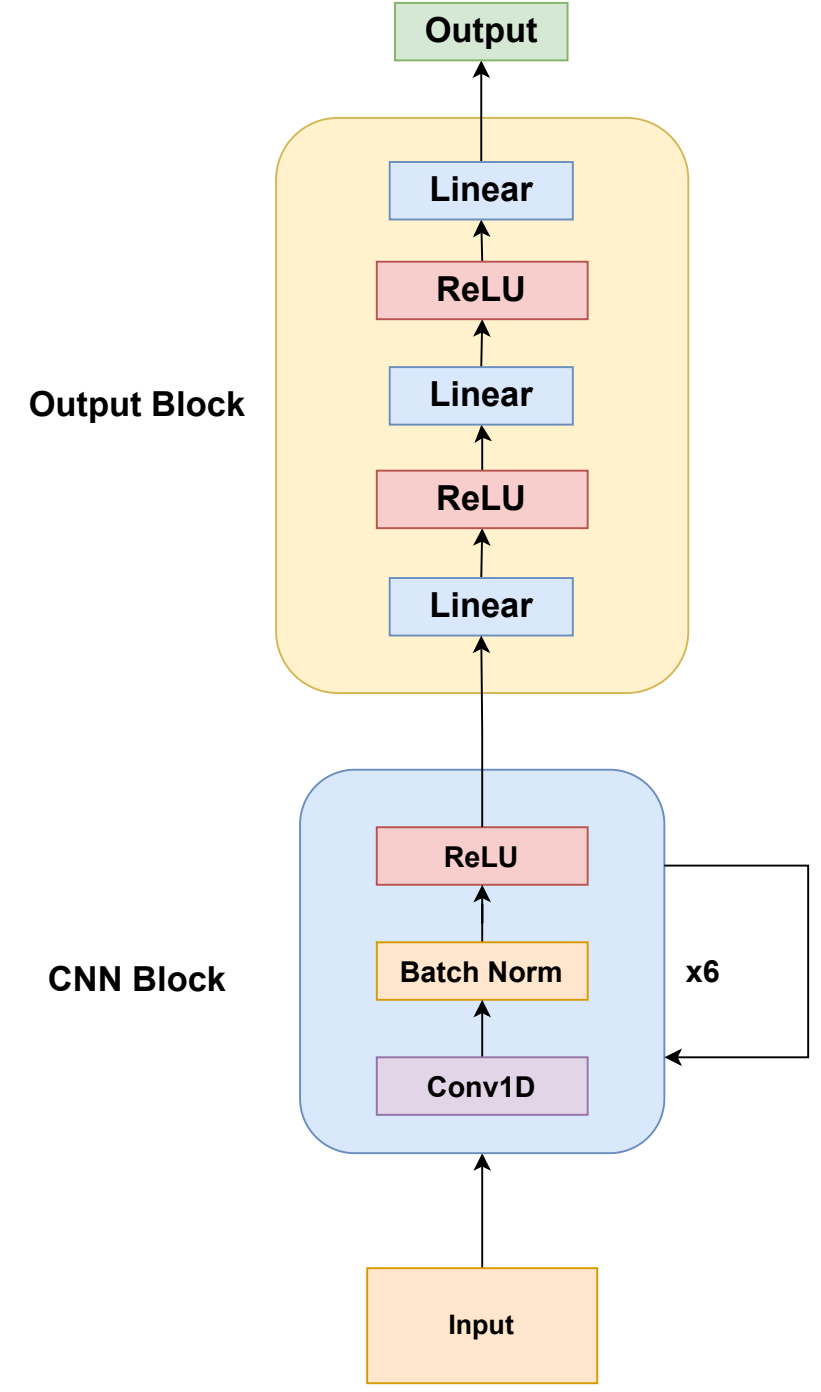
Output
Linear
ReLU
Linear
ReLU
Linear
Output Block
ReLU
Batch Norm
Conv1D
x6
CNN Block
Input