Chenyu Hu

Software Engineer & System Analysist

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Professional Summary

Software engineer with a background in internal tools and developer platforms, especially for edge and embedded systems. Experienced in release automation, container lifecycle management, CI/CD infrastructure, and cross-platform software delivery. Proven ability to lead architectural efforts and enable high-quality, reproducible builds across device and cloud systems. Passionate about improving engineering velocity and system reliability through tooling and infrastructure.

Core Competencies

- **Languages:** C#, TypeScript, C/C++, Python, Java, VB
- **Infrastructure:** CI/CD, Build Automation, Docker, DevOps, Azure DevOps, GitHub Actions, Gitlab
- **Tooling:** Container Orchestration, Shadow/Digital Twin Agents, Internal SDK Development, Release Pipelines
- **Architecture:** Clean Architecture, DDD, Microservices, Event-Driven Design
- **Messaging:** NATS JetStream, Protobuf, RPC, Pub/Sub
- **Database:** PostgreSQL, Oracle, Hadoop, SQL
- **AI & Data Science:** LangChain, RAG, Machine Learning, Tensorflow
- **Others:** Edge Computing, IoT, Semiconductor Process, Device R&D

Professional Experience

Assistant Manager — Advantech — Taoyuan, Taiwan — 02/2025 - Present

- Built **ServiceFramework**, a developer SDK that abstracts NATS RPCs, contracts, and service initialization, accelerating modular service onboarding and release.
- Designed **ShadowAgent**, a resilient edge-to-cloud sync daemon enabling digital twin state convergence with offline fallback, delta reconciliation, and controlled merge semantics.
- Engineered **Transceiver**, a cloud-edge messaging router supporting telemetry, command dispatch, and audit trail via stream-based NATS pipelines.
- Implemented **Container Management** tooling for version-controlled deployment of edge workloads, with features for rollback, configuration mutation, and runtime monitoring.
- Served as **Clean Architecture reviewer** across teams; maintained shared libraries for service registry, load balancing, distributed telemetry, and fault isolation.

Senior Software Engineer — UMC — Tainan, Taiwan — 08/2022 - 08/2024

- Led the architectural overhaul of **UEDA 5.0** using Clean Architecture principles to unify heterogenous fab data sources and protocols, solving multi-site concurrency and data integrity challenges.
- Built **DSM Bot**, a secure RAG-powered assistant integrating identity-aware document retrieval with LDAP permissions, enabling natural language interface to internal production intelligence.
- Delivered a function-calling API layer for algorithmic summaries (e.g., WIP lot tracing, timeline diagnostics), consumed by internal tools and automated chat workflows.

Device R&D Engineer — UMC — Hsinchu, Taiwan — 08/2018 - 08/2022

- Led **NWR Project**, improving device isolation to enhance yield by 5% across 28eHV and 22eHV platforms.
- Developed **Co-cut Tool**, a CAD-assisted layout optimizer reducing experimental costs by over 50%.
- Created **U2C**, a DRC language translator for CAD flows, cutting development time by 30%.
- Contributed to display IC and OLED process R&D via novel WAT key design and electrical analysis.

SELECTED PROJECTS

- **EdgeSync Platform** — Container orchestration for edge deployments with full observability, rollback, and state recovery via NATS JetStream.
- **ServiceFramework SDK** — Internal tooling for RPC abstraction, templated onboarding, test automation, and versioning.
- **UEDA 5.0** — Modular analytics refactor for production traceability using Clean Architecture and CI pipelines.
- **DSM Bot** — RAG-based chatbot with secure document access control, integrated into CI.

EDUCATION

MS in Material Science and Engineering — National Tsing Hua University — 2014 - 2018

- GPA: 3.97
- Thesis: Production of Graphite from Catalytic Liquid Cast Iron Bath

BS in Material Science and Engineering — National Tsing Hua University — 2010 - 2014

- GPA: 3.61