

# Rain Hu

Senior Software & Optimization Engineer

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## PROFESSIONAL SUMMARY

Senior software engineer with experience in scalable AIoT systems, semiconductor process optimization, and full-stack development. Proven ability to lead microservices and infrastructure projects using .NET, NATS, and Docker. Expert in Clean Architecture, DDD, and TDD practices in Agile/Scrum environments. Adept at translating domain knowledge into impactful software for both industrial computing and chip manufacturing.

## CORE COMPETENCIES

<b>Languages:</b> C#, Python, TypeScript, C++	<b>Frameworks:</b> .NET, React, ABP
<b>Architecture:</b> Microservices, DDD, Clean Arch	<b>Concurrency:</b> NATS, Docker, RCP
<b>DevOps:</b> CI/CD, TDD, GitHub Actions	<b>AI Tools:</b> TensorFlow, LangChain, RAG
<b>Databases:</b> PostgreSQL, Oracle, SQL	<b>Semiconductor:</b> Yield, Layout, DRC, TCAD

## PROFESSIONAL EXPERIENCE

<b>Assistant Manager / Senior Software Engineer</b> <i>Advantech</i>	<i>02/2025 - Present</i> <i>Taoyuan, Taiwan</i>
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- Led development of EdgeSync and Device Shadow for real-time AIoT synchronization at scale using .NET, NATS, and Docker.
- Architected scalable, testable systems with Clean Architecture and DDD; promoted TDD across Agile teams.
- Delivered SDKs and APIs supporting cross-device AI deployment; built CI/CD pipelines to streamline delivery.

<b>Senior Software Engineer</b> <i>UMC</i>	<i>08/2022 - 10/2024</i> <i>Tainan, Taiwan</i>
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- Built UEDA 5.0 platform enabling cross-fab data analysis (Taiwan, Japan, Singapore, China); boosted query speed 40%.
- Developed DSM Bot with RAG and LangChain, accelerating knowledge retrieval in semiconductor manufacturing.
- Led system refactor to support cross-database logic via Clean Architecture.

<b>Device R&amp;D Engineer</b> <i>UMC</i>	<i>08/2018 - 08/2022</i> <i>Hsinchu, Taiwan</i>
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- Developed mask layout optimization algorithm improving yield by 5% in 22nm/28nm/40nm HKMG processes.
- Built internal EDA tools (e.g., layout translators, optimization pipelines), reducing engineering workload by 30–50%.
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- Created U2C, a tool for translating between different DRC languages, reducing CAD development time by 30%

## SELECTED PROJECTS

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- **EdgeSync (Advantech)** – Infrastructure for real-time edge-cloud sync using NATS JetStream; core to AIoT Digital Twin platform.
- **DSM Bot (UMC)** – RAG-based AI assistant for fab engineers; reduced information lookup time significantly.
- **NWR (UMC)** – Algorithm-driven layout transformation tool that improved yield by 5% without layout redesign.
- **UEDA 5.0 (UMC)** Led development of an enterprise-wide integrated analysis platform including data integration across multiple databases

## EDUCATION

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**MS, Material Science & Engineering**

*National Tsing Hua University*

*2014 - 2018*

*GPA: 3.97*

**BS, Material Science & Engineering**

*National Tsing Hua University*

*2010 - 2014*

*GPA: 3.61*