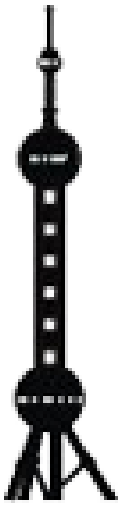

2020 ISICAS

International Symposium on Integrated Circuits and Systems

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WELCOME MESSAGE FROM THE GENERAL CHAIRS

Ladies and Gentlemen:

On behalf of the Organizing Committee, we are pleased to welcome you to the 3rd IEEE International Symposium on Integrated Circuits and Systems (ISICAS2020) to be held virtually between 27th and 28th August 2020! Without your participation, ISICAS2020 would not be a successful event.

ISICAS was established in 2018 as an IEEE Circuits and Systems Society's new initiative to provide a platform for everyone to present high-quality original works with experimental results in the areas of circuits and systems. Topics vary from analog, digital, power, biomedical, sensor interfaces, communication systems, just to name a few. The past two conferences have been a great success for the community to exchange ideas and communicate with each other.

ISICAS2020 was originally planned in Shanghai, China. Due to the outbreak of COVID-19 epidemic, the conference has been moved to a virtual platform, instead of face-to-face meetings in 2018 and 2019. However, we are thrilled about the opportunity to create an engaging virtual conference that will be rewarding for both presenters and attendees. The authors will upload video presentations so that the audience can view them before the online author-audience meeting, and one month after. To facilitate interactions between conference attendees, we have assigned a firing line to each talk – the session chair will lead a 10-minute technical discussion for each presentation. We hope the conference attendees will find this approach to be useful. In addition to one additional month for accessing the conference materials, ISICAS2020 provides free registration for students and non-authors. We encourage anyone interested in the latest development of circuits and systems to register at conference website: http://www.isicas.org.

This year we received a total of 196 initial submissions, directly to the journals, which were handled by 33 Guest Editors and Associate Editors of corresponding journals. There are two keynote presentations and 80 full paper presentations, where the technical papers will be published in four Special Issues of the IEEE Transactions on Circuits and Systems – I (TCAS-I), of the IEEE Transactions on Circuits and Systems – II (TCAS-II), of the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), and the IEEE Open Journal of Circuits and Systems (OJCAS). The program is made up of three-track presentations.

Many individuals have contributed a great deal of time and energy to making the ISICAS conference and the special issues successful. The Technical Program Chair, Prof. Guoxing Wang, and Guest Editors/Technical Program Co-Chairs, Prof. Elena Blokhina for TCAS-I, Prof Yajun Ha for TCAS-II, Timothy Constandinou for TBioCAS, and Zhihua Wang for OJCAS, together with the Technical Program Committee members, Associate Editors, reviewers, and authors have put in tremendous effort to produce a wonderful technical program. Special thanks to Editor-in-Chiefs of participating journals, Prof. Weisheng Zhao of TCAS-I, Prof. Jose M. de la Rosa of TCAS-II, Prof. Guoxing Wang of TBioCAS, and Prof. Gabrele Manganaro of OJCAS, for their support of ISICAS2020 Special Issues.

Best Regards,
Yong Lian, Amara Amara, Franco Maloberti
General Co-Chairs, ISICAS2020
On behalf of the organizing committee

COMMITTEE

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International Advisor:
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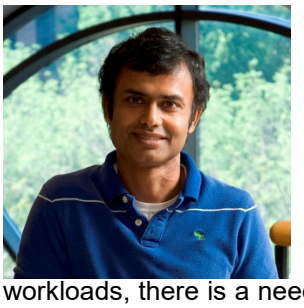
SPONSORS/SUPPORTERS

KEYNOTE SPEAKER 1



Professor Kaushik Roy, Purdue University

Resistive Crossbars as Matrix-Vector Multiplication Engine for Machine Learning Applications: Opportunities and Challenges

Abstract: Traditional computing systems based on von Neumann architectures are fundamentally bottle-necked by the transfer speeds between memory and processor. With growing computational needs of today's application space, dominated by Machine Learning (ML) workloads, there is a need to design special purpose computing systems operating on the principle of co-located memory and processing units. Such an approach, commonly known as 'In-memory computing', can potentially eliminate expensive data movement costs by computing inside the memory array itself. To that effect, crossbars based on resistive switching Non-Volatile Memory (NVM) devices has shown immense promise in serving as the building blocks of in-memory computing systems, as their high storage density can overcome scaling challenges that plague CMOS technology today. Adding to that, the ability of resistive crossbars to accelerate the main computational kernel of ML workloads by performing massively parallel, in-situ matrix vector multiplication (MVM) operations, makes them a promising candidate for building area and energy-efficient systems. However, the analog computing nature in resistive crossbars introduce approximations in MVM computations due to device and circuit level nonidealities. Further, analog systems pose high cost peripheral circuit requirements for conversions between the analog and digital domain. Thus, there is a need to understand the entire system design stack, from device characteristics to architectures, and perform effective hardware-software co-design to truly realize the potential of resistive crossbars as future computing systems. In this talk, we will present a comprehensive overview of NVM crossbars for accelerating ML workloads. We describe, in detail, the design principles of the basic building blocks, such as the device and associated circuits, that constitute the crossbars. We explore non-idealities arising from the device characteristics and circuit behavior and study their impact on MVM functionality of NVM crossbars for machine learning hardware.

Biography: Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. He also the director of the center for brain-inspired computing (C-BRIC) funded by SRC/DARPA. His research interests include neuromorphic and emerging computing models, neuro-mimetic devices, spintronics, device-circuit-algorithm co-design for nano-scale Silicon and non-Silicon technologies, and low-power electronics. Dr. Roy has published more than 700 papers in refereed journals and conferences, holds 18 patents, supervised 85 PhD dissertations, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill).

Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Humboldt Research Award in 2010, 2010 IEEE Circuits and Systems Society Technical Achievement Award (Charles Desoer Award), Distinguished Alumnus Award from Indian Institute of Technology (IIT), Kharagpur, Fulbright-Nehru Distinguished Chair, DoD Vannevar Bush Faculty Fellow (2014-2019), Semiconductor Research Corporation Aristotle award in 2015, and best paper awards at 1997 International Test Conference, IEEE 2000 International Symposium on Quality of IC Design, 2003 IEEE Latin American Test Workshop, 2003 IEEE Nano, 2004 IEEE International Conference on Computer Design, 2006 IEEE/ACM International Symposium on Low Power Electronics & Design, and 2005 IEEE Circuits and system society Outstanding Young Author Award (Chris Kim), 2006 IEEE Transactions on VLSI Systems best paper award, 2012 ACM/IEEE International Symposium on Low Power Electronics and Design best paper award, 2013 IEEE Transactions on VLSI Best paper award. Dr. Roy was a Purdue University Faculty Scholar (1998-2003). He was a Research Visionary Board Member of Motorola Labs (2002) and held the M. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay) and Global Foundries visiting Chair at National University of Singapore. He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, IEEE Transactions on VLSI Systems, and IEEE Transactions on Electron Devices. He was Guest Editor for Special Issue on Low-Power VLSI in the IEEE Design and Test (1994) and IEEE Transactions on VLSI Systems (June 2000), IEE Proceedings -- Computers and Digital Techniques (July 2002), and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (2011). Dr. Roy is a fellow of IEEE.

KEYNOTE SPEAKER 2

Professor Shaojun Wei, Tsinghua University

Software-defined AI Chip - from the perspective of Architecture Innovation

Abstract: Over the past three decades, Application Specific Integrated Circuit (ASIC) is employed to meet specific system requirements. A wide variety and small size are the advantages of ASIC. However, the diversity of applications contradicts the high investment in ASIC R&D with the process technology going to 1Xnm. To realize an ASIC corresponding to the application in a low-cost way, a hardware scheme with the same topology as the C/C++ description should be the most direct implementation and the most efficient as well. Reconfigurable chip is both software and hardware programable. The hardware architecture and functions change dynamically in real-time with the change of software algorithm while ensuring flexibility. Thus it is also called a software-defined chip. The wide adaptability of the software-defined chip makes it a strong competitor to replace ASIC, FPGA, and general-purpose processors. Artificial intelligence (AI) is ubiquitous and AI chip has become a research hotspot in recent years. AI algorithms vary in different applications and the algorithms will continue to evolve. AI services are migrating from the cloud to the edge nowadays. Performance demands and power consumption constraints require AI to deployed on an energy-efficient computing engine. Reconfigurable architecture is the ideal solution for intelligent computing since its programmability and dynamic reconfigurability of architecture can adapt algorithm evolution and diversity of applications and greatly improves energy efficiency as well. Dynamically reconfigurable technology brings the ability to bear the diversity and evolution of AI algorithms. Software-defined AI chips are expected to provide a new route for China's chip technology to get rid of imitation.

Biography: Dr. Shaojun Wei graduated from the Department of Radio & Electronics of Tsinghua University, China, in 1984 and received his Master degree in engineering. He received his Doctor degree in Applied Science from the Faculté Polytechnique de Mons (FPMs), Belgium, in 1991.

Dr. Shaojun Wei is now the professor of Tsinghua University; Chief Scientist of the State Key Science and Technology Project; Member of the National Integrated Circuit Industry Development Advisory Committee; Vice President of China Semiconductor Industry Association (CSIA) and President of Fabless Chapter CSIA. Dr. Wei was the President & CEO of Datang Telecom Technology Co., Ltd. and the CTO of Datang Telecom Industry Group between 2001-2006.

Dr. Wei has been working on VLSI design methodologies research and reconfigurable computing technology research. He has published more than 200 peer-reviewed papers and 6 monographs. He owns more than 110 patents including 14 US patents. Dr. Wei is the Fellow of Chinese Institute of Electronics (CIE) and the IEEE Fellow.

Dr. Wei had won many awards including China National Second Award for Technology Invention (2015), China National Second Award for Technology Progress (2001), SIPO & WIPO Patent Golden Award (2003, 2015), First Award for Science and Technology of Ministry of Education (2014, 2019), China, First Award for Technology Invention of CIE (2012, 2017), EETimes China IC Design Achievement Award (2018), Aspencore Outstanding Contribution Award of the Year/Global Electronic Achievement Awards (2018) and SEMI Special Contribution Award (2019) and etc. He was selected to be the recipient of the 2020 IEEE CAS Industrial Pioneer Award.

TECHNICAL PROGRAM GRID

Day 1: 27th August 2020

Time	Duration	Meeting Room A	Meeting Room B	Meeting Room C
20:00 – 20:10	10 min	Opening Speech by Conference Chair		
20:10 – 21:10	60 min	Keynote Speech 1		
21:10 – 21:15	5 min	Break out to respective rooms		
21:15 – 22:05	50 min	Session 1-A RF Clock Circuitry	Session 2-B Digital Circuit	Session 3-C Digital Systems & Accel. I
22:05 – 22:10	5 min	Break		
22:10 – 23:00	50 min	Session 4-A RF Receiver	Session 5-B Data Converter I	Session 6-C Digital Systems & Accel II
23:00 – 23:05	5 min	Break		
23:05 – 00:05	60 min	Session 7-A Temp. Sensors & References	Session 8-B Data Converter II	Session 9-C Analog Circuits

Day 2: 28th August 2020

Time	Duration	Meeting Room A	Meeting Room B	Meeting Room C
20:00-21:00	60 min	Keynote Speech 2		
21:00-21:05	5 min	Break out to respective rooms		
21:05-22:05	60 min	Session 10-A DC-DC Converters	Session 11-B Security Circuits	Session 12-C Sensors I
22:05-22:10	5 min	Break		
22:10-23:00	50 min	Session 13-A Power Mgt. I	Session 14-B RF Transmitters	Session 15-C Digital System & Accel. III
23:00-23:05	5 min	Break		
23:06-00:05	60 min	Session 16-A Power Mgt. II		Session 18-C Sensors II

TECHNCIAL PROGRAM - Day 1: 27th August 2020

Session 1-A: RF Clock Circuitry
Room: Zoom Room A

Paper 1
Title: A Picosecond-Resolution Digitally-Controlled Timing Generator with One-Clock-Latency at Arbitrary Instantaneous Input
Authors: Jaehan Park, Cheolmin Ahn, Jaehyeong Hong, and Jae-Yoon Sim
Institutes: Department of Creative IT Engineering, Pohang University of Science and Technology, Pohang, South Korea; Department of Electronic and Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea
Abstract: This paper presents an all-digital burst-mode digital-to-time converter (DTC) which generates a valid output in one-clock latency. The implemented DTC in 28nm LP CMOS shows the maximum peak INL error of 5.34ps in a seamless conversion range of from 16ps to 2850ps. The proposed scheme has no limit on the theoretical conversion range and can be limitlessly expanded simply by allocating more bits to a counter, while keeping picosecond resolutions.

Paper 2
Title: A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications
Authors: Davide De Caro, Gennaro Di Meo, Ettore Napoli, Nicola Petra and Antonio G.M. Strollo
Institutes: Dept. of Electrical Engineering and Information Technology, University of Napoli Federico II, Italy
Abstract: The increase of clock frequency in digital circuits exacerbates the electromagnetic interference (EMI) between devices. Spread-spectrum techniques reduce the electromagnetic noise lowering harmonic peaks of the clock signal by means of frequency modulation. In System-on-Chips (SoCs) another requirement in many applications is the coexistence of both modulated and un-modulated clock domains. In these cases, suitable synchronization systems are used to allow data to cross the boundary between spread and un-spread clock domains. In this paper we present a spread-spectrum clock generator (SSCG) able to provide both spreaded and un-spreaded clocks. The spreaded clock has a specially designed modulation profile, allowing at the same time a seamless synchronization-free interface between spreaded and un-spreaded clock domains and a large EMI reduction. The paper presents the derivation of the new highly discontinuous modulation profile (that allows to achieve an EMI reduction up to 15.8dB) and implementation details of an all-digital SSCG able to provide the developed modulation waveform. A test chip has been fabricated in UMC 65nm CMOS technology, using a novel dual-output digitally controlled delay line. The circuit can generate both spread and un-spread clocks (double output mode) or the spread clock alone (single output mode). Area occupation is 0.102mm2, whereas power consumption is 48.5mW in double output mode and 34mW in single output mode.

Paper 3

Title: Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools

Authors: Ricardo Martins, Nuno Lourenço, Nuno Horta, Shenke Zhong, Jun Yin, Pui-In Mak, and Rui P. Martins

Institutes: Instituto de Telecomunicações, Instituto Superior Técnico – Universidade de Lisboa, Lisboa, Portugal; State-Key Laboratory of Analog and Mixed-Signal VLSI / IME and ECE / FST, University of Macau, Macao, China

Abstract: Optimal voltage-controlled oscillator (VCO) design for ultralow-power (ULP) radios has to fulfill simultaneously multiple requirements such as frequency tuning range, phase noise, power consumption, and frequency pushing. The manual design struggles to approach the full potential that a given topology can achieve. In this work, we prove the role of electronic design automation (EDA) tools by fully supporting the complex design of a ULP complementary Class-B/C hybrid-mode VCO. In the 1st step of the EDA-assisted flow, we perform a worst-case corner of worst-case tuning sizing optimization over a 108- dimensional performance space, offering sizing solutions with power consumption down to 145 μW at the worst-case. In the 2nd step, we introduce an automatic layout generation tool to offer valuable insights into the post-layout design space and devise a ready-for-tape-out fine optimization strategy. The hybrid-mode VCO prototyped in 65-nm CMOS occupies a die area of 0.165 mm2 and dissipates 297 μW from a 0.8 V supply at 5.1 GHz. The phase noise at 1 MHz offset is -110.1 dBc/Hz, resulting in a competitive Figure-of-Merit (FoM) of 189.4 dBc/Hz well-suited for ULP applications.

Paper 4

Title: A Calibration-free Ring-Oscillator PLL with Gain Tracking Achieving 9% Jitter Variation over PVT

Authors: Xiaofeng Yang, Chi-Hang Chan, Yan Zhu and R. P. Martins

Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI / Institute of Microelectronics; Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao, China

Abstract: This paper presents a calibration-free and lowjitter phase-locked loop (PLL) with small performance degradation over PVT. We introduce an open-loop discrete-time phase noise cancellation (OPDTPNC) technique to achieve a wideband filtering and circuit inner-gain-tracking for PVT stabilization. The OPDTPNC is an effective phase realignment that enables a filtering bandwidth ~1/4 of the reference clock frequency. Besides, with the common structures and PVT tracking bias for sampler and corrector of the OPDTPNC, the prototype PLL maintains its low jitter under a wide range of PVT variations. Eventually, by cascading a Type-II PLL with the OPDTPNC, the proposed hybrid PLL attains the benefits of both Type-II PLL and injection-locked clock multiplier (ILCM). Fabricated in 28-nm CMOS with an active area of 0.023mm2 it consumes 4.1 mV from a 1 V supply with a reference spur of -63 dBc. The measured rms jitter of the 2.4 GHz PLL is 248 fs and 686 fs with and without OPDTPNC, respectively. When the temperature, supply and loop gain vary from 0 to 100˚C, ±5%, and 6dB, respectively, the jitter performance only degrades less than 9%.

Paper 5

Title: A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-only Switched-Capacitor Arrays with a 187.6-dBc/Hz FOM

Authors: Yunbo Huang, Yong Chen, Hao Guo, Pui-In Mak and Rui P. Martins

Institutes: State-Key Laboratory of Analog and Mixed-Signal VLSI / IME, and ECE / Faculty of Science and Technology, University of Macau, Macao, China; Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisboa, Portugal

Abstract: A millimeter-wave current-reuse voltage-controlled oscillator (VCO) features a single-turn multi-tap inductor and two separate differential-only switched-capacitor arrays to improve the power efficiency and phase noise (PN). Specifically, a singlebranch complementary VCO topology, in conjunction with a multi-resonant Resistor-Inductor-Capacitor-Mutual inductance (RLCM) tank, allows sharing the bias current and reshaping the impulse-sensitivity-function. The latter is based on an areaefficient RLCM tank to concurrently generate two high qualityfactor differential-mode resonances at the fundamental and 2ndharmonic oscillation frequencies. Fabricated in 65-nm CMOS technology, our VCO at 27.7 GHz shows a PN of -109.91-dBc/Hz at 1-MHz offset, while consuming just 3.3 mW at a 1.1-V supply. It corresponds to a Figure-of-Merit (FOM) of 187.6 dBc/Hz. The frequency tuning range is 15.3% (25.2 to 29.4 GHz) and the core area is 0.116 mm2.

Session 2-B: Digital Circuit

Room: Zoom Room B

Paper 1

Title: A Robust Hardened Latch Featuring Tolerance to Double-Node-Upset in 28nm CMOS for Spaceborne Application

Authors: Yan Li, Xu Cheng, Chiyu Tan, Jun Han, Yuanfu Zhao, Liang Wang, Tongde Li, Mehdi B. Tahoori and Xiaoyang Zeng

Institutes: State Key Lab. of ASIC and System, Fudan University, Shanghai, China; Chair of Dependable Nano Computing, Karlsruhe Institute of Technology, Karlsruhe, Germany; Beijing Microelectronics Technology Institute, Beijing, China

Abstract: Soft errors induced by high energy particles have been a severe concern in integrated circuits. Especially in advanced nanoscale technology nodes, the phenomenon of multi-node-upset caused by charge sharing is becoming a crucial issue. However, this problem remains a challenge as there are only few mitigation methods. This study demonstrates a cost-efficient latch named CROUT featuring double-node-upset tolerance. Integrating coupled Schmitt-triggers and four always-on high-threshold transistors, CROUT is highly reliable in the presence of double-node-upset. To further validate this, a test chip was fabricated in the 28nm CMOS process and tested in a heavy-ion radiation environment. The experimental results indicated that the radiation tolerance is about 2x higher than the standard latches. Moreover, compared to other state-of-the-art multi-node-upset tolerant latches, its logarithmic power-delay-product (PDP) is reduced by ~6x. The results are promising and offer new high reliable and cost-effective latch dedicated to the aerospace field, which further can be made into a standard cell for application in large-scale circuits.

Paper 2

Title: Silicon Evaluation of Multimode Dual Mode Logic for PVT-Aware Datapaths

Authors: Inbal Stanger, Netenel Shavit, Ramiro Taco, Marco Lanuzza and Alexander Fish
Institutes: Emerging Nanoscaled Integrated Circuits and Systems Labs, Faculty of Engineering, Bar-Ilan University, Ramat Gan, Israel; Universidad San Francisco de Quito, Quito, Ecuador; Universita degli Studi della Calabria, DIMES, Cosenza, Italy

Abstract: This brief presents the unique capability of the multimode Dual Mode Logic (DML) design technique to define run-time adaptive datapaths to overcome process and environmental (i.e. temperature and voltage) variations. A proof-of-concept benchmark circuit was designed and fabricated in 65 nm technology. Measurements performed on 10 test chips, while considering supply voltage spanning 0.6V to 1.2V and temperature variations ranging from -40 °C to 125 °C confirmed the effectiveness of this approach to compensate for severe process, voltage and temperature (PVT) variations.

Paper 3

Title: A 0.46V-1.1V Transition-Detector with In-Situ Timing-Error Detection and Correction Based on Pulsed-Latch Design in AES Accelerator

Authors: Xinchao Shang, Weiwei Shan, Jiaming Xu, Minyi Lu, Yiming Xiang, Longxing Shi and Jun Yang
Institutes: Southeast University, Nanjing, Jiangsu, P. R. China; Spreadtrum Communications, Tianjin, P. R. China

Abstract: To overcome the minimum-delay constraint of latch based error detection and correction (EDAC) techniques, we propose a technique of using pulse latch and transition detector (TD). This method is also advantageous in no need of error recovery by time-borrowing characteristics of the latch. To detect timing violations and minimize the area overhead, we design a quick-response 15-transistor transition detector cover a wide-voltage range from near-threshold voltage (NTV) to SuperVth. Test chips are fabricated in 28nm CMOS process. Silicon measurements demonstrate that the whole design has achieved up to 64.3% energy saving with 180mV additional voltage scaling, compared to the conventional worst-case design at the expense of 4.3% area overhead.

Paper 4

Title: High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder

Authors: Amit Kumar Panda, Rakesh Palisetty and Kailash Chandra Ray
Institutes: Dept. of EEE, BITS Pilani Hyderabad, Telangana, India; Department of ECE, KL University, Vaddeswaram, AP, India; Department of Electrical Engineering, IIT Patna, Bihta, Patna, Bihar, India

Abstract: Three-operand binary adder is the basic functional unit to perform the modular arithmetic in various cryptography and pseudorandom bit generator (PRBG) algorithms. Carry-save adder (CS3A) is the widely used technique to perform the threeoperand addition. However, the ripple carry stage in the CS3A leads to high propagation delay of . Moreover, a parallel prefix two-operand adder such as Han-Carlson (HCA) can also be used for three-operand addition that significantly reduces the critical path delay at the cost of additional hardware. Hence, a new high-speed and area-efficient adder architecture is proposed using pre-compute bitwise addition followed by carry-prefix computation logic to perform the three-operand binary addition that consumes substantially less area, low power and drastically reduces the adder delay to . The proposed architecture is implemented on FPGA device for functional validation, and also synthesized with the commercially available 32nm CMOS technology library. The post-synthesis results of the proposed adder reported 3.12, 5.31 and 9.28 times faster than the CS3A for 32-, 64- and 128- bit architecture respectively. Moreover, it has lesser area, lower power dissipation and smaller delay than the HC3A adder. Also, the proposed adder achieves the lowest ADP and PDP than the existing three-operand adder techniques.

Paper 5

Title: Efficient Implementation of a Threshold Modified Min-Sum Algorithm for LDPC Decoders

Authors: Yanfang Liu, Wei Tang, and David G. M. Mitchell
Institutes: Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM, USA

Abstract: In this brief, we present a hardware efficient implementation of a threshold modified min-sum algorithm (MSA) to improve the performance of a low density parity-check (LDPC) decoder. The proposed architecture introduces a novel lookup table based threshold attenuation technique, called threshold attenuated MSA (TAMSA). The proposed TAMSA implementation is shown to improve bit error rate (BER) performance compared to the conventional AMSA and MSA with no extra hardware cost. Furthermore, a layered version of the TAMSA implementation is investigated to reduce hardware cost. Utilizing circuit optimization techniques, including a parallel computing structure, the proposed layered TAMSA field programmable gate array (FPGA) implementation results show that the modified architecture requires no extra circuit power or circuit area compared to conventional AMSA, and 0.07 extra leaf cells compared to conventional MSA.

Session 3-C: Digital System & Accelerator I

Room: Zoom Room C

Paper 1

Title: An Efficient Massive MIMO Detector Based on Second-order Richardson Iteration: From Algorithm to Flexible Architecture

Authors: Jiaming Tu, Mengdan Lou, Jianfei Jiang, Dewu Shu, and Guanghui He
Institutes: School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China

Abstract: Aiming at reducing the complexity of minimum mean square error (MMSE) detection in massive multiple-input multiple-output (MIMO) systems, this paper proposes a detection algorithm with high convergence rate and an efficient hardware architecture based on second-order Richardson iteration (SORI). In the proposed algorithm, a pre-iteration-based initialization method is presented to accelerate the convergence without extra complexity. In addition, the approximation of relaxation factor and the log-likelihood ratio (LLR) is introduced to further reduce computing load. Theoretical analysis demonstrates the advantages of the proposed algorithm in fast convergence and low complexity, and simulation results show that the proposed algorithm can efficiently approach MMSE performance. Based on this algorithm, a flexible hardware architecture is designed with deeply pipelined to support $128\times U$ ($8 \leq U \leq 32$) massive MIMO detection with the configurable number of iterations, and a folded dual-mode systolic array (DMSA) is fully utilized to achieve the flexibility with low hardware consumption. Implemented on Xilinx Virtex-7 FPGA and SMIC 40nm CMOS technology, the proposed detector is competitive in terms of energy and area efficiency compared to state-of-the-art iterative detectors, and it can adapt to the varied channel condition and the number of users in massive MIMO systems.

Paper 2

Title: A Hybrid 3D Interconnect with 2x Bandwidth Density Employing Orthogonal Simultaneous Bidirectional Signaling for 3D NoC

Authors: Srinivasan Gopal, Sourav Das, Partha Pratim Pande, and Deukhyoun Heo
Institutes: School of Electrical Engineering and Computer Science, Washington State University, WA USA; Intel Corporation, Hillsboro, OR, USA; Intel Corporation, Santa Clara, CA, USA

Abstract: For the first time, this work presents a wirelesswireline hybrid 3D interconnect that employs orthogonal simultaneous bidirectional signaling for 3D Network-on-chip to achieve 2x bandwidth density. We combine wireless near-field inductive coupling channel (NFIC) encompassing wireline through-silicon vias (TSV) to leverage orthogonal simultaneous bidirectional (SBD) signaling. This technique provides an efficient way of doubling interconnect bandwidth in the same area by means of passive wireless and wireline interconnects. The proposed hybrid 3D interconnect shows at least -70dB of NFICTSV isolation in the band of interest. We also present a comprehensive link analysis to derive the energy-area trade-off of an NFIC link and its fundamental performance limits. Further, we demonstrate on how equalization has the potential to decouple the fundamental energy-area tradeoff. The prototype transceiver measures a simultaneous bidirectional data and clock communication at an effective data rate of 6.6 Gb/s consuming 263 fJ/bit in 65 nm CMOS bulk process. The developed hybrid 3D interconnect architecture exhibits a 2× improved link performance over state-of-the-art 3D capacitive link. A hybrid 3D Network-on-chip (3D NoC) implementation is demonstrated using the proposed hybrid interconnect technology and shows a 50% lower area and cost for the same energy-delay-product (EDP) over the conventional TSV based links.

Paper 3

Title: Machine Learning-based Approach for Hardware Faults Prediction

Authors: Kasem Khalil, Omar Eldash, Ashok Kumar, and Magdy Bayoumi
Institutes: Center of Advanced Computer Studies, University of Louisiana at Lafayette, USA

Abstract: Hardware failures are undesired but a common problem in circuits. Such failures are inherently due to the aging of circuitry or variation in circumstances. In critical systems, customers demand the system never to fail. Several self-healing and fault tolerance techniques have been proposed in the literature for recovering a circuitry from a fault. Such techniques come to the rescue when a fault has already occurred but they are typically uninformed about the possibility of an impending failure (i.e., fault prediction), which can be used as a pre-stage to fault tolerance and self-healing. This paper presents an approach to early fault prediction of circuits. The proposed method uses Fast Fourier Transform (FFT) to get the fault frequency signature, Principal Component Analysis (PCA) to get the most important data with reduced dimension, and Convolutional Neural Network (CNN) to learn and classify the fault. The proposed method is validated for working in different circuits by testing it using two circuits: comparator and amplifier. The comparator and amplifier are implemented using 45 nm technology on HSPICE to extract the failures dataset in terms of voltage, current, temperature, noise, and delay. This extracted data is used for training the proposed approach using Tensorflow. To the best of our knowledge, this is the first work of fault prediction at the transistor level for hardware system. The proposed approach considers aging, short-circuit, and open-circuit faults, and it provides a fault prediction accuracy of 98.93% and 98.91% for comparator and amplifier circuits, respectively. The proposed method is tested for two different circuits for its validation, and it consumes 1.08 W for Altera Arria 10 GX FPGA device.

Paper 4

Title: A 1.15 TOPS/W Energy-efficient Capsule Network Accelerator for Real-time 3D Point Cloud Segmentation in Mobile Environment

Authors: Gwangtae Park, Dongseok Im, Donghyeon Han, and Hoi-Jun Yoo
Institutes: School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, South Korea

Abstract: An energy-efficient capsule network accelerator is proposed for real-time 3D point cloud segmentation in mobile devices. The proposed accelerator adopts the pipelined heterogeneous core architecture to achieve 1.55× throughput enhancement. Furthermore, the proposed dynamic route skipping controller predicts unimportant operations and skips them to reduce the external memory access by 39.1%. At last, the new squash activation function unit exploits the look-up table (LUT) based computing with L2-norm approximation to minimize the power and area overhead. The proposed architecture is implemented with the FPGA, Altera Cyclone V 5CEBA9F31C7 and we test capsule network-based 3D point cloud segmentation application. It consumes 2.15 W power and shows 0.05 TOPS/W energy-efficiency. Also, the architecture is simulated with the 65nm CMOS technology, showing 94.3mW power consumption and 1.15 TOPS/W energy-efficiency.

Paper 5

Title: Efficient FPGA Implementation of K-Nearest-Neighbor Search Algorithm for 3D LIDAR Localization and Mapping in Smart Vehicles

Authors: Hao Sun, Xinzhe Liu, Qi Deng, Weixiong Jiang, Shaobo Luo, and Yajun Ha
Institutes: ShanghaiTech University

Abstract: K-Nearest-Neighbor search (KNN) has been extensively used in the localization and mapping based on 3D laser point clouds in smart vehicles. Considering the real-time requirement of localization and stringent battery constraint in smart vehicles, it is a great challenge to develop highly energy-efficient KNN implementations. Unfortunately, previous KNN implementations either cannot build search data structure efficiently or cannot search efficiently in massive and unevenly distributed point clouds. To solve the issue, we propose a new framework to optimize the implementation of KNN on FPGAs. First, we propose a novel data structure with a spatial subdivision method, which can be built efficiently even for massive point clouds. Second, based on our data structure, we propose a KNN search algorithm which is able to search in unevenly distributed point clouds efficiently. We have implemented the new framework on both FPGA and GPU. Energy efficiency results show that our proposed method is on average 2.1 times and 6.2 times higher than the state-of-the-art implementations of KNN on FPGA and GPU platform, respectively.

Session 4-A: RF Receiver
Room: Zoom Room A

Paper 1
Title: Fully Integrated Digital GaN-based LSK Demodulator for High-Temperature Applications
Authors: Ahmad Hassan, Mostafa Amer, Yvon Savaria and Mohamad Sawan
Institutes: Department of Electrical Engineering, Polytechnique Montréal, QC, Canada; School of Engineering, Westlake University, Hangzhou; the Institute of Advanced Study, Westlake Institute for Advanced Study, Hangzhou, China
Abstract: We present the first Gallium Nitride (GaN)-based demodulator system dedicated to demodulating Load-Shift Keying (LSK) modulated signals that can operate at high temperature (HT). GaN500 technology is adopted to implement the proposed demodulator. Stable DC output characteristics of epitaxial AlGaN/GaN Heterojunction Field Effect Transistors (HFETs) operating at up to 500ºC enable designing HT ICs. Conventional digital gates such as inverters, NAND2, NAND3, delay elements and a D Flip-Flop are employed to implement the proposed demodulator. The demodulation system is fabricated on a 2.67 mm2 silicon carbide (SiC) substrate and experimentally validated at 160oC, whereas the building blocks (inverters and NANDs) show a stable operation at HT up to 400oC. A minimum of 1 V amplitude difference can be detected between the high voltage level (HVL = ± 5 V) and low voltage level (LVL = ± 4 V) of an applied LSK modulated signal to recover transmitted digital data. Two high-voltage supply levels (±14 V) are required to operate the system. Its total power consumption is 3.4 W.

Paper 2
Title: A Package Aware QLMVF Receiver Front End
Authors: Sesha Sairam Regulagadda, Nagaveni S and Ashudeb Dutta
Institutes: Department of Electrical Engineering, Indian Institute of Technology Hyderabad, India
Abstract: This paper presents a 2.4 GHz receiver front end in the form of architecture of quadrature LNA-Mixer-VCO-filter (QLMVF) cell in 180 nm CMOS with split-transconductance amplifiers (TCAs). Instead of a single stack-current-reusing QLMV scheme, the proposed design employs two separate current reuse stages with a passive mixer to provide better flicker noise and linearity performance. A varactor is integrated at the input of low noise amplifier (LNA) To tolerate package parasitic effect. The quad-flat-no-leads (QFN) packaged receiver provides a measured maximum conversion gain of 40 dB, a noise figure (NF) of 10 dB, and a third-order input intercept point (IIP3) of -5 dBm with a spurious-free dynamic range (SFDR) of 60 dB. The front end consuming 2.7 mW of power from a 1.8 V supply and occupies an area of 1.5 mm2.

Paper 3

Title: High Sensitivity and Dynamic-Range 25 Gbaud/s Silicon Receiver Chipset with Current-Controlled DC Adjustment Path and Cube-Shape Ge-on-Si PD

Authors: Xiaojun Bi, Member, IEEE, Jian Li, Zhen Gu, Bo Tang, Chaodi Sheng, Yan Yang, and Qinfen Xu

Institutes: School of Optical and Electronic Information and Wuhan National Laboratory for Optoelectronics, Huazhong University of Science & Technology, Wuhan, People's Republic of China; Shenzhen Institute of Huazhong University of Science & Technology, Shenzhen, People's Republic of China; Integrated Circuit Advanced Process R&D Center, Institute of Microelectronics of Chinese Academy of Sciences, Beijing, People's Republic of China.

Abstract: This paper presents a high sensitivity and dynamic range 25 Gbaud optical receiver including the CMOS transimpedance amplifier (TIA) and Ge-on-Si photodetector. In the TIA with a DC bypassing path, instead of deploying a voltagecontrolled path with a fixed feedback strength, a currentcontrolled path with gm-adjusting ability is proposed to minimize the noise amplified by the feedback loop and achieve high sensitivity. In addition, in the optical part, a Ge-on-Si photodetector with cube-shape Ge is proposed to boost the responsivity, which therefore overcomes the noise contribution from the TIA and enhance the overall sensitivity of the cascaded optical receiver. The CMOS transimpedance amplifier includes a 3-stage transimpedance pre-amplifier, a 4-stage post amplifier, a CML buffer stage and a DC offset cancellation block. Measurement results show a transimpedance of 66-71 dBΩ, a SDD21 bandwidth of 18.5 GHz, an input-referred noise current density of 11.1 pA/√Hz, a BER of 1×10-12@26 μA and a power consumption of 105 mW. The FOM is 5.2 which is the lowest, to the best of the authors' knowledge. The photodetector achieves a responsivity of 0.57 A/W at 1550 nm and a bandwidth of 40 GHz. The optical receiver achieves an optical sensitivity of -11.7 dBm. Compared with the prior arts, the proposed receiver demonstrates distinct sensitivity and FOM enhancement.

Paper 4

Title: A 56-to-66 GHz CMOS Low-Power Phased-Array Receiver Front-End with a Hybrid Phase Shifting Scheme

Authors: Majid Yaghoobi, Milad Haghi Kashani, Mohammad Yavari, and Shahriar Mirabbasi

Institutes: Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran; Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada

Abstract: This paper presents a millimeter-wave phasedarray receiver front-end with compact size and low-power consumption. A combination of local oscillator (LO) and radio frequency (RF) phase-shifting schemes is used to reduce the power consumption and RF path loss. Moreover, in the implementation of active circuits, a bulk isolation technique is used to achieve a higher power gain with a minimum number of stages. This technique is also utilized in the RF path phase shifter switches to mitigate the loss. To validate the proposed architecture, a single-element 56-to-66 GHz phased-array receiver front-end is fabricated in a 65-nm bulk CMOS process. Based on the measurement results, the receiver achieves a power gain of ~14.85 dB and a minimum noise figure (NF) of 5.7 dB. The measured average RMS phase and gain errors are ~3.5° and ~0.45 dB, respectively. The input 1-dB compression point (P-1dB) of the receiver chain is about –19 dBm. The complete receiver, including active balun and required buffers (excluding the LO), consumes ~50 mW from a 1-V power supply and excluding the pads occupies a silicon area of 0.93 mm2.

Paper 5

Title: An Efficient Sinusoid-like Pseudo Random Sequence Modulator/Demodulator System with Reduced Adjacent Channel Leakage and High Rejection to Random and Systematic Interference

Authors: Jian Shao, Aydin Ilker Karsilayan, Christopher T. Rodenbeck and Jose Silva-Martinez
Institutes: Texas A&M University, College Station, TX, USA; Sandia National Laboratories, Albuquerque, NM, USA; U.S. Naval Research Laboratory, Washington, DC, USA

Abstract: Emerging wireless communication services require the efficient use of available spectrum and improved co-existence of different standards placed in adjacent frequency bands. Coexistence with leakage from primary users in adjacent channels, which falls in the band of interest, is a primary concern for existing and emerging technologies. In this paper, a mixed signal IC technique based on direct sequence spread spectrum is proposed to improve co-existence of radar systems with commercial wireless communication systems. A sinusoid-like pseudo-random sequence is introduced to reduce leakage from radar systems into adjacent channels. The proposed approach reduces the radar signal leakage on adjacent channels by about 22dB when compared with the conventional binary pseudo-random sequence. The proposed technique randomizes narrow and wideband systematic in-band interference, after which interference power can be effectively attenuated through averaging techniques. Experimental results from a 40nm CMOS technology modulator/demodulator prototype demonstrates the feasibility of the proposed architecture. The modulator and demodulator system requires a silicon area of 0.0459mm2 and consumes 4.33mW in total.

Session 5-B: Data Converter I
Room: Zoom Room B

Paper 1

Title: A 2 nW 0.25 V 140 dB-FOM inverter-based first order ΔΣ modulator

Authors: Alessandro Catania, Lorenzo Benvenuti, Andrea Ria, Giuseppe Manfredini, Massimo Piotto, and Paolo Bruschi
Institutes: Dipartimento di Ingegneria dell'Informazione, University of Pisa, Pisa, Italy; Sensichips s.r.l., Aprilia (LT) - Italy; IEIIT-PISA, CNR, Pisa, Italy

Abstract: In this work, we introduce an ultra-low voltage, ultra-low power, inverter-based, discrete-time, 1st order ΔΣ modulator. It exploits an original switched-capacitor integrator to achieve interesting performances with supply voltages as low as 0.25 V. It also employs a clock-boosting technique to improve pass gate operation. A prototype has been designed and produced using a 0.18 μm CMOS process by UMC. The modulator reaches an SNDR of 37.2 dB at a voltage of 0.25 V, with a power consumption of only 2.1 nW, corresponding to a FOM of 140.3 dB. The DC characteristics show an offset of 4.3 mV, a gain error of 2.5% (standard deviations), with an INL of 0.6%.

Paper 2

Title: A 10-MHz BW 77.3-dB SNDR 640-MS/s GRO-based CT MASH ΔΣ Modulator

Authors: Mohammad Honarparvar, Jose M. de la Rosa, and Mohamad Sawan
Institutes: Polystim Neurotech Lab, Department of Electrical Engineering, Polytechnique Montreal, Montreal, QC, Canada; CenBRAIN, School of Engineering, Westlake University, and Institute of Advanced Technology, Hangzhou, China; Instituto de Microelectronica de Sevilla, IMSE-CNM, CSIC/Univ. de Sevilla, Sevilla, Spain.

Abstract: We present in this paper a novel multi-stage noiseshaping (MASH) 3-1 continuous-time (CT) delta-sigma modulator (ΔΣM) with gated ring oscillator based quantizers (GROQs) in both stages of the cascade. The use of GROQs increases the linearity performance with respect to the conventional voltage controlled oscillator based quantizers (VCOQs) and allows a more robust extraction of the front-end stage quantization error in the time domain, thus making the proposed architecture more suitable to implement high-order expandable scaling-friendly MASH ΔΣMs, in which the back-end stages are implemented by mostly-digital GRO-based time-to-digital converters (TDCs). The circuit has been fabricated in a 65-nm CMOS technology with 1-V supply voltage, and it operates at 640-MHz sampling frequency to digitize 10-MHz signals. To the best of the authors' knowledge, this is the first reported experimental validation of a GRO-based CT MASH ΔΣM, featuring a 79.8-dB signal to noise ratio (SNR) at −2.2-dBFS, a 77.3-dB signal to (noise + distortion) ratio (SNDR) at −4-dBFS and a dynamic range (DR) of 81.7 dB, with a power consumption of 12-mW. These metrics demonstrate state-of-the-art performance with a DR-based Schreier FOM of 170.9 dB.

Paper 3

Title: 1.5-to-3.0 GHz Tunable RF ΣΔ ADC with a Fixed Set of Coefficients and a Programmable Loop Delay

Authors: Alhassan Sayed, Tamer Badran, Marie-Minerve Louerat and Hassan Aboushady
Institutes: Sorbonne Universite, CNRS, LIP6 Laboratory, Paris, France; Faculty of Engineering, Minia University, Egypt; Faculty of Engineering, AASTMT, Alexandria, Egypt

Abstract: In this paper, we present a tunable bandpass RF Sigma-Delta modulator with a fixed set of coefficients. The sampling frequency,fs, is tuned with the center frequency,f0,in order to maintain a fixed normalized center frequency,f0/fs. Any variation in the loop delay is compensated to maintain a fixed normalized loop-delay td/Ts. The bandpass Sigma-Delta,reported in this paper, is based on an LC resonator with tunable center frequency from 1.5 to 3.0 GHz and a corresponding sampling frequency from 6.0 to 12.0 GHz. For an oversampling ratio of 64, the ADC achieves the same SNDR of 37 dB and the same Dynamic Range of 45 dB over the complete tuning range. This performance is achieved for a band with of 47 MHz at 1.5 GHz and a Bandwidth of 93 MHz at 3 GHz. The ADC,fabricated in a 65 nm CMOS process, consumes only 13 mW from a 1.2 V supply. In order to compare this circuit with the state of the art, we use not only the conventional ADC Figure of Merit but we also use a Figure of Merit dedicated to RF circuits.In this case, the measured chip center frequency, noise figure and non-linearity are also taken into account in the comparison.

Paper 4

Title: An Inverter-Based Continuous Time Sigma Delta ADC with Latency-Free DAC Calibration

Authors: Yuekang Guo, Jing Jin, Xiaoming Liu, and Jianjun Zhou

Institutes: Center for Analog/RF IC, School of Microeletronics, Shanghai Jiao Tong University, Shanghai, China

Abstract: This paper presents a wide bandwidth inverter-based continuous time sigma delta (CTSD) analog-to-digital converter (ADC) with a latency-free calibration to suppress the nonlinearity originating from the feedback digital-to-analog converter (DAC). The modulator in the ADC uses a fourth-order architecture with 4-bit quantization. To compensate the excess loop delay (ELD), the proportional-integrating element (PI-element) is employed in the loop filter where the problem of no real solution in conventional PI-element compensation method is solved. In addition, the twostage inverter-based amplifiers are used in the loop filter to improve power efficiency. To suppress nonlinearity of the 4-bit DAC, a background calibration method based on modified quantizer is proposed which would not introduce additional latency thus ensuring stability of the modulator. The CTSD ADC achieves 64.6 dB SNDR and 71.2 dB SFDR over a 75 MHz signal bandwidth before calibration, and the SNDR and the SFDR can be improved to 67.3 dB and 82.3 dB respectively after calibration. The ADC consumes 38 mW from supply voltages of 1.1/1.8 V with an active area of 0.675 mm2 in 40 nm CMOS.

Paper 5

Title: Multi-Channel Analog-to-Digital Conversion Techniques Using a Continuous-Time Delta-Sigma Modulator Without Reset

Authors: R. S. Ashwin Kumar and Nagendra Krishnapura

Institutes: Department of Electrical Engineering, Indian Institute of Technology Madras, India

Abstract: Two methods are presented for implementing a multi-channel ADC using a continuous-time delta-sigma modulator (CTDSM) without resetting its states. The first is adapted from a method used with a discrete-time delta-sigma modulator (DTDSM). It uses a sample-and-hold (S/H) at the Nyquist rate before the modulator and an adaptive equalizer at the Nyquist rate after the modulator for flattening the equivalent frequency response and eliminate memory. With the newly proposed π-shifted filter, instead of flattening the equivalent discrete-time frequency response, it is merely ensured that the equivalent frequency response is symmetric about w = π/2. In the time domain, this means that the equivalent impulse response at the Nyquist rate has zero-valued odd samples ensuring no cross-talk between two multiplexed inputs. Compared to the adaptive equalizer used for flattening the frequency response, this filter consumes three times lower power while occupying half the area. A two-channel ADC is demonstrated using both the adaptive equalizer & the π-shifted filter. The ADC uses a CTDSM running at 6.144 MHz with an oversampling ratio (OSR) of 64, yielding a per-channel bandwidth of 24 kHz. The prototype in 180 nm achieves a peak SNR/SNDR/DR of 91.7 dB/84.9 dB/98 dB and consumes 1.33 mW per channel with adaptive equalizer. The SNR/SNDR/DR is 90.5 dB/83.7 dB/97 dB with a power consumption of 0.86 mW per channel with the π-shifted filter.

Session 6-C: Digital System & Accelerator II
Room: Zoom Room C

Paper 1
Title: FPGA-based Low-Visibility Enhancement Accelerator for Video Sequence by Dynamic Clip-Threshold Adaptive Histogram Equalization
Authors: Canran Xu, Zizhao Peng, Xuanzhen Hu, Wei Zhang, Lei Chen, Fengwei An
Institutes: School of Microelectronics, Southern University of Science and Technology, China; Pengcheng Lab, Shenzhen, China; Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, Southern University of Science and Technology, China
Abstract: In the natural and practical scenario, the captured video sequence under bad weather situations or low light conditions often suffers from poor visibility and low-contrast problems. This hurts the performance of the high-level processing, e.g. object tracking or recognition. In this paper, we develop an FPGA-based low-visibility enhancement accelerator for video sequence by adaptive histogram equalization with dynamic clipthreshold (AHEwDC) which is determined by the visibility assessment. The main goal is to improve the low visibility with high image quality for both hazy and low-light video sequences in realtime. Firstly, a concept to quantify the visual perception based on supervised learning is to estimate the visibility score. Then, to avoid the problem of noise amplification in the conventional method, we propose a visibility assessment model to find an optimal clip-threshold. The contrast energy of gray channel, yellow-blue channel and red-green channel, average saturation, and gradients are statistical features in the model to describe the visibility of an image. Finally, to meet the speed requirement for video sequence processing, a specified hardware architecture for both visibility assessment and AHEwDC is implemented on FPGA. Besides, a mean spatial filter for cumulative distribution functions (CDFs) of the AHE is developed for suppressing the noise caused by a single-color local region. The demonstration system on the DE1-SoC platform with the Intel Cyclone V FPGA device with the max working frequency of 75.84 MHz is capable of processing 30 fps FHD (1920×1080) video.

Paper 2
Title: Binary Classifiers for Data Integrity Detection in IoT Edge Devices
Authors: Arlene John, Rajesh C Panicker, Barry Cardiff, Yong Lian and Deepu John
Institutes: School of Electrical and Electronic Engineering, University College Dublin, Ireland; Department of Electrical and Computer Engineering, National University Singapore, Singapore; Department of Electrical Engineering & Computer Science, Lassonde School of Engineering, York University, Toronto, Canada
Abstract: This paper presents a comparison of several artificial intelligence (AI) based binary classifiers for detecting the integrity of data obtained from Internet of Things (IoT) enabled wearable sensors. Detecting the integrity of data at the network edge facilitates the elimination of corrupted or unusable data, which translates to a lower amount of data stored and transmitted. This reduces the storage and power requirements of IoT devices without a reduction in functionality. In this work, we explore several machine learning-based classifiers to check the integrity of electrocardiogram (ECG) data. The feature vectors are derived from low complexity kurtosis and skewness based Signal Quality Indices (SQIs). From the experiments, it is found that a bagged ensemble of 3 neural networks achieves the highest detection accuracy of 99.47 %. We also estimated the complexity and power consumed by the various classifier implementations and classifier fusion implementations. The energy consumed by the ensemble classifier was estimated to be around 0.039 nJ.

Paper 3

Title: Hardware Efficient Tiny Yolo CNN based on Booth Multiplier and WALLACE Tree Adders

Authors: Fasih Ud Din Farrukh, Chun Zhang, Yancao Jiang, Zhonghan Zhang, Ziqiang Wang, Zhihua Wang and Hanjun Jiang

Institutes: Institute of Microelectronics (IME), Tsinghua University; Tsinghua National Laboratory for Information Science and Technology, China

Abstract: Convolutional Neural Network (CNN) has attained high accuracy and it has been widely employed in image recognition tasks. In recent times, deep learning-based modern applications are evolving and it poses a challenge in research and development of hardware implementation. Therefore, hardware optimization for efficient accelerator design of CNN remains a challenging task. A key component of the accelerator design is a processing element (PE) that implements the convolution operation. To reduce the amount of hardware resources and power consumption, this article provides a new processing element design as an alternate solution for hardware implementation. Modified BOOTH encoding (MBE) multiplier and WALLACE tree-based adders are proposed to replace bulky MAC units and typical adder tree respectively. The proposed CNN accelerator design is tested on Zynq-706 FPGA board which achieves a throughput of 87.03 GOP/s for Tiny-YOLO-v2 architecture. The proposed design allows to reduce hardware costs by 24.5% achieving a power efficiency of 61.64 GOP/s/W that outperforms the previous designs.

Paper 4

Title: Low-Cost Adaptive Exponential Integrate-and-Fire Neuron Using Stochastic Computing

Authors: Shanlin Xiao, Wei Liu, Yuhao Guo, and Zhiyi Yu

Institutes: School of Electronics and Information Technology, Sun Yat-sen University, Guangzhou, China; School of Microelectronics Science and Technology, Sun Yat-sen University, Zhuhai, China

Abstract: Neurons are the primary building block of the nervous system. Exploring the mysteries of the brain in science or building a novel brain-inspired hardware substrate in engineering are inseparable from constructing an efficient biological neuron. Balancing the functional capability and the implementation cost of a neuron is a grand challenge in neuromorphic field. In this paper, we present a low-cost adaptive exponential integrate-and-fire neuron, called SC-AdEx, for large-scale neuromorphic systems using stochastic computing. In the proposed model, arithmetic operations are performed on stochastic bit-streams with small and low-power circuitry. To evaluate the proposed neuron, we perform biological behavior analysis, including various firing patterns. Furthermore, the model is synthesized and implemented physically on FPGA as a proof of concept. Experimental results show that our model can precisely reproduce wide range biological behaviors as the original model, with higher computational performance and lower hardware cost against state-of-the-art AdEx hardware neurons.

Paper 5
Title: A ReRAM-Based Computing-in-Memory Convolutional-Macro with Customized 2T2R Bit-cell for AIoT chip IP Applications
Authors: Fei Tan, Yiming Wang, Liran Li, Tian Wang, Feng Zhang, Xinghua Wang, Jianfeng Gao and Yongpan Liu
Institutes: School of Information and Electronics, Beijing Institute of Technology, Beijing, P. R. China; Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics Chinese Academy of Sciences, Beijing, P .R. China; Department of Electronic Engineering, Tsinghua University, Beijing, P. R. China.
Abstract: To reduce the energy-consuming and time latency incurred by Von Neumann architecture, this paper developed a complete computing-in-memory (CIM) convolutional macro based on ReRAM array for the convolutional layers of a LeNet-like convolutional neural network (CNN). We binarized the input layer and the first convolutional layer to get higher accuracy. The proposed ReRAM-CIM convolutional macro is suitable as an IP core for any binarized neural networks' convolutional layers. This work customized a bit-cell consisting of 2T2R ReRAM cells, regarded $\mathbf{9 \times 8}$ bit-cells as one unit to achieve high hardware compute accuracy, great read/compute speed, and low power consuming. The ReRAM-CIM convolutional macro achieved 50 ns product-sum computing time for one complete convolutional operation in a convolutional layer in the customized convolutional neural network (CNN), with an accuracy of 96.96\% on MNIST database and a peak energy efficiency of 58.82 TOPS/W.

Session 7-A: Temp. Sensors & References
Room: Zoom Room A

Paper 1
Title: A Dynamic-Biased Resistor-Based CMOS Temperature Sensor with a Duty-Cycle-Modulated Output
Authors: Zhong Tang, Yun Fang, Xiaopeng Yu, Shi Zheng, Ling Lin and Nianxiong Tan
Institutes: Zhejiang University, Institute of VLSI Design; Vango Technologies, Inc.
Abstract: This brief presents a resistor-based CMOS temperature sensor with a duty-cycle-modulated output. A dynamic-biased resistive analog front-end (AFE) is proposed to generate voltages with positive and negative temperature dependencies. The voltages are then converted into a digital-friendly duty-cycle-modulated output, which can be proceeded by digital systems directly. Fabricated in a standard 0.13-μm CMOS process, this sensor occupies a silicon area of 0.025 mm and can operate with a supply voltage as low as 0.8 V. It has a measured inaccuracy of ±0.85 ºC (3σ) from -40 ºC to 85 ºC after a two-point calibration. Measured at room temperature, it shows a resolution of 0.226 ºC in a 0.25-ms conversion time while dissipating 12.5 μW.

Paper 2
Title: A 490-pW SAR Temperature Sensor with a Leakage-Based Bandgap-Vth Reference
Authors: Bumjin Park, Youngwoo Ji and Jae-Yoon Sim
Institutes: Department of Electronic and Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea
Abstract: This paper presents a temperature sensor that combines a leakage-based bandgap-Vth reference and an asynchronous SAR. The proposed sensor is implemented with 0.18 μm CMOS technology. By sampling leakage-based biases directly in the SAR ADC, the sensor consumes 490 pW at 20 ºC with a conversion time of 200 ms and stably works with a 1-point calibration, showing a ±2.35 ºC peak-to-peak inaccuracy from -10 to 100 ºC. The proposed sensor can operate across a wide range of supply voltage of 1 V to 2.1 V, with a supply sensitivity of 1.073 ºC/V.

Paper 3

Title: A +0.88/−0.95℃ (3σ) Inaccuracy, 1.99-μW Time-Domain CMOS Temperature Sensor with 2nd-Order ΔΣ Modulator and On-Chip Reference Clock

Authors: Yang Chen, Zihao Jiao, Weijun Guan, Quan Sun, Xiaofei Wang, Ruizhi Zhang and Hong Zhang

Institutes: School of Microelectronics, Xi'an Jiaotong University, Xi'an, China; Shaanxi Provincial Institute of Metrology Science, Xi'an, China

Abstract: This paper presents a compact and low-power time-domain CMOS temperature sensor intended for Internet of Things. To eliminate the off-chip reference clock that is commonly needed for time-domain CMOS temperature sensors, a precise on-chip reference clock is designed to measure the temperature-dependent delay generated by an inverter chain with even stages. In the reference clock circuit, a relaxation oscillator showing discharging phases with negative temperature coefficient (TC) is designed, which are compensated by 2 identical inverter-chains with positive-TC delay, resulting in a reference clock with nearly temperature-independent pulse width and period. In addition, a 2nd-order hybrid time-voltage delta-sigma (ΔΣ) modulator with feedforward path is proposed to quantize the temperature-dependent delay of the main inverter chain, achieving 100-mK resolution only in about 25-ms conversion time. Fabricated in 0.18-μm CMOS, measurement results show that the best (worst)-case TC of the clock's reference time is 3 (11) ppm/°C and the temperature sensor achieves a 3σ inaccuracy of +0.88/−0.95°C from −20°C to 80°C. The prototype occupies 0.45-mm2 chip area and consumes 1.99-μW from a 1.8-V supply at room temperature.

Paper 4

Title: A -40°C to 120°C, 169 ppm/°C Nano-Ampere CMOS Current Reference

Authors: Qiwei Huang, Chenchang Zhan, Lidan Wang, Zhiqun Li and Quan Pan,

Institutes: School of Microelectronics, the Southern University of Science and Technology, Shenzhen, China; School of Information Science and Engineering, Southeast University, Nanjin, China; Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, China; Institute of RF- & OE-ICs, Southeast University, Nanjing, China

Abstract: This brief presents a nano-ampere CMOS current reference (CCR) for low power application with a wide temperature range from -40 °C to 120 °C. The current reference is generated by the division of a temperature-independent voltage and resistance in a simple way. The low temperature-independent voltage is generated based on the threshold voltage difference between two same-type NMOS transistors with different channel lengths working in the subthreshold region, while the temperature-independent resistance is made up by two poly resistors, whose temperature coefficients are opposite. By designing a low voltage to allow for a small resistance, the CCR circuit takes a small chip area while generating nano-ampere current. The proposed CCR circuit was implemented in a standard 0.18-μm CMOS process and its active area is 0.054 mm2 . Among the measured 10 samples, the average output current is 11.6 nA and the average temperature coefficient is 169 ppm/°C.

Paper 5

Title: A 0.5-V Supply, 36nW Bandgap Reference with 42ppm/°C Average Temperature Coefficient Within -40°C to 120°C

Authors: Chi-Wa U, Wen-Liang Zeng, Man-Kay Law, ChiSeng Lam, and Rui Paulo Martins
Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China; Institute of Microelectronics, University of Macau, Macao, China; Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao, China

Abstract: This paper presents a switched capacitor network (SCN)-based bandgap voltage reference (BGR) circuit designed and implemented in a 65nm standard CMOS process with a wide temperature range, high precision, low supply voltage and low power consumption for IoT device application. The proposed BGR employs a 2x charge pump with ripple optimization design to supply the VEB generator, which can relax VDD from 0.9V to 0.5V. A proportional to absolute temperature (PTAT) current source is proposed to bias the PNP BJT in order to reduce the nonlinearity of VEB. Moreover, a voltage divider SCN with low leakage consideration to form the complementary to absolute temperature (CTAT) voltage is designed to reduce the nonlinearity of its coefficient, while a seriesparallel SCN with adjusted clock swing to form the PTAT voltage is designed to improve the line regulation of the BGR. The measurement result shows that the proposed BGR has a temperature coefficient (TC) of 42 ppm/°C at 0.5V supply within −40 °C to 120 °C. The line regulation is 3.2mV/V or 0.64%/V from 0.5V to 1V. Based on 6-chip test result, it shows a 3σ/μ variation of 3.08% before trimming, while 0.36% after trimming.

Paper 6

Title: A Nano-Watt Dual-Output Subthreshold CMOS Voltage Reference

Authors: Jie Lin, Lidan Wang, Yan Lu and Chenchang Zhan
Institutes: Institute of Microelectronics / State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China; School of Microelectronics, Southern University of Science and Technology, Shenzhen, China

Abstract: A dual-output CMOS voltage reference is presented for ultra-low power applications that require two or more different voltage references. The VREF1 is designed by employing the VTH difference between two devices to compensate the temperature coefficient (TC) of the thermal voltage. The VREF2 is generated by feeding a current mirrored from the first reference voltage's supply current into a diode-connected-transistor load. In such a way, two different voltage references can be generated in one compact and simple design to reduce the devices and chip area significantly, compared to two separate voltage references in a conventional design. Fabricated in a 0.18-μm CMOS process, the proposed CMOS voltage reference can provide two references of 331.8 and 660.3 mV with variation coefficients of 0.53% and 0.42%, respectively. The average TCs of VREF1 and VREF2 for a temperature range of -40 to 125ºC are measured as 41.7 and 24.5 ppm/oC, respectively. The line sensitivity (LS) of VREF1 is 0.0505 %/V with 0.6-1.8 V supply, and the LS of VREF2 is 0.114 %/V with 0.8-1.8 V supply. The measured results show a competitive power supply ripple rejection, and the power consumption is only 4.12 nW with 0.8-V minimum supply at 25oC, while the active area is 0.0108 mm2.

Session 8-B: Data Converter II
Room: Zoom Room B

Paper 1
Title: Improved Continuous-Time Delta-Sigma Modulators with Embedded Active Filtering
Authors: Saravana Manivannan and Shanthi Pavan
Institutes: Department of Electrical Engineering, Indian Institute of Technology, Madras
Abstract: Continuous-time ΔΣ modulators used in wireless transceivers need to digitize small desired signals that are accompanied by large out-of-band interferers. In such applications, it is desirable that the CTΔΣM have a low-pass signal transfer function whose bandwidth can be specified. Many architectures present themselves as potential candidates to realize such filtering-CTΔΣMs . This work investigates these threads and concludes that a CTΔΣM with an embedded Rauch filter is a compelling design choice. The theory is supported by measurement results from a filtering-CTΔΣM test chip that achieves a peak SNDR of 76.7 dB in a 1 MHz signal bandwidth. Measurements demonstrate improved power efficiency and outof-band linearity when compared to prior art.

Paper 2
Title: Near-Optimal Decoding of Incremental Delta-Sigma ADC Output
Authors: Bo Wang, Man-Kay Law, Samir Brahim Belhaouari, and Amine Bermak
Institutes: Division of Information and Computing Technology, College of Science and Engineering, Hamad Bin Khalifa University, Doha, Qatar; State Key Laboratory of Analog and Mixed-Signal VLSI, Macau University, Macau, China
Abstract: This paper presents a nonlinear digital decoder (reconstruction filter) for incremental delta-sigma modulators. This decoder utilizes both the magnitude and pattern information of the modulator output to achieve accurate input estimation. Compared to the conventional linear filters with the same oversampling ratio, it can improve the converter's signal-toquantization noise ratio (SQNR) by a few dB to a few 10's of dB with slight thermal noise performance degradation. Using the proposed decoder, the modulator's OSR can be a few times less while achieving the same resolution and data rate, thus minimizing the modulator as well as its peripheral circuits' energy consumption. In this paper, the proposed decoder is optimized for digital implementation, with its function being verified using a modulator prototype. This decoder is mainly designed for dc or near-dc signal conversions and it does not provide frequency notches.

Paper 3
Title: A 14b, Two fold Time-Interleaved Incremental ΔΣ ADC using Hardware Sharing
Authors: P. Vogelmann, J. Wagner, M. Ortmanns
Institutes: Ulm University, Institute of Microelectronics
Abstract: High-resolution, single-loop incremental DeltaSigma (I-ΔΣ) ADCs require large oversampling ratios to sufficiently suppress quantization noise. This limits the bandwidth of most designs to the low-kHz range. To overcome this problem, the presented proof-of-concept design makes use of time interleaving two third-order I-ΔΣ modulators with embedded hardware sharing that helps to enhance the efficiency of the presented modulator. The modulator is fully reconfigurable in a way that both channels can either be operated time interleaved or independent from each other. This is a means of enhancing the flexibility and efficiency of the modulator depending on the application scenario. The presented design was fabricated in a 180 nm technology node.

Paper 4

Title: A 12-Bit 125-MS/s 2.5-Bit/Cycle SAR-Based Pipeline ADC Employing A Self-Biased Gain Boosting Amplifier

Authors: Chulhyun Park, Tao Chen, Kyoohyun Noh, Dadian Zhou, Suraj Prakash,Mohammad H. Naderi, Aydin I Karsilayan, Degang Chen, Randall L Geiger and Jose Silva-Martinez

Institutes: Analog and Mixed-Signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX, USA; Department of Electrical and Computer Engineering, Iowa State University, Ames, IA, USA

Abstract: This paper introduces a 12 bit 2.5 bit/cycle SARbased pipeline ADC employing a self-bias gain boosting amplifier. The single-stage amplifier achieves a low-frequency gain of 37 dB, while consuming 1.3 mW of power consumption with 1.3 V of analog power supply. A 2.5 bit/cycle SAR ADC realizes as the sub-ADC in each stage, and reduces both power consumption and silicon area. A two-channel sampling architecture is employed to double the sampling rate and thereby maximize circuit efficiency. A digital calibration technique is used to reduce non-linearity and mismatches due to the RDAC, as well as gain error and offset of the open-loop residue amplifier. The prototype ADC was fabricated in TSMC 40-nm technology, and consumes 10.71 mW with 1.1 V / 1.3 V digital / analog power supplies. When operating at 125 MS/s, the ADC achieves an SFDR of 66.59 dB before calibration and 80.3 dB after calibration when measured at Nyquist frequency. The experimental results show a Walden FoM of 101 fJ/c.-s. before calibration and 47 fJ/c.-s. after calibration.

Paper 5

Title: A Configurable Noise-Shaping Band-Pass SAR ADC with Two-Stage Clock-Controlled Amplifier

Authors: Zihao Jiao, Yang Chen, Xiaobo Su, Quan Sun, Xiaofei Wang, Ruizhi Zhang, Hong Zhang

Institutes: School of Microelectronics, Xi'an Jiaotong University, Xi'an, China; School of Microelectronics, Xidian University, Xi'an, China

Abstract: This paper presents an 8×-oversampling successive approximation register (SAR) analog-to-digital converter (ADC) with configurable center frequency of noise shaping (NS), which permits the signal passband being configured to any one of the 8 equally divided sub-bands in the first Nyquist band. The configurable noise shaping is realized by an error-feedback (EF) structure with an adjustable 2-tap switched-capacitor (SC) FIR filter. Taking advantage of the sub-bands' symmetry, the selection of the 8 sub-bands are determined by only a 2-bit controlled variable capacitor in the FIR filter in addition to one bit indicating which half-band the target sub-band is in. As a result, the configuration circuit is area efficient and introduces very little parasitic into the critical EF path. A 2-stage clock-controlled amplifier (CAMP) is proposed for the EF path, which can ensure gain and speed simultaneously through allocating reasonable currents into the gain stage and the driving stage separately. Implemented in 65-nm CMOS process, measurement results under a sampling rate of 10 MSPS show that the prototype achieves signal-to-noise-and-distortion (SNDR) of 71.9~74.6dB in the 8 sub-bands with 625-KHz bandwidth, corresponding to a Scherier FoM of 171.4 -174 dB. The ADC prototype occupies 0.03-mm2 core area and consumes 70-μW average power at 1-V supply voltage.

Paper 6

Title: An Error Amplifier with a Low Power Multi-Mode Voltage Clamper for Transient Enhancement and High Reliability

Authors: Ze-kun Zhou, Anqi Wang, Yunkun Wang, Jiani Wang, Yue Shi, Zhuo Wang, and Bo Zhang
Institutes: State key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, China; College of Communication Engineering, Chengdu University of Information Technology, Chengdu, China

Abstract: This paper proposes a low power area-efficient multi-mode voltage clamper circuit called pseudo differential pair and applies it into an error amplifier (EA) which can be used in DC-DC converters as a practical design example. In addition to a normal amplifying mode, the error amplifier has two extra operation modes with the help of the voltage clamper, which can limit the maximum output voltage and the maximum sink current, respectively. By inserting this pseudo differential pair of only three transistors in the intermediate stage of the amplifier, a voltage-current feedback is introduced to achieve the voltage limiting function without bringing resistive load to the output stage or unwanted effects to the input stage. The frequency compensation of the EA is also reused in the voltage limiting loop to make the whole block more compact. The circuit is implemented in a 0.35 μm BCD process. The verification results match the theoretical analysis very well, which proves that the proposed voltage clamper can effectively enhance transient response of the converter control loop and improve system reliability. Only additional 0.001689 mm2 active area is occupied for about 2X transient speed improvement with fair open loop amplifying performance.

Session 9-C: Analog Circuits

Room: Zoom Room C

Paper 1

Title: A 90-nm 640 MHz 2×VDD Output Buffer with 41.5% Slew Rate Improvement Using PVT Compensation

Authors: Jian-An Wang, Yuan-Yao Zhao, and Zheng-Ping Zhang
Institutes: Science and Technology on Analog Integrated Circuit Laboratory, Chongqing, China; College of Electronics Engineering/Chongqing International Semiconductor College, Chongqing University of Posts and Telecommunications, Chongqing, China

Abstract: This paper presents a 2×VDD output buffer using the encoded compensation technique to minimize slew rate (SR) deviation caused by PVT (process, voltage, temperature) variations. The process detectors can both detect all five process corners and ensure the compensation code unchanged in VT variations. Besides, the charging paths of the proposed voltage level converter (VLC) are independent and directly driven by logic gate, which applied in output stage to speed output buffer data rate up. The proposed design is implemented using a typical 90 nm 1.2 V 1P9M CMOS process, where the core area of a single output buffer is 400 μm×56 μm. The measured maximum data rate is 640/480 MHz given 1.2/2.5 V supply voltage, and the power consumption is 32.2 mW at 640 MHz data rate. the slew rate variation improvement is 41.5%/41.9% by PVT detection and SR compensation for VDDIO=1.2/2.5 V, respectively.

Paper 2

Title: A Generic Nano-Watt Power Fully Tunable 1-D Gaussian Kernel Circuit for Artificial Neural Network

Authors: Ahmed Reda, Liang Qi, Yongfu Li, and Guoxing Wang
Institutes: Bio-circuits and systems Laboratory, Department of MicroNano Electronics and MoE Key Lab of Artificial Intelligence, Shanghai Jiao Tong University, Shanghai, China

Abstract: This paper presents an ultra-low-power generic fully tunable analog 1-D Gaussian kernel (GK) circuit, which is employed as an activation neuron for the radial basis function artificial neural network. In the proposed GK circuit, the maximum likelihood, center, and width of the Gaussian profile can be independently controlled. Besides, we have developed a mathematical model for the proposed GK circuit and further verified them experimentally. Thereby, the presented modeling can be employed to facilitate the off-chip learning of the neural network hardware. Fabricated in 180 nm CMOS process, the prototype demonstrates the full tunability of the proposed GK circuit and good agreement between the experimental measurements and mathematical model. The relative error of the measured width of the GK's profile is less than 7 % compared to the value predicted by the presented mathematical model. The total power consumption is 13.5 nW with a supply voltage of 0.9 V, and the core circuit occupies 0.013 mm2.

Paper 3

Title: A 50μW Fully Differential Interface Amplifier with a Current Steering Class AB Output Stage for PPG and NIRS Recordings

Authors: Shuang Song, Qiuyang Lin, Chris van Hoof and Nick van Helleputte
Institutes: IMEC, Heverlee, Belgium; KU Leuven, Leuven, Belgium

Abstract: This paper presents a low-power fully differential optical sensor interface amplifier for photoplethysmography (PPG) and near infrared spectroscopy (NIRS) recordings. The proposed amplifier employs a stacked current reuse input stage that provides a DC biasing voltage for the photodiode, reducing the parasitic capacitance. The output stage exploits a fully differential current steering class AB topology with a self-regulated common mode voltage, providing a 70μA input current range with minimized quiescent current. Moreover, the interface amplifier can be reconfigured as either single-ended mode suitable for photo detectors biased at a high voltage or fully differential mode for those biased at a low voltage. This amplifier is implemented in a standard 0.18μm CMOS process and characterized experimentally. Measurement results show that, with a 1.5V supply, the amplifier can provide up to 1V biasing voltage for the photodiode and consumes a static power of around 50μW. It achieves a dynamic range of 97dB in fully differential mode with an input referred noise of 67pArms in 32Hz band and 102dB in single -ended mode with an input referred noise of 582pArms.

Paper 4

Title: A CMRR Enhancement Circuit Employing Gm-Controllable Output Stage for Capacitively Coupled Instrumentation Amplifier

Authors: Hyuntak Jeon, Jun-Suk Bang and Minkyu Je
Institutes: School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea; Samsung Electronics, Hwaseong, South Korea

Abstract: The capacitively coupled instrumentation amplifier (CCIA) is broadly used for neural signal acquisition. Although it is suitable for various biopotential recording applications, the CCIA is vulnerable to capacitor mismatches, which degrades the commonmode rejection ratio (CMRR). The neural signals with small amplitude can be easily contaminated by large-amplitude commonmode (CM) interferences due to the degraded CMRR. This paper presents a CMRR enhancement circuit for the CCIA, with which the capacitor mismatches can be compensated in a power-efficient manner. In the proposed CCIA, the gains of a pair of output stages are controlled separately to reject the output signals generated by the CM interferers in the presence of capacitor mismatches. Employing the proposed CMRR enhancement scheme, the implemented CCIA achieves a CMRR over 90 dB from 10 Hz to 1 kHz and 3.4-μVrms integrated input-referred noise (IRN) while only consuming 1.5 μW per channel.

Paper 5

Title: InP DHBT Single-Stage and Multiplicative Distributed Amplifiers for Ultra-wideband Amplification

Authors: Temitope Odedeyi, Stavros Giannakopoulos, Herbert Zirath and Izzat Darwazeh
Institutes: Department of Electronic and Electrical Engineering, University College London, London, UK; Microwaves Electronic Laboratory, Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, Göteborg, Sweden

Abstract: This paper highlights the gain-bandwidth merit of the single stage distributed amplifier (SSDA) and its derivative multiplicative amplifier topologies (i.e. the cascaded SSDA (CSSDA) and the matrix SSDA (M-SSDA)) for ultra-wideband amplification. Two new monolithic microwave integrated circuit (MMIC) amplifiers are presented: an SSDA MMIC with 7:1 dB average gain and 200 GHz bandwidth, with a high frequency gain tuning range of 5 dB to 12 dB; and the world's first M-SSDA, which has a 12 dB average gain and 170 GHz bandwidth. Both amplifiers are based on an Indium Phosphide DHBT process with 250 nm emitter width. To the authors best knowledge, the SSDA has the widest bandwidth for any single stage amplifier reported to date. Furthermore, the three tier M-SSDA has the highest bandwidth and gain-bandwidth product for any matrix amplifier reported to date.

Paper 6

Title: Low-Voltage Gate-Leakage-Based Timer Using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS

Authors: Atsuki Kobayashi and Kiichi Niitsu
Institutes: Nagoya University, Nagoya, Japan; Precursory Research for Embryonic Science and Technology (PRESTO), Japan Science and Technology Agency, Saitama, Japan

Abstract: Energy-efficient timer circuits are required in numerous applications for periodic operations, such as performing measurements and communicating data. In this paper, we present a gate-leakage-based timer that utilizes an amplifier-less replica-bias switching technique to generate a stable frequency, which can operate at a low supply voltage. To guarantee a stable oscillation frequency in a small circuit area, the proposed design adopts an architecture that discharges a pre-charged capacitor through a resistive element (gate-leaking MOS capacitor) with a low-leakage switch. In the proposed switching technique, the low-voltage timer operates by tracking the discharging terminal of the capacitor and biasing the reference voltages of two switch units, thereby enabling the minimization of the leakage current without the need for analog amplifier circuits. The high supply sensitivity of the timer is addressed by regulating the supply voltage using a native NMOS header (NNH). The proposed design is fabricated using the 55-nm deeply depleted channel (DDC) CMOS technology, which has a strong body coefficient and occupies an active circuit area of 0.0022 mm2 . The measurements show that the proposed design can achieve an energy-per-cycle value of 25 pJ/cycle at a supply voltage of 350 mV when body biasing is applied. The measured Allan deviation floor is 200 ppm at room temperature. The timer exhibits an average temperature sensitivity of 810 ppm/◦C for four samples. Moreover, a reduction in the supply sensitivity by a factor of 26 using the NNH is demonstrated in an active circuit area of 0.0034 mm2.

TECHNCIAL PROGRAM - Day 2: 28th August 2020

Session 10-A: DC-DC Converters
Room: Zoom Room A

Paper 1
Title: A Fully Integrated Step-Down Switched-Capacitor DC-DC Converter with Dual Output Regulation Mechanisms
Authors: Po-Han Chen, Hao-Chung Cheng, and Po-Hung Chen
Institutes: National Chiao Tung University, Hsinchu, Taiwan
Abstract: This paper proposes a fully integrated step-down switched-capacitor (SC) DC-DC converter using 0.18-μm CMOS technology for system-on-chip applications. The proposed stepdown switched-capacitor DC-DC converter used two control mechanisms: the switch array modulation technique to regulate the output voltage and the voltage ripple modulation technique to adjust the output voltage ripple of the converter as the loading current varied. As a result, the proposed converter could generate a regulated output voltage with low voltage ripple. The converter core performed at conversion ratios of 1/3 and 1/2 under an input voltage of 1.8 V. The measurement results on 180-nm technology showed that the proposed fully integrated step-down switchedcapacitor DC-DC converter could achieve a peak power conversion efficiency of 74.1% and maintain power conversion efficiency at levels over 70% within loading ranges between 1.4 and 5 mA. The output voltage ripple was controlled at levels under 63.4 mV within a loading current ranging between 0.1 and 5 mA.

Paper 2
Title: Inductorless DC/DC Converter for Aerospace Applications with Insulation Features
Authors: G. Ciarpi and S. Saponara
Institutes: Dep. of Information Eng.- University of Pisa, Pisa, Italy
Abstract: The future satellites for scientific missions require ever more sensible instrumentations to detect new phenomena, which is extremely sensitive to electromagnetic disturbance. For this reason, in this paper, an inductorless DC/DC converter with very low electromagnetic emission levels is presented. It, avoiding the use of cumbersome transformers and inductors, is able to converter wide input voltage range, from 6 V to 60 V, in two points of load at 5 V and 1.65 V, saving weight and space. An innovative insulating stage, based on Switched-Capacitor architecture, is introduced in the converter to increase its fault-tolerant property. The whole converter is fabricated in 0.35 μm HV-CMOS technology and electrically characterized by experimental measurements. Specific tests for space compliance were performed as Total Ionization Dose and Single Event Effect tests, highlighting the feasibility use of the converter in Earth-Moon travels.

Paper 3

Title: A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery

Authors: Wen-Liang Zeng, Edoardo Bonizzoni, Chi-Wa U, Chi-Seng Lam, Sai-Weng Sin, U-Fat Chio, Franco Maloberti, and Rui Paulo Martins

Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China; Institute of Microelectronics, University of Macau, Macau, China; Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau, China; Department of Electrical, Computer and Biomedical Engineering, University of Pavia, Pavia, Italy

Abstract: This brief presents a successive-approximationregister (SAR) analog-to-digital converter (ADC) assisted DC-DC buck converter, which operates in discontinuous conduction mode (DCM) and achieves fast load transient recovery characteristics. The power inductor of the buck converter uses the bond-wire inductance. During the load transient, the dynamic low-power SAR ADC samples the converterís undershoot/overshoot output voltage and controls the programmable current pump circuit to charge/discharge the output capacitor, thus speeding up and smoothing the load transient response. An additional compensation circuit is also designed to ensure the stability of the voltage mode control loop and the current pump. The chip fabricated in a 65-nm CMOS technology occupies an area of 1 mm2 . The converter, switching at 100 MHz, achieves a peak power efficiency of 81% when VIN = 1.2 V, VOUT = 1 V and ILoad = 50 mA. When the load current steps from 2 mA to 50 mA, the measured undershoot/overshoot voltage is 101/92 mV, and the recovery time is 175/406 ns.

Paper 4

Title: A 4-MHz Digitally Controlled Voltage-Mode Buck Converter with Embedded Transient Improvement Using Delay Line Control Techniques

Authors: Qiwei Huang, Chenchang Zhan, and Jinwook Burm

Institutes: School of Microelectronics, Southern University of Science and Technology, Shenzhen, China; Department of Electronic Engineering, Sogang University, Seoul, Korea; Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, China; Department of Electronic Engineering, Sogang University, Seoul, Korea

Abstract: In this paper, a digitally controlled voltage-mode buck converter with embedded transient improvement using delay line-based control techniques is presented. Two voltage-controlled delay lines (VCDL's) are used to convert the difference between the feedback and reference voltages to a delay time difference. The delay difference is then fed to the multiple-outputs bang-bang phase detector (MOBBPD), which converts the input delay difference to multiple-bits digital codes in a simple nonlinear way. The MOBBPD scheme leads to high resolution for small output ripple and improved response when large load transient happens in a low-cost way. A digital loop filter (DLF) accumulates the MOBBPD output codes to control the duty cycle through a novel digital pulse width modulator (DPWM) to regulate the output voltage. By designing the coefficients of the DLF, a type-II compensator can be achieved through the integral and proportional paths to make the loop stable. The proposed DPWM, which consists of a divide-by-8 frequency divider, two delay lines and a few simple digital logics, achieves a wide tunable range of duty cycle under various process corners and supply voltages. A proof-of-concept design of the proposed buck converter was fabricated in a standard 0.18 μm CMOS technology. The measured results show that it achieves a very wide output voltage range from 0.1 V to 3.5 V for a input supply range from 2.4 V to 3.6 V. With a 400 mA step in the load current, the overshoot/undershoot is less than 87 mV and the 1% settling time is less than 16 μs. The peak efficiency is 95.2% with 250 mA load current at 2.4 V output voltage with 3.3 V input voltage.

Paper 5

Title: A 470nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter With Seamless Mode Selection for IoT Application

Authors: Wen-Liang Zeng, Yuan Ren, Chi-Seng Lam, Sai-Weng Sin, Weng-Keong Che, Ran Ding and Rui Paulo Martins

Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China; Institute of Microelectronics, University of Macau, Macau, China; Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau, China; Allwinner Technology Co., Ltd., Zhuhai, Guangdong, China

Abstract: An ultra-low quiescent current dual-mode buck converter system is designed for IoT application, which includes a double clock time (DCT) and a pulse-width-modulation (PWM) control modes. The proposed DCT mode can reduce the conversion loss over a wide loading range from nA-to-mA and achieve seamless mode transition from DCT to PWM control. Implemented in a 0.18μm CMOS, this converter achieves a peak efficiency of 92.7%/94.7% in DCT/PWM and >80% efficiency from 10 4μA to 50 mA (5000x), with a wide input voltage from 2 V to 5 V. A quiescent current of 470 nA including bandgap voltage reference and internal oscillator is achieved. The DCT-to-PWM mode selection mechanism achieves an undershoot of 80 mV at 11 μs recovery time when load current jumps from 6.67 μA to 50 mA.

Paper 6

Title: A Switched-Capacitor DC-DC Converter Powering an LC Oscillator to Achieve 85% System Peak Power Efficiency and -65dBc Spurious Tones

Authors: Alessandro Urso, Yue Chen, R. Bogdan Staszewski, Johan Dijkhuis, Stefano Stanzione, Yao-Hong Liu, Wouter A. Serdijn, and Masoud Babaie

Institutes: Technische Universiteit Delft

Abstract: In this paper, we propose a new scheme to directly power a 4.9–5.6 GHz LC oscillator from a recursive switchedcapacitor DC-DC converter. A finite-state machine is integrated to automatically adjust the conversion ratio and switching frequency of the converter such that its DC output voltage is within ±5% of the desired 1V across input voltage range 1.3–2.2 V and <2 mA load current conditions. A gate-driver circuit is embedded in each switch of the converter to guarantee constant on-resistance across PVT variations without sacrificing device reliability. Furthermore, a spur reduction block (SRB) is embedded in the oscillator to suppress the ripple induced spurs by stabilizing its tail current. Both the converter and the oscillator are implemented in 40-nm CMOS technology. The measured peak power efficiency of the converter is 87%, while its spot noise is <1.5 nV/pHz, which does not degrade the phase noise of the oscillator. The SRB suppresses the spur to < −65 dBc under the 30 mVpp ripple of the converter.

Session 11-B: Security Circuits
Room: Zoom Room B

Paper 1
Title: A 15-Gb/s 0.0037-mm2 0.019-pJ/Bit Full-Rate Programmable Multi-Pattern Pseudo-Random Binary Sequence Generator
Authors: Junfeng Hu, Zhao Zhang and Quan Pan
Institutes: School of Microelectronics, and Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, Southern University of Science and Technology, China; Graduate School of Advanced Science and Engineering, Hiroshima University, Higashi-Hiroshima, Japan
Abstract: This brief presents a compact low-power programmable multi-pattern pseudo-random binary sequence (PRBS) generator. It is capable of producing 27-1, 215-1, 223-1 and 231-1 test patterns to meet multiple testing requirements. To reduce power and area, the full-rate architecture with the truly-single-phase clock logic (TSPC) D-flip-flops (DFF) instead of the current-mode logic (CML) DFF is adopted. The multiplexer (MUX) merged TSPC DFF is proposed to avoid the delay of the MUX in conventional multiple pattern PRBS generators. Hence, the critical path delay is reduced, and thus, the maximum data rate can be improved. Fabricated in a 40-nm CMOS process (260-GHz fT), this PRBS occupies a core active area of 0.0037 mm2 and operates at a maximum data rate of 15 Gb/s. The measured power consumption is 8.778 mW with 1.1-V supply. The figure-of-merit (FoM) is 0.019 pJ/bit at the pattern length of 231-1.

Paper 2
Title: Unified Hardware for High-Throughput AES-Based Authenticated Encryptions
Authors: Shotaro Sawataishi, Rei Ueno and Naofumi Homma
Institutes: Tohoku University Sendai-shi, Japan
Abstract: This paper presents an efficient unified hardware for up-to-date authenticated encryptions with associated data (AEADs). Although some major AEADs share several fundamental components (e.g., advanced encryption standard (AES), block chaining, and XOR-Encryption-XOR (XEX) scheme), each AEAD is equipped with a unique mode of operation and/or subfunctions, which makes it difficult to integrate various AEADs in a hardware efficiently. The proposed hardware in this paper efficiently unifies the fundamental components to perform a set of AEADs with minimal area and power overheads. The proposed configurable datapath is adapted to a set of peripheral operations (e.g., block chaining and XEX), dictated by the given AEAD algorithm. In this study, we also demonstrate the validity of the proposed hardware through an experimental design adapted to four AES-based AEADs. Consequently, we confirm that the proposed hardware can perform the four AEADs with quite smaller area than the sum of the each dedicated AEAD hardware, comparable throughput and power consumption. In addition, we confirmed that the proposed hardware is superior to software implementation on general-purpose processor in terms of both throughput and power consumption.

Paper 3

Title: A Reconfigurable Random Number Generator Based on the Transient Effects of Ring Oscillators

Authors: Burak Acar and Salih Ergun

Institutes: TUBITAK - Informatics and Information Security Research Center, Kocaeli, Turkey

Abstract: This study presents a reconfigurable Random Number Generator (RNG) based on transient effect of ring oscillators. Users can select a method based on the irregular sampling of a regular waveform or on the regular sampling of an irregular waveform to obtain a random bit sequence to be used in different applications, such as lightweight cryptography or high-security communication. The entropy is acquired by exploiting Transient Effect Ring Oscillators (TEROs). The proposed fully-digital RNG structure is firstly implemented on a Zynq-7000 FPGA (Field Programmable Gate Array) without any post-processing method such as the Von Neumann. In addition to the RNG structure, an on-the-line test module based on FIPS 140-2 is also implemented to check the randomness of the produced data statistically in real time. Users can change the statistical test parameters according to their desired security levels. Finally, an ASIC (Application Specific Integrated Circuits) implementation of the proposed RNG is done following the Cadence digital design flow for the TSMC 180 nm CMOS process. The implemented ASIC design occupies an area of 0.85 mm x 0.85 mm and the estimated power required is 11.827 mW.

Paper 4

Title: IC Random Number Generator Exploiting Two Simultaneous Metastable Events of Tetrahedral Oscillators

Authors: Recep Günay and Salih Ergün

Institutes: TUBITAK Bilisim ve Bilgi Guvenligi Ileri Teknolojiler Arastirma Merkezi, V.P. of Testing and Evaluation; TUBITAK Bilgi Guvenligi Ileri Teknolojileri Arastirma Merkezi, Informatics and Information Security Research Center; ERGTECH Research Center,

Abstract: A low-cost random number generator (RNG) based on a tetrahedral ring oscillator, which can be utilized in cryptographic systems, is presented. The proposed design exploits two metastable events in the oscillator caused by turning on and off three additional inverters in the classical tetrahedral oscillator, which improves entropy. The design is implemented on FPGA as a proof of concept, but the ASIC implementation will be carried out in the future. A method has been devised to implement this circuit on FPGA. Techniques to increase randomness have been used, such as adjusting the sampling signal considering 1 and 0 balance of the output. The proposed design is compared with the classical tetrahedral oscillator based RNG, and it is observed to be better. The RNG is tested with the National Institute of Standard and Technology (NIST) test suite to prove randomness. The design occupies an area of 0.0036mm2 with a power consumption of 200mW and a bit rate of 10Mb/s. The number of oscillators has been dropped by 60% compared to the classical method.

Paper 5

Title: A 0.04% BER Strong PUF with Cell-Bias-Based CRPs Filtering and Background Offset Calibration

Authors: JiaHao Liu, Yan Zhu, Chi-Hang Chan, and Rui Paulo Martins
Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China

Abstract: This paper presents a low bit error rate (BER) strong PUF based on the dynamically amplified subthreshold current array (DA-SCA) with cell-bias-based challenge-response-pairs (CRPs) filtering method. The highly nonlinear subthreshold characteristic of the DA-SCA ensures a strong resilience to machine learning (ML) attacks and it simultaneously achieves low power and compact area. The current difference of two SCAs originated by the manufacturing process is amplified and converted into a voltage difference which is further digitized by the background offset-calibrated oscillator collapse-based comparator. Fabricated in 65 nm CMOS LP technology, the 64- bit DA-SCA PUF shows an average BER of 4.7% in the worst case for the temperature range of -20 to 80°C and a supply variation of ±10%. Moreover, the proposed cell-bias-based CRPs filtering method dramatically suppresses the BER to 0.04% while discarding only 9.5% CRPs. The power consumption of the proposed PUF is merely 2.4 μW at 125 Kb/s and it occupies 0.024 mm2, including the on-chip calibration circuit. The proposed PUF demonstrates resistance against machine learning (ML) attacks across 100K training samples, limiting the prediction accuracy to ~50%.

Paper 6

Title: A 108 F2/bit Fully Reconfigurable RRAM PUF Based on Truly Random Dynamic Entropy of Jitter Noise

Authors: Qiang Zhao, Wenhan Zheng, Xiaojin Zhao, Yuan Cao, Feng Zhang, and Man-Kay Law
Institutes: College of Electronics and Information Engineering, Shenzhen University, Shenzhen, China; College of IoT Engineering, Hohai University, Changzhou, China; Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China; State Key Laboratory of Analog and Mixed-Signal VLSI, Institute of Microelectronics, and FST-ECE, University of Macau, Macau, China

Abstract: In this paper, we present a fully reconfigurable resistive random access memory (RRAM) physical unclonable function (PUF) based on the truly random dynamic entropy of the ubiquitous jitter noise, which is intrinsically different from most previously demonstrated PUF implementations with semiconductor fabrication's process variation as the static entropy source. In addition, the proposed RRAM PUF is operated by configuring the mainstream RRAM cells to either high resistance state (for '1') or low resistance state (for '0'), according to the customized ring oscillator (RO) true random number generator's digital output that is determined by the random jitter noise. By completely removing the need of dedicated split resistance circuitry (SRC) in existing RRAM PUFs, the proposed implementation is fully compatible with the SET/RESET operations of the RRAM array for mainstream memory applications, leading to minimized design overhead and enhanced reliability without SRC-caused error bits. Fabricated using 130 nm standard complementarymetal-oxide-semiconductor (CMOS) process plus post-processing dedicated to the RRAM devices, the proposed RRAM PUF cell features an ultra-compact footprint of 1.82 μm2 (i.e., 108 F2), which is capable of generating ∼107 PUF bits per cell due to the time-variant property of jitter noise and the full reconfigurability of the RRAM PUF. This significantly innovates all the previous weak PUF implementations based on the static entropy source of process variation, where the maximum bit number per PUF cell is always limited and fixed after the chip fabrication. Meanwhile, ultra-low native unstable bits of 0.28% and bit error rate (BER) per 10◦C of 0.03% can be achieved for the fabricated RRAM PUF. Moreover, by passing the widely-adopted bias test, National Institute of Standards and Technology (NIST) test and autocorrelation function (ACF) test under various VT conditions, the true randomness of the customized RO TRNG' dynamic entropy is validated using 65 nm standard CMOS process. Compared with the state-of-the-art weak PUF implementations, the native unstable bits is improved by 5.36× and the BER per 10◦C is improved by 4×, even under the widest operating temperature range from −50◦C to 150◦C.

Session 12-C: Sensors 1
Room: Zoom Room C

Paper 1
Title: A Digital Capacitive MEMS Microphone for Speech Recognition with Fast Wake-up Feature using a Sound Activity Detector
Authors: Youngtae Yang, Byunggyu Lee, Jun Soo Cho, Suhwan Kim, and Hyunjoong Lee
Institutes: Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea; Inter-University Semiconductor Research Center (ISRC), Seoul National University, Seoul, South Korea; Gwanak Analog Co., Ltd.
Abstract: This paper presents a digital capacitive MEMS microphone for speech recognition with fast wake-up feature using a sound activity detector. The proposed microphone wakes up only when an acoustic event within the voice-band occurs using the sound activity detector, which can significantly reduce the average current consumption. All wake-up processes are performed on-chip, which enables the fast wake-up feature to prevent missing keywords. In addition, the proposed deglitching technique is applied to prevent the sound activity detector from responding to non-acoustic signals such as glitch signals. An auxiliary low-dropout regulator is used to further reduce the wake-up time. Our microphone consumes only 16 μA in deep-sleep mode. In active mode, a high-performance readout circuit converts the voice signal into a digital signal. The proposed microphone achieves an A-weighted signal-to-noise ratio (SNR) of 62.8 dBA and an acoustic overload point of 119.4 dB sound pressure level. The readout circuit itself of our microphone, fabricated in a 0.18 μm CMOS process, has an A-weighted SNR of 65.8 dBA.

Paper 2
Title: A Wireless Multi-Channel Capacitive Sensor System for Efficient Glove-based Gesture Recognition with AI at the Edge
Authors: Jieming Pan, Yuxuan Luo, Yida Li, Chen-Khong Tham, Chun-Huat Heng and Aaron Voon-Yew Thean
Institutes: Department of Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore; Institute of VLSI Design, College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China
Abstract: This paper presents a wireless smart glove based on multi-channel capacitive pressure sensors that are able to recognize 10 American Sign Language gestures at the edge. In this system, 16 capacitive sensors are fabricated on a glove to capture the hand gestures. The sensor data is captured by a 16-channel CDMA-like capacitance-to-digital converter for training/inference at the edge device. Unlike the conventional approach where the capacitive information is recovered before further signal processing, our proposed system approach takes advantage of the capability of the machine learning (ML) algorithms and directly processes the code-modulated signals without demodulation. As a result, it reduces the input data throughput fed into the ML algorithms by 20×. The on-site ML implementation significantly reduces decision-making latency and lowers the required data throughput for wireless transmission by at least 4×. The highest testing classification accuracy of our system achieved is 99.7%, with a <0.1% difference from the conventional demodulated sensing scheme.

Paper 3

Title: Hand Gesture Recognition Using Three-Dimensional Electrical Impedance Tomography

Authors: Dai Jiang, Yu Wu and Andreas Demosthenous

Institutes: Department of Electronic and Electrical Engineering, University College London, Torrington Place, London, U.K.

Abstract: This brief presents a 16-electrode electrical impedance tomography (EIT) system for hand gesture recognition. The hardware of the system is based on integrated circuits including a 12-bit high spectral purity current-steering DAC implemented in 0.18 μm CMOS technology, a current driver and an instrumentation amplifier in 0.35 μm CMOS technology. Both 2D and 3D EIT electrode arrangements were tested for hand gesture recognition. It is shown that using machine learning algorithms, eight hand gestures can be distinguished from the measured bio-impedance data with an accuracy of 97.5% when the electrodes are placed on a single wristband, and an accuracy of 99.5% with the same number of electrodes distributed on two wristbands for 3D EIT measurement. In particular 3D EIT demonstrated significant superiority in its ability to discriminate between gestures with similar muscle contractions.

Paper 4

Title: Design of Stage-Selective Negative Voltage Generator to Improve On-Chip Power Conversion Efficiency for Neuron Stimulation

Authors: Shiau-Pin Lin and Ming-Dou Ker

Institutes: Biomedical Electronics Translational Research Center, National Chiao-Tung University, Taiwan

Abstract: Dedicated to neuron stimulation circuits, a stage-selective negative voltage generator is proposed to enhance the overall power efficiency. Since the supplied voltage of the stimulus driver is subject to applications and treatments, an extensive output requirement of supply is demanded to achieve energy-efficient stimulation. The charge pump is implemented as a negative voltage generator for on-chip design. In a limited area, excess power loss is eliminated by reconfiguring the cascaded architecture and clocks. Digitally programmable voltage levels can be outputted by varying the number of stages dynamically. The function of stage selection is achieved by the proposed stage-selective scheme. With appreciate control, the stage-selective negative voltage generator can maintain higher power efficiency under different output voltage levels and loading conditions. The technique improves 40% power conversion ratio at most but only leads to an increment of 8%in area occupation. The measured output voltage covers from –0.3 V to –9.3 V within a maximum 5.5-mA output current, which is verified in a 0.25-μm BCD process.

Paper 5

Title: Ultra-low Power CMOS Image Sensor with Two-step Logical Shift Algorithm-based Correlated Double Sampling Scheme

Authors: Keunyeol Park, Jee Hun Yeom, and Soo Youn Kim

Institutes: Department of semiconductor science, Dongguk University, Seoul, South Korea

Abstract: This paper presents an ultra-low power counter structure for a column-parallel single-slope analog-to-digital converter (SS-ADC) in CMOS image sensors. The proposed counter employs a two-step logical shift algorithm-based correlated double sampling (CDS) scheme. The logical shift algorithm can reduce parasitic capacitances, driving frequency, and inner toggling nodes by using the minimum number of transistors and a single-direction counter structure. Moreover, the two-step counting and double data rate scheme in the LSB counter can halve the operating clock frequency, resulting in further decreased power consumption. A prototype sensor was fabricated using a 110 nm CMOS image sensor process. The measurement results show that the proposed SS-ADC with two-step counter consumes 2.2 μW power per column and shows a differential nonlinearity of +0.38/ −0.25 LSB and an integral nonlinearity of +0.75/ −0.5 LSB. The total power consumption is 2.25 mW for 640 × 480 effective image resolution at 60 frame rates with 3.3 V/1.5 V supply voltage.

Paper 6

Title: A Supervised Speech Enhancement Method for Smartphone-Based Binaural Hearing Aids

Authors: Zhuoyi Sun, Yingdan Li, Hanjun Jiang, Fei Chen, Xiang Xie and Zhihua Wang

Institutes: Beijing Innovation Center for Future Chips and Department of Microelectronics and Nanoelectronics, Tsinghua University, Beijing, China; Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, School of Microelectronics, Tianjin University, Tianjin, China; Tsinghua Shenzhen International Graduate School, Shenzhen, Guangdong, China

Abstract: It is essential but quite challenging to alleviate speech information loss and distortion while developing the speech processing algorithms in hearing aids. Recently, many speech enhancement methods based on deep learning are proven effective. However, most of the algorithms fail to achieve real-time processing, which is significant for hearing aids, especially for a smartphone-centered binaural hearing aid system. A supervised speech enhancement method based on an RNN structure is proposed to address the real-time problem. The problem is explored as a resource-constrained speech intelligibility improvement problem with the target of improving speech intelligibility at low SNR situations. Both the objective and subjective experimental results, using the standard evaluation metrics and the experiments on volunteers, respectively, have verified the superiority of the proposed method.

Session 13-A: Power Management 1

Room: Zoom Room A

Paper 1

Title: 83.9% Efficiency 100-mV Self-Startup Boost Converter for Thermoelectric Energy Harvester in IoT Applications

Authors: Zhongxia Shang, Yang Zhao, Wei Gou, Li Geng, and Yong Lian

Institutes: Department of Electrical Engineering and Computer Science, York University, Toronto, Canada; Microelectronics Department, Xi'an Jiaotong University, Xi'an, China

Abstract: This paper presents a boost converter with high efficiency for thermo-electrical energy generator (TEG). An on-time calibration based pulse skipping modulation (OTC-PSM) scheme is proposed to reduce the power of the controller. A hardware-efficient maximum power point tracking (MPPT) circuit is introduced for the constant internal resistance source of TEG. The proposed design has been implemented in a standard 180 nm CMOS process, achieving a high efficiency of 83.9% at 120mV input voltage and output power of 600 μW. The proposed OTC-PSM scheme saves considerable power in achieving high efficiency as well as low output ripple. Also, the proposed MPPT is simple and easy to implement for low cost.

Paper 2

Title: Resistance Compression Dual-band Differential CMOS RF Energy Harvester under Modulated Signal Excitation

Authors: Nagaveni S, Pramod Kaddi, Ashwini Khandekar, and Ashudeb Dutta
Institutes: Department of Electrical Engineering, Indian Institute of Technology, Hyderabad, India; Samsung Semiconductor India Research and Development center, Bangalore, India; Intel India Pvt. Ltd, Bangalore, India

Abstract: This paper proposes a resistance compression dualband differential CMOS RF energy harvester for harvesting power at dual frequencies. The use of resistance compression dual-band matching network minimizes the sensitivity of the RFDC converter for the variation in the input power and the rectifier load. The proposed system can work at 914 MHz and 2.4 GHz for arbitrary complex impedance simultaneously. The design is fabricated in a standard CMOS 0.18 μm technology and provides a regulated output voltage of 1 V. The cumulative efficiency in the presence of two frequencies shows an improvement of 14.2% with concern to single frequency (914 MHz at -14 dBm). Also maintains the efficiency of >20% for the input power range of -16 ~ 0 dBm. Also studied and analysed the implication of Wi-Fi bandwidth (72 MHz), OFDM modulation, and 64- QAM modulation on the efficiency and sensitivity of the system concerning continuous input signal. Observed the improvement in the efficiency with the peak-to-average power ratio.

Paper 3

Title: A 115x Conversion-Ratio Thermoelectric Energy-Harvesting Battery Charger for the Internet of Things

Authors: Ming-Jie Chung, Tetsuya Hirose, Takahito Ono and Po-Hung Chen
Institutes: National Chiao Tung University, Hsinchu, Taiwan; Osaka University, Osaka, Japan; Tohoku University, Sendai, Japan

Abstract: This paper presents a high-conversion-ratio (HCR), high-voltage-tolerant (HVT) energy-harvesting battery charger using 0.18-μm standard CMOS for Internet of Things (IoT). To reduce conversion ratio (CR) of inductive power converter and optimize overall power efficiency, the proposed charger cascades a boost converter and reconfigurable charge pump. Different from the high-voltage device, the standard CMOS process has lower parasitic capacitance and on-resistance; therefore, it can reduce switching and conduction loss. The reconfigurable charge pump dynamically changes the number of pumping stages according to the output voltage (VOUT) by automatic configuration selector (ACS). To manage the limited power from a thermoelectric generator (TEG), the converter works under the discontinuous conduction mode (DCM). The zero-current detector (ZCD) employs an analog comparator with digital offset compensator and digital comparator to control off-time (TOFF) quickly and accurately. The self-idle constant on-time (SI-COT) and idle mode both control the mechanism, helping to further reduce static power dissipation. As a result, the proposed converter can achieve peak efficiency of up to 76% at a 92× conversion ratio with output power ranging from 10 "9 to 1.9 mW. The available input voltage ranges are 40 to 400 mV, and the dual output voltage ranges are 1 to 1.6 V and 2 to 4.6 V for VBOOST and VOUT, respectively.

Paper 4

Title: Generic Wireless Power Transfer and Data Communication System Based on a Novel Modulation Technique

Authors: Aref Trigui, Mohamed Ali, Sami Hached, Jean-Pierre David, Ahmed Chiheb Ammari, Yvon Savaria and Mohamad Sawan

Institutes: Department of Electrical Engineering, Polytechnique Montreal, Montreal, QC Canada; Microelectronics Department, Electronics Research Institute, Cairo, Egypt; Electrical and Computer Engineering Department, College of Engineering, Sultan Qaboos University, Oman; CenBRAIN, School of Engineering, Westlake University and Westlake Institute for Advanced Study, Hangzhou, China.

Abstract: This paper presents a wireless power and downlink data transfer system for medical implants operating over a single 10 MHz inductive link. The system is based on a Carrier Width Modulation (CWM) scheme for high-speed communication and efficient power delivery using a novel modulator circuit design. Unlike conventional modulation techniques, the data rate of the proposed CWM is not limited by the quality factors of the primary and secondary coils. The functionality of the new modulation method is proven using a hybrid implementation comprising a custom-integrated demodulator circuit and boardlevel discrete components. The proposed Wireless Power and Data Transfer (WPDT) system is also capable of operating under a wide range of data rates. It allows a maximum data rate of 3:33 Mb=s for a maximum power delivery of 6:1 mW at 1 cm coils separation distance. The system can recover more power, reaching 55 mW at 100 kb=s. Due to the system genericity, an operator can select the best compromise between power and data rates in accordance to application or current need, without reconfiguring the receiver. Another advantage of this modulation technique is the simple implementation and the ultra-low power consumption of the CWM demodulator despite its high-speed demodulation.

Paper 5

Title: Digital Battery Management Unit with Built-In Resistance Compensation, Modulated Frequency Detection and Multi-Mode Protection for Fast, Efficient and Safe Charging

Authors: Ji-Xuan Li, Sai-Weng Sin, U-Fat Chio, Ya-Jie Wu, Chi-Seng Lam, and Rui P. Martins

Institutes: State Key Laboratory of Analog and Mixed-Signal VLSI & Institute of Microelectronics, University of Macau, Macau, China; Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao, China

Abstract: This paper presents a digital battery management unit (BMU) with built-in resistance (BIR) compensation, modulated frequency detection (MFD), and multi-mode protection (MMP) techniques to realize fast, efficient and safe charging. The charger incorporates the proposed BMU based on the low-dropout (LDO) regulator. With BIR compensation, a large rated current in the proposed pulsed constant current (PCC) mode charges the battery, and reduces the charging time by omitting the constantvoltage (CV) mode. The MFD technique allows continuous monitoring and obtains precise BIR compensation with accelerating sampling speed. The MMP technique can alleviate safety concerns while charging, including over-voltage protection (OVP), over-current protection (OCP), and the proposed accidental fluctuation protection (AFP). The digital BMU, implemented in 28 nm CMOS, occupies 0.014 of silicon area. $\mathbf{mm2}$ Experimental results show that the proposed circuit saves 73.3% of charging time with 1.5A charging current, and 21.5% ADC dynamic power with 1A charging current. For the digital controller IC, the power consumption is 59.1 μW.

Session 14-B: RF Transmitters
Room: Zoom Room B

Paper 1
Title: A 48 Gb/s PAM-4 Transmitter With 3-Tap FFE Based on Double-Shielded Coplanar Waveguide in 65-nm CMOS
Authors: Hyungrok Do, Jeongho Hwang, Hong-Seok Choi, Deog-Kyoon Jeong
Institutes: Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea; Inter-University Semiconductor Research Center, College of Engineering, Seoul National University, Seoul, South Korea
Abstract: A power and area-efficient pulse-amplitude modulation 4 (PAM-4) transmitter using 3-tap feed-forward equalizer (FFE) based on a slow-wave transmission line is presented. Passive delay line is adopted for generating equalizer tap to overcome the high clocking power consumption. The transmission line achieves high slow-wave factor of 15 with double floating metal shields around the differential coplanar waveguide. The physical dimensions of the transmission line are determined to have low loss and a high slow-wave factor with a small chip area by optimization with 3-D electromagnetic simulations. The transmitter includes 4:1 multiplexers (MUXs) and a quadrature clock generator for high-speed data generation in a quarter-rate system. The 4:1 MUX utilizes 2-UI pulse generator and the input configuration is determined by qualitative analysis. The chip is fabricated in 65-nm CMOS technology and occupies area of 0.151 mm2 . The proposed transmitter system exhibits the energy efficiency of 3.03 pJ/b at the data rate of 48 Gb/s with PAM-4 signaling.

Paper 2
Title: A 9Gb/s Wide Output Range Transmitter with 2D Binary-Segmented Driver and Dual-Loop Calibration for Intra-Panel Interfaces
Authors: Yong-Un Jeong, Jihwan Park, Mino Kim, Joo-Hyung Chae, Jaekwang Yun, Hyunjoong Lee and Suhwan Kim
Institutes: Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea; Inter-University Semiconductor Research Center (ISRC), Seoul National University, Seoul, South Korea; SK Hynix, Icheon 17336, South Korea
Abstract: This paper presents a 9Gb/s transmitter for intra-panel interfaces, with dual-loop calibration and a 2D binary-segmented driver. The dual-loop calibration during the training period compensates the transmitter output for the variations in operating conditions such as supply voltage and reference current. The 2D binary-segmented driver provides wide range and high resolution output characteristics, and independent adjustments for VOD, VCM and FFE strength while maintaining signal integrity. The transmitter reduces power consumption by optimizing the output for the channel. A prototype chip, fabricated in a 55nm CMOS process, occupies 0.057mm2. It provides FFE strength from 0dB to 26.4dB, common-mode voltage from 260mV to 690mV, and differential output voltage from 100mVppd to 1200mVppd, which varies by less than 4% across supply voltage and reference current variations. It also consumes 36mW at a data-rate of 9Gb/s with a 1.2V supply.

Paper 3

Title: Spur Minimization Techniques for Ultra-Low-Power Injection-Locked Transmitters

Authors: Chung-Ching Lin, Huan Hu, and Subhanshu Gupta
Institutes: Washington State University, Pullman, WA, USA

Abstract: Frequency multiplying wireless transmitters (TX) employing harmonic injection-locked technique benefit from high energy efficiency and less hardware complexity but largely suffer from reference spurs that violate the TX spectral specifications. This work proposes a self-aligned phase-locked loop (PLL) in conjunction with harmonic injection locking technique to achieve significantly improved spur performance under ultra-low-power (ULP) operations for sub-GHz IoT TXs. The on-chip type-I PLL calibrates the phase error in the ring oscillator (RO) in real-time and avoids large spurs induced from the frequency deviation in the harmonic injection locking. A compact zero power consumption twin-T notch filter for spur suppression is implemented within the PLL loop to tackle the rail-to-rail voltage jump that comes from the output of the phase detector (PD). Designed and fabricated in the TSMC 180 nm CMOS process, the proposed frequency multiplying TX occupies an active area of only 0.0413 mm2. The lowest power consumption with >3X improved energy-efficiency is observed while consistently achieving >62 dB spur suppression with -14 dBm output at 915 MHz. The TX supports OOK modulation with an average power consumption of 200.9 μW only at 3 Mb/s data rate achieving a normalized 66.97 pJ/bit energy efficiency.

Paper 4

Title: A U-Band PLL Using Implicit Distributed Resonators for Sub-THz Wireless Transceivers in 40 nm CMOS

Authors: Zipeng Chen, Wei Deng, Haikun Jia, Yibo Liu, Jianxi Wu, Pingda Guan, Jinyu Zhu, Luhong Mao, Zhihua Wang and Baoyong Chi
Institutes: Institute of Microelectronics, Tsinghua University, Beijing, China; School of Electrical and Information Engineering, Tianjin University, Tianjin, China.

Abstract: A U-band phase-locked loop (PLL) with implicit distributed resonators in the voltage-controlled oscillator (VCO) and injection-locked frequency divider (ILFD) using 40 nm CMOS is investigated in this paper. While LC-based, transformer-based, and distributed resonators are typically adopted for mm-wave and sub-terahertz applications, implicit distributed resonators are proposed to enhance the oscillation frequency of the VCO and expand the locking range of the ILFD. The operating principles and the characteristics of the proposed implicit distributed resonators are discussed for intuitive insight. The presented PLL occupies 0.53 mm2 core area and has 81.8 mW power consumption. The PLL achieves a measured frequency range of 8.15 GHz (16%) from 46.75 GHz to 54.9 GHz. The measured phase noise is -91.8 dBc/Hz at 1 MHz offset frequency from a carrier of 46.75 GHz. The proposed U-band PLL can provide a clear and stable local oscillation signal for the transceivers operating at mm-wave and sub-terahertz (sub-THz) frequency band.

Paper 5

Title: An Open Loop Digitally Controlled Hybrid Supply Modulator Achieving High Efficiency for Envelope Tracking with Baseband up to 200-MHz

Authors: Zeqiang Chen, Qin Xia, Li Dong, Shiquan Fan, Kefeng Han, Zhuoqi Guo, Zhongming Xue and Li Geng

Institutes: School of Microelectronics, Xi'an Jiaotong University, Xi'an, Shaanxi, P.R. China

Abstract: Envelope tracking (ET) is an effective way to improve the efficiency of power amplifier (PA) for 5G communication systems. To understand the restriction of the hybrid supply modulator (HSM) for ultra-wide band ET applications, an extended power loss model and a Short Time Fourier Transform (STFT) methodology are put forward to be the fundamental guide of the control methodology. An average voltage alignment (AVA) algorithm is proposed, which aligns the current waveforms by using pre-cached envelope signals to reduce the power loss due to the mismatch. Furthermore, a digital low pass filter (LPF) is integrated in the AVA controller, aiming at eliminating the necessity of very high-speed switches in HSM, which reduces the difficulty of hardware facility. The prototype chip is fabricated with a standard 0.18 μm CMOS technology and fulfilled with the discrete components on the PCB to verify the methodology and the system. Measurement results show that the proposed method extends the tracking bandwidth up to 200-MHz, and achieves 20% efficiency increment with the maximum 20 MHz switching frequency decrement comparing to the normal hysteresis comparison logic. The proposed strategy successfully push the HSM ET application to hundreds of MHz compared with the previous level of 10-MHz.

Session 15-C: Digital System & Accelerator III

Room: Zoom Room C

Paper 1

Title: An Energy-Efficient Dual-Field Elliptic Curve Cryptography Processor for Internet of Things Applications

Authors: Ling-Yu Yeh, Po-Jen Chen, Chen-Chun Pai, and Tsung-Te Liu

Institutes: Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan; MediaTek Inc., Hsinchu, Taiwan

Abstract: This brief presents an energy-efficient elliptic curve cryptography (ECC) processor for Internet of Things (IoT) security applications. The proposed processor supports dual-field computations, and employs various design techniques across the algorithm, architecture, and arithmetic circuit levels to minimize power and energy consumption. The proposed elliptic curve point multiplication (ECPM) algorithm employs signed binary representation (SBR) with the m-ary method to reduce both area and energy consumption, while avoiding attack from simple power analysis (SPA). In addition, the proposed hybrid modular arithmetic architecture effectively increases the hardware utilization to reduce both area and energy cost. Finally, the proposed processor uses an energy-efficient data flow to further minimize memory overhead for group operations. The proposed ECC processor achieves 51.6% and 50.5% lower energy consumption for each GF(p) and GF(2m) ECPM operation, respectively, when compared to state-of-the-art ECC designs. Index Terms—Elliptic curve cryptography (ECC), hardware security, low power, energy-efficient, dual field, side-channel attacks, Internet of Things (IoT).

Paper 2

Title: A Multi-class Objects Detection Coprocessor with Dual Feature Space and Weighted Softmax

Authors: Zhihua Xiao, Peng Xu, Xianglong Wang, Lei Chen and Fengwei An
Institutes: School of Microelectronics, Southern University of Science and Technology, China; Pengcheng Lab, Shenzhen, China; Technology and Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, Southern University of Science and Technology, China

Abstract: A critical mission for mobile robot vision is to detect and classify different objects with low power consumption. In this paper, we propose a multi-class object detection coprocessor using the combinational feature of the Histogram of Oriented Gradient (HOG) and Local Binary Pattern (LBP) together with weighted Softmax classifier. The architecture is compact and hardware-friendly since the cell-based feature extraction unit and block-level normalization reuse the SRAMs for storing one-row cell and one-row block. Meanwhile, the working frequency of the feature extraction and block-normalization unit is synchronized to the image sensor for low dynamic power. Furthermore, for satisfying the intrinsically feature of the hardware, an only-once sliding-detection-window (OOSDW) mechanism is developed for object detection and classification in different sizes. The classification result of our method with dual feature space and Softmax classifier outperforms 80% previous classical approaches in the Fashion MNIST dataset. The experimental result shows that the hardware-resource usage of the FPGA implementation, which is capable of 60 fps VGA video. It is similar or even less than that of previous work using only the HOG feature and single-class classifier.

Paper 3

Title: Always-On 674μW @ 6.2GOP/s Error Resilient Binary Neural Networks with Aggressive SRAM Voltage Scaling on a 22nm IoT End-Node

Authors: Alfio Di Mauro, Francesco Conti, Pasquale Davide Schiavone, Davide Rossi and Luca Benini
Institutes: Integrated Systems Laboratory, D-ITET, ETH Zurich, Zurich, Switzerland; Energy-Efficient Embedded Systems Laboratory, DEI, University of Bologna, Bologna, Italy

Abstract: Binary Neural Networks (BNNs) have been shown to be robust to random bit-level noise, making aggressive voltage scaling attractive as a power-saving technique for both logic and SRAMs. In this work, we introduce the first fully programmable IoT end-node system-on-chip (SoC) capable of executing software-defined, hardware-accelerated BNNs at ultralow voltage. Our SoC exploits a hybrid memory scheme where error-vulnerable SRAMs are complemented by reliable standardcell memories to safely store critical data under aggressive voltage scaling. On a prototype in 22nm FDX technology, we demonstrate that both the logic and SRAM voltage can be dropped to 0.5V without any accuracy penalty on a BNN trained for the CIFAR- 10 dataset, improving energy efficiency by 2.2X w.r.t. nominal conditions. Furthermore, we show that the supply voltage can be dropped to 0.42V (50% of nominal) while keeping more than 99% of the nominal accuracy (with a bit error rate ∼1/1000). In this operating point, our prototype performs 4Gop/s (15.4 Inference/s on the CIFAR-10 dataset) by computing up to 13 binary ops per pJ, achieving 22.8 Inference/s/mW while keeping within a peak power envelope of 674uW – low enough to enable always-on operation in ultra-low power smart cameras, longlifetime environmental sensors, and insect-sized pico-drones.

Paper 4

Title: A Partially Binarized Hybrid Neural Network System for Low-power and Resource Constrained Human Activity Recognition

Authors: Antonio De Vita, Alessandro Russo, Danilo Pau, Luigi Di Benedetto, Alfredo Rubino, and Gian Domenico Licciardo

Institutes: Department of Industrial Engineering of the University of Salerno, Fisciano (SA), Italy; System Research and Applications, STMicroelectronics, Agrate Brianza (MB), Italy

Abstract: A custom Human Activity Recognition system is presented based on the resource-constrained Hardware (HW) implementation of a new partially binarized Hybrid Neural Network. The system processes data in real-time from a single triaxial accelerometer, and is able to classify between 5 different human activities with an accuracy of 97.5% when the Output Data Rate of the sensor is set to 25 Hz. The new Hybrid Neural Network (HNN) has binary weights (i.e. constrained to +1 or −1) but uses non-binarized activations for some layers. This, in conjunction with a custom pre-processing module, achieves much higher accuracy than Binarized Neural Network. During pre-processing, the measurements are made independent from the spatial orientation of the sensor by exploiting a reference frame transformation. A prototype has been realized in a Xilinx Artix 7 FPGA, and synthesis results have been obtained with TSMC CMOS 65 nm LP HVT and 90 nm standard cells. Best result shows a power consumption of 6.3 μW and an area occupation of 0.2 mm2 when real-time operations are set, enabling in this way, the possibility to integrate the entire HW accelerator in the auxiliary circuitry that normally equips inertial Micro Electro-Mechanical Systems (MEMS).

Session 16-A: Power Management II

Room: Zoom Room A

Paper 1

Title: A 100 MHz, 0.8-to-1.1 V, 170 mA Digital LDO with 8-Cycles Mean Settling Time and 9-Bit Regulating Resolution in 180-nm CMOS

Authors: Zheyi Yuan, Shiquan Fan,Chenxi Yuan, and Li Geng

Institutes: School of Microelectronics, Xi’an Jiaotong University, Xi’an, Shaanxi, P.R. China

Abstract: This paper presents an all-digital low dropout regulator (DLDO) with high regulating resolution and fast transient tracking by combining novel interval-searching algorithm and recover acceleration techniques. By bringing forth an enhanced interval-searching algorithm (ISA) with 9-bit register regulating precision, the output can be stabilized within 8 cycles when the load changes. A recover acceleration (RA) technique is proposed to improve the transient response and stability. The DLDO is fabricated with standard 180-nm CMOS process. The proposed DLDO needs 390 pF output capacitance and can provide as much as 170 mA load current. The measured load regulation is 0.11 mV/mA at 0.9 V output with 160 mA load current range. The maximum current efficiency is up to 99.71%. The two FOMs of 2.03 ps and 0.362 pF are also achieved to illustrate the merits of this design.

Paper 2

Title: A Fully Integrated High-Power-Supply-Rejection Linear Regulator with an Output-Supplied Voltage Reference

Authors: Yan-Peng Chen and Kea-Tiong Tang
Institutes: Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan

Abstract: This study proposes an output capacitorless linear regulator with a high power supply rejection (PSR) ratio for a wireless power transmission system. To achieve high PSR performance toward a noisy input voltage, a fully-integrated voltage reference circuit supplied by the output voltage is used. The reference circuit that is supplied directly by Vout can isolate the reference voltage from the noisy input voltage, thereby reducing the requirement of the conventional bulky low-pass filter and achieving superior PSR performance. In addition, the regulator uses an N-type pass transistor and a dual-feedback structure to achieve a wideband ripple-filtering ability and a fast transient response. The proposed regulator is fabricated using commercial TSMC 0.18-μm CMOS technology, and occupies an area of 0.1054 mm2 including reference circuit. The proposed regulator supplies biomedical implants 10mA load current at 1.1V output voltage. The regulator achieved a PSR performance of −48 and −56 dB against the input and charge pump at 10 MHz, respectively. The unity gain bandwidth (UGB) of the regulator was 291MHz while consuming a total quiescent current of 276μA.

Paper 3

Title: An NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28-nm CMOS

Authors: Xiaofei Ma, Yan Lu, Qiang Li, Wing-Hung Ki, and Rui P. Martins
Institutes: Institute of Integrated Circuits and Systems, University of Electronic Science and Technology of China, Chengdu, China; State Key Laboratory of Analog and Mixed-Signal VLSI and FST-DECE, University of Macau, Macao, China; Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

Abstract: This paper presents an NMOS digital low-dropout regulator (LDO) with fast transient response and ultra-low quiescent current, to provide a tunable power supply for nearthreshold voltage computing circuits in internet-of-things (IoT) devices. An LDO with an NMOS power transistor can enjoy the intrinsic fast transient response of the source-follower-like power stage, contributing to the proportional (P) part of the control loop. A shift-register-based digital control serves as an excellent candidate for the integral (I) part of the control loop. In addition, we propose a NAND-gate-based high-pass analog path (NAP) as the derivative (D) part of the loop, making the whole control scheme a complete PID control, therefore, achieving a fast transient response. We fabricated two versions of the prototype chip, one with a 30-pF on-chip load capacitor and a fast-transient on-chip load, and the other with no load capacitor, in 28-nm CMOS. The proposed NMOS digital LDO with NAP can handle the load transient of 160 mA/ns with 810-nA quiescent current, achieving 117-mV voltage undershoot. With the proposed techniques, we can achieve nearly two orders of better FoM when comparing it to the state-of-the-art works.

Paper 4

Title: LDO with Improved Common Gate Class AB OTA Handles any Load Capacitors and Provides Fast Response to Load Transients

Authors: Cristian Răducan, Alina-Teodora Grăjdeanu, Cosmin-Sorin Plesa, Marius Neag, Andrei Negoiță, Marina Țopa

Institutes: Technical University of Cluj-Napoca, Romania; Infineon Technologies, Bucharest, Romania

Abstract: This paper proposes an LDO with fast response to load transients that can handle any practical capacitive loads. These features are mainly due to a novel frequency compensation circuit tailored for its error amplifier, which is based on an improved version of the popular common gate amplifier. A simple yet effective approach to the small-signal analysis of LDO with multiple feedback loops is employed to analyse intuitively the LDO and derive key design constraints. Simulation and measurement results performed on a test chip implemented in standard 130nm CMOS process validated the proposed LDO. It requires only 0.7µA quiescent current but exhibits an excellent response to load transients: when the load current jumps from 0A to 100mA in 1µs the output voltage presents an undershoot of 76mV and an overshoot of 198mV, without decoupling capacitors. It compares well against seven LDOs designed with common gate error amplifiers for similar levels of supply voltage, output voltage and current and against seven fast LDOs employing different error amplifiers. A figure-of-merit that considers the quiescent current, the maximum load current and capacitance, as well as the output voltage deviation, yielded a value for our LDO 39.8 times better than for the nearer competitor that employs common gate amplifier and 6 times better than the one employing a different error amplifier. When considering edge time and process scaling the performance of the proposed LDO is 4.8, respectively 4.5, times better than the second best in both comparisons.

Paper 5

Title: A Low-Profile High-Efficiency Fast Battery Charger with Unifiable Constant-Current and Constant-Voltage Regulation

Authors: Yong Qu,Wei Shu, Lei Qiu, Yen-Cheng Kuan, Shiuh-hua Wood Chiang, and Joseph S. Chang

Institutes: Zero-Error Systems, Singapore; College of Electronical Information and Engineering, Tongji University, Shanghai, China; International College of Semiconductor Technology, National Chiao Tung University, Hsinchu, Taiwan; Department of Electrical and Computer Engineering, Brigham Young University, Provo, UT, USA; School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore

Abstract: Present universal serial bus (USB) battery chargers often suffer from limitations to meet the increasing demand for quick charging due to compromised power efficiency and complicated hardware implementation. In this paper, we propose a charge unifiable (QU) control scheme that enables a battery charger to improve power efficiency in a low-profile hardware manner. This scheme features fully soft-switching (vis-à-vis hard switching) and single control scheme (vis-à-vis multiple) for distinct constant current (CC) and constant voltage (CV) charging modes. To the best of authors' knowledge, the proposed QU control scheme is the first to simultaneously offer fully softswitching, innate CC-and-CV regulation, and seamless CC-to-CV transition. To verify the proposed design, we monolithically realize a low-profile high-efficiency fast battery charger based on this scheme. The prototype embodying a tiny 470-nH output inductor supports a maximum input voltage of 16V, output voltage of 2.2-4.2 V, output current of 0.1-2 A, and peak power efficiency of 96.2%. When benchmarked against state-of-the-art counterparts, the proposed charger features at least 2.1× smaller inductor and 7.2% higher power efficiency at both the maximum and the minimum output power charging scenarios. Further, this charger is the only design that features ≥91% power efficiency in the whole load range.

Paper 6

Title: Fully-Integrated Reconfigurable Charge Pump with TwoDimensional Frequency Modulation for Self-Powered Internet-of-Things Applications

Authors: Hao-Chung Cheng, Wen-Tuan Tsai, Po-Han Chen and Po-Hung Chen
Institutes: National Chiao Tung University, Hsinchu, Taiwan

Abstract: In this paper, we propose a fully-integrated reconfigurable charge pump in a 0.18-μm CMOS process; this converter is applicable for self-powered Internet-of-Things applications. The proposed charge pump uses a two-dimensional frequency modulation technique, which combines both the pulsefrequency modulation (PFM) and pulse-skip modulation (PSM) techniques. The PFM technique adjusts the operating frequency of the converter according to the variations in the load current, and the PSM technique regulates the output voltage. The proposed two-dimensional frequency modulation technique can improve the overall power conversion efficiency and the response time of the converter under light load conditions. A photovoltaic cell was chosen as the input source of the proposed converter. To adapt to the variations in the output voltage of a photovoltaic cell under different light illumination intensities, we built a reconfigurable converter core with multiple power conversion ratios of 2, 2.5, and 3 for the regulated output voltage of 1.2 V when the input voltage ranged from 0.53 V to 0.7 V. Our measurement results prove that the proposed capacitive power converter could achieve a peak power conversion efficiency of 80.8%, and the efficiency was more than 70% for the load current that ranged from 10 μA to 620 μA.

Session 18-C: Sensors 2

Room: Zoom Room C

Paper 1

Title: A Noise-reduced Light-to-frequency Converter for Sub-0.1% Perfusion Index Blood SpO2 Sensing

Authors: Fang Tang, Zhipeng Li, Tongbei Yang, Lai Zhang, Xichuan Zhou, Shengdong Hu, Zhi Lin, Ping Li, Bo Wang, Amine Bermak
Institutes: Chongqing Engineering Laboratory of High Performance Integrated Circuits, School of Microelectronics and Communication Engineering, Chongqing University (CQU), China; Guangdong Biolight Meditech Co., Ltd.; College of Science and Engineering, Hamad Bin Khalifa University, Qatar.

Abstract: To improve the SpO$_2$ sensing system performance for hypoperfusion (low perfusion index) applications, this paper proposes a low-noise light-to-frequency converter scheme from two aspects. First, a low-noise photocurrent buffer is proposed by reducing the amplifier noise floor with a transconductance-boost (g$\rm{_m}$-boost) circuit structure. Second, a digital processing unit of pulse-frequency-duty-cycle modulation is proposed to minimize the quantization noise in the following timer by limiting the maximum output frequency. The proposed light-to-frequency sensor chip is designed and fabricated with a 0.35-μm CMOS process. The overall chip area is 1$\times$0.9 mm^2 and the typical total current consumption is about 1.8 mA from a 3.3-V power supply at room temperature. The measurement results prove the proposed functionality of output pulse duty cycle modulation, while the SNR of a typical 10-kHz output frequency is 59 dB with about 9-dB improvement when compared with the conventional design. In-system experimental results show that the minimum measurable PI using the proposed blood SpO$_2$ sensor could be as low as 0.06\% with 2-percentage-point error of SpO$_2$. The proposed chip is suitable for portable low-power high-performance blood oximeter devices especially for hypoperfusion applications.

Paper 2

Title: Design of Dual-Mode Stimulus Chip with Built-In High Voltage Generator for Biomedical Applications

Authors: Ting-Yang Yen and Ming-Dou Ker
Institutes: Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

Abstract: A dual-mode stimulus chip with a built-in high voltage generator was proposed to offer a broad-range current or voltage stimulus patterns for biomedical applications. With an on-chip built-in high voltage generator, this stimulus chip could generate the required high voltage supply without additional supply voltage. With a nearly 20 V operating voltage, the overstress and reliability issues of the stimulus circuits were thoroughly considered and carefully addressed in this work. This stimulus system only requires an area of 0.22 mm2 per single channel and is fully on-chip implemented without any additional external components. The dual-mode stimulus chip was fabricated in a 0.25-μm 2.5V/5V/12V CMOS (complementary metal-oxide-semiconductor) process, which can generate the biphasic current or voltage stimulus pulses. The current level of stimulus is up to 5 mA, and the voltage level of stimulus can be up to 10 V. Moreover, this chip has been successfully applied to stimulate a guinea pig in an animal experiment. The proposed dual-mode stimulus system has been verified in electrical tests and also demonstrated its stimulation function in animal experiments.

Paper 3

Title: Low Power Optimisations for IoT Wearable Sensors Based on Evaluation of Nine QRS Detection Algorithms

Authors: Jiamin Li, Adnan Ashraf, Barry Cardiff, Rajesh C Panicker, Yong Lian, and Deepu John
Institutes: Department of Electrical and Computer Engineering, National University Singapore, Singapore; School of Electrical and Electronic Engineering, University College Dublin, Ireland; Department of Electrical Engineering & Computer Science, Lassonde School of Engineering, York University, Toronto, Canada

Abstract: This paper aims to reduce the power consumption of electrocardiography based wearable healthcare devices, by introducing power reduction approaches and considerations at system level design, where we have the highest potential to influence power. It focuses, in particular, on algorithm design and implementation, data acquisition, and transmission under constrained resources. A thorough investigation of the suitability of nine existing algorithms for on-sensor QRS feature detection is conducted, with respect to metrics such as sensitivity, positive predictivity, power consumption, parameter choice and time delay. Optimization of data acquisition on CPU-based IoT systems is performed, and the current consumption is reduced by thrice using a combination of direct memory access (DMA) list approach and low-level register manipulations for task delegation. The acquisition data rate, sampling rate, buffer and batch size are also optimised. To reduce the power consumption by data transmission, the effect of on-sensor versus off-sensor processing is investigated. While focusing on the CPU-based system with experiments performed on a generic low-power wearable platform, the design optimization and considerations proposed in this work could extend to custom designs and allow further investigation into QRS detection algorithm optimization for wearable devices.

Paper 4

Title: Ultrasensitive Magnetoelectric Sensing System for pico-Tesla MagnetoMyoGraphy

Authors: Siming Zuo, Julius Schmalz, Mesut-Ömür Özden, Martina Gerken, Jingxiang Su, Florian Niekiel, Fabian Lofink, Kianoush Nazarpour and Hadi Heidari

Institutes: Microelectronics Lab, James Watt School of Engineering, University of Glasgow, UK; Institute of Electrical Engineering and Information Technology, Kiel University, Kiel, Germany; Fraunhofer Institute for Silicon Technology ISIT, Fraunhoferstr, Itzehoe, Germany; School of Engineering and Biosciences Research Institute, Newcastle University, Newcastle

Abstract: MagnetoMyoGraphy (MMG) with superconducting quantum interference devices (SQUIDs) enabled the measurement of very weak magnetic fields (femto to pico Tesla) generated from the human skeletal muscles during contraction. However, SQUIDs are bulky, costly and require working in a temperature-controlled environment, limiting wide-spread clinical use. We introduce a low-profile magnetoelectric (ME) sensor with analog frontend circuitry that has sensitivity to measure pico-Tesla MMG signals at room temperature. It comprises magnetostrictive and piezoelectric materials, FeCoSiB/AlN. Accurate device modelling and simulation are presented to predict device fabrication process comprehensively using the finite element method (FEM) in COMSOL Multiphysics®. The fabricated ME chip with its readout circuit was characterized under a dynamic geomagnetic field cancellation technique. The ME sensor experiment validate a very linear response with high sensitivities of up to 378 V/T driven at a resonance frequency of fres = 7.76 kHz. Measurements show the sensor limit of detections of down to 175 pT/√Hz at resonance, which is in the range of MMG signals. Such a small-scale sensor has the potential to monitor chronic movement disorders and improve the end-user acceptance of human-machine interfaces.

Paper 5

Title: Time Stamp – A Novel Time-to-Digital Demodulation Method for Bioimpedance Implant Applications

Authors: Yu Wu, Dai Jiang, Maryam Habibollahi, Noora Almarri, and Andreas Demosthenous

Institutes: Department of Electronic and Electrical Engineering, University College London, Torrington Place,London, U.K.

Abstract: Bioimpedance analysis is a non-invasive and inexpensive technology to investigate the electrical properties of biological tissues. The analysis requires demodulation to extract the real and imaginary parts of the impedance. Conventional systems use complex architectures such as I-Q demodulation. In this paper, a very simple alternative time-to-digital demodulation method or 'time stamp' is proposed. It employs only three comparators to identify or stamp in the time domain, the crossing points of the excitation signal and the measured signal. In a CMOS proof of concept design, the accuracy of impedance magnitude and phase is 97.06% and 98.81% respectively over a bandwidth of 10 kHz to 500 kHz. The effect of fractional-N synthesis is analysed for the counter-based zero crossing phase detector obtaining a finer phase resolution (0.51˚ at 500 kHz) using a counter clock frequency ($\boldsymbol{fclk}$ = 12.5 MHz). Because of its circuit simplicity and ease of transmitting the time stamps, the method is very suited to implantable devices requiring low area and power consumption.

Paper 6

Title: Long-Term Bowel Sound Monitoring and Segmentation by Wearable Devices and Convolutional Neural Networks

Authors: Kang Zhao, Hanjun Jiang, Zhihua Wang, Ping Chen, Binjie Zhu, Xianglong Duan
Institutes: Institute of Microelectronics (IME), Tsinghua University; Tsinghua National Laboratory for Information Science and Technology, China

Abstract: Bowel sounds (BSs), typically generated by the intestinal peristalses, are a significant physiological indicator of the digestive system's health condition. Recent progress in computerized BS analysis suggests that long-term BS monitoring provides a promising way of understanding the gastrointestinal status. However, long-term BS monitoring also brings several challenges. On the one hand, unlike the short-term abdominal auscultation, in the long-term monitoring, subjects cannot be immobilized all the time. Generally, they are allowed to behave freely within a specified room. In this sense, the wired electronic stethoscopes are not user-friendly. On the other hand, long-term BS monitoring generates massive data. How to pick the BS events-contained segments while ignoring those segments that only include background noises is challenging. In this study, a wearable BS monitoring system is presented. The system features a wearable BS sensor that can record BSs for days long and transmit them wirelessly in real-time. With the system, a total of 20 subjects' BS data under the hospital environment were collected. Each subject is recorded for 24 hours. Through manual screening and annotation, from every subject's BS data, 400 segments were extracted, in which half are BS event-contained segments. Thus, a BS dataset that contains 20 × 400 sound segments is formed. Afterward, CNNs are introduced for BS segment recognition. Specifically, this study proposes a novel CNN design method that makes it possible to transfer the popular CNN modules in image recognition into the BS segmentation domain. Experimental results show that in holdout evaluation with corrected labels, the designed CNN model achieves a moderate accuracy of 91.8% and the highest sensitivity of 97.0% compared with the similar works. In cross validation with noisy labels, the designed CNN delivers the best generability. By using a CNN visualizing technique—class activation maps, it is found that the designed CNN has learned the effective features of BS events. Finally, the proposed CNN design method is scalable to different sizes of datasets.