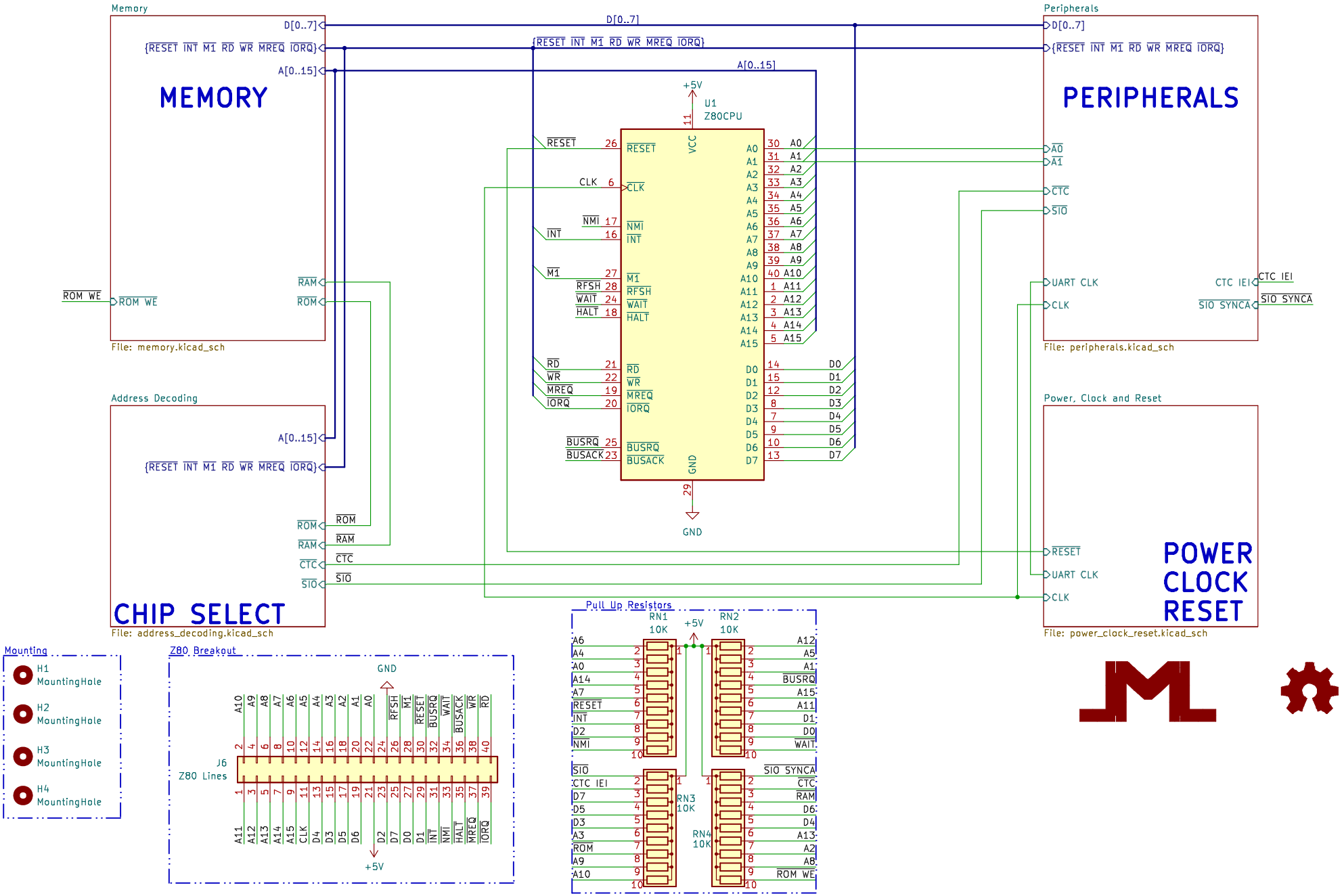
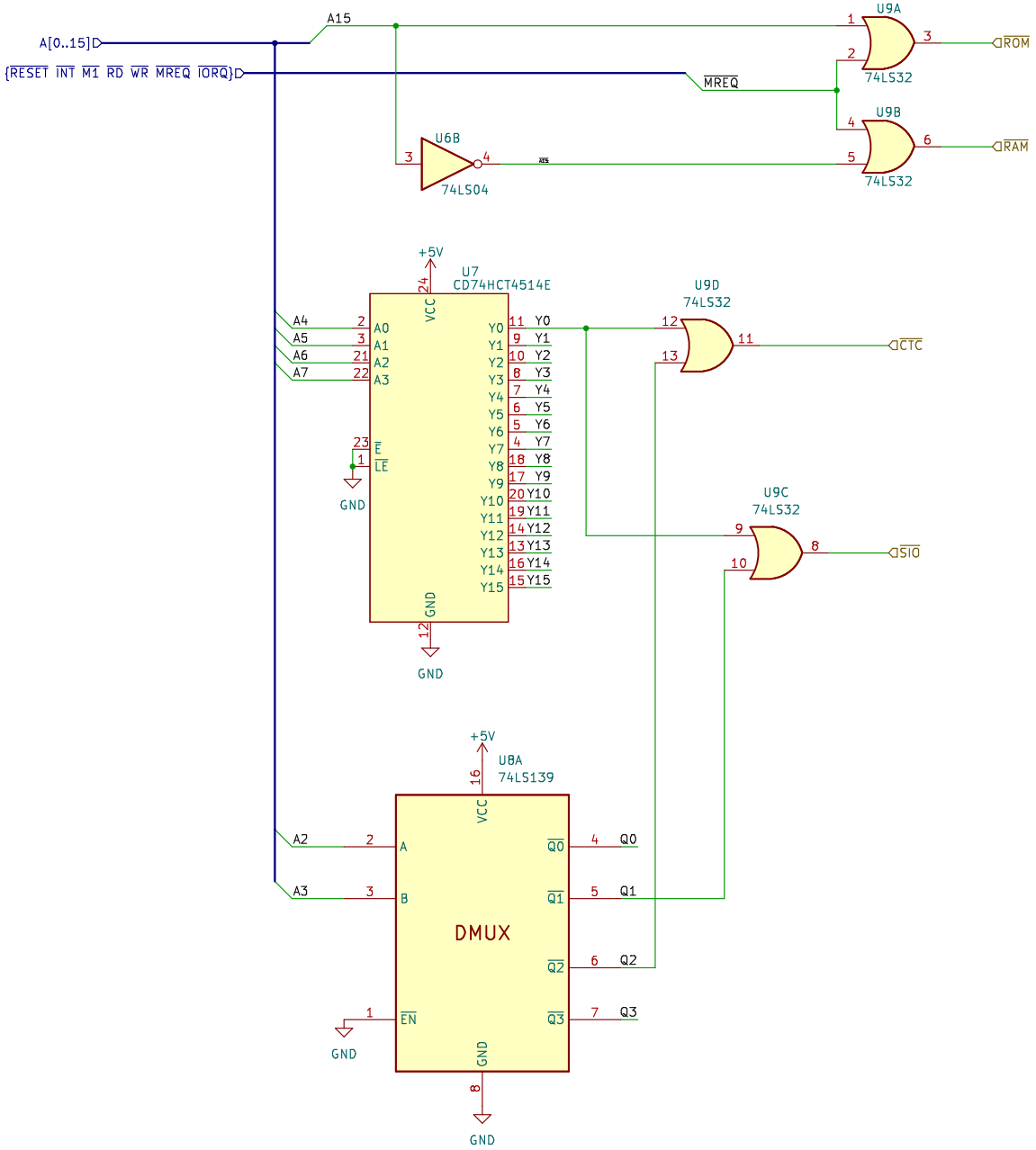
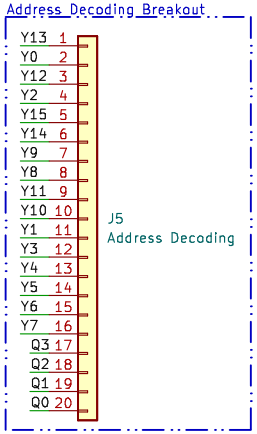
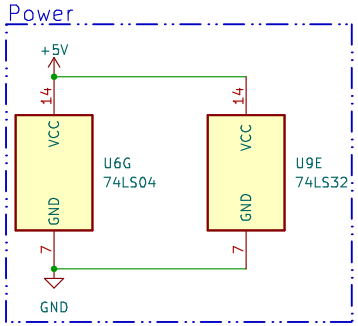
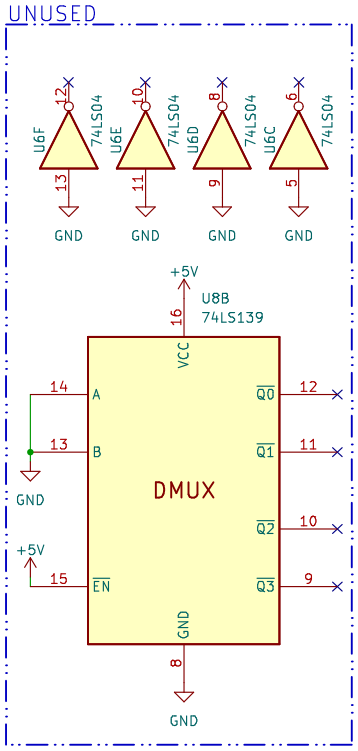

Memory
D[0..7]
{RESET INT M1 RD WR MREQ IORQ}
A[0..15]
MEMORY
ROM WE
RAM
ROM
File: memory.kicad_sch
Address Decoding
A[0..15]
{RESET INT M1 RD WR MREQ IORQ}
ROM
RAM
CTC
SIO
CHIP SELECT
File: address_decoding.kicad_sch
D[0..7]
{RESET INT M1 RD WR MREQ IORQ}
A[0..15]
+5V
U1
Z80CPU
VCC
GND
RESET
CLK
NMI
INT
M1
RFSH
WAIT
HALT
RD
WR
MREQ
IORQ
BUSRQ
BUSACK
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
Peripherals
D[0..7]
{RESET INT M1 RD WR MREQ IORQ}
PERIPHERALS
A0
A1
CTC
SIO
UART CLK
CLK
CTC IEI
SIO SYNCA
File: peripherals.kicad_sch
Power, Clock and Reset
RESET
UART CLK
CLK
POWER
CLOCK
RESET
File: power_clock_reset.kicad_sch
Mounting
H1
MountingHole
H2
MountingHole
H3
MountingHole
H4
MountingHole
Z80 Breakout
GND
+5V
J6
Z80 Lines
Pull Up Resistors
RN1
10K
RN2
10K
RN3
10K
RN4
10K
+5V

CHIP SELECTION LOGIC

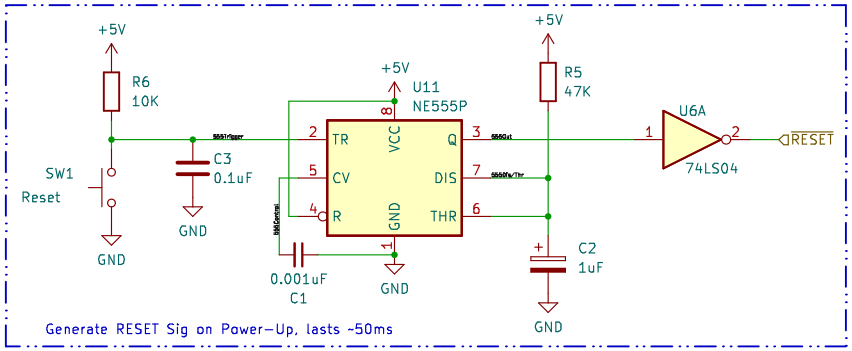




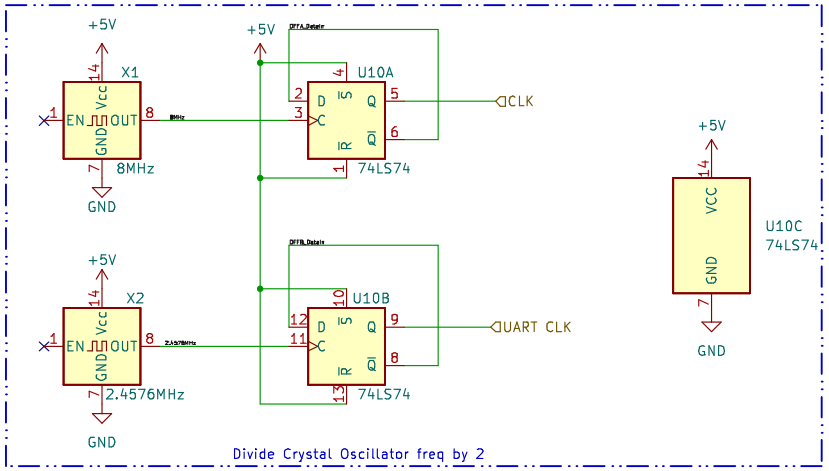




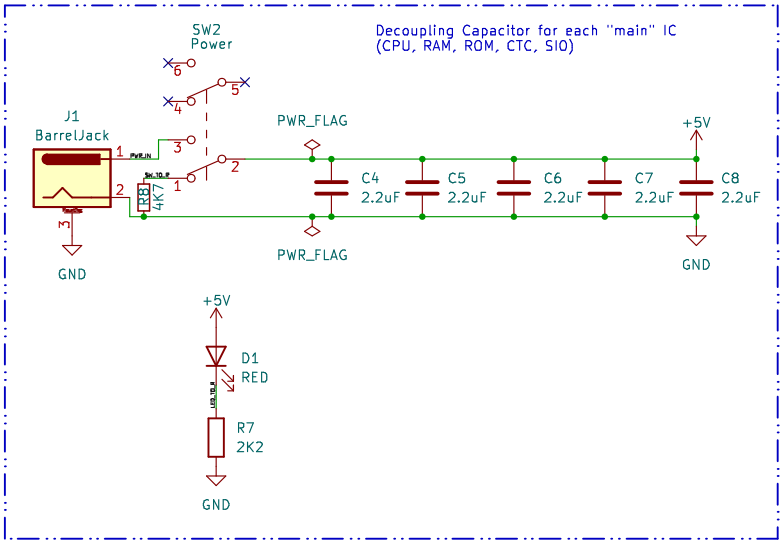
RESET

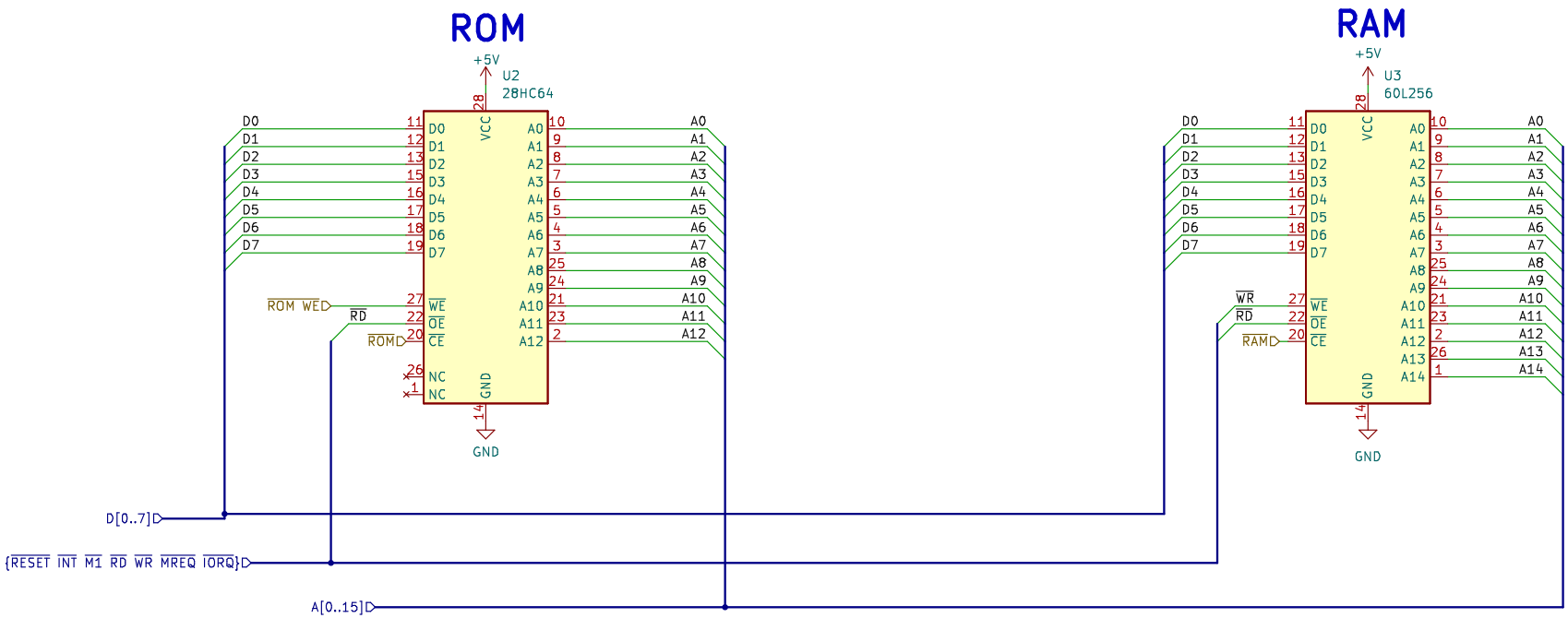


CLOCK



POWER




ROM
+5V
U2
28HC64
D0
D1
D2
D3
D4
D5
D6
D7
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
ROM WE
RD
ROM
NC
NC
GND
RAM
U3
60L256
WR
RAM
D[0..7]
{RESET INT M1 RD WR MREQ IORQ}
A[0..15]

PERIPHERALS