TCES 330: Digital System Design
Course Syllabus, Spring 2018

Instructor: Jie Sheng, Ph.D.
Office: CP 228
Phone: 253-692-4576
Email: shengj2@uw.edu
Office Hours: M&W&F 9:00 to 10:00; or by appointment

Lecture: M & W 10:15-12:20, in ADMC BHS106
Lab: M & W 1:30-3:35; F 10:00-12:05, in CP 206D

I Credit

This is a 5-credit course. There are approximately four hours of lecture and discussion and 2 hours of lab per week.

II Course Description, Objectives, and Outcomes

Description:

Digital system design fundamentals and techniques using programmable logic devices (PLDs). Use SystemVerilog to analyze and design complex digital systems based on field programmable gate arrays (FPGAs). Introduce testing techniques used to verify design and operation of digital systems. Laboratory required.

Prerequisite: TCES 230, TCES 312

Objectives:

- Teach students how to design digital systems using Verilog;
- Introduce students to programmable logic devices;
- Teach students the fundamentals of MOS semiconductor technology;
- Explain students how to use PLDs to implement combinational circuits ;
- Explain students how to use PLDs to implement sequential circuits;
- Teach students how to implement digital systems using PLD; and
- Teach students how to test digital systems.

Outcomes:

At the completion of the class the students shall be able to:

- specify digital circuits using a hardware description language
- simulate the operation of digital circuits using appropriate simulation tools
- verify the correct operation of digital systems
- create reusable modules using a hardware description language
- design state machines using a hardware description language
- implement digital design using programmable logic devices
- verify correct operation of digital systems using laboratory equipment

III Course Topics and Schedule (tentative)

Date	Topics
Week 1	• Introduction, expectations • Introduction to HDLs, • Introduction to Altera software, DE2-115 boards • SystemVerilog basics • Testing SystemVerilog modules
Week 2	• More SystemVerilog constructs • Combinational circuits using SystemVerilog • Vectors • Behavioral SystemVerilog • Arithmetic circuits using Verilog
Week 3	• Procedures • Programming Constructs • Introduction to sequential circuits in SystemVerilog
Week 4	• Flip-flops and registers in SystemVerilog • Registers
Week 5	• Finite State Machines (FSM) using SystemVerilog
Week 6	• CMOS basics • FPGA Implementations • Midterm
Week 7	• Datapath elements • Controlling Datapath with FSMs
Week 8	• Programmable Processors on FPGAs
Week 9	• Programmable Processors, cont. • Program Assembly
Week 10	• Memorial Day observed • Review

IV Course Resources

Required Textbooks

- ***Fundamentals of Digital Logic with Verilog Design, Third Ed.,*** Stephen Brown and Zvonko Vranesic, McGraw-Hill.
- ***Sutherland HDL - Verilog 2001 Online Reference Guide***, (Free pdf Download) (http://www.sutherland-hdl.com/pdfs/verilog_2001_ref_guide.pdf).
- http://svref.renerta.com/
- http://chris.spear.net/systemverilog/

Additional References You May Find Helpful

- ***Digital Design with RTL Design, VHDL, and Verilog, Second Ed.*** Frank Vahid, Wiley 2010 (textbook used in the past).
- ***Verilog for Digital Design***, Vahid and Lysecky (textbook used in the past).
- ***Logic Design and Verification Using SystemVerilog***, Donald Thomas, CreateSpace, an amazon.com company 2016 (a good general SystemVerilog reference).
- ***System Verilog for Verification,*** Chris Spear and Greg Tumbush, Springer 2012 (covers testing techniques and making testbenches using SystemVerilog).
- ***Microelectronic Circuits,*** Sedra and Smith, Oxford (a good electronics reference).
- ***Circuit Design with VHDL,*** Volnei A. Pedroni, MIT Press, 2010 (a good text to learn VHDL once you know Verilog).

Software

- ***Quartus Prime Web Edition, Version 17.0*** **(Required, Free Download)** Altera Corporation. Note: This is NOT the latest version of Quartus, but it is consistent with what's installed in our lab. We have some disks with this software on it you can install, or you can download it from Altera. Just make sure you get the correct version.
- ***ModelSim-Altera Edition for Quartus 17.0*** **(Required, Free Download),** Altera Corporation.
- ***NIOS II Embedded Design Suite (Optional, Free Download)***, Altera Corporation.

Hardware

- **Altera DE2-115** Development and Education Board. This will be provided; check them out in lab. You can either leave these in the lab or take them home. In either case you will be responsible for returning this equipment in order to receive any credit for this course.

V Grading Components

Homework

Assignments given during lectures and on the course Web site (Canvas) are due by the times posted on Canvas. Note that electronic versions of Verilog and other supporting files will often be required. **Also Note: due to the nature of this class and the length of the lecture periods, some 'homework' assignments may be given and collected during the same lecture period. Also there will be occasional in-class quizzes over the assigned reading material.**

Laboratory Exercises

Laboratory projects are group assignments, done in teams of three. Learning to work in groups is so important, **you will not be allowed to perform or turn in laboratory assignments on an individual basis**. An electronic, clearly written lab report is required for each lab assignment per team. The lab report should include the following sections:

- Cover page
- Table of contents
- Requirements
- Design (including SystemVerilog code and block diagrams)
- Test Procedures
- Test Results
- Observations
- Conclusions
- References (if any)
- Appendices (if any)

A sample lab report will be posted on the course Web site.

An Electronic version of SystemVerilog code and associated files will also be turned in for each part of each laboratory project.

The front page shall be signed by each of the team members to indicate their approval. SystemVerilog and supporting files will be turned in electronically, as well. Reports are due as noted on the course Web site, generally the week following the lab completion. Explicit due dates will be posted when the laboratory exercises are assigned.

Exams

There will be one midterm exam and a final exam. All exams will be based on material from lectures, the course text, course handouts, and the laboratory exercises and will be 2 hours in length. The final exam will be comprehensive. **Permission to miss and make-up an exam will only be given in the most extreme circumstances**. Vacations, reunions, ski trips, and so on are **not** considered extreme circumstances. If something important to you is on your calendar for any portion of this quarter, tell me about it **now**.

VI Grading Policy:

Final student evaluation will be based on:

- Midterm 25%
- Final 30%
- Laboratory 20%
- Homework 20%
- In-class quizzes 5%

Grade Equivalence

The UW decimal grading system (described at the following website), will be used: http://www.washington.edu/students/gencat/front/Grading_Sys.htm.

The following table shows the *minimum* decimal grades for the specified percentage scores.

Decimal grades may be adjusted upward from these minimum grades.

Grade	Score	Grade	Score	Grade	Score	Grade	Score
4.0	98-100	3.4	89	2.4	79	1.4	69
3.9	95-97	3.3	88	2.3	78	1.3	68
3.8	93-94	3.2	87	2.2	77	1.2	67
3.7	92	3.1	86	2.1	76	1.1	66
3.6	91	3.0	85	**2.0**	**75**	1.0	65
3.5	90	2.9	84	1.9	74	0.9	64
		2.8	83	1.8	73	0.8	62-63
		2.7	82	1.7	72	0.7	61
		2.6	81	1.6	71	0.0	0-60
		2.5	80	1.5	70		

A 2.0 or greater is required to pass the course.

VII Course Conduct:

Attendance and Participation

Students are encouraged to attend classes or arrange absences in advance. To aid the learning process, students are required to participate in class discussion. Also note the in-class homework and quiz notification, above.

Equipment

An Altera DE2 board will be checked out to you to facilitate your homework and laboratory exercises. You will be responsible for the return of this board at the conclusion of the quarter. If you feel you cannot secure this board away from the laboratory environment, you may store it in one of the lockers in CP 206D.

Software Standards

In order to make your code submissions easier to read (and hence grade) you may be required to follow certain software standards. These may include (but are not limited to):

- **Various conventions <u>will</u> be required to facilitate automated testing**
- Module naming standards
- Capitalization standards
- Indentation standards
- File content standards (e.g., one module per file)
- Compilation and synthesis standards (error-free and only certain warnings are allowed)

These standards will be explained in detail in class and on the course Web site.

VIII Other Policies

Course Changes

The schedule and procedures for this course are subject to change. Changes will be announced in class and posted on Canvas; it is the student's responsibility to learn of and adjust to these changes.

Dropping

Refer to the UW Academic Calendar at Academic Calendar.

Plagiarism and Cheating Policy

Students are encouraged to collaborate regularly with colleagues to gain a deep understanding of the material, and to gain insight on options for problem solutions. Solutions submitted are to display individual knowledge and accomplishment. **Any significant contribution in a submission must be acknowledged and the responsible student or source given due credit.** See Academic Honesty.

Safety Escorts

Safety escorts are available to accompany you to your vehicle 24 hours a day, 7 days a week. Call Campus Safety at **2-4416** from a campus phone, and **253-692-4416** from a non-campus phone.

Reporting Emergencies

From campus phones, report emergencies by dialing **9-911** and state the T-number that is on a sticker on the phone; from non-campus phones dial **911**. Building location numbers are posted on all buildings. For assistance with non-emergencies call Campus Safety at **2-4416** from a campus phone, and **253-692-4416** from a non-campus phone.

Emergency Procedures

In case of emergency, follow your professor's instructions. When an alarm sounds, evacuate the building immediately. MATT, CP, WG, GWP, and BB buildings assemble in the Cragle Parking Lot south of the library. BHS, WCG, and DOU buildings assemble near the transit station next to the Pinkerton Building on Broadway (across from Spaghetti Factory). Pinkerton occupants go to the convention center parking lot north of Pinkerton. For more information

about emergency procedures and information, please go to: http://www.tacoma.uw.edu/campus-safety/campus-safety-security

Disability Support

If you would like to request academic accommodations due to a temporary or permanent disability, contact Lisa Tice, Manager for Disability Support Services (DSS) in the Mattress Factory Bldg, Suite 206. An appointment can be made through the front desk of Student Affairs (692-4400), through Student Development and Success (692-4501), by phoning Lisa directly at 692-4493 (voice) or 692-4413 (TTY), or by e-mail ltice@u.washington.edu. Appropriate accommodations are arranged after you've conferred with the DSS Manager and presented the required documentation of your disability to DSS.