GREEN UNIVERSITY OF BANGLADESH

Department of Computer Science & Engineering

CT-03

Course Code: EEE-203

Course Title: Electronic Devices and Circuits & Pulse Techniques

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Remark

Ans to the Q.NO:1

In cmos technology both N-type and P-type Transistors are used to design wie junctions. The same signal which turns on a transistor of one type is used to turn off a transistor of other type. this characteristic allows the design of dynamic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail. pull up means getting close VDD. so pmos has VDD as resource, naturally when input is zero drain would be pulled up. when output of zero pmos taurns on, it will be pulled up or high. pull down means being output to zero from one too. if input is one a for an inverters in cmos, N transistors will be drive the output to zero as pull down.

If pmos is used to pull down with source as Vss output will be at 0V and similarly, nmos gives VDD minus one threshold as output if source connected to VDD. Noise margin's increase and leakage would increase.

Ans to the Q.NO:02

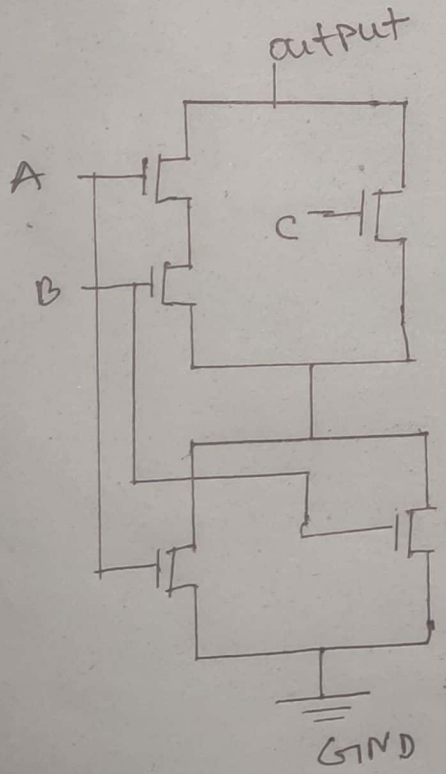
Given,

$$Y = \overline{AB + C \cdot (A+B)}$$

$$Y = (\bar{A}+\bar{B}) \cdot \bar{C} + \bar{A}\bar{B}$$

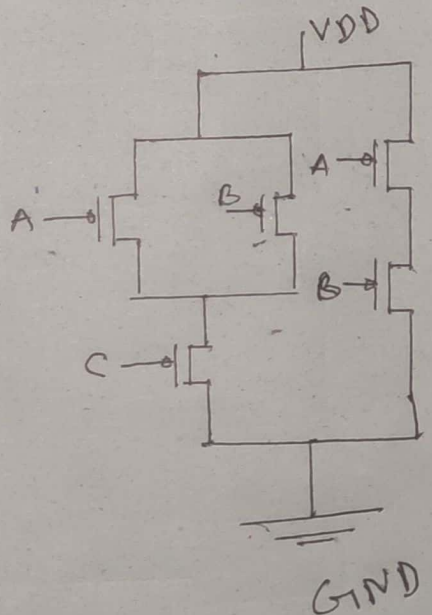
nMOS (pull down network)

$AB + C \cdot (A+B)$

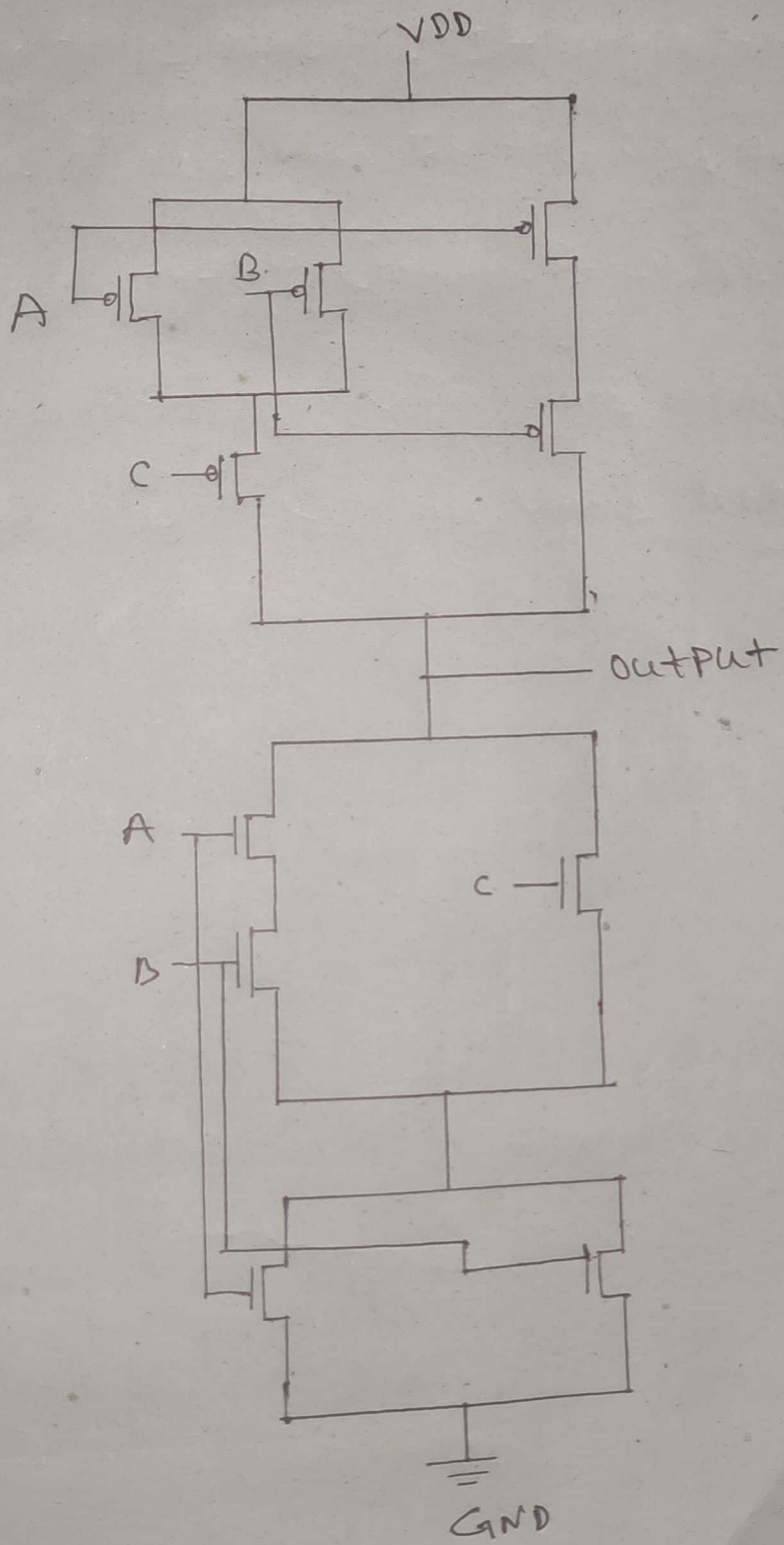


pMOS (pull up network)

$(\bar{A}+\bar{B}) \cdot \bar{C} + \bar{A}\bar{B}$



So, cmos circuit of the given function.



Ans to the Q.NO:03

According to the question, If any of the signals is green the train can go through the green track otherwise not. the characteristic matches with the OR gate characteristics now, designing cmos circuit for the train using NOT and NOR gate.