$$i_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad (5.20)$$

Example 5.1

Consider a process technology for which $L_{min} = 0.4\ \mu m$, $t_{ox} = 8\ nm$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.7\ V$.

(a) Find C_{ox} and k'_n.
(b) For a MOSFET with $W/L = 8\ \mu m/0.8\ \mu m$, calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\ \mu A$.
(c) For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

Solution

(a)
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3}\ F/m^2$$
$$= 4.32\ fF/\mu m^2$$

$$k'_n = \mu_n C_{ox} = 450\ (cm^2/V \cdot s) \times 4.32\ (fF/\mu m^2)$$
$$= 450 \times 10^8\ (\mu m^2/V \cdot s) \times 4.32 \times 10^{-15}\ (F/\mu m^2)$$
$$= 194 \times 10^{-6}\ (F/V \cdot s)$$
$$= 194\ \mu A/V^2$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2}k'_n\frac{W}{L}v_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8}V_{OV}^2$$

which results in

$$V_{OV} = 0.32\ V$$

Example 5.1 *continued*

Thus,

$$V_{GS} = V_t + V_{OV} = 1.02 \text{ V}$$

and

$$V_{DSmin} = V_{OV} = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with v_{DS} very small,

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{OV}}$$

Thus

$$1000 = \frac{1}{194 \times 10^{-6} \times 10 \times V_{OV}}$$

which yields

$$V_{OV} = 0.52 \text{ V}$$

Thus,

$$V_{GS} = 1.22 \text{ V}$$

Example 5.2

Consider an NMOS transistor fabricated in a 0.18-μm process with $L = 0.18$ μm and $W = 2$ μm. The process technology is specified to have $C_{ox} = 8.6$ fF/μm², $\mu_n = 450$ cm²/V·s, and $V_{tn} = 0.5$ V.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100$ μA.
(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50$ μA.
(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3$ V. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by –0.01 V.

Solution

First we determine the process transconductance parameter K_n

$$K_n = \mu_n C_{ox}$$
$$= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2$$
$$= 387 \text{ μA/V}^2$$

$$= 387\ \mu A/V^2$$

and the transistor transconductance parameter k_n

$$k_n = K_n\left(\frac{W}{L}\right)$$

$$= 387\left(\frac{2}{0.18}\right) = 4.3\ mA/V^2$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22\ V$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72\ V$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22\ V$$

(b) With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$I_D = k_n\left[V_{OV}\ V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$50 = 4.3 \times 10^3\left[0.22\,V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44\,V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06\ \text{V} \quad \text{and} \quad V_{DS} = 0.39\ \text{V}$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06\ \text{V}$$

Example 5.2 *continued*

(c) For $v_{GS} = 0.7\ \text{V}$, $V_{OV} = 0.2\ \text{V}$, and since $V_{DS} = 0.3\ \text{V}$, the transistor is operating in saturation and

$$\begin{aligned} I_D &= \frac{1}{2} k_n V_{OV}^2 \\ &= \frac{1}{2} \times 4300 \times 0.04 \\ &= 86\ \mu\text{A} \end{aligned}$$

Now for $v_{GS} = 0.710\ \text{V}$, $v_{OV} = 0.21\ \text{V}$ and

$$= 86\ \mu A$$

Now for $v_{GS} = 0.710$ V, $v_{OV} = 0.21$ V and

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8\ \mu A$$

and for $v_{GS} = 0.690$ V, $v_{OV} = 0.19$ V, and

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6\ \mu A$$

Thus, with $\Delta V_{GS} = +0.01$ V, $\Delta i_D = 8.8\ \mu A$; and for $\Delta V_{GS} = -0.01$ V, $\Delta i_D = -8.4\ \mu A$.

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in v_{GS} are kept small. This is just a preview of the "small-signal operation" of the MOSFET studied in Sections 5.4 and 5.5.

Example 5.3

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 32\ \mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

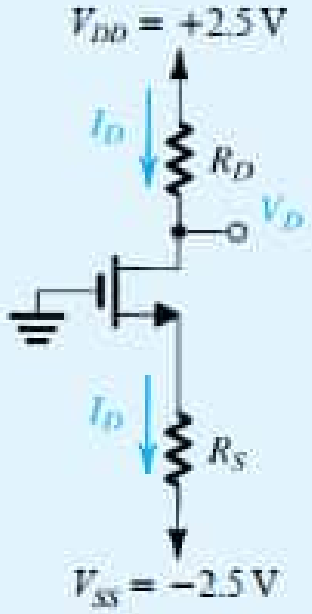


Figure 5.21 Circuit for Example 5.3.

Solution

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{2.5 - 0.5}{0.4} = 5\ \text{k}\Omega$$

$$= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

To determine the value required for R_S, we need to know the voltage at the source, which can be easily found if we know V_{GS}. This in turn can be determined from V_{OV}. Toward that end, we note that since $V_D = 0.5$ V is greater than V_G, the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of I_D to determine the required value of V_{OV}.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

Then substituting $I_D = 0.4$ mA $= 400$ μA, $\mu_n C_{ox} = 100$ μA/V^2, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at −1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

$$= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the $i-v$ relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = K_n'(W/L)$ and V_{tn}. Neglect channel-length modulation (i.e., $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

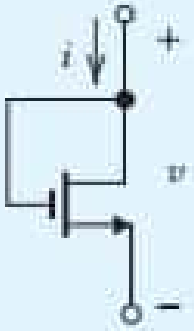


Figure 5.22

Solution

Since $v_D = v_G$ implies operation in the saturation mode,

$$i_D = \frac{1}{2}K_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

Now, $i = i_D$ and $v = v_{GS}$, thus

$$i = \frac{1}{2}K_n'\left(\frac{W}{L}\right)(v - V_{tn})^2$$

Replacing $K_n'\left(\frac{W}{L}\right)$ by k_n results in

$$i = \frac{1}{2}k_n(v - V_{tn})^2$$

Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $K_n(W/L) = 1$ mA/V^2.

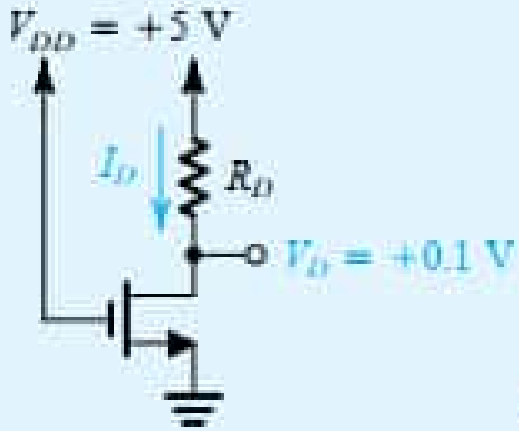


Figure 5.23 Circuit for Example 5.5.

Example 5.5 *continued*

Solution

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_{tn} = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1)\times 0.1 - \frac{1}{2}\times 0.01\right]$$

$$= 0.395 \text{ mA}$$

The required value for R_D can be found as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors—in this case, 12 kΩ; see Appendix G. Since the transistor is operating in the triode region with a small V_{DS}, the effective drain-to-source resistance can be determined as follows:

$$r_{DS} = \frac{V_{DS}}{I_D}$$

$$= \frac{0.1}{0.395} = 253 \ \Omega$$

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

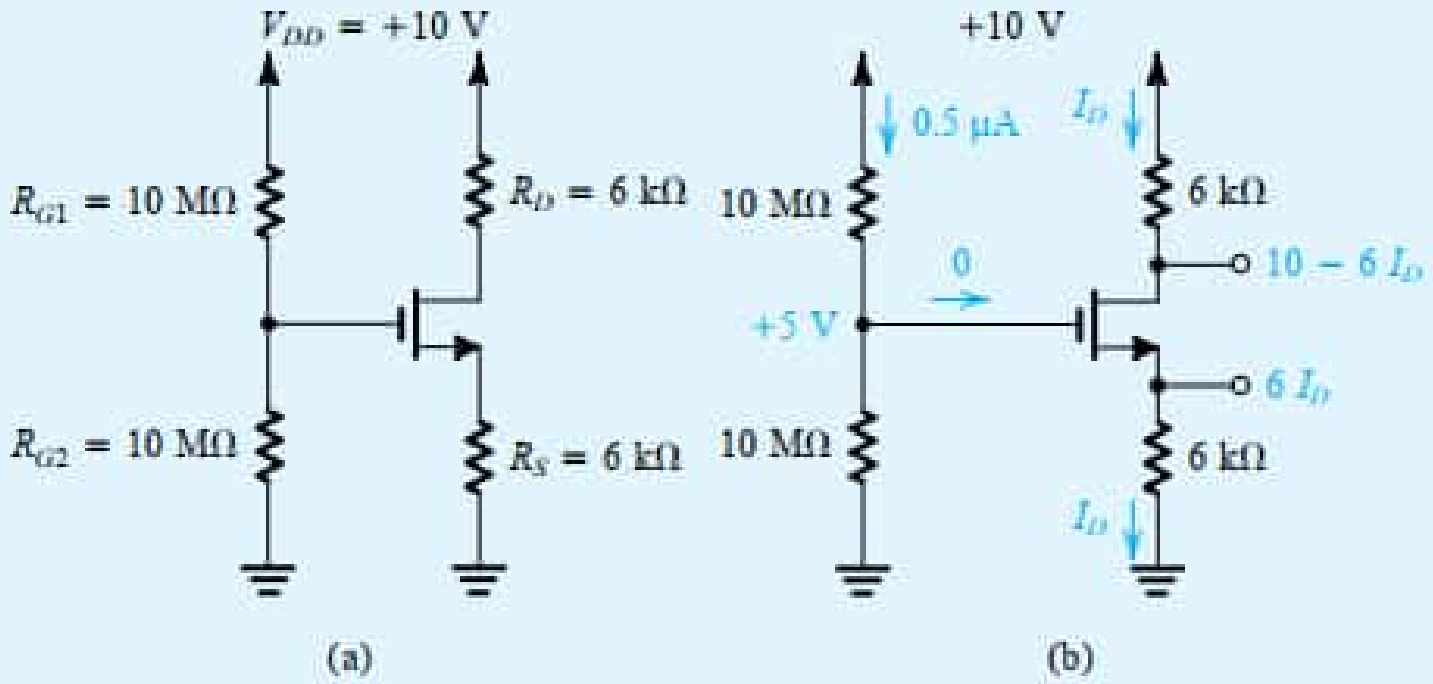


Figure 5.24 **(a)** Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$

$$R_{G2} + R_{G1} \qquad 10 + 10$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) $\times$ 6 (kΩ) $= 6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus, I_D is given by

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{tn})^2$$

$$= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

which results in the following quadratic equation in I_D:

$$18I_D^2 - 25I_D + 8 = 0$$

Example 5.6 *continued*

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_{to}$, the transistor is operating in saturation, as initially assumed.

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the enhancement-type PMOS transistor have $V_{tp} = -1$ V and $k_p'(W/L) = 1$ mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

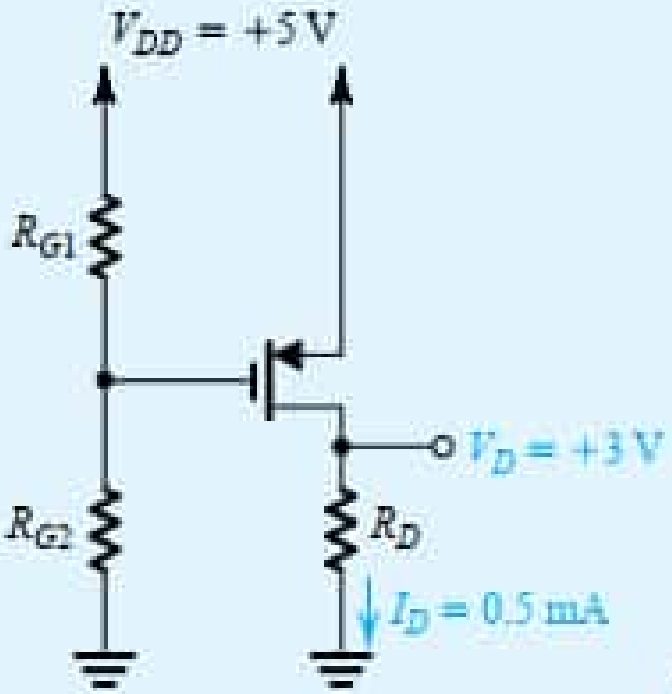


Figure 5.25 Circuit for Example 5.7.

Solution

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k_p' \frac{W}{L} |V_{OV}|^2$$

Substituting $I_D = 0.5$ mA and $k_p' W/L = 1$ mA/V^2, we obtain

$$|V_{OV}| = 1 \text{ V}$$

and

$$V_{SG} = |V_{tp}| + |V_{OV}| = 1 + 1 = 2 \text{ V}$$

Since the source is at +5 V, the gate voltage must be set to +3 V. This can be achieved by the appropriate selection of the values of R_{G1} and R_{G2}. A possible selection is $R_{G1} = 2$ MΩ and $R_{G2} = 3$ MΩ.

The value of R_D can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ kΩ}$$

Saturation-mode operation will be maintained up to the point that V_D exceeds V_G by $|V_{tp}|$: that is, until

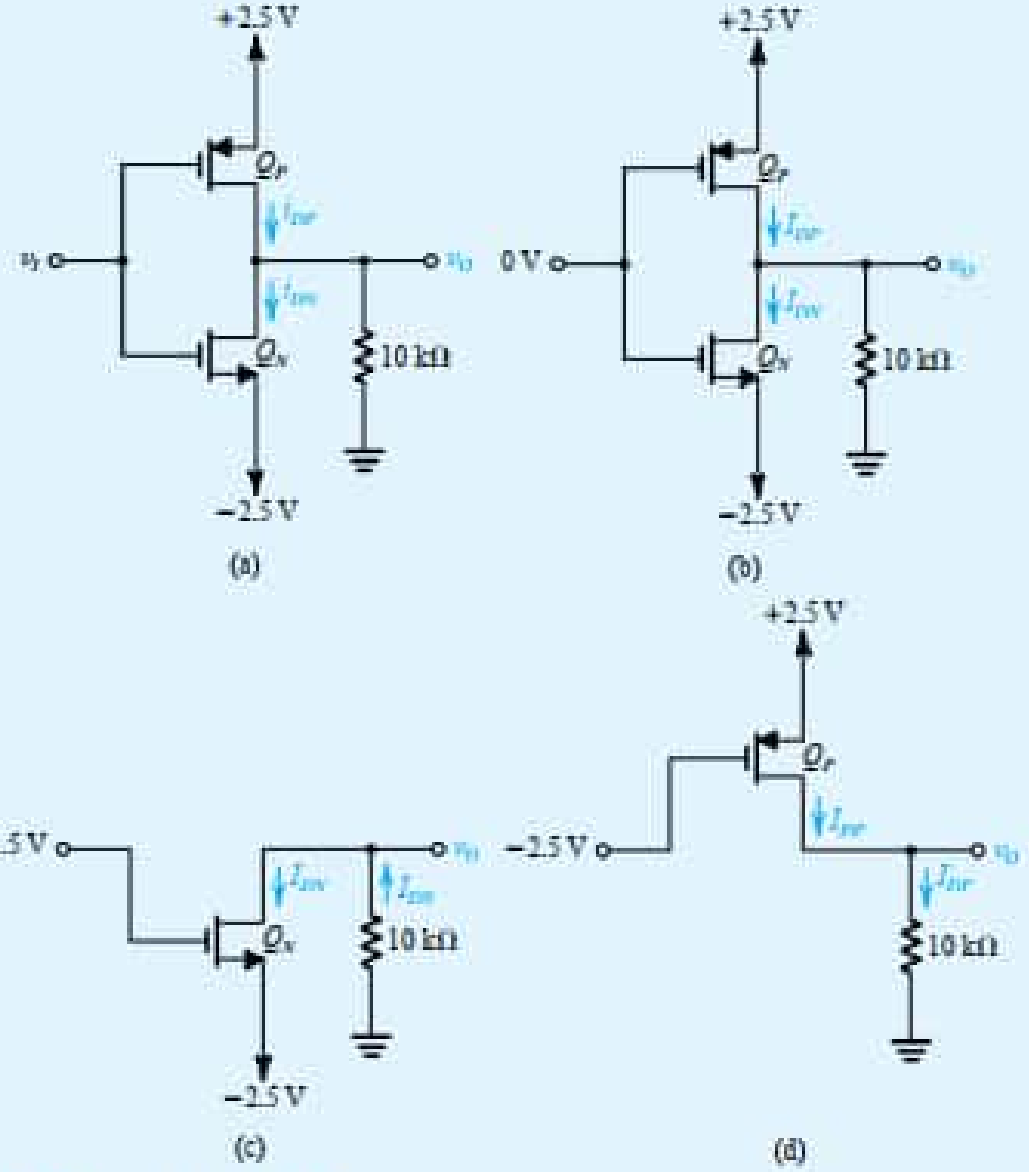
$$V_{D_{max}} = 3 + 1 = 4 \text{ V}$$

This value of drain voltage is obtained with R_D given by

$$R_D = \frac{4}{0.5} = 8 \text{ kΩ}$$

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents I_{DN} and I_{DP} as well as the voltage v_O for $v_I = 0\ \text{V}$, +2.5 V, and −2.5 V.



Solution

Figure 5.26(b) shows the circuit for the case $v_I = 0$ V. We note that since Q_n and Q_p are perfectly matched and are operating at equal values of $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0$ V. Thus both Q_n and Q_p are operating with $|V_{DS}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \tfrac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_p will have a V_{SG} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 5.26(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_{tn}, causing Q_n to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$\begin{aligned} I_{DN} &= k_n'(W_n/L_n)(V_{GS} - V_{tn})V_{DS} \\ &= 1[2.5 - (-2.5) - 1][v_O - (-2.5)] \end{aligned}$$

From the circuit diagram shown in Fig. 5.26(c), we can also write

$$I_{DN}(\text{mA}) = \frac{0 - v_O}{10\ (\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \qquad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 5.26(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_n will be off. Thus $I_{DN} = 0$, Q_p will be operating in the triode region with $I_{DP} = 2.44$ mA and $v_O = +2.44$ V.

Example 5.9

Consider the amplifier circuit shown in Fig. 5.29(a). The transistor is specified to have $V_t = 0.4$ V, $k_n' = 0.4$ mA/V^2, $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, and $V_{GS} = 0.6$ V.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV}, I_D, V_{DS}, and A_v.

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence find the maximum allowable amplitude of a sinusoidal v_{gs}.

Solution

(a) With $V_{GS} = 0.6$ V, $V_{OV} = 0.6 - 0.4 = 0.2$ V.

Thus,

$$I_D = \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA}$$

$$V_{DS} = V_{DD} - R_D I_D$$

$$= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V}$$

Since V_{DS} is greater than V_{OV}, the transistor is indeed operating in saturation. The voltage gain can be found from Eq. (5.37),

$$A_v = -k_n V_{OV} R_D$$

$$= -0.4 \times 10 \times 0.2 \times 17.5$$

$$= -14 \text{ V/V}$$

An identical result can be found using Eq. (5.38).

(b) Since $V_{OV} = 0.2$ V and $V_{DS} = 0.4$ V, we see that the maximum allowable negative signal swing at

An identical result can be found using Eq. (5.38).

(b) Since $V_{OV} = 0.2$ V and $V_{DS} = 0.4$ V, we see that the maximum allowable negative signal swing at the drain is 0.2 V. In the positive direction, a swing of +0.2 V would not cause the transistor to cut off and thus is allowed. Thus the maximum symmetrical signal swing allowable at the drain is ±0.2 V. The corresponding amplitude of v_{gs} can be found from

$$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2\text{ V}}{14} = 14.2\text{ mV}$$

Since $\hat{v}_{gs} \ll V_{OV}$, the operation will be reasonably linear (more on this in later sections).

Greater insight into the issue of allowable signal swing can be obtained by examining the signal waveforms shown in Fig. 5.30. Note that for the MOSFET to remain in saturation at the negative peak of v_{ds}, we must ensure that

$$v_{DSmin} \geq v_{GSmin} - V_t$$

that is,

$$0.4 - |A_v|\hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

which results in

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3\text{ mV}$$

This is a more precise result than the one obtained earlier.

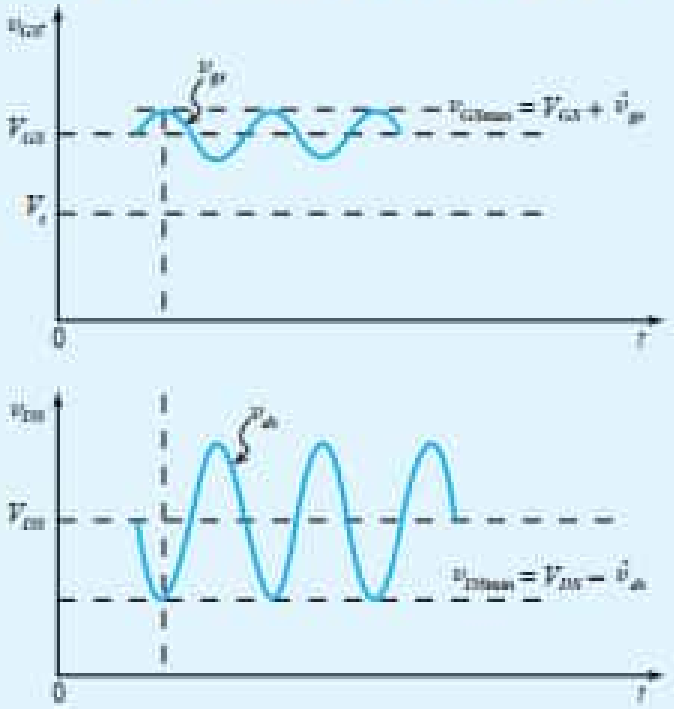


Figure 5.30 Signal waveforms at gate and drain for the amplifier in Example 5.9. Note that to ensure operation in the saturation region at all times, $v_{DSmin} \geq v_{GSmin} - V_t$.