GENERAL Single-PORT REGISTER FILE
512 WORDS X 32 BITS, MUX 2
SMIC 0.11um LOGIC PROCESS

Version 0.1.a

OVERVIEW

The Single-Port Register File is designed for SMIC's 0.11um CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40^{o} C to 125^{o}C.

The write enable (WEN), chip enable (CEN), address (A[0:n]) and data in (D[0:n]) signals are latched on the rising-edge of the clock. When CEN is low and WEN is high the memory will be in read operation. Data is read from the location specified by the address A[0:i], and is output on the output port Q[0:n].When CEN and WEN are both low the memory will be in write operation. The word on the data port D[0:n] will be written into the location specified by the address A[0:i] and the data will appear on the output port Q[0:n].

When CEN is high the memory is in standby mode. Meanwhile, the data stored in memory is retained but cannot be read or written.

CONFIGURATION:

PARAMETER	VALUE
Mux	2
Words	512
Bits	32
Width	202.485um
Height	303.17um
Area	61387.377um^{2}

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
A[8:0]	Input	Address Inputs
D[31:0]	Input	Data Inputs
WEN	Input	Write Enable
CEN	Input	Chip Enable
CLK	Input	Clock Input
Q[31:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	SS CORNER 1.08V, -40°C		SS CORNER 1.08V, 125°C		FF CORNER 1.32V, -40°C		FF CORNER 1.32V, 0°C		FF CORNER 1.32V, 125°C		TT CORNER 1.2V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	1.891		2.290		0.808		0.866		1.043		1.379	
Ta	Access Time[1]		1.719		2.082	0.735		0.787		0.948			1.254
Tas	Address Setup	0.585		0.600		0.340		0.359		0.408		0.417	
Tah	Address Hold	0.254		0.244		0.168		0.171		0.183		0.195	
Tds	Data Setup	0.374		0.352		0.240		0.252		0.277		0.267	
Tdh	Data Hold	0.363		0.425		0.239		0.248		0.302		0.288	
Tws	Write Enable Setup	0.493		0.471		0.287		0.301		0.333		0.340	
Twh	Write Enable Hold	0.242		0.222		0.156		0.158		0.162		0.179	
Tcs	Chip Enable Setup	0.668		0.605		0.275		0.283		0.304		0.368	
Tch	Chip Enable Hold	0.000		0.000		0.000		0.000		0.000		0.000	
Tckh	Clock High	0.040		0.040		0.040		0.040		0.040		0.040	
Tckl	Clock Low	0.330		0.330		0.220		0.220		0.220		0.220	
Tckr	Clock Rise Skew		1.000		1.000		0.500		0.500		0.500		0.600

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

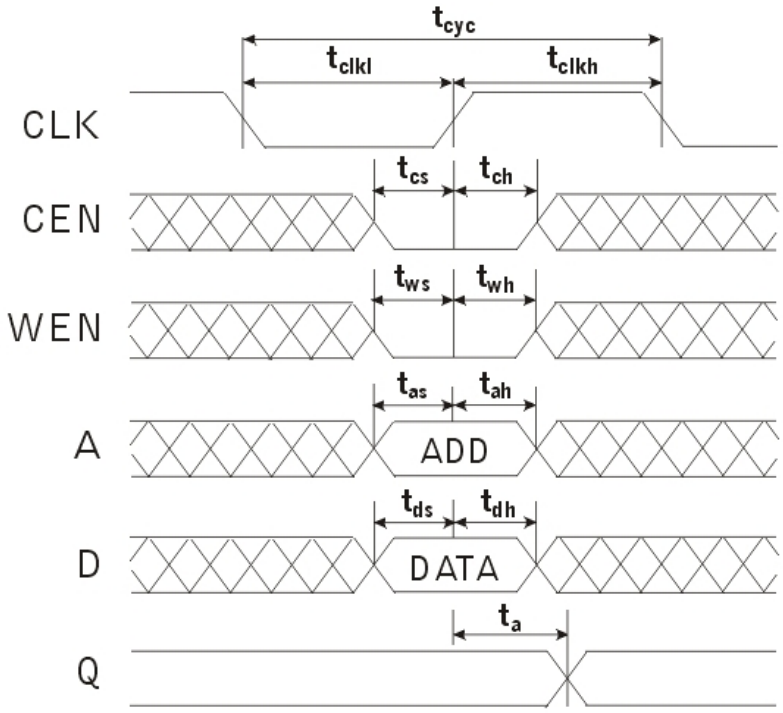
POWER:(UNITS=uA/Mhz)

PARAMETER	SS CORNER 1.08V, -40C	SS CORNER 1.2V, 125C	FF CORNER 1.32V, -40C	FF CORNER 1.32V, 0°C	FF CORNER 1.32V, 125°C	TT CORNER 1.2V, 25°C
AC Current	13.114	13.563	17.483	17.616	18.597	15.315
Read AC Current	13.121	13.560	17.460	17.616	18.602	15.316
Write AC Current	13.108	13.566	17.507	17.616	18.592	15.313
Standby Power (mW)	0.001468	0.047146	0.012005	0.024921	0.816679	0.009942

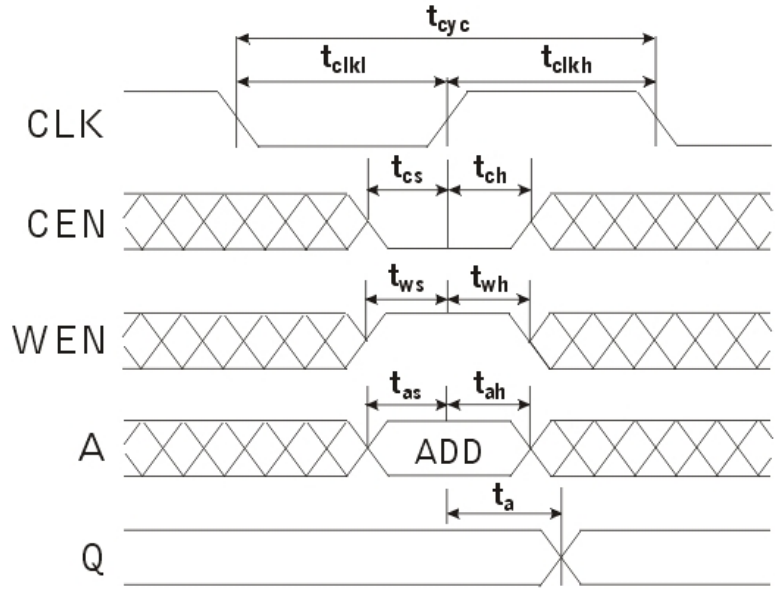
Power simulation conditions:

1. 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	0.1.a	

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